Customizable HSB Sensor Interfaces on Lattice CertusPro-NX Platforms

Reference Design

FPGA-RD-02326-1.3

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Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviations	Definition
APB	Advanced Peripheral Bus
AXI	Advanced eXtensible Interface
BOOTP	Bootstrap Protocol
CDC	Clock Domain Crossing
CRC	Cyclic Redundancy Check
CMOS	Complementary Metal-Oxide-Semiconductor
DDR	Dual Data Rate
D-PHY	Digital Physical Layer
EBR	Embedded Block RAM
ECB	Ethernet Control Bus
FPGA	Field-Programmable Gate Array
FW	Firmware
GUI	Graphical User Interface
HDL	Hardware Description Language
Hex	Hexadecimal
HIF	Host Interface
HSB	Holoscan Sensor Bridge
I2C	Inter-Integrated Circuit
ICMP	Internet Control Message Protocol
IP	Intellectual Property (Core)
MAC	Media Access Control
MIPI	Mobile Industry Processor Interface
MPCS	Multi-Protocol Communication Stack
NGC	NVIDIA GPU Cloud
PCB	Printed Circuit Board
PCS	Physical Coding Sublayer
PDC	Platform Design Constraint
PFU	Programmable Function Unit
PLL	Phase-Locked Loop
PTP	Precision Time Protocol
PMA	Physical Medium Attachment
PROM	Programmable Read-Only Memory
SDK	Software Development Kit
SERDES	Serializer/Deserializer
SFP	Small Form-factor Pluggable
SPI	Serial Peripheral Interface
STA	Static Timing Analysis
UDP	User Datagram Protocol
YAML	YAML Ain’t Markup Language

1. Introduction

This user guide describes the reference design for customizable HSB sensor interfaces, on the Lattice CertusPro™-NX platforms. The supported platforms include the CertusPro-NX Versa Board and the CertusPro-NX Sensor-to-Ethernet Bridge Board. These boards function as the Holoscan Sensor Bridge between connected sensors and the NVIDIA host. The customizable interfaces in this reference design are divided into two interface categories.

- **Sensor Interface**
  This reference design targets a MIPI CSI-2 camera sensor. The sensor interface is designed to be flexible and scalable, allowing you to integrate multiple camera sensors based on your requirements. The system supports various configurations to meet diverse imaging needs.
- **Host Interface**
  The host interface focuses on Ethernet connectivity and supports multiple link speeds to accommodate varying data throughput requirements. This enables seamless communication between the sensor bridge and host systems.

Note:

- On the CertusPro-NX Versa Board, one Ethernet port and one camera connector are available for testing.
- On the CertusPro-NX Sensor-to-Ethernet Bridge Board, one Ethernet port and two camera connectors are available for testing.

The primary objective of the reference design is to establish a robust and reliable bridge between the HSB interfaces and the NVIDIA host. The reference design leverages NVIDIA's Holoscan Sensor Bridge solution and integrates smoothly within the broader NVIDIA ecosystem, enabling high-performance sensor data processing and transmission. An overview of the key components of the NVIDIA Holoscan Sensor Bridge solution and ecosystem is as follows:

1. Sensors
   - Targets the MIPI CSI-2 camera sensor.
2. Holoscan Sensor Bridge
   - Lattice CertusPro-NX Versa Board and CertusPro-NX Sensor-to-Ethernet Bridge Board function as the Holoscan Sensor Bridge solution.
   - Performs sensor data pre-processing to reduce computational load on the host system.
   - The reference design is implemented in the Lattice FPGA targeting LFCPNX-100 speed grade 9 device. The key components of the reference design include:
     - Sensor Interface
       - Supports MIPI CSI-2 camera sensors which are highly configurable to accommodate various camera sensors with different MIPI lanes and lane rates.
       - Supports an LVDS DDR receiver interface connection to an external FPGA device capable of handling multiple MIPI CSI-2 (D-PHY) channels for high-speed sensor input. For example, on the CertusPro-NX Sensor-to-Ethernet Bridge Board, the CrossLink-NX device serves as an external interface to the MIPI CSI-2 camera sensor and uses LVDS DDR receiver interface to transfer raw CSI-2 data to the CertusPro-NX device for processing.
     - Hololink IP
       - Acts as a bridge between the sensor interface and the host system.
       - Handles data encapsulation, synchronization, and buffering to ensure smooth transmission of high-throughput sensor data.
     - Host Interface (Ethernet link)
       - Provides a high-speed Ethernet link to the host, supporting 1GbE or 10GbE speeds.
       - Enables low-latency, and high-bandwidth communication.
3. Host (NVIDIA Jetson AGX Orin/Thor Developer Kit)
   - Runs the Holoscan SDK to process incoming data.
   - Performs real-time AI inference, visualization, and decision-making.
   - Strems processed data to the cloud or other edge devices.

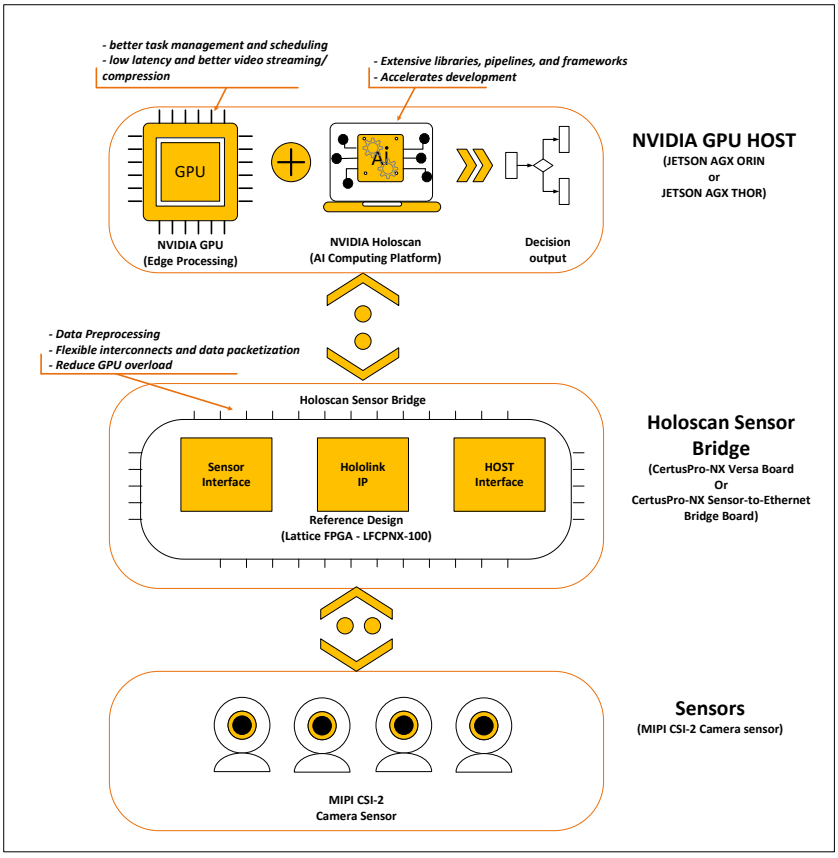


Figure 1.1. Overview of Customizable HSB Sensor Interface RD with NVIDIA ecosystem

1.1. Reference Design: Quick Facts

1.1.1. CertusPro-NX Versa Board with Jetson AGX Orin/Thor

Table 1.1. Summary of CertusPro-NX Versa Board with NVIDIA Jetson AGX Orin

General	Target Devices	CertusPro-NX FPGA (LFCPNX-100-9LFG672I)
	Source code format	Verilog and SystemVerilog
Simulation	Functional simulation	N/A
	Timing simulation	N/A
	Testbench	N/A
	Testbench format	N/A
Software Requirements	Software tool and version	Lattice Radiant™ software, version 2025.2.0.48.0
	IP version (if applicable)	• CSI-2/DSI D-PHY Rx IP v2.1.0 • OSC IP v1.4.0 • PLL IP v1.9.1 • 10GbE Ethernet PCS IP Core v1.3.0 • 10GbE Ethernet MAC IP Core v1.1.0 • Tri-speed Ethernet v2.1.0 (MAC + SGMII (SERDES)) • Hololink IP v2511
	Host Software (AGX Orin)	• JetPack 6.2.1 • NVIDIA Holoscan SDK 3.7.0 • NVIDIA Jetson Linux 36.4.4 • HSB SDK 2.5.0

Hardware Requirements	Board	• CertusPro-NX Versa Board • IMX258 camera module • Ethernet 10GBase-T (Cat 6 RJ-45) SFP+ module (10GbE Ethernet) • 10/100/1000BASE-T SFP module (1GbE Ethernet) • Display Monitor
	Host	• NVIDIA Jetson AGX Orin Developer Kit
	Cable	• DisplayPort cable • Ethernet Cat 6 cable

Table 1.2. Summary of CertusPro-NX Versa Board with NVIDIA Jetson AGX Thor

General	Target Devices	CertusPro-NX FPGA (LFCPNX-100-9LFG672I)
	Source code format	Verilog and SystemVerilog
Simulation	Functional simulation	N/A
	Timing simulation	N/A
	Testbench	N/A
	Testbench format	N/A
Software Requirements	Software tool and version	Lattice Radiant™ software, version 2025.2.0.48.0
	IP version (if applicable)	• CSI-2/DSI D-PHY Rx IP v2.1.0 • OSC IP v1.4.0 • PLL IP v1.9.1 • 10GbE Ethernet PCS IP Core v1.3.0 • 10GbE Ethernet MAC IP Core v1.1.0 • Tri-speed Ethernet v2.1.0 (MAC + SGMII (SERDES)) • Hololink IP v2511
	Host Software (AGX Thor)	• JetPack 7.0 • NVIDIA Holoscan SDK 3.7.0 • NVIDIA Jetson Linux 38.2 • HSB SDK 2.5.0
Hardware Requirements	Board	• CertusPro-NX Versa Board • IMX258 camera module • Display Monitor
	Host	• NVIDIA Jetson AGX Thor Developer Kit
	Cable	• DisplayPort cable • 100G QSFP28 to 4×25G SFP28 Breakout Active Optical Cable (AOC)

1.1.2. CertusPro-NX Sensor-to-Ethernet Bridge Board with Jetson AGX Orin

Table 1.3. Summary of CertusPro-NX Sensor-to-Ethernet Bridge Board with NVIDIA Jetson AGX Orin

General	Target Devices	CertusPro-NX FPGA (LFCPNX-100-9LFG672C) CrossLink-NX FPGA (LIFCL-17-9BG256C)
	Source code format	Verilog and SystemVerilog
Simulation	Functional simulation	N/A
	Timing simulation	N/A
	Testbench	N/A
	Testbench format	N/A
Software Requirements	Software tool and version	Lattice Radiant™ software, version 2025.2.0.48.0
	IP version (if applicable)	• LVDS DDR Receiver IP v1.7.0 • OSC IP v1.4.0 • PLL IP v1.9.1 • 10GbE Ethernet PCS IP Core v1.3.0 • 10GbE Ethernet MAC IP Core v1.1.0 • Hololink IP v2511 • CrossLink-NX FPGA bitstream
	Host Software (AGX Orin)	• JetPack 6.2.1 • NVIDIA Holoscan SDK 3.7.0 • NVIDIA Jetson Linux 36.4.4 • HSB SDK 2.5.0
Hardware Requirements	Board	• CertusPro-NX Sensor to Ethernet Bridge Board • IMX274 camera module • Ethernet 10GBase-T (Cat 6 RJ-45) SFP + module (10GbE Ethernet) • Display Monitor
	Host	• NVIDIA Jetson AGX Orin Developer Kit
	Cable	• DisplayPort cable • Ethernet Cat 6 cable

1.2. Quick-Start Guides

IMX258 Camera Streaming Setup – see Implementing the Reference Design section

Instructions for setting up and streaming video from the IMX258 camera module to the NVIDIA Jetson AGX Orin/Thor developer kit over a 1GbE/10GbE Ethernet connection.

IMX274 Camera Streaming Setup – see Implementing the Reference Design section

Instructions for setting up and streaming video from the IMX274 camera module to the NVIDIA Jetson AGX Orin developer kit over a 10GbE Ethernet connection.

Jetson AGX Orin Developer Kit Setup

Steps for setting up the NVIDIA Jetson AGX Orin developer kit.

Jetson AGX Thor Developer Kit Setup

Steps for setting up the NVIDIA Jetson AGX Thor developer kit.

1.3. Features

Key features of the reference design include:

- Sensor Interface
  - Supports one or more camera sensors.
  - Designed to be customizable, allowing flexible configuration of the MIPI CSI-2 RX D-PHY interface.
  - Enables integration of various camera types.
  - The interface type can be configured to support either the MIPI CSI-2 RX interface or the LVDS DDR receiver interface.
- Hololink IP
  - Acts as a bridge between the sensor interface and the host system.
  - Implements Ethernet packetization and supports streaming DMA, control interfaces, and transport abstraction.
  - Enables low-latency, high-throughput data transfer from sensors to compute platforms.
  - Supports Precision Time Protocol (PTP) per IEEE 1588-2019 specification. PTP synchronizes the Hololink IP's internal time with the host time, enabling the host to act as the Time Transmitter and send PTP packets.
- Host Interface (Ethernet link)
  - Supports Ethernet channels with a link speed of 1GbE or 10GbE.
  - Uses UDP over Ethernet to stream sensor data directly to GPU memory.
  - Enables real-time AI inference and visualization with minimal latency.
  - In testing, the CertusPro-NX Versa Board was used with a single Ethernet port configured for either 1GbE or 10GbE.

Features are enabled and implemented according to the target platform configured as a Holoscan Sensor Bridge. For detailed instructions, see the Customizing the Reference Design for CertusPro-NX Versa Board section and the Customizing the Reference Design for a CertusPro-NX Sensor to Ethernet Bridge Board section. You can tune the reference design to meet your own platform requirement.

1.4. Naming Conventions

1.4.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.4.2. Signal Names

- *_n* are active low (asserted when value is logic 0)
- *_i* are input signals
- *_o* are output signals

2. Directory Structure and File Overview

The following figure illustrates the directory structure of the reference design.

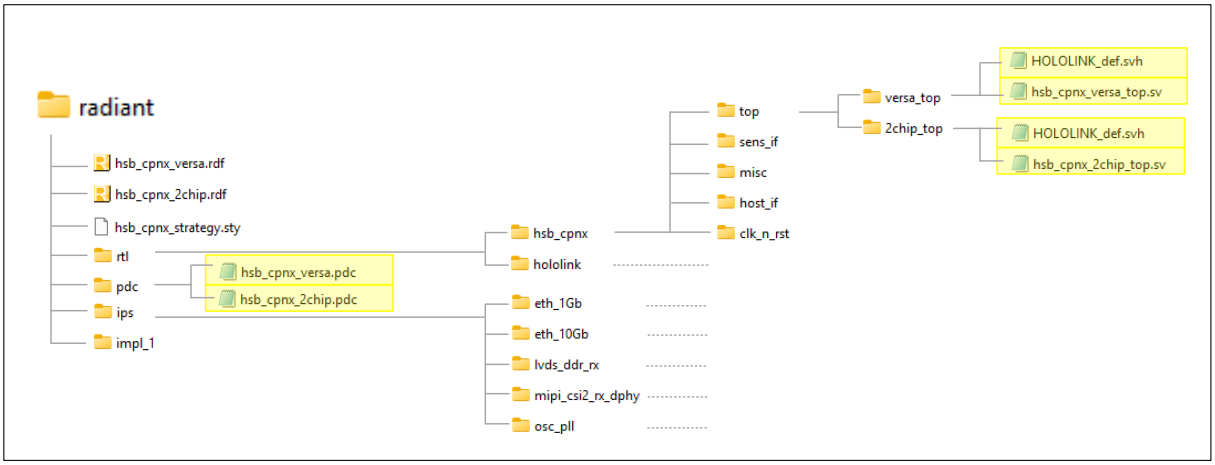


Figure 2.1. Directory Structure

Table 2.1. Folder Structure Description

Reference Design Specific	Folder/File	Description
Common Folders/files	radiant/rtl/hsb_cpnx/	This folder contains HDL code for the sensor interface, host interface, top-level design and other components.
	radiant/rtl/hololink/	This folder contains the encrypted Hololink IP. The current version is v2511.
	radiant/ips	This folder contains IP cores used in the reference design, including the oscillator, PLLs, MIPI CSI-2 RX D-PHY IP, Ethernet 10GbE IP, Tri-Speed Ethernet (MAC + SGMII/SERDES), and the CrossLink-NX (LIFCL-17) FPGA as an external device, along with other supporting components.
	radiant/hsb_cpnx_strategy.sty	This strategy file is shared by both reference designs. It includes custom settings optimized for improved place-and-route results.
	radiant/imp_1	This folder contains reports and logs generated during FPGA bitstream-generation compilation.
	bitstream/	The bitstream folder contains the FPGA-compiled bitstream for each reference design. Each reference design generates its own bitstream. For the CertusPro-NX Sensor-to-Ethernet Bridge Board, two FPGA bitstreams are produced: one for the CertusPro-NX device and one for the CrossLink-NX device.
CertusPro-NX Versa Board	radiant/hsb_cpnx_versa.rdf	This file is the Lattice Radiant software project file for the CertusPro-NX Versa reference design.
	radiant/pdc/hsb_cpnx_versa.pdc	This folder contains the PDC files for the CertusPro-NX Versa Board.
	radiant/rtl/hsb_cpnx/top/versa_top /hsb_cpnx_versa_top.sv	This file is the top-level module file for the CertusPro-NX Versa Board reference design.
	radiant/rtl/hsb_cpnx/top/versa_top /HOLOLINK_def.svh	This file contains the define switches used in the CertusPro-NX Versa Board reference design.

Reference Design Specific	Folder/File	Description
CertusPro-NX Sensor to Ethernet Bridge Board	radiant/hsb_cpnx_2chip.rdf	This file is the Lattice Radiant software project file for the CertusPro-NX Sensor-to-Ethernet Bridge Board reference design.
	radiant/pdc/hsb_cpnx_versa.pdc	This folder contains the PDC files for the CertusPro-NX Sensor-to-Ethernet Bridge Board.
	radiant/rtl/hsb_cpnx/top/2chip_top/ hsb_cpnx_2chip_top.sv	This file is the top-level module file for the CertusPro-NX Sensor-to-Ethernet Bridge Board reference design.
	radiant/rtl/hsb_cpnx/top/2chip_top/ HOLOLINK_def.svh	This file contains the define switches used in the CertusPro-NX Sensor-to-Ethernet Bridge Board reference design.

The project folder structure and files are shared between the two reference designs targeted for the CertusPro-NX Versa Board and the CertusPro-NX Sensor-to-Bridge Board. Some folders and files are common to both reference designs, while others are specific to each design.

The files highlighted in Figure 2.1 (radiant/rtl/hsb_cpnx/top/versa_top/HOLOLINK_def.svh, radiant/rtl/hsb_cpnx/top/2chip_top/HOLOLINK_def.svh, radiant/rtl/hsb_cpnx/top/versa_top/hsb_cpnx_versa_top.sv, radiant/rtl/hsb_cpnx/top/2chip_top/hsb_cpnx_2chip_top.sv, radiant/pdc/hsb_cpnx_versa.pdc and radiant/pdc/hsb_cpnx_2chip.pdc) are important. You must modify these files when developing your custom reference design.

3. Functional Description

3.1. NVIDIA Host Developer Kits

This section provides an overview of the NVIDIA host developer kit, highlighting key features of the Jetson AGX Orin and Jetson AGX Thor developer kits. For additional information, refer to the NVIDIA Developer webpage and search for Jetson Developer Kits.

3.1.1. Jetson AGX Orin Developer Kit

Figure 3.1. Jetson AGX Orin Developer Kit

The NVIDIA Jetson AGX Orin is a compact, high-performance edge-AI platform for workloads that require substantial on-device AI processing. It delivers 200–275 INT8 TOPS of compute through an Ampere-architecture GPU with 1,792–2,048 CUDA cores and 56–64 Tensor Cores. The system integrates either an 8-core or 12-core Arm Cortex-A78AE CPU running up to 2.2 GHz and 32 GB or 64 GB of LPDDR5 memory with 204.8 GB/s bandwidth. These resources enable efficient execution of complex AI pipelines and high-throughput data streams.

Jetson AGX Orin supports NVIDIA's software stack, including Isaac for robotics, DeepStream for vision AI, and Riva for conversational AI, allowing you to build applications across multiple AI and robotics domains.

Jetson AGX Orin provides a single Multi-Gigabit Ethernet (MGBE) interface. Depending on the carrier board and PHY implementation, the interface typically supports 1GbE, 2.5GbE, 5GbE, and 10GbE Ethernet. This bandwidth is sufficient for receiving UDP-based sensor data from a Holoscan Sensor Bridge, although it operates at lower throughput than NVIDIA Thor's 25GbE Ethernet interfaces. In the current reference design, only the 1GbE and 10GbE Ethernet link speeds are enabled.

Orin supports Precision Time Protocol (PTP) through its integrated MGBE interface, enabling accurate time synchronization with attached sensors. The platform fully supports UDP transport, providing low-latency, real-time data streaming. Although its Ethernet bandwidth is lower than that of NVIDIA Thor, Orin can accommodate multiple sensor inputs as long as the combined throughput remains within the capacity of the MGBE interface.

3.1.2. Jetson AGX Thor Developer Kit

Figure 3.2. Jetson AGX Thor Developer Kit

NVIDIA Jetson AGX Thor is a next-generation robotics and physical-AI computing platform built for highly demanding real-time sensor workloads. It provides up to 2,070 FP4 TFLOPS of AI compute powered by the NVIDIA Blackwell GPU architecture, offering more than 7.5× greater AI performance and substantially improved energy efficiency compared to Jetson AGX Orin.

The system integrates 128 GB of LPDDR5X memory with 273 GB/s of bandwidth, enabling efficient handling of large-scale multimodal data streams, including high-resolution camera, LiDAR, and radar inputs. To meet real-time robotics requirements, Jetson AGX Thor includes a 14-core Arm Neoverse-V3AE CPU that provides deterministic compute performance for sensor fusion, perception, and rapid decision-making. When combined with the NVIDIA Holoscan framework, the platform can execute complex sensor pipelines with sub-10 ms latency, supporting advanced autonomous-system and robotics workloads.

Jetson AGX Thor provides high-bandwidth Ethernet connectivity for integration with the Holoscan Sensor Bridge. The system includes a QSFP28 interface supporting four 25 Gbps Ethernet links, delivering a combined throughput of 100 Gbps. This capacity allows the host to ingest multiple high-rate UDP sensor streams from imaging and ranging devices without performance bottlenecks. Thor also incorporates a 5 Gb RJ45 Ethernet port that can be used for system control, secondary data paths, or redundancy, depending on system requirements.

All high-speed Ethernet interfaces on Jetson AGX Thor support IEEE-1588 Precision Time Protocol (PTP), enabling accurate alignment of sensor timestamps when used with the Holoscan Sensor Bridge. This capability is essential for synchronized streaming across multiple sensors, including cameras, LiDAR, radar, and microphones. Thor also provides full UDP transport support, offering low-latency, non-blocking data delivery suitable for real-time systems. With its 25GbE Ethernet links, the platform can maintain continuous high-throughput UDP streams, ensuring reliable frame-level sensor data reception even under heavy system load.

3.2. Lattice-Powered Holoscan Sensor Bridge Platforms

This section provides an overview of the targeted Lattice-powered Holoscan Sensor Bridge platform. The supported CertusPro-NX platforms include the CertusPro-NX Versa Board and the CertusPro-NX Sensor-to-Ethernet Bridge Board.

3.2.1. CertusPro-NX Versa Board

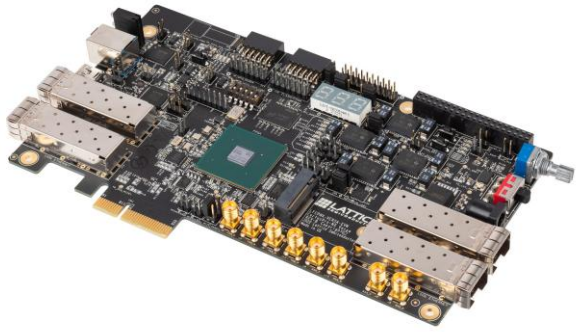


Figure 3.3. CertusPro-NX Versa Board

The CertusPro-NX Versa Board is a flexible FPGA evaluation and development platform based on the CertusPro-NX FPGA (LFCPNX-100-9LFG672I). It enables designers to prototype and validate a wide range of high-performance connectivity and processing use cases. The board extends the FPGA's functionality through multiple industry-standard interfaces, including dual SFP ports supporting 10-Gigabit Ethernet and 1-Gigabit SGMII, two SERDES channels, PCIe Gen3 x4, and a MIPI CSI-2 camera connector, providing robust options for data acquisition and high-speed communication.

The CertusPro-NX Versa Board provides essential development features, including LPDDR4 memory, GPIO indicators, push-buttons, DIP switches, onboard boot flash for configuration storage, and an FT2232H USB-to-JTAG interface for FPGA programming and debugging. These capabilities make the platform well-suited for designing and validating systems that incorporate video bridging, sensor interfaces, networking protocols, and PCIe-based acceleration.

Engineers can leverage extensive expandability through SFP cages, PMOD connectors, Raspberry Pi HAT support, and SERDES access ports, making the Versa Board a versatile hardware platform for edge-AI and sensor-processing applications. The board supports both endpoint and root-port modes for PCIe Gen3, enabling flexible FPGA integration in host-centric systems or deployment as an intelligent controller within distributed architectures. For additional information, refer to the CertusPro-NX Versa Board User Guide (FPGA-EB-02053).

3.2.2. CertusPro-NX Sensor-to-Ethernet Bridge Board

Figure 3.4. CertusPro-NX Sensor-to-Ethernet Bridge Board

The CertusPro-NX Sensor-to-Ethernet Bridge Board is an FPGA-based connectivity platform that links a variety of sensor interfaces to high-speed Ethernet networks. It integrates both CertusPro-NX and CrossLink-NX FPGA devices, enabling flexible sensor data ingestion through AXI-Stream and APB control buses and converting this data into Ethernet packets for downstream processing.

This board is specifically optimized for low-latency, high-throughput sensor streaming, and it seamlessly integrates with the NVIDIA Holoscan Sensor Bridge, providing a complete end-to-end solution for real-time sensor ingestion. The reference design available with the board ensures that data captured at the FPGA's sensor interface reliably arrives in system DRAM, and it supports advanced features such as streaming DMA, transport abstraction, Linux sockets, and ConnectX SmartNIC acceleration using GPUDirect RDMA.

To support high-bandwidth networking, the board provides up to two 10-Gigabit Ethernet channels, enabling the transport of multiple high-rate sensor streams over UDP or other low-latency protocols to hosts such as Jetson AGX Orin or NVIDIA IGX Orin. The platform's open-source software stack, configurable FPGA IP blocks, and programmable system-control framework allow rapid customization of sensor inputs, making the bridge board well-suited for AI-enabled edge systems that require robust sensor fusion. For additional details, refer to the CertusPro-NX Sensor-to-Ethernet Board User Guide (FPGA-EB-02069).

3.3. Hololink IP and Customizable Interfaces

3.3.1. Overview

The NVIDIA Holoscan Sensor Bridge FPGA IP works with the Holoscan software to provide a sensor-agnostic platform that transfers data from various sensors to an Ethernet-connected host.

The Holoscan Sensor Bridge FPGA IP comprises three main components: the Sensor Interface IP, the Hololink IP, and the Host Interface IP. The block diagram of the Holoscan Sensor Bridge FPGA IP is illustrated in Figure 3.5. The Sensor Interface and Host (Ethernet) Interface blocks are implemented using FPGA vendor-specific logic. In this reference design, Lattice Semiconductor is responsible for the integration and maintaining the IP for both the Sensor Interface and Host Interface components.

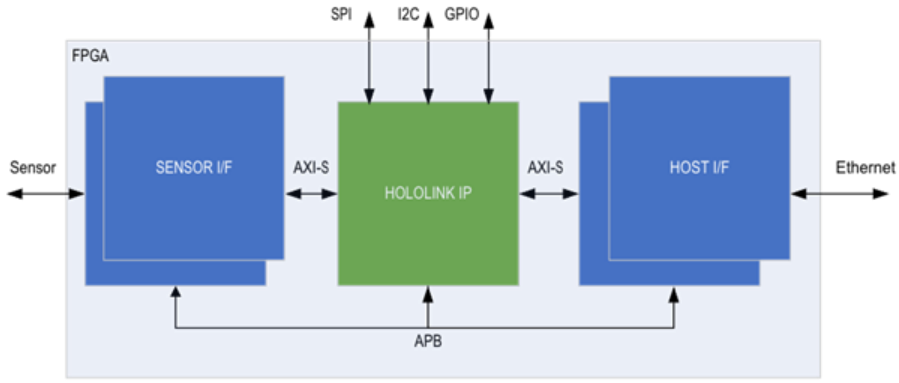


Figure 3.5. Holoscan Sensor Bridge IP in FPGA

The Holoscan Sensor Bridge FPGA IP streamlines FPGA development, offering scalability and configurability to support a wide range of sensor-to-host applications.

Key functions of the Holoscan Sensor Bridge IP include:

- Encapsulation of sensor data: Converts AXI-Stream sensor data into Ethernet UDP AXI-Stream format for host-side processing.
- Network protocol support: Implements BOOTP, ICMP, and NVIDIA-defined Ethernet Control Bus (ECB) protocols.
- Event and control packet transmission: Sends enumeration and control event packets based on predefined conditions.
- Peripheral interface control: Manages SPI, I2C, and GPIO interfaces to configure sensors and other onboard components.

A detail explanation on the Nvidia Hololink IP is provided in the NVIDIA documentation webpage. Search for *Holoscan Sensor Bridge,* and select *v2.5.0* release. You are encouraged to review the document for further understanding. This section provides only an overview of the IP.

3.3.2. Sensor Interface

3.3.2.1. MIPI CSI-2 RX D-PHY Sensor Interface

The customizable MIPI CSI-2 camera sensor interface has two capabilities:

- **Scalability**
  Refers to the ability of the MIPI CSI-2 sensor interface to increase or decrease the number of sensor interfaces based on user platform requirements.
- **Configurability**
  Refers to the ability to configure each camera sensor interface individually, such as setting different MIPI CSI-2 sensor lane and lane rates.

The MIPI CSI-2 RX D-PHY IP serves as the primary interface for MIPI CSI-2 image sensors. Because the reference design targets the LFCPNX-100 device package, only the soft MIPI CSI-2/DSI RX D-PHY IP is supported. This configurable IP block receives MIPI CSI-2 data streams and converts them into 8-bit, 16-bit, or 32-bit parallel data, depending on the lane configuration selected during IP generation.

The IP allows you to set the MIPI CSI-2 lane rate based on the camera sensor's requirements. It also generates an output byte clock derived from the data type and forwards it to the AXIS blocks. If the sensor provides a continuous D-PHY clock, you should disable the RX_FIFO and drive clk_byte_fr_i directly using clk_byte_hs_o.

Compared to the hardened version, the soft MIPI CSI-2 RX D-PHY IP has performance limitations that vary by FPGA family and package. For detailed specifications and configuration guidance, see the CSI-2/DSI D-PHY Rx IP Core User Guide (FPGA-IPUG-02081).

MIPI CSI-2 Raw Data to AXI-Stream Payload

Figure 3.6 shows the block diagram of the MIPI CSI-2 interface, which outputs MIPI CSI-2 RAW data. The interface includes two primary components: the MIPI CSI-2 RX D-PHY IP and the MIPI CSI-2 to AXIS Payload Converter.

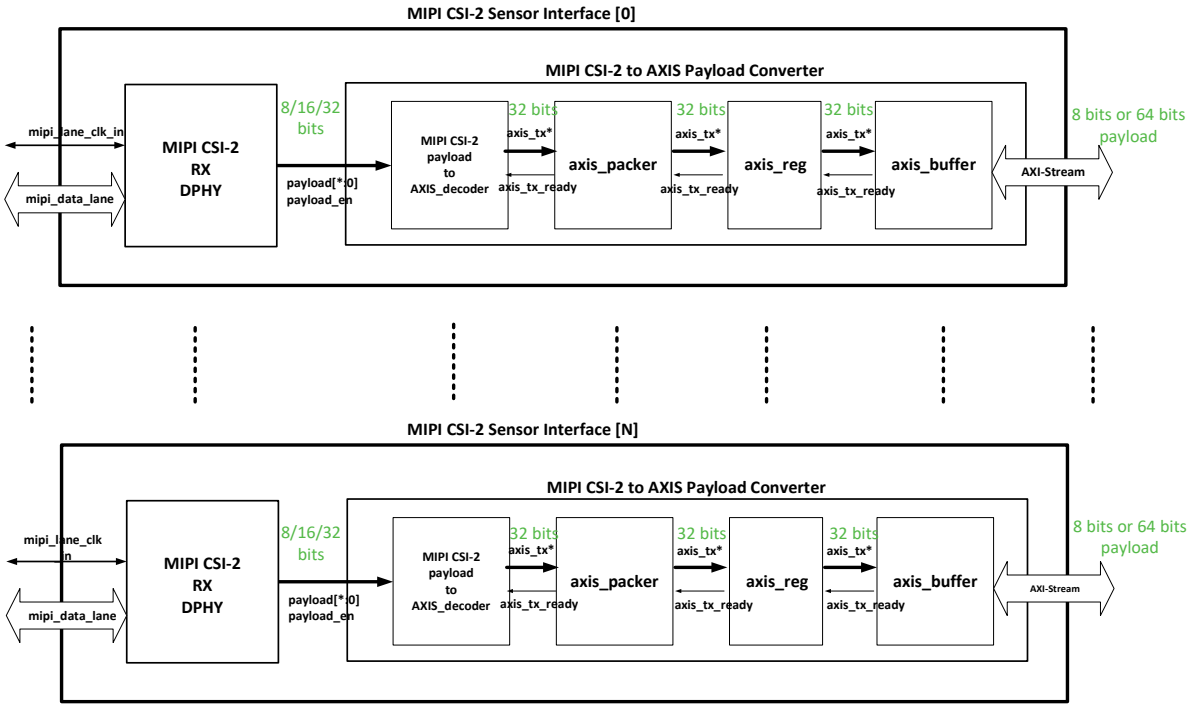


Figure 3.6. Overview block diagram of MIPI CSI-2 interface

The Payload Converter bridges the MIPI CSI-2 protocol and the AXI4-Stream (AXIS) interface. It extracts image data packets from the CSI-2 stream and formats them as AXIS-compatible payloads for subsequent processing. The module supports parallel RAW10 output in 8-bit, 16-bit, or 32-bit formats, as provided by the MIPI CSI-2 RX D-PHY IP. AXIS-compatible payloads follow the data formatting requirements of the AXI4-Stream protocol.

1. Structured data words: Payloads are aligned into fixed-width data words.
   - TDATA[31:0]: Carries the payload of the MIPI CSI-2 RAW10
2. Control signals: Each payload includes AXIS control signals:
   - TVALID: Indicates valid data
   - TREADY: Handshake signal from the receiver
   - TLAST: Marks the end of a frame or packet
   - TKEEP[3:0]: Specifies which bytes in the data word are valid
   - TUSER[1:0] Typically used for user-defined metadata
     - tuser[0] is asserted during cycles containing embedded data (MIPI Data Type = 0x12)
     - tuser[1] is asserted on the final clock cycle of a long packet, indicating the line end signal
   - AXIS Packer Module:

     A key feature of this module is its handling of the TKEEP signal, which indicates the validity of individual bytes within each data word. The AXIS Packer filters out invalid TKEEP bits, ensuring that only valid image data is included in the output stream. This helps maintain data integrity and prevents downstream modules from processing corrupted or incomplete payloads.
   - AXIS REG Module

     The AXIS Reg module acts as a simple register stage within the AXIS data path. Its primary function is to shift and hold one cycle of AXIS data, which helps manage timing, pipeline depth, and synchronization between modules.

- AXIS Buffer Module
  The AXIS Buffer module receives AXI4-Stream data from the AXIS Reg module and transfers it through a dual-clock FIFO (DC_FIFO) to support clock domain crossing (CDC). This enables reliable data movement between components that operate in separate clock domains.
  Key functions include:
  - Data buffering: Temporarily stores AXIS data and control signals to manage timing differences.
  - Clock-domain crossing: Uses a DC_FIFO to safely transfer data between asynchronous clock domains.
  - Flow control: Maintains AXIS protocol integrity using TVALID, TREADY, and TLAST signals across domains.

  The AXIS Buffer module is essential in systems where the CSI-2 receiver and downstream AXIS processing blocks operate on separate clocks, ensuring smooth and reliable data streaming.

3.3.2.2. LVDS DDR Receiver Interface

The CertusPro-NX Sensor-to-Ethernet Bridge design uses the Lattice LVDS DDR Receiver IP to acquire high-speed LVDS-serialized image data from the camera sensor. The IP deserializes the DDR LVDS data stream and outputs pixel-domain parallel video data, which is then passed through the internal processing pipeline to the Ethernet transmission path. LVDS offers reduced signal swing and lower power consumption compared to traditional signaling methods, making it common in modern CMOS image sensors. The interface includes one differential clock pair and multiple differential data pairs, with the clock center-aligned to the data.

In the Holoscan Sensor Bridge architecture, sensor data can enter through two distinct ingestion paths:

- MIPI CSI-2 path: CSI-2 sensors interface with the CrossLink-NX FPGA, which uses its integrated MIPI D-PHY Hard IP to receive and decode CSI-2 data streams.
- LVDS path: LVDS-based sensors connect directly to the CertusPro-NX FPGA, which incorporates the LVDS DDR Receiver IP for high-speed deserialization, word alignment, and RAW10/RAW12 data reconstruction.

Both video streams whether sourced from the CSI-2 or LVDS interface are ultimately delivered to the CertusPro-NX, where they are packetized and transmitted over a 10GbE Ethernet link to an NVIDIA host for Holoscan processing. This functional split enables the Sensor Bridge to support multiple sensor interface standards while maximizing FPGA resource efficiency. Figure 3.7 shows the LVDS DDR receiver interface used in the CertusPro-NX Sensor-to-Ethernet Bridge board.

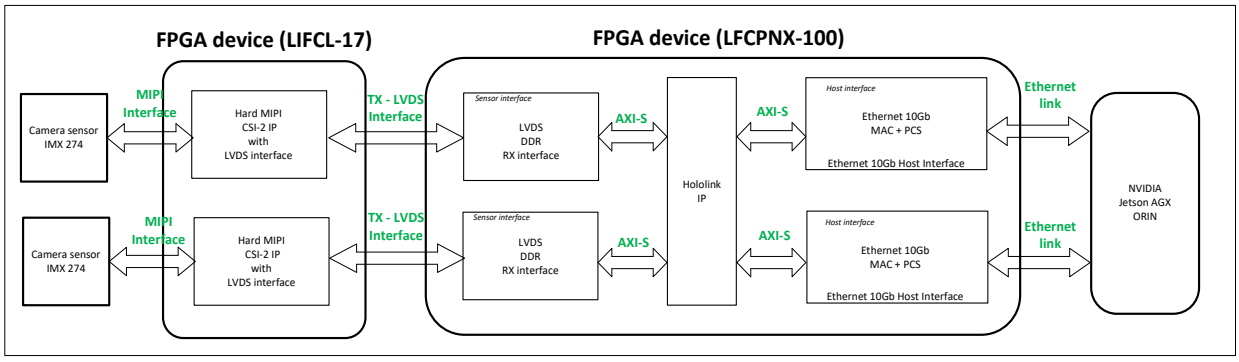


Figure 3.7. LVDS DDR Receiver Interface on the CertusPro-NX Sensor-to-Ethernet Bridge Board

3.3.3. Host Interface through Ethernet Link

The CertusPro-NX device provides high-speed Ethernet connectivity using integrated IP cores and external transceiver modules. This section describes the available 1GbE and 10GbE Ethernet configurations, along with their key components, integration methods, and functional behavior.

3.3.3.1. Ethernet 1GbE Support with 10/100/1000 Mbps SFP Transceiver

The CertusPro-NX device supports 1GbE Ethernet using 10/100/1000BASE-T SFP transceivers. This configuration leverages the Lattice Tri-Speed Ethernet IP, which provides a flexible, robust solution for Ethernet connectivity at 10 Mbps, 100 Mbps, and 1GbE speeds.

Key Components:

- **Tri-Speed Ethernet IP Core**
  Supports MAC + SGMII (SERDES) mode for high-speed serial data transfer. Compliant with IEEE 802.3 and Cisco SGMII standards, it enables auto-negotiation for speed and duplex and includes statistics counters for monitoring.
- **High-Level Block Diagram Components**
  - MAC Core: Handles Ethernet frame processing (CRC checks, filtering) and interfaces with user logic via AXI4-Stream for both transmit and receive paths.
  - SGMII PCS (SERDES): Converts GMII data into serialized differential signals using 8b/10b encoding at 1.25 Gbps. Supports auto-negotiation and link establishment.
  - Host Interface: Configurable via AXI4-Lite, APB, or AHB-Lite for MAC and PCS settings, including speed, duplex mode, and interrupt handling.

The MAC core processes Ethernet frames and passes GMII data to the SGMII PCS, which serializes it for transmission through the SFP transceiver. This architecture ensures reliable, efficient Ethernet communication for embedded applications.

3.3.3.2. Ethernet 10GbE Support with 10GBase-T SFP+ Transceiver

The CertusPro-NX device supports 10GbE Ethernet using SFP+ transceivers, enabling high-speed data communication for bandwidth-intensive applications. The solution integrates multiple IP cores and hardware components.

Key Components:

- **MAC IP Core**
  Manages Ethernet frame-level operations, including encapsulation, CRC generation, and flow control. Interfaces with system logic via AXI or Avalon, depending on the FPGA architecture.
- **PCS IP Core (Physical Coding Sublayer)**
  Handles low-level physical layer functions and interfaces directly with the SFP+ module.
  Features:
  - Encoding/Decoding: Supports 64b/66b schemes.
  - Scrambling/Descrambling: Maintains signal integrity.
  - Clock Data Recovery (CDR): Aligns incoming data with system clock.
  - Link Synchronization: Establishes and maintains stable link.
  - Error Handling: Optional Forward Error Correction (FEC) for enhanced reliability.
- **SFP+ Transceiver Module**
  A compact, hot-swappable module for 10GbE connections.
  Features:
  - Hot-Swappable: Enables module replacement without system shutting down the system.
  - Media Support: Compatible with copper and fiber (such as, SR for short-range, LR for long-range).
  - Diagnostics: Supports real-time monitoring of temperature, power, and signal quality.
  - Transmission range: Varies from a few meters (copper) to tens of kilometers (fiber).

The MAC and PCS IP cores work together to prepare and transmit Ethernet frames through the SFP+ module. This setup ensures high-speed, low-latency communication suitable for advanced networking applications.

3.4. Dual-Boot Feature

Dual Boot allows an FPGA to store and load multiple configuration bitstreams (images) from an external SPI flash. This capability provides a reliable fallback mechanism, ensuring the system remains operational even if a primary or alternate configuration becomes corrupted. In a typical deployment, the FPGA contains a primary bitstream (default boot image) and a golden bitstream (safe recovery image).

Key functional behaviors are described below:

- Normal boot flow:
  Upon power-up, the device attempts to load the primary bitstream. If loading fails, the FPGA automatically falls back to the golden bitstream, ensuring a valid configuration is always active.
- Fallback and robustness:
  If the FPGA fails to load an alternate bitstream, such as when a bitstream is corrupted, it automatically falls back to the golden bitstream.
- External flash address mapping:
  Each bitstream image is assigned to a fixed starting address in SPI flash. These addresses must match those defined in the design (example boot_addr parameters) and in the Radiant Deployment Tool configuration.

For more details on the multi-boot feature on the Nexus platform, refer to the Nexus Multi-Boot User Guide.

3.5. Clocking and Reset Scheme

3.5.1. CertusPro-NX Versa Board

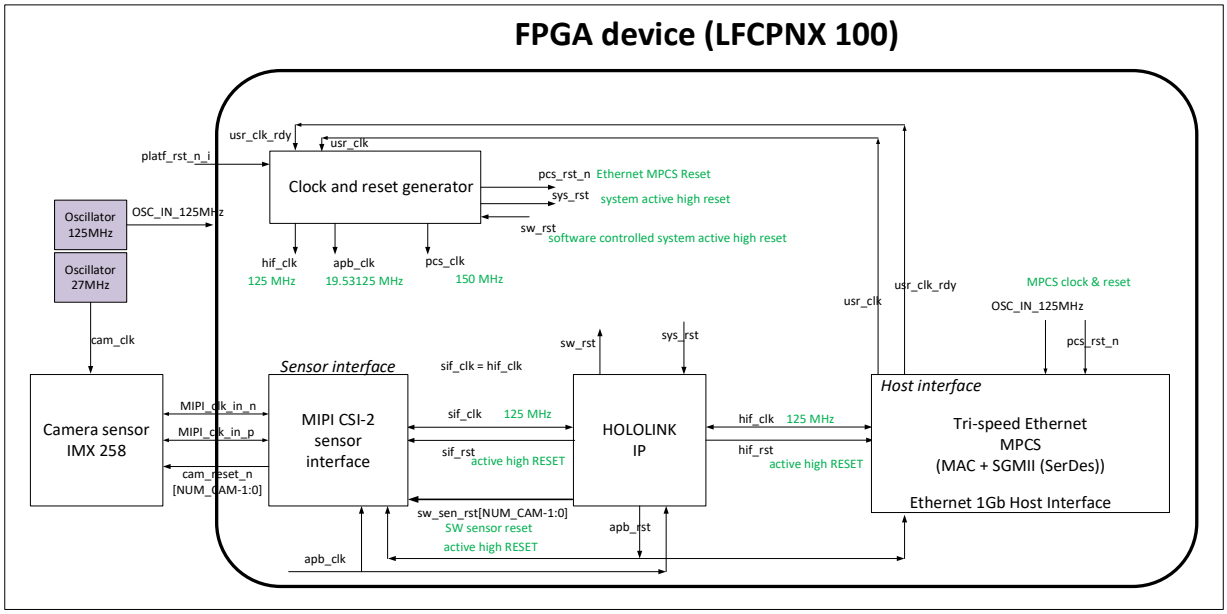


Figure 3.8. Reset and Clock Domain Block Diagram for Ethernet 1GbE

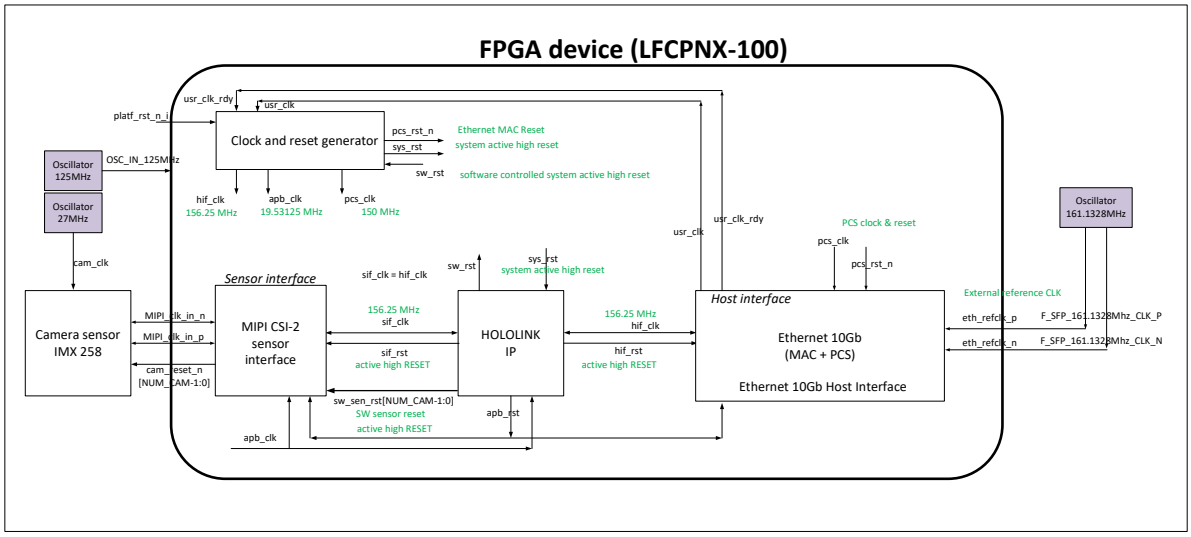


Figure 3.9. Reset and Clock Domain Block Diagram for Ethernet 10GbE

The following tables list the clock frequencies and their distribution.

Table 3.1. Clock Domain Distribution for Reference design with Ethernet 1GbE

Clocks	Frequency (MHz)	Description
usr_clk	125	PCS output clock used as reference clock for the PLL to generate system clocks (such as, apb_clk and hif_clk).
OSC_IN_125MHz	125	Platform clock input used for MPCS IP and debug hook signals.
hif_clk	125	Host interface clock used as AXIS clock for host interface.
sif_clk	125	Directly assigned from hif_clk and is used for the AXIS clock for sensor interface.
apb_clk	19.5313	APB bus clock.

Table 3.2. Clock Domain Distribution for Reference design with Ethernet 10GbE

Clocks	Frequency (MHz)	Description
usr_clk	322.266	PCS output clock is used as reference clock for the PLL to generate system clocks (such as, apb_clk and hif_clk).
pcs_clk	150	PCS calibration clock.
OSC_IN_125MHz	125	Platform clock input used for debug hook signals.
hif_clk	156.25	Host interface clock used as AXIS clock for host interface.
sif_clk	156.25	Directly assigned from hif_clk and is used as the AXIS clock for sensor interface.
apb_clk	19.5313	APB bus clock.

Table 3.3. Reset Distribution applicable for both Ethernet 10GbE and 1GbE

Clocks	Description
sw_sen_rst[NUM_CAM-1:0]	Register-controlled sensor reset. The reset signal width increases based on the number of assigned cameras. Details are discussed in the Customizing the Reference Design section.
sw_sys_rst	Register-controlled system reset. Used to reset system-level logic. Also triggers reset for hif_rst, apb_rst, and sif_rst.
apb_rst	Reset APB logic
hif_rst	Reset Host logic
sif_rst	Reset Sensor logic

3.5.2. CertusPro-NX Sensor-to-Ethernet Bridge Board

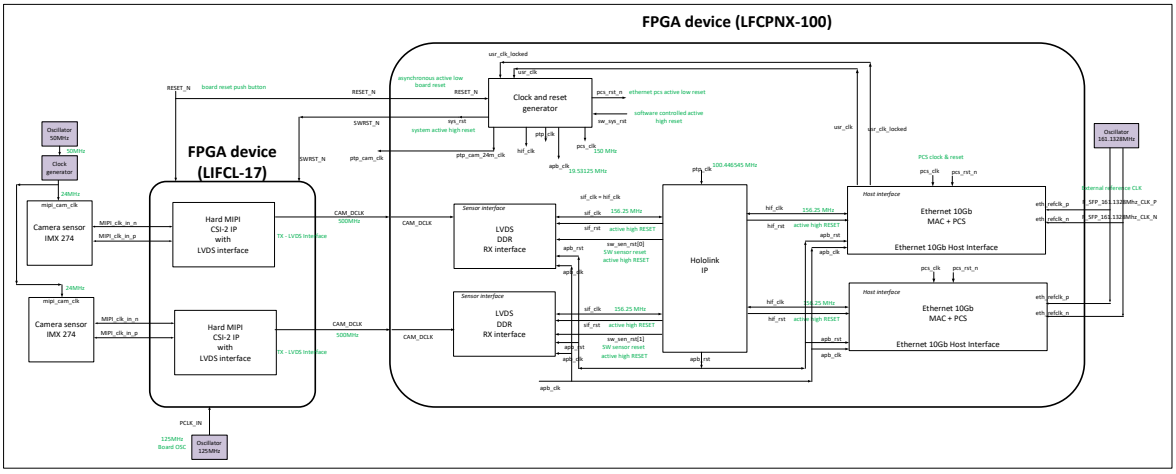


Figure 3.10. Reset and Clock Domain Block Diagram

The following table lists the clock frequencies and their distribution.

Table 3.4. Clock Domain Distribution for CertusPro-NX Sensor-to-Ethernet Bridge Board

Clocks	Frequency (MHz)	Description
mipi_cam_clk	24	Camera sensor clock is generated by the platform oscillator and divider.
PCLK_IN	125	Platform input clock.
CAM_DCLK[1:0]	500	CAM_DCLK is LVDS data clock which is generated in Crosslink-NX device via PLL with the reference clock = PCLK_IN.
usr_clk	322.266	PCS output clock use as reference clock for the PLL to generate system clocks (such as, apb_clk and hif_clk).
pcs_clk	150	PCS calibration clock.
hif_clk	156.25	Host interface clock used as AXIS clock for host interface.
sif_clk	156.25	Directly assigned from hif_clk and is used as the AXIS clock for sensor interface.
apb_clk	19.5313	APB bus clock.

Table 3.5. Reset Distribution for CertusPro-NX Sensor-to-Ethernet Bridge Board

Reset	Description
RESET_N	Platform push button reset.
SWRST_N	System reset which reset the CrossLink-NX device.
sw_sys_rst	Register-controlled software system reset. Used to reset system-level logic. Also triggers reset for hif_rst, apb_rst, and sif_rst.
apb_rst	Reset APB logic
hif_rst	Reset Host logic
sif_rst	Reset Sensor logic

4. Customizing the Reference Design

4.1. Customization Steps for the Reference Design

This section provides a detailed walkthrough of the steps required to configure the reference design and to verify the customized reference design. Figure 4.1 illustrates the steps involved to enable customization and support for various customer-specific configurations. Detailed explanation is provided in this section. However, details on reference design compilation and implementation are covered separately in Compiling the Reference Design section and Implementing the Reference Design section.

The screenshots provided in this section are for reference only. The details may vary depending on the version of the IP or software being used.

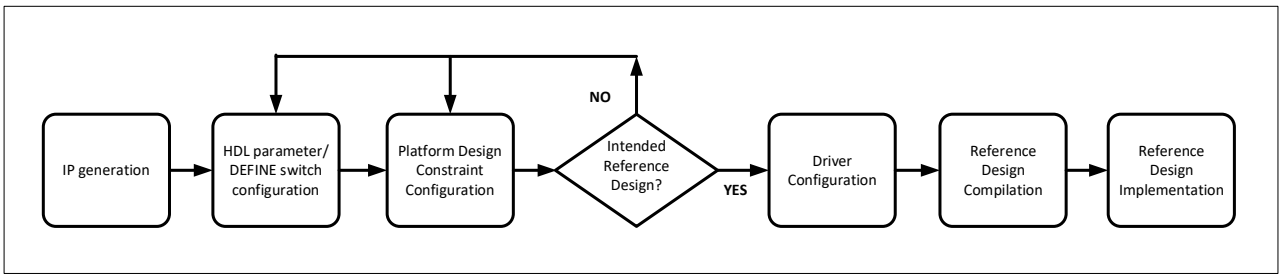


Figure 4.1. Steps Flow to Customize and Verify the Reference Design

4.1.1. Selecting the Holoscan Sensor Bridge Board

Customization of the reference design depends on the target hardware platform. The design can be implemented on Lattice-provided platforms—such as the CertusPro-NX Versa Board or the CertusPro-NX Sensor-to-Ethernet Bridge Board—or on a user-designed custom platform. In this reference design, several HDL parameters are preset for specific platforms to simplify integration; these mappings are described in later sections. Users developing custom platforms may define additional parameters as needed to meet their system requirements.

4.1.2. Generating the IP

4.1.2.1. MIPI CSI-2 RX D-PHY IP Generation

The reference design enables the MIPI CSI-2 RX D-PHY IP to interface with MIPI CSI-2 camera sensors. Two configuration methods are supported:

Method 1: Runtime configuration of the MIPI CSI-2 IP

To support runtime configuration, the MIPI CSI-2 RX D-PHY IP is initially set to a high-speed default configuration. This ensures that the IP can be reconfigured to lower operating settings during system runtime. Table 4.1 lists the default parameters applied for runtime configuration.

A key limitation of this approach is the longer FPGA compilation time. Because the design must accommodate the highest-speed MIPI CSI-2 RX D-PHY settings, the Place-and-Route process requires significantly more time to close timing, resulting in noticeably longer bitstream-generation cycles.

Table 4.1. Selected Runtime Configuration for MIPI CSI-2 RX D-PHY IP

MIPI Lane Rate (Mbps)	MIPI Lane Number	MIPI RX D-PHY IP name
1500	4 lanes	mipi_csi2_rx_dphy_flex.ipx

Method 2: Preset configuration of the MIPI CSI-2 IP

The MIPI CSI-2 RX D-PHY IP is generated based on the specifications of the camera sensor being used. The key parameters to configure includes:

- Number of data lanes
- MIPI lane rate
- Gear Ratio (fixed to 8)
- MIPI synchronizer clock frequency (fixed to 150 MHz)

These parameters must be correctly set before generating the IP to ensure compatibility with the camera sensor. The gear ratio for the CertusPro-NX family device is fixed at 8, and the MIPI synchronizer clock frequency in the reference design is set to 150 MHz. The reference design also provides preconfigured MIPI CSI-2 RX D-PHY IPs for users to choose from. The table shows the available IP configuration option that the user can select. The IP is selected based on user settings, which will be explained in the HDL Parameter and Define Switch Configuration section.

Table 4.2. MIPI CSI-2 RX D-PHY IP configuration options

MIPI Lane Rate (Mbps)	MIPI Lane Number	MIPI RX D-PHY IP name
720	1 lane	mipi_csi2_rx_DPHY_720Mbps_1L.ipx
	2 lanes	mipi_csi2_rx_DPHY_720Mbps_2L.ipx
	4 lanes	mipi_csi2_rx_DPHY_720Mbps_4L.ipx
960	2 lanes	mipi_csi2_rx_DPHY_960Mbps_2L.ipx
	4 lanes	mipi_csi2_rx_DPHY_960Mbps_4L.ipx
1440	4 lanes	mipi_csi2_rx_DPHY_1440Mbps_4L.ipx
1500	4 lanes	mipi_csi2_rx_DPHY_1500Mbps_4L.ipx

4.1.2.2. LVDS Image Sensor Receiver Interface IP

The Lattice LVDS (Low Voltage Differential Signaling) DDR Receiver IP is specifically used for the CertusPro-NX Sensor-to-Ethernet Bridge board. The Lattice LVDS DDR Receiver IP's configuration is shown in Figure 4.2.

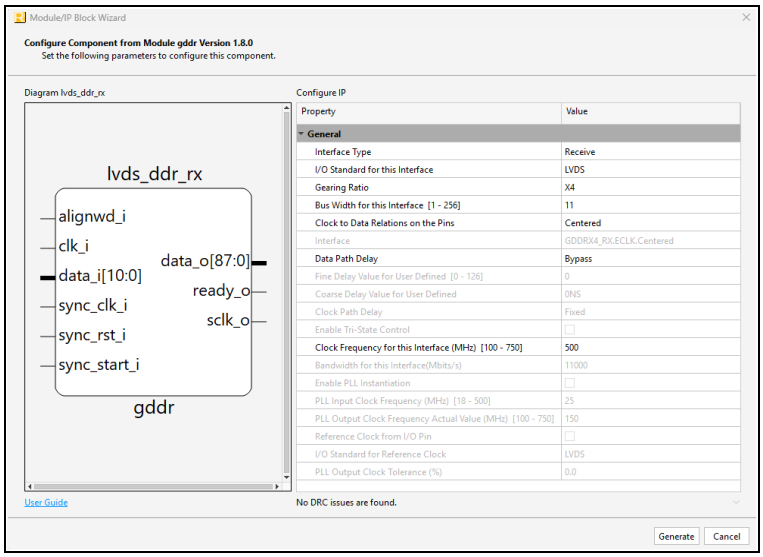


Figure 4.2. MIPI CSI-2 RX D-PHY IP Generation Module

4.1.2.3. Hololink IP

Hololink IP is owned by NVIDIA, and updates the latest Hololink IP source code on GitHub at the following link, GitHub - nvidia-holoscan/holoscan-sensor-bridge at 2.5.0. Currently, the reference design integrates the latest available Hololink IP, which is version 2511.

4.1.2.4. Ethernet IP Generation

Specific Ethernet IPs are required to support 1GbE or 10GbE link speeds in the CertusPro-NX FPGA device. To support a 1GbE link speed, the Tri-speed Ethernet v2.1.0 (MAC + SGMII (SERDES) IP is used. To support Ethernet 10GbE link speed, the Ethernet PCS IP Core v1.3.0 and MAC IP Core v1.1.0 are used. The Ethernet Lane ID must be correctly set (Lane ID = 6) to meet the platform requirements for the CertusPro-NX Versa Evaluation Board before generating the IP. For the CertusPro-NX Sensor-to-Ethernet Bridge board, the Ethernet PCS lane ID must bet set to 2 and 3 respectively as two Ethernet ports are used. Figure 4.3 shows the Tri-speed Ethernet v2.1.0 (MAC + SGMII (SERDES)) IP generation for 1GbE Ethernet link-speed support. Figure 4.4 shows the Ethernet 10GbE MAC IP generation, and Figure 4.5 shows the Ethernet 10GbE PCS IP generation module's GUI.

Note: IP versions may vary as they are updated periodically. The figures below are for illustration purposes.

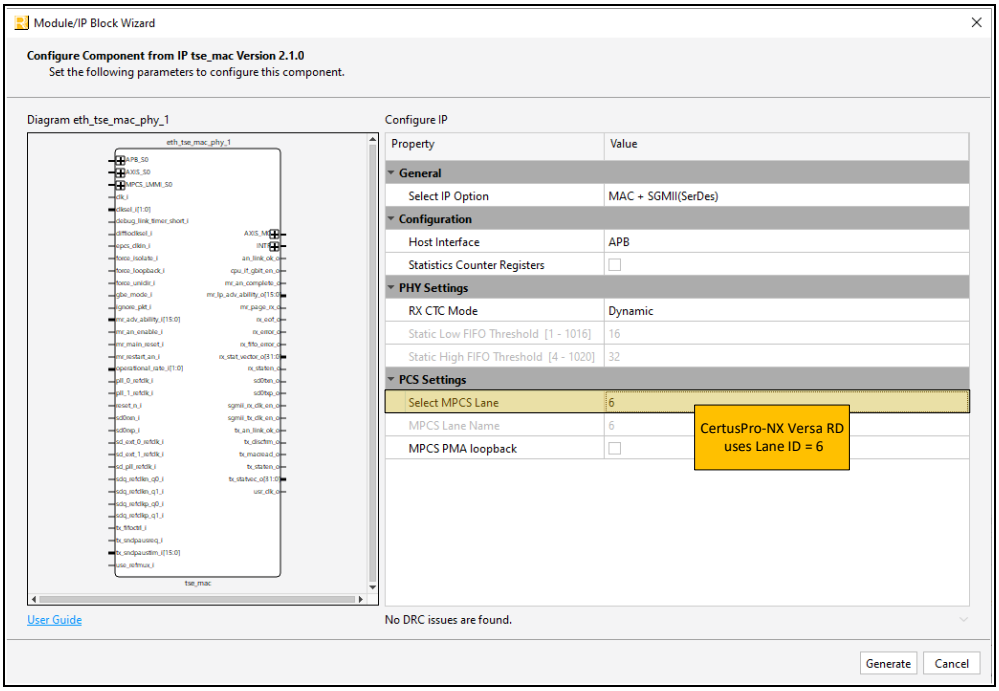


Figure 4.3. Ethernet 1GbE (MAC + SGMII SERDES) IP Generation

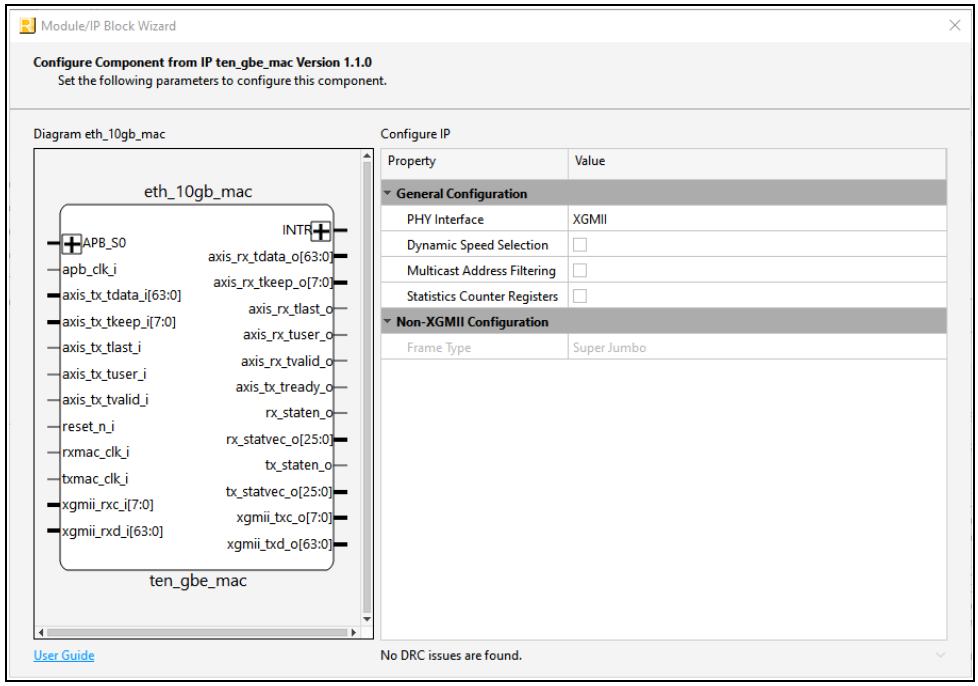


Figure 4.4. Ethernet 10GbE MAC IP Generation

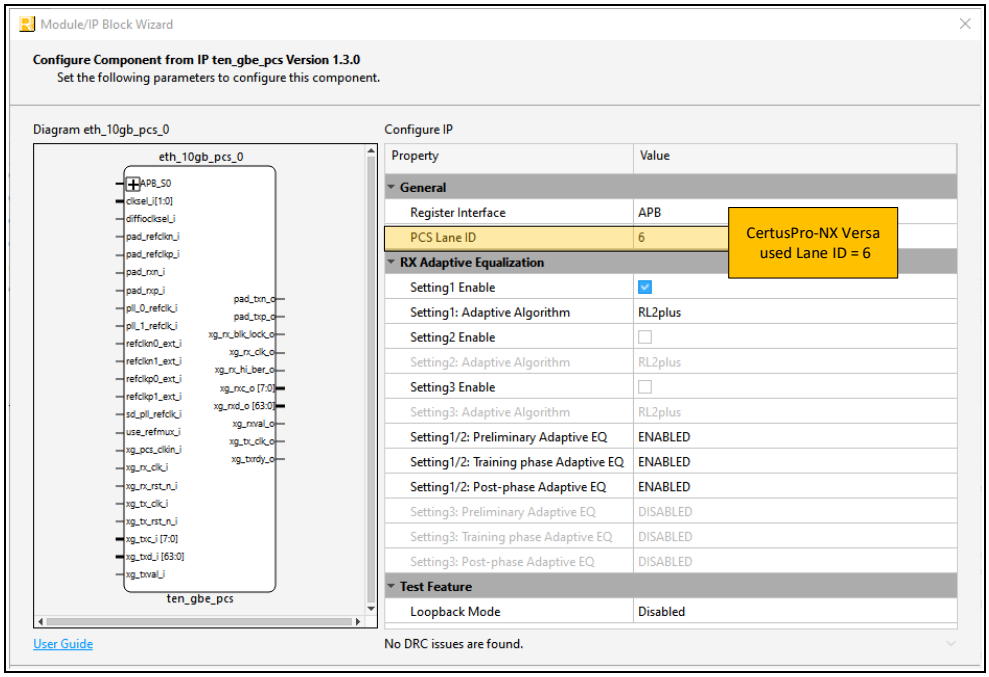


Figure 4.5. Ethernet 10GbE PCS IP Generation

4.1.3. Configuring the HDL Parameter and DEFINE Switch

Configure the HDL parameters and Define switches to reflect the desired hardware setup. These configurations modify the HDL design prior to compilation and affect the following aspects:

- Number of camera sensor interfaces
- MIPI CSI-2 configuration
  - Method 1: Runtime configuration of the MIPI CSI-2 IP
  - Method 2: Preset configuration of the MIPI CSI-2 IP (configure number of lanes per camera sensor and MIPI lane rate used for each camera sensor)
- Number of camera reset outputs
- I2C control peripherals for each camera sensor
- AXI-Stream ports connecting the sensor interface to the Hololink IP
- AXI-Stream ports connecting the Hololink IP to the host interface (Ethernet link)
- Ethernet link speed: 1GbE or 10GbE
- Number of Ethernet links used as host interface
- Ethernet PCS lane ID configuration

These changes should be made in the DEFINE file to ensure proper integration. The DEFINE file differs for each HSB platform and is located at the following paths:

```
<project_name>/radiant/rtl/hsb_cpnx/top/versa_top/HOLOLINK_def.svh
<project_name>/radiant/rtl/hsb_cpnx/top/2chip_top/HOLOLINK_def.svh
```

Configurations such as cameras reset outputs, I2C camera controls, and AXI-Stream ports for the sensor/host interface are automatically configured based on the number of camera sensors and assigned Ethernet 1GbE or 10GbE links. Figure 4.6 shows the DEFINE switches that need to be changed in HOLOLINK_def.svh file. These settings must be carefully configured to ensure the HDL design reflects the intended hardware setup and supports the required camera sensor interfaces.

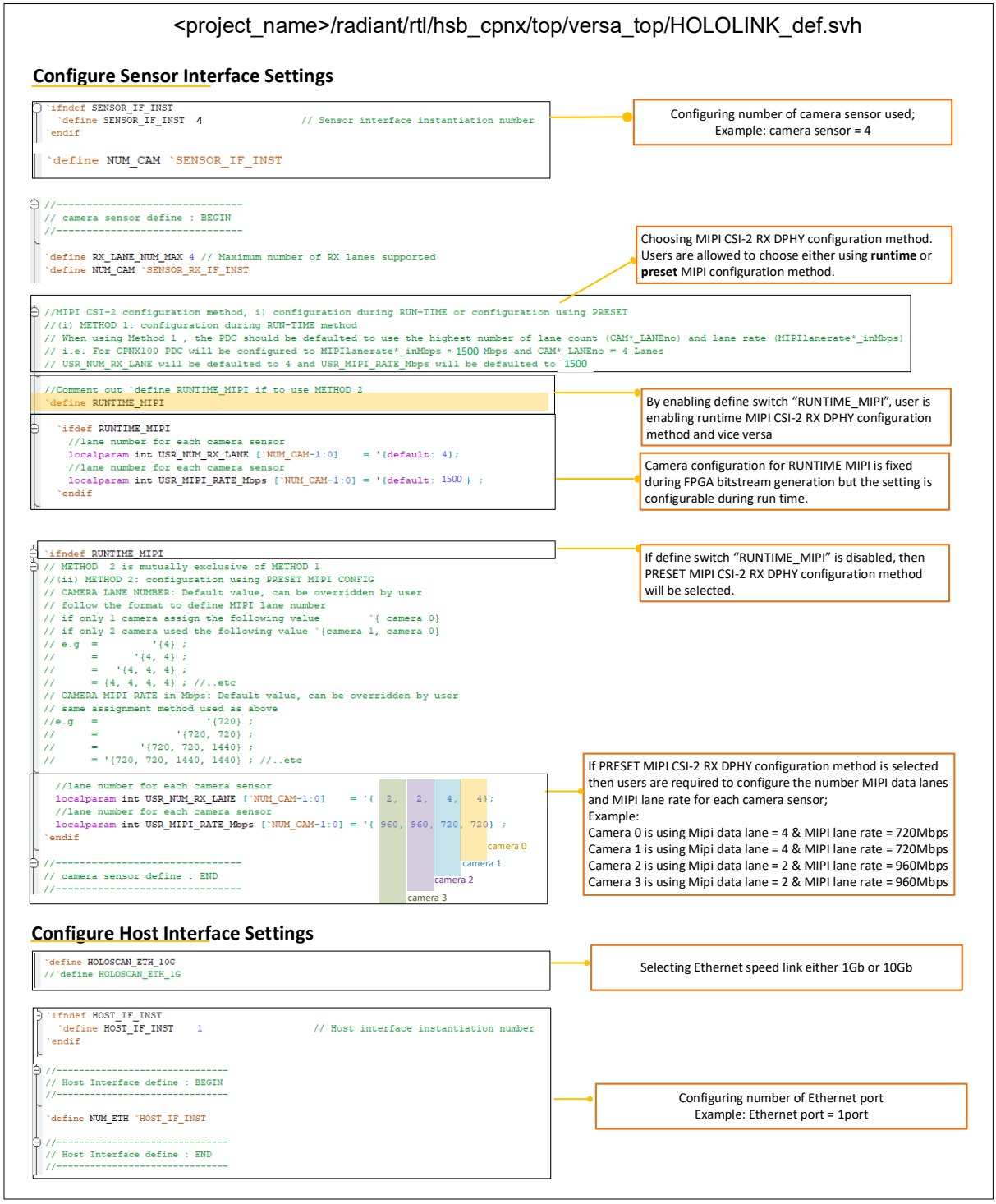


Figure 4.6. Define Switch Setting in HOLOLINK_def.svh File

Note: Figure 4.6 screenshot shows an example setting of four camera sensors. If more or less cameras are required for the intended reference design, the array size for USR_NUM_RX_LANE[`NUM_CAM-1:0] and USR_MIPI_RATE_Mbps[`NUM_CAM-1:0] change. Therefore, the data assigned to it are trimmed or added based on the intended camera number usage.

4.1.4. Configuring the Platform Design Constraint

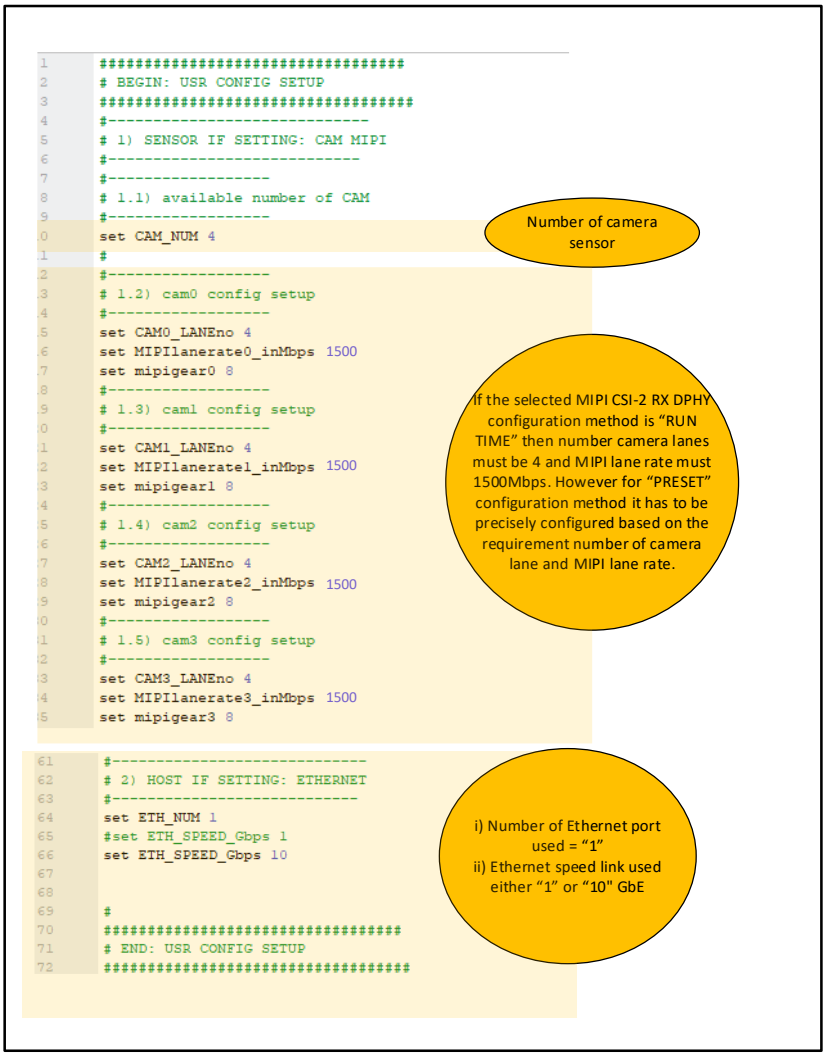
Once the HDL design configuration is finalized, platform design constraints in the PDC file are updated. PDC template files are provided for the relevant reference designs and their location in the project folder is stated in Table 4.3.

Table 4.3. PDC Template Files

Reference design	PDC template file location
CertusPro-NX Versa Board	<project_name>/radiant/pdc/hsb_cpnx_versa.pdc
CertusPro-NX Sensor to Ethernet Board	<project_name>/radiant/pdc/hsb_cpnx_2chip.pdc

Use the runtime MIPI CSI-2 RX D-PHY configuration method only when the PDC file sets the MIPI parameters as follows:

- MIPI lane rate: 1500 Mbps
- MIPI lane count: 4




```
1  ###################################
2  # BEGIN: USR CONFIG SETUP
3  ###################################
4  #-----------------------------
5  # 1) SENSOR IF SETTING: CAM MIPI
6  #-----------------------------
7  #------------------
8  # 1.1) available number of CAM
9  #------------------
10 set CAM_NUM 4
11 #
12 #------------------
13 # 1.2) cam0 config setup
14 #------------------
15 set CAM0_LANEno 4
16 set MIPIlanerate0_inMbps 1500
17 set mipigear0 8
18 #------------------
19 # 1.3) cam1 config setup
20 #------------------
21 set CAM1_LANEno 4
22 set MIPIlanerate1_inMbps 1500
23 set mipigear1 8
24 #------------------
25 # 1.4) cam2 config setup
26 #------------------
27 set CAM2_LANEno 4
28 set MIPIlanerate2_inMbps 1500
29 set mipigear2 8
30 #------------------
31 # 1.5) cam3 config setup
32 #------------------
33 set CAM3_LANEno 4
34 set MIPIlanerate3_inMbps 1500
35 set mipigear3 8

61 #-----------------------------
62 # 2) HOST IF SETTING: ETHERNET
63 #-----------------------------
64 set ETH_NUM 1
65 #set ETH_SPEED_Gbps 1
66 set ETH_SPEED_Gbps 10
67
68
69 #
70 ###################################
71 # END: USR CONFIG SETUP
72 ###################################
```

Figure 4.7. PDC File Setting for CertusPro-NX Versa Board

Figure 4.7 shows the PDC file settings for the number of camera sensors, data lane, and lane rates used for each camera sensor, as well as the number of Ethernet ports and link speed, configurable to 1GbE or 10GbE. If fewer cameras are used, the lane numbers for undefined cameras will be ignored. For example, if the number of cameras is 1, the lane number values set for cameras 2, 3, and 4 will be ignored.

The steps to update the platform design constraints include:

- Pin assignment at the top level of the HDL design
- Defining timing constraints

Proper configuration of these constraints is essential to produce the intended reference design. However, the PDC file template provided with the reference design allows users to choose 1, 2, 3, or 4 camera sensors.

4.1.4.1. Pin Assignment for MIPI CSI-2 Camera Sensor Interface

In this section, the focus is solely on the MIPI CSI-2 camera sensor interface. The pins that need to be updated at the HDL top level are the camera MIPI clock lane, camera MIPI data lane, camera sensor reset, and camera I2C control. Special attention is required for the MIPI data lane assignment due to the use of two-dimensional array coding method at the HDL top-level design.

MIPI clock and data lanes are differential signals, and the pins assigned to them must be high-speed differential I/O types. For CertusPro-NX FPGAs, the typical I/O type used for MIPI clock and data lanes is LVDS (Low Voltage Differential Signaling) I/O pairs. Special handling is required when setting pin assignments for MIPI data lanes, as the reference design's top level uses a two-dimensional array coding method. This affects how the assignments are defined and mapped in PDC file. Table 4.4 illustrates the correct pin assignment approach under these conditions in the PDC file up to four cameras.

Table 4.4. PDC pin assignment for 2D Array for MIPI Data Lane

Camera	SystemVerilog Pin Name	PDC Mapped Pin Name
Camera 0	mipi_cam_data_p[0][0]	mipi_cam_data_p[0]
	mipi_cam_data_n[0][0]	mipi_cam_data_n[0]
	mipi_cam_data_p[0][1]	mipi_cam_data_p[1]
	mipi_cam_data_n[0][1]	mipi_cam_data_n[1]
	mipi_cam_data_p[0][2]	mipi_cam_data_p[2]
	mipi_cam_data_p[0][2]	mipi_cam_data_n[2]
	mipi_cam_data_p[0][3]	mipi_cam_data_p[3]
	mipi_cam_data_p[0][3]	mipi_cam_data_n[3]
Camera 1	mipi_cam_data_p[1][0]	mipi_cam_data_p[4]
	mipi_cam_data_n[1][0]	mipi_cam_data_n[4]
	mipi_cam_data_p[1][1]	mipi_cam_data_p[5]
	mipi_cam_data_n[1][1]	mipi_cam_data_n[5]
	mipi_cam_data_p[1][2]	mipi_cam_data_p[6]
	mipi_cam_data_p[1][2]	mipi_cam_data_n[6]
	mipi_cam_data_p[1][3]	mipi_cam_data_p[7]
	mipi_cam_data_p[1][3]	mipi_cam_data_n[7]
Camera 2	mipi_cam_data_p[2][0]	mipi_cam_data_p[8]
	mipi_cam_data_n[2][0]	mipi_cam_data_n[8]
	mipi_cam_data_p[2][1]	mipi_cam_data_p[9]
	mipi_cam_data_n[2][1]	mipi_cam_data_n[9]
	mipi_cam_data_p[2][2]	mipi_cam_data_p[10]
	mipi_cam_data_p[2][2]	mipi_cam_data_n[10]
	mipi_cam_data_p[2][3]	mipi_cam_data_p[11]
	mipi_cam_data_p[2][3]	mipi_cam_data_n[11]

Camera	SystemVerilog Pin Name	PDC Mapped Pin Name
Camera 3	mipi_cam_data_p[3][0]	mipi_cam_data_p[12]
	mipi_cam_data_n[3][0]	mipi_cam_data_n[12]
	mipi_cam_data_p[3][1]	mipi_cam_data_p[13]
	mipi_cam_data_n[3][1]	mipi_cam_data_n[13]
	mipi_cam_data_p[3][2]	mipi_cam_data_p[14]
	mipi_cam_data_p[3][2]	mipi_cam_data_n[14]
	mipi_cam_data_p[3][3]	mipi_cam_data_p[15]
	mipi_cam_data_p[2][3]	mipi_cam_data_n[15]

4.1.4.2. Timing Constraint for MIPI CSI-2 Camera Sensor Interface

Using the PDC template from reference design, you can configure the timing constraint for the MIPI CSI-2 camera sensor interface by assigning the MIPI lane rate, as shown in Figure 4.7. In the PDC file, this value will be used to assign the timing constraint required for the MIPI clock input.

4.1.5. Verifying the Reference Design Configuration

You are expected to verify whether the configured setting delivers the target reference design. There are two steps required for you to verify: first, check the Lattice Radiant software's hierarchy list to confirm the selected camera number and camera configuration. Secondly, you need to check the clock summary details in the timing analysis report to ensure the assigned timing constraint matches the target configuration. Figure 4.8 shows a screenshot of the reference design implemented on the CertusPro-NX Versa Board. If the verified design is not the target reference design, then you are required to review the HDL parameters, DEFINE switch configuration, and PDC configuration.

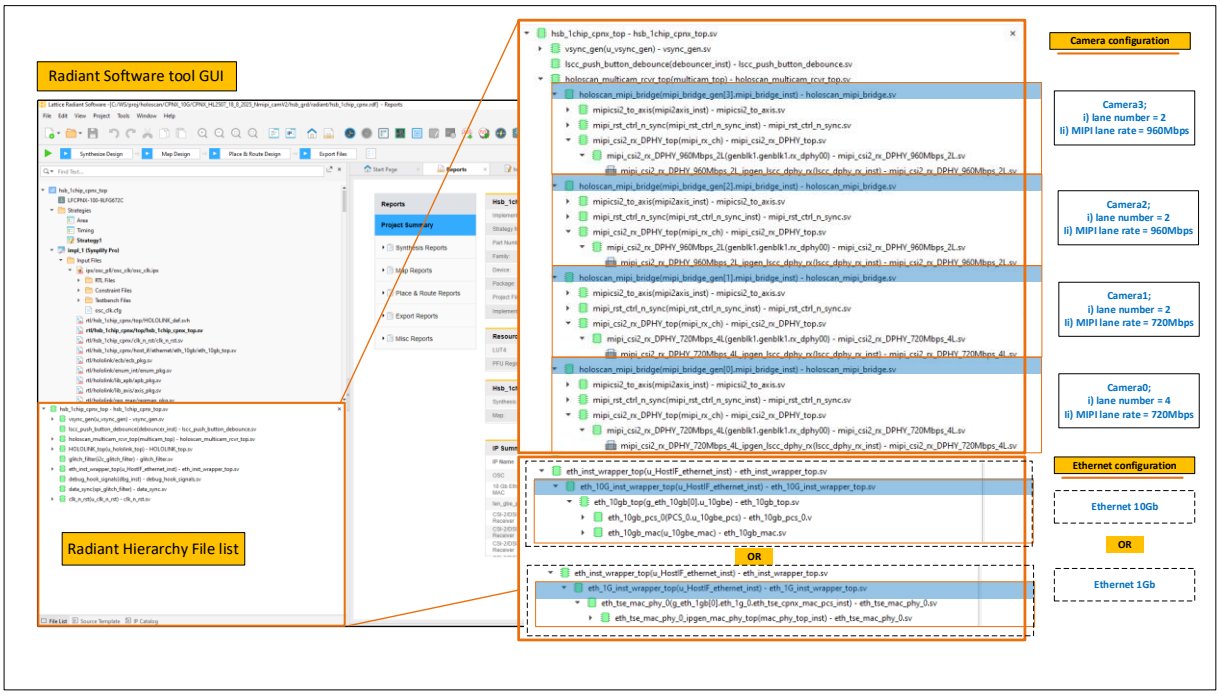


Figure 4.8. Screenshot of Lattice Radiant Software Hierarchy File List

4.1.6. Configuring the MIPI CSI-2 D-PHY IP at Runtime

The MIPI CSI-2 RX D-PHY IP supports runtime configuration of the MIPI lane count and lane rate through the software driver API. Below are the steps to configure the runtime MIPI CSI-2 RX D-PHY IP:

1. Enabling Runtime Configuration

   Enable runtime control by adding the RUNTIME_MIPI preprocessor macro to:

   `<project_name>/radiant/rtl/hsb_cpnx/top/versa_top/HOLOLINK_def.svh`

   See Figure 4.9.

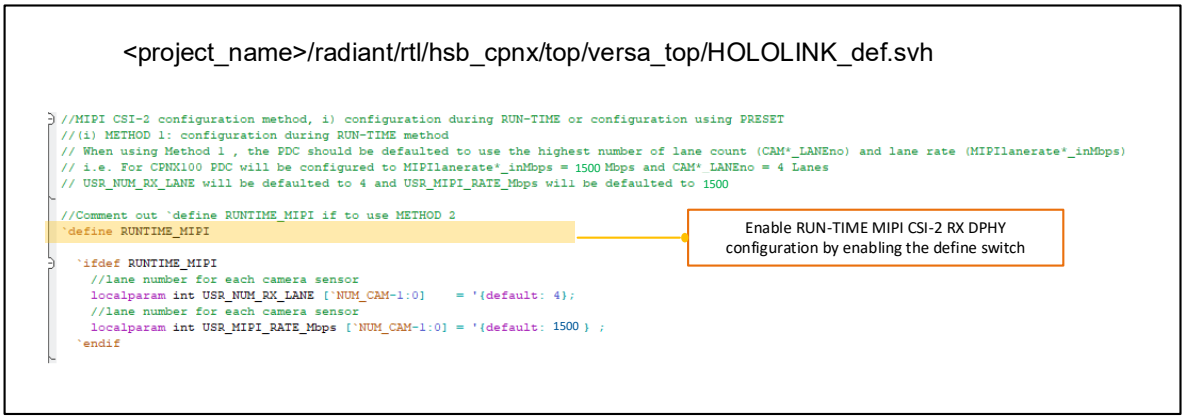


Figure 4.9. Preprocessor Macro to Enable Runtime MIPI CSI-2 D-PHY IP

2. Configuring Runtime Parameters

   After runtime configuration is enabled, use the configure_mipi_lane driver API to set the desired lane count and lane rate through the Control and Status Register (CSR). Figure 4.10 shows an example configuration for a four-lane, 720-Mbps setup using the script located at:

   `<holoscan-sensor-bridge>/examples/linux_imx258_player.py.`

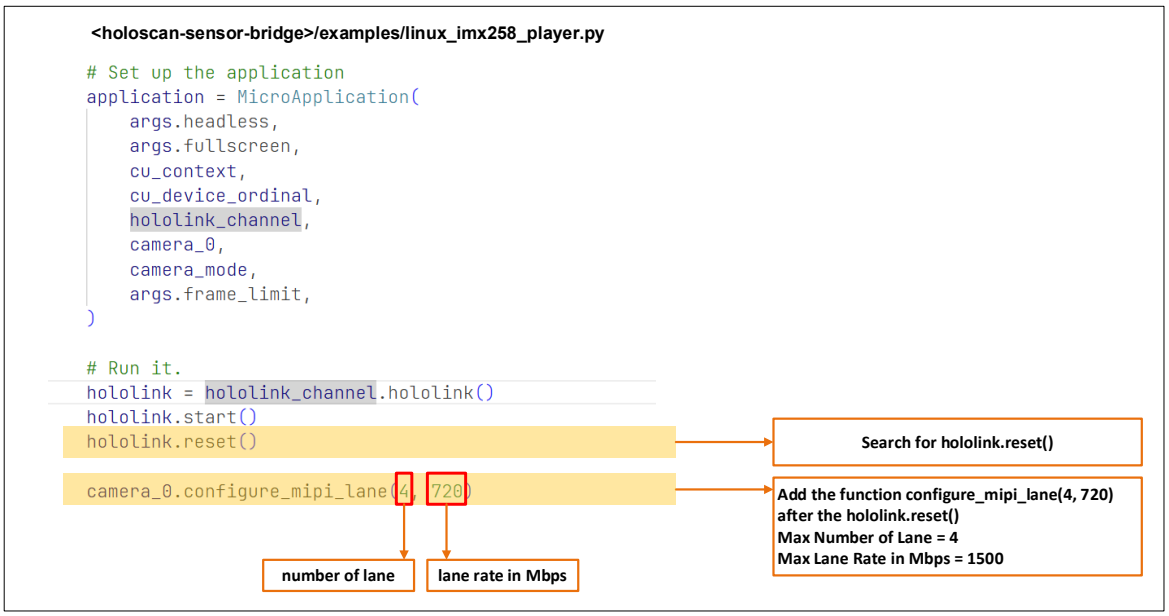


Figure 4.10. Configuring Runtime MIPI using Software Driver API

4.1.7. Configuring the Driver and Applying the Patch

The driver configuration must be adapted for the specific reference design. Because each camera sensor uses distinct I2C control signals, the driver must be updated to correctly detect and communicate with the intended sensor, ensuring proper initialization and operation.

Configuration support for the IMX258 sensor is described in the Applying Patch to Support the IMX258 Camera Module section. To enable this support, follow the procedure outlined from Configuring the AGX Orin Developer Host Kit through Applying Patch to Support the IMX258 Camera Module section.

4.2. Customizing the Reference Design for the CertusPro-NX Versa Board

Figure 4.11 shows an overview of a configured CertusPro-NX Versa board block diagram.

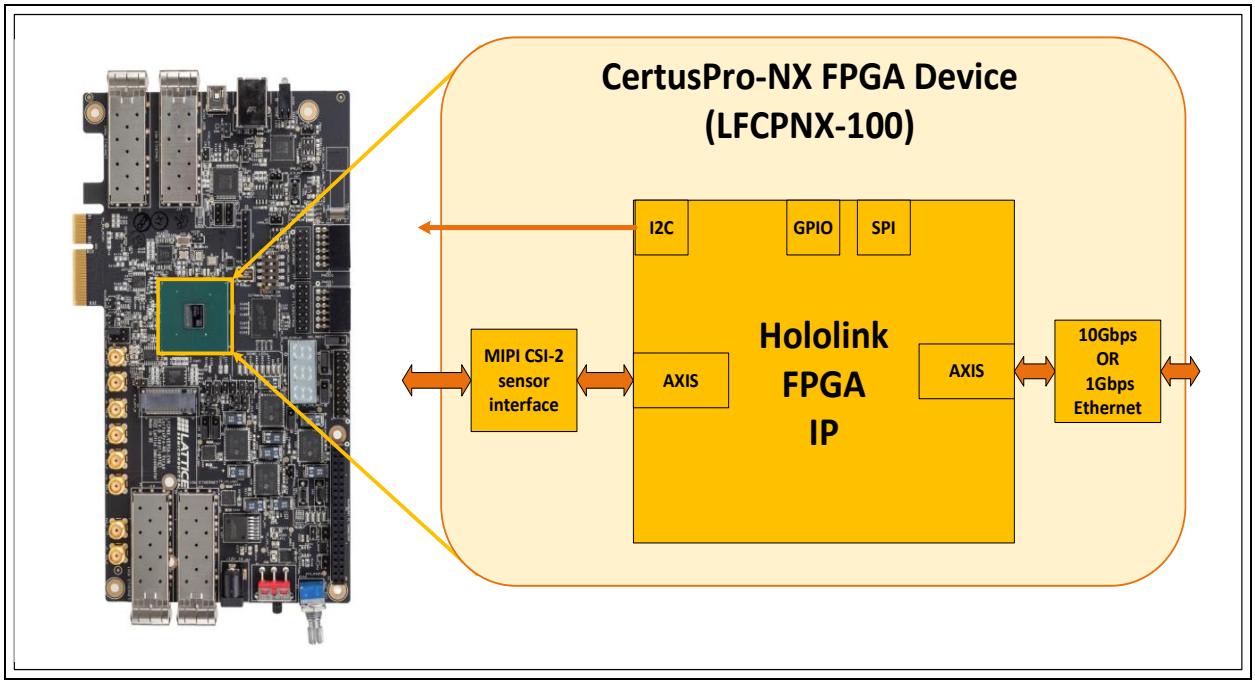


Figure 4.11. CertusPro-NX Versa Board Block Diagram

Table 4.5 shows the configuration required for the reference design to fit onto the CertusPro-NX Versa Board

Table 4.5. Configuration for the reference design to fit into the CertusPro-NX Versa Board

Sensor / Host Interface	Features		Configuration
Camera sensor interface	Number of camera sensors		1
	Preset MIPI configuration method		—
	1	Camera 0: MIPI lane number	4
	2	Camera 0: MIPI lane rate	720 Mbps
Ethernet Link	Number of Ethernet port		1
	Ethernet link speed		1GbE or 10GbE

To customize the reference design, follow the steps below.

Note: This reference design is already integrated with a preset MIPI RX D-PHY IP configuration, latest Hololink IP version 2511, and Ethernet IPs.

1. Customize the reference design to match the CertusPro-NX Versa board specifications.
2. Configure HDL Parameter and DEFINE Switch.

   The reference design need to be configured by changing the settings of the HDL parameter and DEFINE switch to meet the CertusPro-NX Versa board requirement using this file:

   `<project_name>/radiant/rtl/hsb_cpnx/versa_top/HOLOLINK_def.svh`

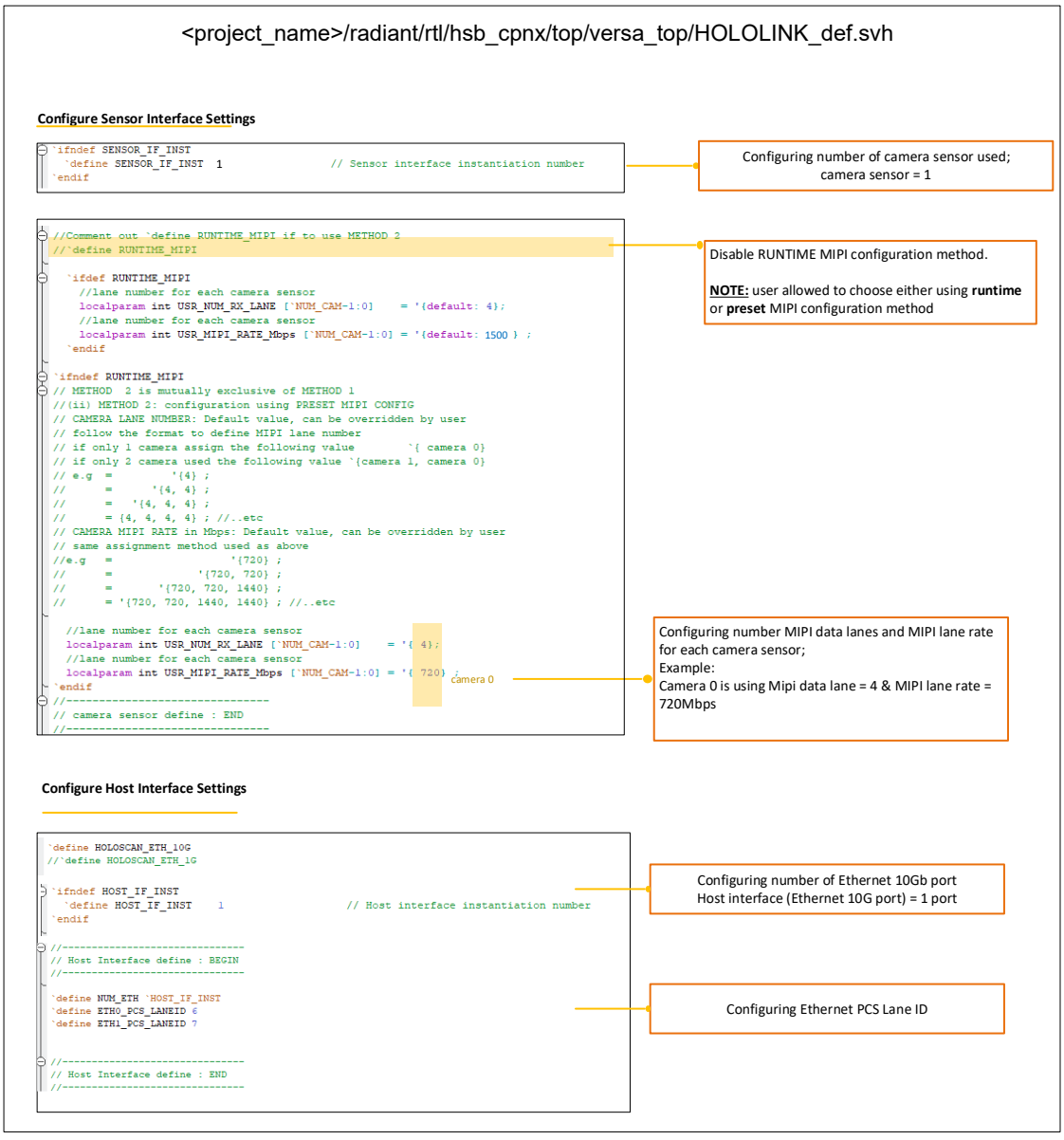


Figure 4.12. Required HDL Parameter and DEFINE Switch Configuration

3. Review the PDC configuration file.

   Figure 4.13 shows a screenshot of the *<project_name>/radiant/pdc/hsb_cpnx_versa.pdc* file.

Figure 4.13. PDC Configuration File

4. Configure the driver. For details on how to configure the driver, refer to the Applying Patch to Support the IMX258 Camera Module section. To enable driver configuration support, follow the steps from Configuring the AGX Orin Developer Host Kit section through the Applying Patch to Support the IMX258 Camera Module section.
5. Verify the reference design configuration. Review the Lattice Radiant software hierarchy file list and the clock summary from the place-and-route timing report. Figure 4.14 shows the reference design in the Lattice Radiant software hierarchy file list. The reference design is now ready for compilation and implementation.

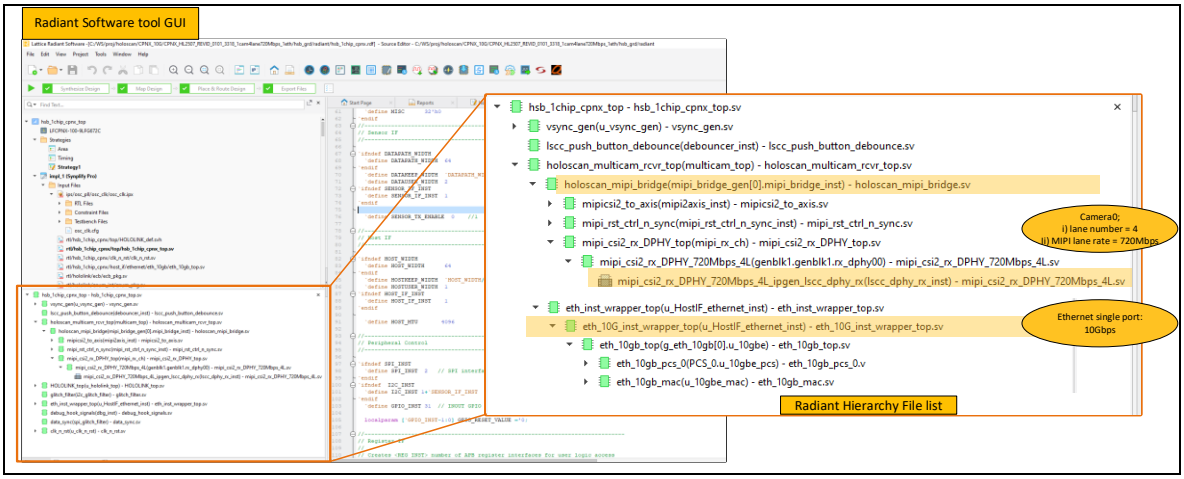


Figure 4.14. Lattice Radiant Software Hierarchy File List

4.3. Customizing the Reference Design for the CertusPro-NX Sensor-to-Ethernet Bridge Board

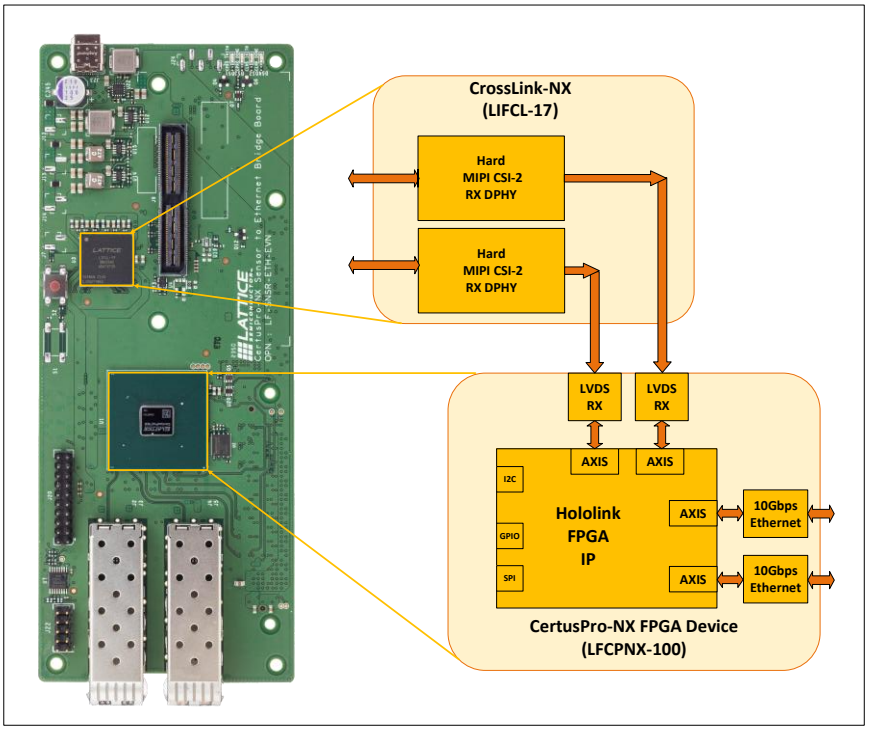


Figure 4.15. CertusPro-NX Sensor-to-Ethernet Bridge Board Block Diagram

Table 4.6 shows the configuration required for the reference design to run on the CertusPro-NX Sensor-to-Ethernet Bridge Board. The configuration for this reference design is fixed because the board is designed for a very specific use.

Table 4.6. Configuration for the reference design to fit into the CertusPro-NX Sensor-to-Ethernet Bridge Board

Sensor/Host interface	Features	Configuration
CrossLink-NX external device	2 MIPI CSI-2 Hard D-PHY	1 prebuild bitstream
LVDS DDR receiver interface	Number of LVDS DDR receiver	2
Ethernet Link	Number of Ethernet port	2
	Ethernet link speed	10GbE

To customize the reference design, follow the steps below.

Note: This reference design includes a prebuilt FPGA bitstream for the CrossLink-NX device that supports two MIPI CSI-2 Hard D-PHY interfaces, LVDS DDR RX IP, the latest Hololink IP (version 2511), and Ethernet IPs.

1. Customize the reference design to match the CertusPro-NX Sensor-to-Ethernet Bridge board specifications.
2. Program the prebuilt FPGA bitstream for the CrossLink-NX device on the platform.
3. Configure the HDL Parameter and DEFINE Switch.

   The reference design needs to be configured by changing the settings of the HDL parameter and DEFINE switch to meet the CertusPro-NX Sensor-to-Ethernet Bridge board requirement using this file:

   `<project_name>/radiant/rtl/hsb_cpnx/top/2chip_top/HOLOLINK_def.svh`

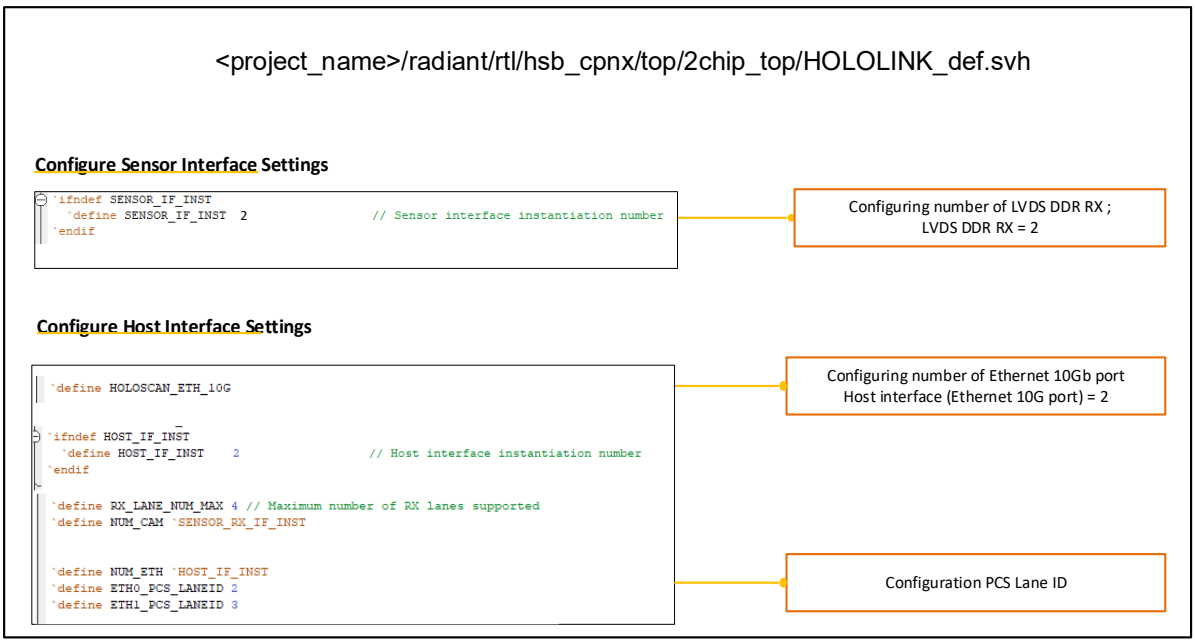


Figure 4.16. Required HDL Parameter and DEFINE Switch Configuration

4. Review the PDC configuration file, *<project_name>/radiant/pdc/hsb_cpnx_2chip.pdc* and make the changes accordingly.
5. Verify the reference design configuration. Review the Lattice Radiant software hierarchy file list and the clock summary from the place-and-route timing report. Figure 4.17 shows the reference design in the Lattice Radiant software hierarchy file list. The reference design is now ready for compilation and implementation.

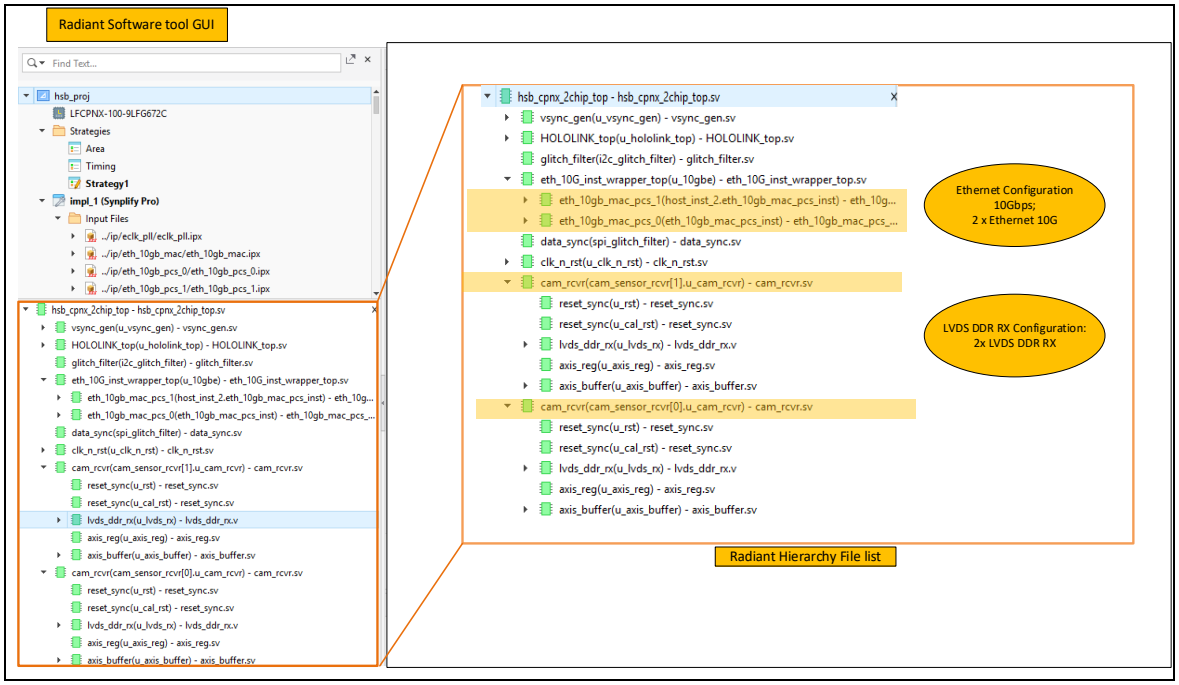


Figure 4.17. Lattice Radiant Software Hierarchy File List

5. Compiling the Reference Design

This section describes how to compile the reference design using Lattice Radiant software. For more details on the Lattice Radiant software, please refer to the Lattice Radiant Software User Guide. The screenshots in this section are for reference only; details may vary depending on the software version and the FW ID, Board ID and date code used.

5.1. Configuring the Reference Design Parameters

To configure the reference design parameters, refer to the details in the Customizing the Reference Design section.

5.2. Assigning a Revision ID for Each Bitstream

To assign a revision ID for the bitstream, update the top-level HDL file hsb_cpnx_versa_top.sv for the CertusPro-NX Versa board as shown in Figure 5.1 or hsb_cpnx_2chip_top.sv for the CertusPro-NX Sensor-to-Ethernet Bridge board shown in Figure 5.2.

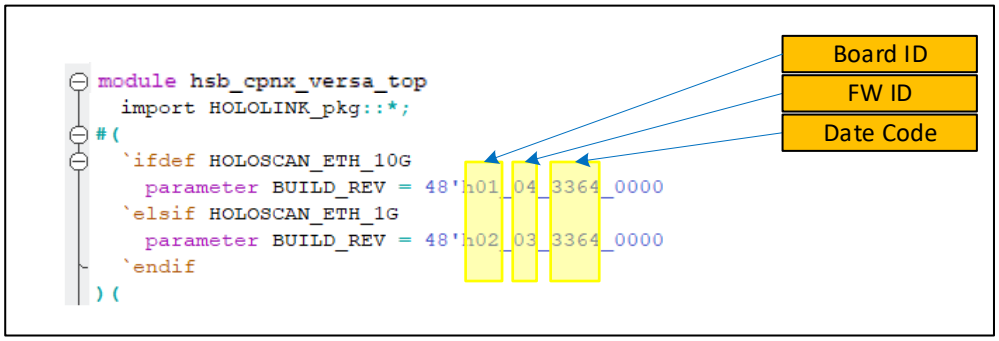


Figure 5.1. Revision ID assignment (hsb_cpnx_versa_top.sv)

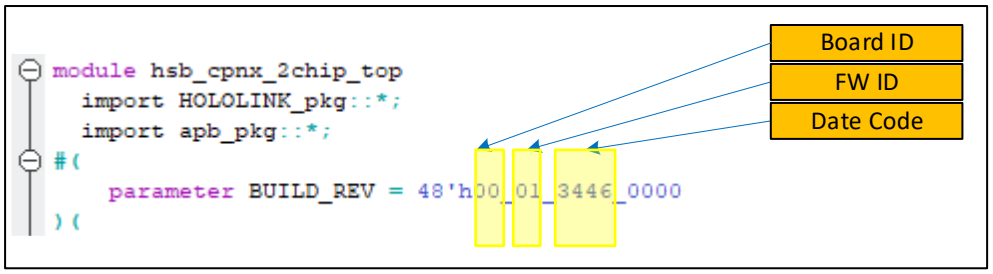


Figure 5.2. Revision ID assignment (hsb_cpnx_2chip_top.sv)

The Board ID is stored in a 1-byte hexadecimal value determined by the HSD platform and the configured Ethernet link speed. Table 5.1 lists the Board ID values for each supported HSB platform and link-speed combination. The firmware (FW) ID is also stored in a 1-byte hexadecimal value and increments with each bitstream release.

Table 5.1. Board ID Representation in Hexadecimal

HSD Board with Ethernet Link Speed	Board ID
CertusPro-NX Versa board with Ethernet speed 1Gbps	0x02
CertusPro-NX Versa board with Ethernet speed 10Gbps	0x01
CertusPro-NX Sensor to Ethernet Bridge board with Ethernet speed 10Gbps	0x00

The date code indicates when the release bitstream was generated. It is stored in a 2-byte hexadecimal format, as shown in Figure 5.3. The figure provides an example that converts the date November 4, 2025 from decimal to binary and hexadecimal formats.

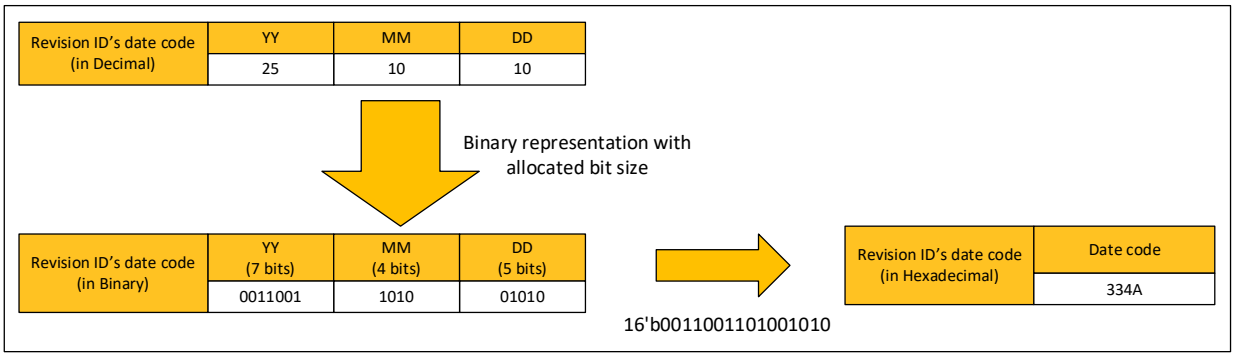


Figure 5.3. Revision ID Date Code Representation

5.3. Configuring the Lattice Radiant Software to Compile the Reference Design

1. Launch the Lattice Radiant software, as shown in Figure 5.4. Note that the project is compiled using the Lattice Radiant software version 2025.2.0.48.0

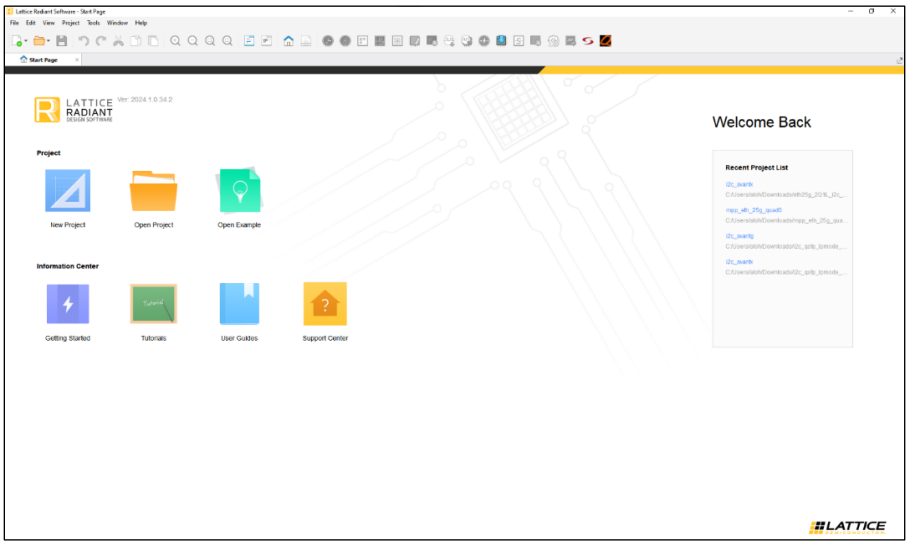


Figure 5.4. Lattice Radiant Software

2. Click **File** > **Open Project.** From the project database, open the Lattice Radiant software project file. To open the CertusPro-NX Versa board project file use *hsb_cpnx_versa.rdf*, or to open the CertusPro-NX Sensor-to-Ethernet Bridge board project file use *hsb_cpnx_2chip.rdf,* as shown in Figure 5.5.

Figure 5.5. Open Project File for CertusPro-NX Versa Board

3. Modify the Place and Route design strategy details under **Strategy1 > Place & Route Design**. Refer to Figure 5.6. The seed run count has been increased to 4 for this reference design, allowing you to select the reference design with the best place-and-route result and the best STA report. Specify multiple seeds for placement and routing during implementation[1].

Note:

1. This is controlled by the Placement Iteration setting under the Place and Route Design strategy in the Lattice Radiant software, which determines how many placement and routing iterations are performed. Each iteration uses a different cost table, resulting in a unique placement strategy and generating a distinct Uniform Database (.udb) file. By exploring multiple placement options, you increase the likelihood of achieving better timing closure and overall design performance. Using multiple seeds is beneficial for complex designs as it provides alternative implementations that may meet timing more effectively.

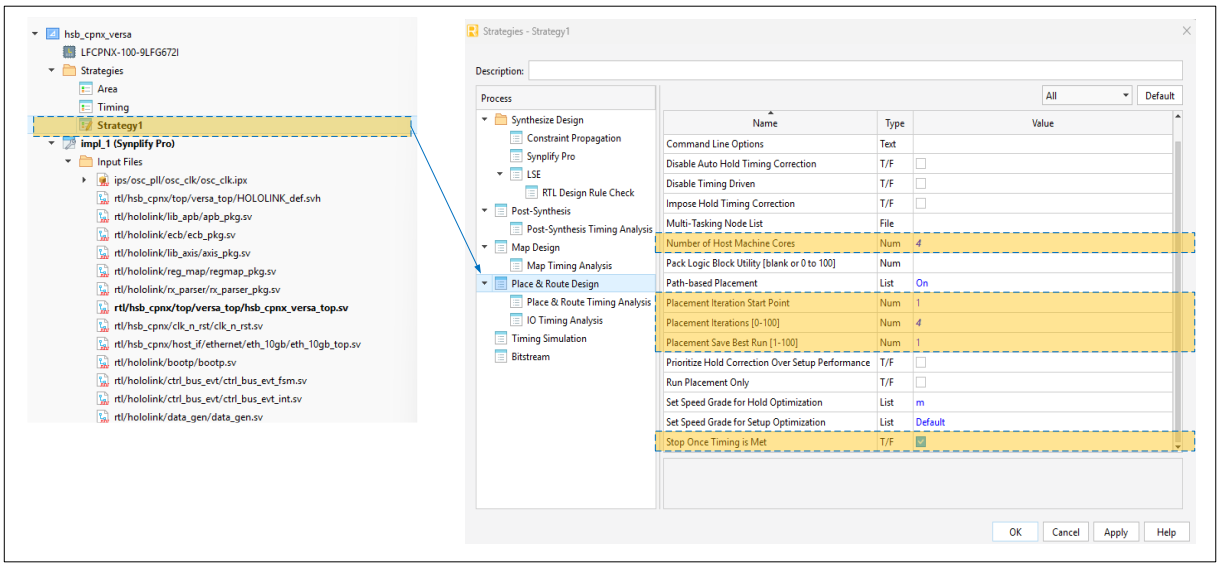


Figure 5.6. Place and Route Design Strategy

For further details on configuring the Lattice Radiant Software, refer to Lattice Radiant User Guide.

5.4. Generating the Bitstream

To create the FPGA bitstream file, click **Export Files** to generate the bit file. View the log message in the Export Reports folder for the generated bitstream.

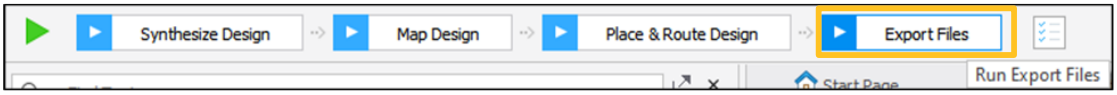


Figure 5.7. Generate and Export Bitstream File

6. Implementing the Reference Design

The following table provides an overview of the compatibility of various CertusPro-NX board types with different NVIDIA Jetson modules and their respective Ethernet speed capabilities.

Table 6.1. Matrix of CertusPro-NX Platform and Jetson Modules

Board Type	Jetson Module		Ethernet Speed	
	AGX Orin	AGX Thor	1GbE	10GbE
CertusPro-NX Versa Board	✓	—	✓	—
	✓	—	—	✓
	—	✓	—	✓
CertusPro-NX Sensor-to-Ethernet Bridge Board	✓	—	—	✓

6.1. Hardware Requirements

6.1.1. CertusPro-NX Versa Board and NVIDIA Jetson AGX Orin

- NVIDIA Jetson AGX Orin developer kit
- Lattice CertusPro-NX Versa Board
- IMX258 camera sensor module – contact Lattice Sales for more information
- Ethernet 10GBase-T (Cat 6 RJ-45) SFP+ Module (Ethernet 10GbE support) – tested with 6COM 10GBASE SFP+ RJ-45 Module
- 10/100/1000BASE-T SFP module (Ethernet 1GbE support) – tested with FS 10/100/1000BASE-T RJ45 SFP Module
- CAT6 Ethernet cable (support 1GbE/10GbE)
- Type-C USB cable
- DisplayPort cable (for AGX Orin)
- Monitor with DisplayPort support (for AGX Orin)
- Keyboard (for AGX Orin)
- Mouse (for AGX Orin)
- Mini USB Type-A cable for programming
- 12 V power supply
- Host Orin AGX power adapter

6.1.2. CertusPro-NX Versa Board and NVIDIA Jetson AGX Thor

- NVIDIA Jetson AGX Thor developer kit
- Lattice CertusPro-NX Versa Board
- 13 MP IMX258 camera module – contact Lattice Sales for more information
- 100G QSFP28 to 4×25G SFP28 Breakout Active Optical Cable (AOC) – tested with FS 100G QSFP28 to 4×25G Breakout AOC
- Type-C to Type-A USB Cable
- DisplayPort Cable (for AGX Thor)
- Monitor with DisplayPort Support (for AGX Thor)
- Keyboard (for AGX Thor)
- Mouse (for AGX Thor)
- Mini USB to USB-A cable (for programming)
- 12 V power supply (for CertusPro-NX Versa Board)
- Power adapter (for AGX Thor)

6.1.3. CertusPro-NX Sensor-to-Ethernet Bridge Board and NVIDIA Jetson AGX Orin

- NVIDIA Jetson AGX Orin developer kit
- CertusPro-NX Sensor to Ethernet Bridge Board
- Leopard Imaging IMX274 Dual Camera Sensor Module – contact Lattice Sales for more information
- Ethernet 10GBase-T (Cat 6 RJ-45) SFP+ Module (Ethernet 10GbE support) – tested with 6COM 10GBASE SFP+ RJ-45 Module
- Lattice Programming Cables
- CAT6 Ethernet cable (support 10GbE)
- Type-C to Type-A USB Cable
- DisplayPort Cable (for AGX Orin)
- Monitor with DisplayPort Support (for AGX Orin)
- Keyboard (for AGX Orin)
- Mouse (for AGX Orin)
- Mini USB to USB-A cable (for programming)
- 5 V power supply (for CertusPro-NX Sensor to Ethernet Bridge Board)
- Power adapter (for AGX Orin)

6.2. Software Requirements

6.2.1. Jetson AGX Orin

- Jetpack 6.2.1
- NVIDIA Jetson Linux 36.4.4
- NVIDIA Holoscan SDK 3.7.0
- Holoscan Sensor Bridge (HSB) SDK 2.5.0

6.2.2. Jetson AGX Thor

- Jetpack 7.0
- NVIDIA Jetson Linux 38.2
- NVIDIA Holoscan SDK 3.7.0
- Holoscan Sensor Bridge SDK 2.5.0

Figure 6.1 shows the hardware setup for the Jetson AGX Orin host and Lattice CertusPro-NX Versa Board.

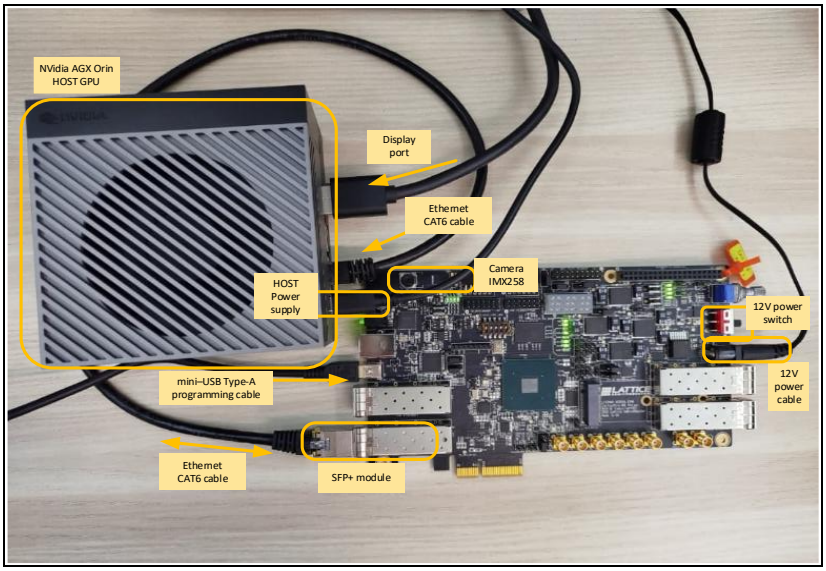


Figure 6.1. Hardware Setup

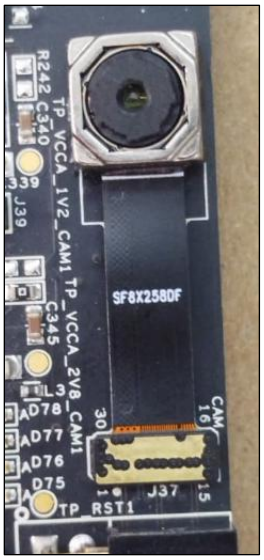


Figure 6.2. Camera Sensor Connection

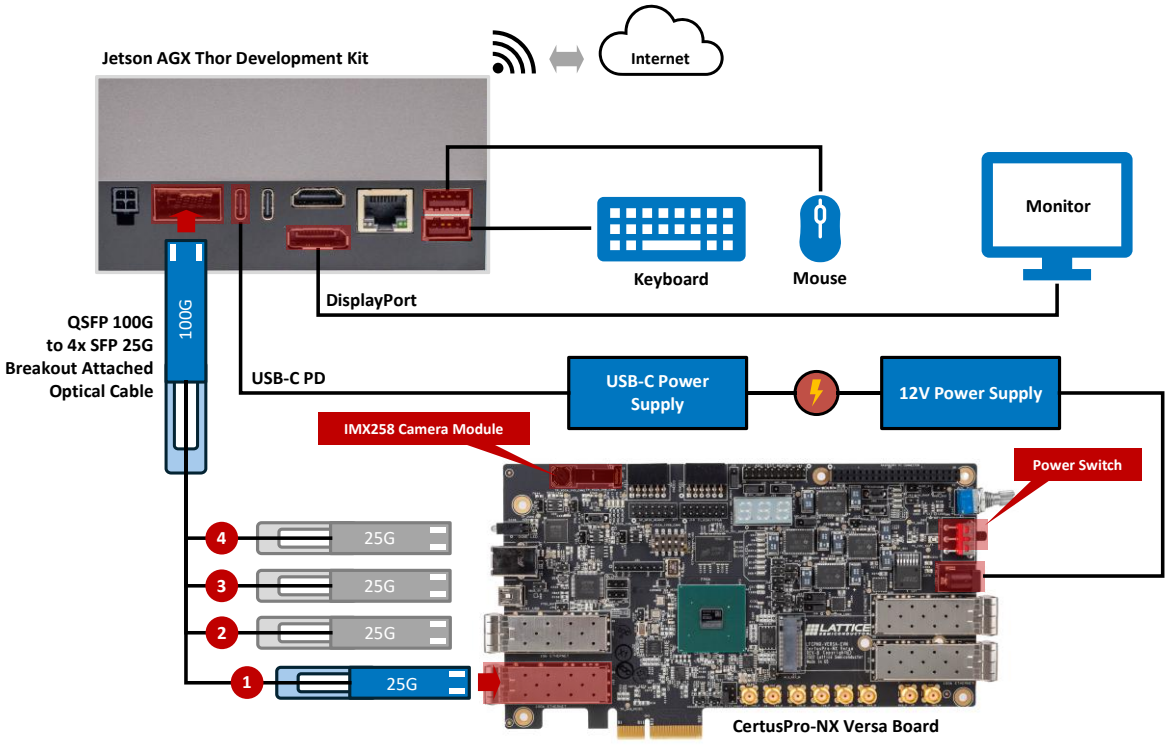


Figure 6.3. Setup with AGX Thor for 10GbE Ethernet

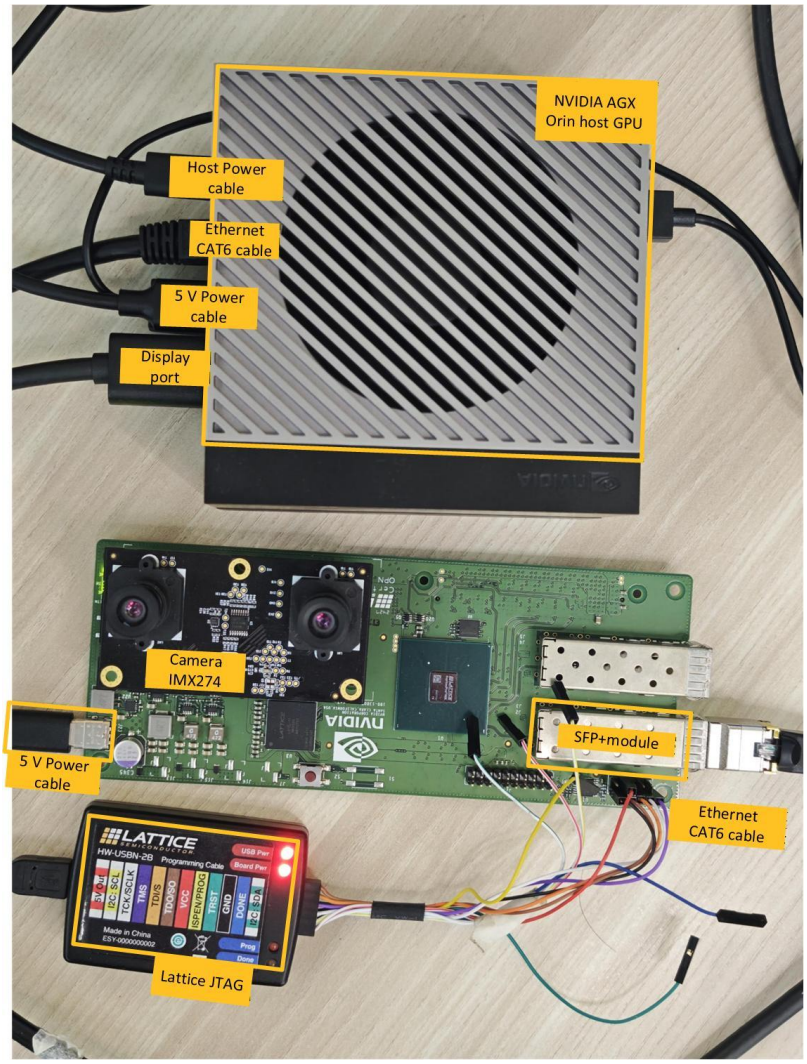


Figure 6.4. Hardware Setup for using CertusPro-NX Sensor-to-Ethernet Bridge Board with AGX Orin

6.3. NVIDIA Platform Host Setup

6.3.1. Jetson AGX Orin Developer Kit

6.3.1.1. Setting Up the Jetson AGX Orin Developer Kit

To set up the Jetson AGX Orin Developer Kit, follow the steps below. These steps are to be executed on an Ubuntu host PC terminal.

1. Set up an Ubuntu 22.04 host PC with at least 8 GB of RAM and an internet connection. Connect the Ubuntu host to the Jetson AGX Orin using a USB cable as shown in Figure 6.5.

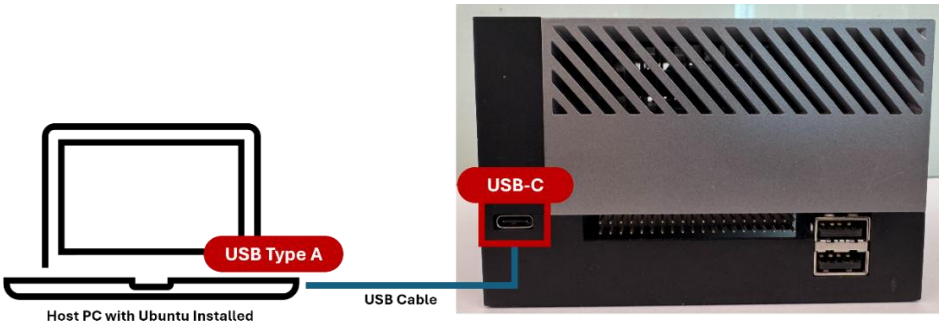


Figure 6.5. Ubuntu Host PC and Jetson AGX Orin Developer Kit Setup

2. Download and install the NVIDIA SDK Manager:

```
wget https://developer.download.nvidia.com/compute/cuda/repos/ubuntu2204/x86_64/cuda-keyring_1.1-1_all.deb
sudo dpkg -i cuda-keyring_1.1-1_all.deb
sudo apt-get update
sudo apt-get -y install sdkmanager
```

3. Place the AGX Orin into recovery mode by pressing and holding the recovery button as shown in Figure 6.6. While holding the recovery button, press the reset button and release it. Wait for about three seconds or more, then release the recovery button.

Figure 6.6. Recovery and Reset Button

4. Launch SDK Manager from the terminal, type:

```
sdkmanager
```

5. Log in using your NVIDIA developer credentials if you are using the SDK Manager for the first time. Select the checkbox, **Stay logged in**, then click the **LOGIN** button.

6. Select **Jetson AGX Orin [64 GB Developer Kit version]** as the target hardware after the SDK Manager window appears. Then click **OK**.

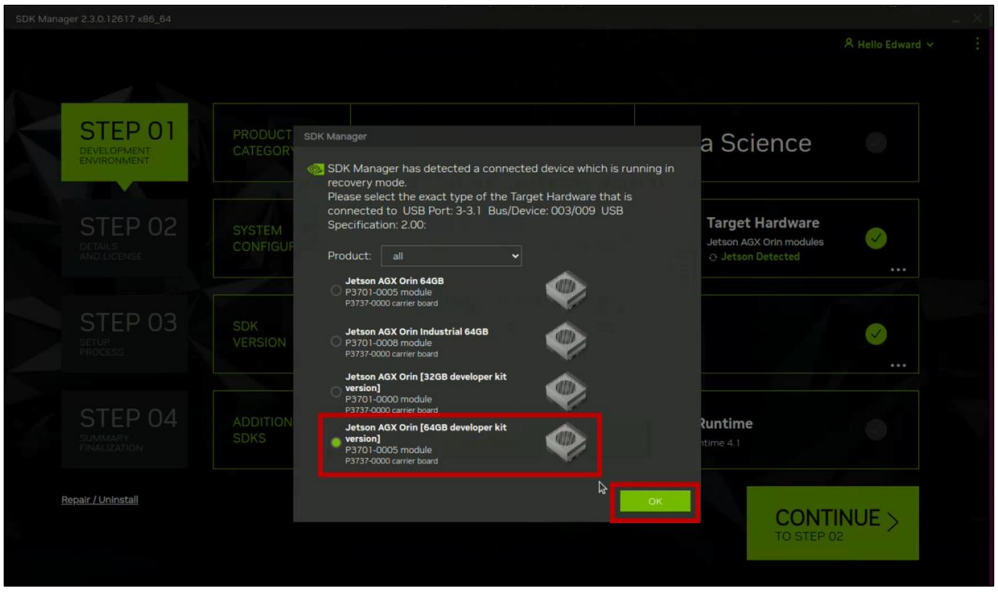


Figure 6.7. Jetson AGX Orin [64GB Developer Kit Version]

7. Click the **…** icon at **(A)** as shown in Figure 6.8, and select **JetPack 6.2.1 (Rev. 1)**. Then, click **CONTINUE** to proceed.

Figure 6.8. JetPack 6.2.1 (Rev.1)

8. Leave all settings as default, and select **I accept the terms and conditions of the license agreements**. Then, click **CONTINUE** to proceed with the installation process.

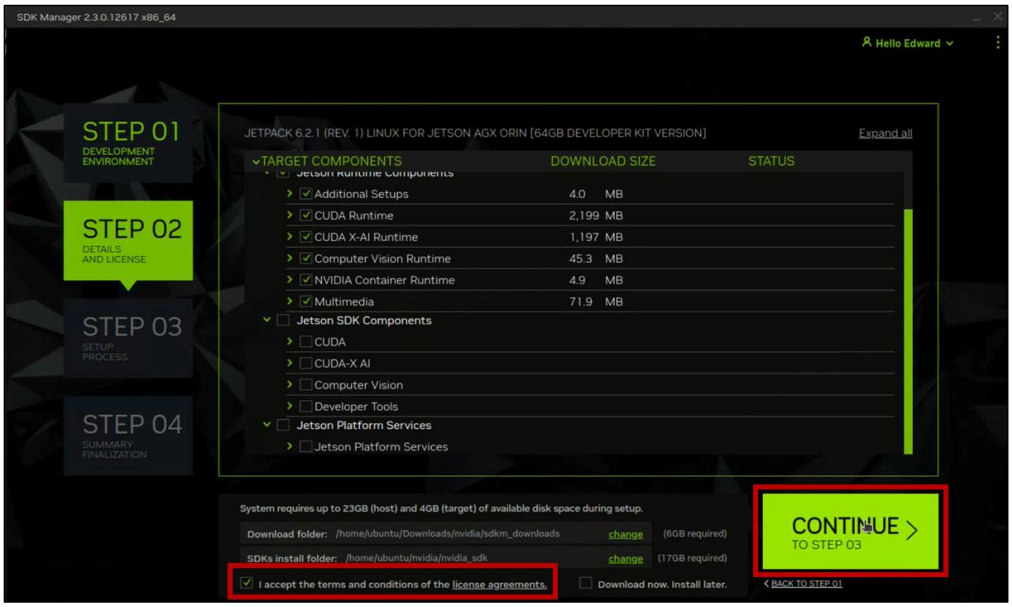


Figure 6.9. Terms and Conditions – License Agreement

9. In **STEP 03 – SETUP PROCESS,** as shown in Figure 6.10, wait for the download operation and OS image creation process to complete.

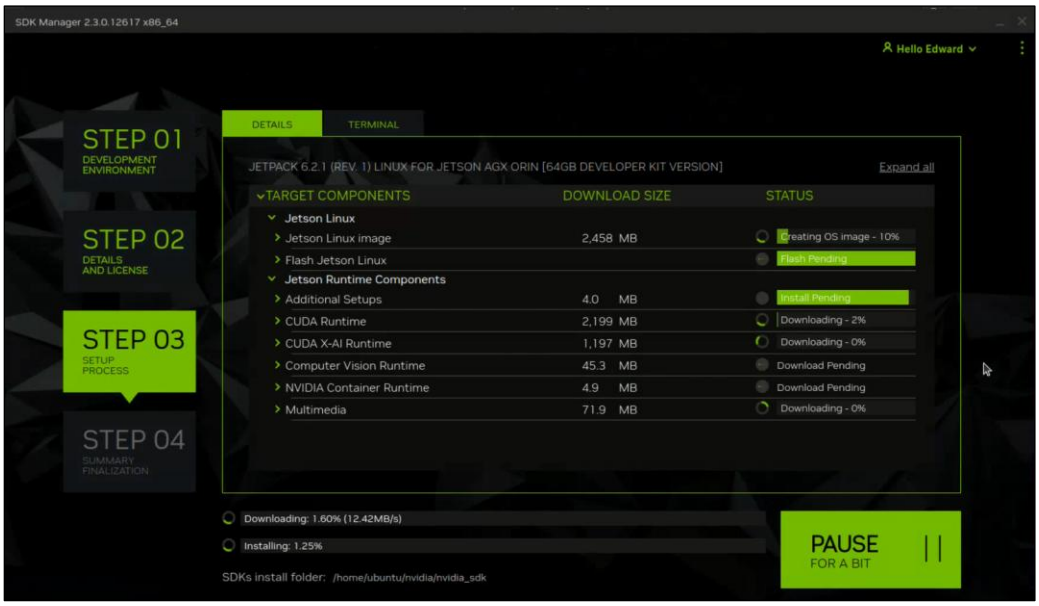


Figure 6.10. Download Operation and OS Image Creation

10. When prompted for a flash setup, enter the desired username to access the AGX Orin system, see letter **(A)** in Figure 6.11, along with the password at **(B)**. Select **Pre-Config** from the dropdown at **(C)** and **EMMC** as the storage device at **(D)**. Then, click **Flash** to proceed.

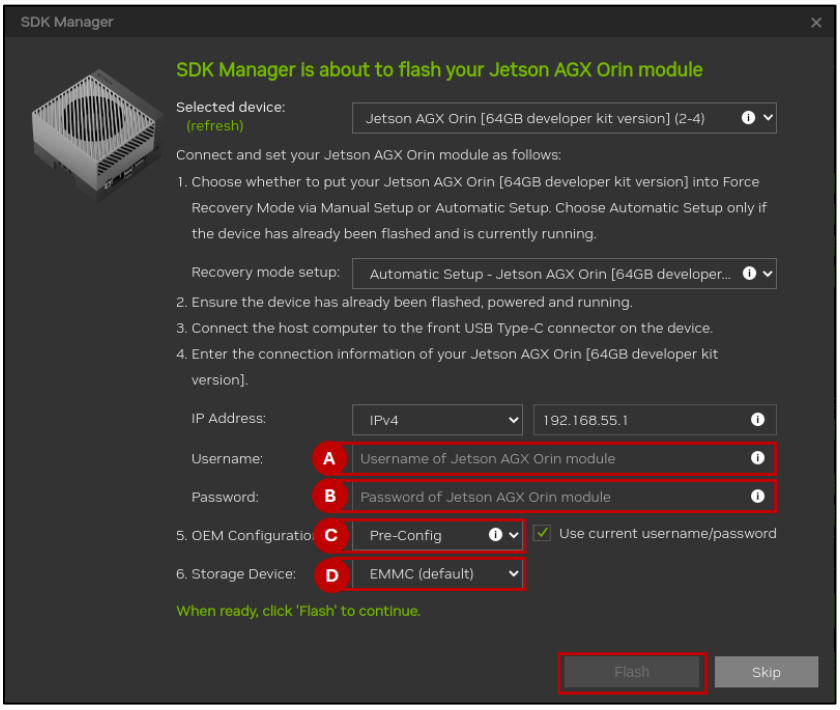


Figure 6.11. SDK Manager

11. Complete **STEP 04 – SUMMARY FINALIZATION** to finish the setup. Reset the Jetson AGX Orin system by pressing the reset button as shown in Figure 6.6. Then proceed to the next section to configure the Jetson AGX Orin itself.

Figure 6.12. Summary Finalization

6.3.1.2. Configuring the AGX Orin Developer Kit

The customizable HSB sensor interface reference design is supported by the Jetson AGX Orin system running at JetPack 6.2.1. The following steps are one-time setup procedures and should be executed directly on the AGX Orin terminal, outside the Holoscan Sensor Bridge (HSB) docker container. All commands assume the HSB is connected via eno1 (the Ethernet interface on the Jetson AGX Orin).

1. Install git-lfs (some data files in the HSB source repository use it).
```
sudo apt-get update
sudo apt-get install -y git-lfs
```
2. Grant the user permission to the docker subsystem.
```
sudo usermod -aG docker $USER
```
3. Reboot the AGX Orin to apply the changes.
```
sudo reboot
```
4. Increase the network receive buffer size to support Linux sockets.
```
echo 'net.core.rmem_max = 31326208' | sudo tee /etc/sysctl.d/52-hololink-rmem_max.conf
sudo sysctl -p /etc/sysctl.d/52-hololink-rmem_max.conf
```
5. Assign a static IP address (192.168.0.101) to the onboard network port.
```
EN0=eno1
sudo nmcli con add con-name hololink-$EN0 ifname $EN0 type ethernet ip4 192.168.0.101/24
sudo nmcli connection up hololink-$EN0
```
6. Power-on the CertusPro-NX Versa board and ensure it is properly connected. Then, ping to check connectivity.
```
ping 192.168.0.101
```
7. Isolate a processor core from the Linux kernel when running Linux socket-based examples[1].

   To isolate that core, edit the /boot/extlinux/extlinux.conf file.
```
sudo apt install nano
sudo apt update
sudo nano /boot/extlinux/extlinux.conf
```
8. Add the setting isolcpus=2 to the end of the line that begins with **APPEND.**

   Your file should resemble the following:
```
TIMEOUT 30
DEFAULT primary

MENU TITLE L4T boot options

LABEL primary
      MENU LABEL primary kernel
      LINUX /boot/Image
      ...
      APPEND ${cbootargs} ...<other-settings>... isolcpus=2
```
   Save and exit by pressing **Ctrl+O**, then **Enter**, followed by **Ctrl+X.**

   *Note: The sensor bridge applications can run the network receiver process on a different core by setting the environment variable **HOLOLINK_AFFINITY** to the desired core*.

   The command below is shown for demonstrating the use of HOLOLINK_AFFINITY and is not required for system setup.
```
HOLOLINK_AFFINITY=0 python3 examples/linux_imx258_player.py
```

9. Run the **jetson_clocks** tool at startup to set the core clocks to their maximum.

```
JETSON_CLOCKS_SERVICE=/etc/systemd/system/jetson_clocks.service
cat <<EOF | sudo tee $JETSON_CLOCKS_SERVICE >/dev/null
[Unit]
Description=Jetson Clocks Startup
After=nvpmodel.service

[Service]
Type=oneshot
ExecStart=/usr/bin/jetson_clocks

[Install]
WantedBy=multi-user.target
EOF
sudo chmod u+x $JETSON_CLOCKS_SERVICE
sudo systemctl enable jetson_clocks.service
```

10. Set the Jetson AGX Orin power mode to **MAXN** for optimal performance. You can change this setting via the L4T power dropdown menu in the upper-right corner of the screen, as indicated by **(A)**. Click **(B)** to select the **MAXN** option.

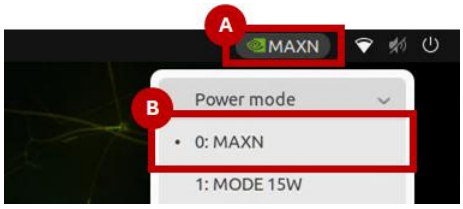


Figure 6.13. MAXN Power Mode

11. Reboot Jetson AGX Orin to apply changes.

```
sudo reboot
```

12. Enable PTP for **$EN0** to synchronize timestamps in received data with the host system time. Install the **linuxptp** tool, then create a systemd service file to run **phc2sys** at boot time, ensuring the clock in **$EN0** is synchronized with the system clock.

```
sudo apt update && sudo apt install -y linuxptp
EN0=eno1
PHC2SYS_SERVICE=/etc/systemd/system/phc2sys-$EN0.service
cat <<EOF | sudo tee $PHC2SYS_SERVICE >/dev/null
[Unit]
Description=Copy system time to $EN0
Requires=NetworkManager.service
After=NetworkManager.service
After=timemaster.service

[Service]
Type=simple
ExecStartPre=timeout 3m bash -c "until [ \"\$(nmcli -g GENERAL.STATE device show $EN0)\" =
\"100 (connected)\" ]; do sleep 1; done"
ExecStart=/usr/sbin/phc2sys -c $EN0 -s CLOCK_REALTIME -O 0 -S 0.0001

[Install]
WantedBy=multi-user.target
EOF
```

13. Configure it for execution at startup, and start it now.

```
sudo chmod u+x $PHC2SYS_SERVICE
sudo systemctl enable phc2sys-$EN0.service
sudo systemctl start phc2sys-$EN0.service
```

14. Next, run **ptp4l** to send PTP SYNC messages to **$EN0**.

```
cat <<EOF | sudo tee /etc/linuxptp/hsb-ptp.conf >/dev/null
# This configuration is appropriate for NVIDIA Holoscan sensor bridge
# applications, where PTP messages are sent over L2 and a 1/2 second interval.
[global]
logSyncInterval -1
logMinDelayReqInterval -1
network_transport L2
EOF
```

15. Create a systemd service to run **ptp4l**.

```
PTP4L_SERVICE=/etc/systemd/system/ptp4l-$EN0.service
cat <<EOF | sudo tee $PTP4L_SERVICE >/dev/null
[Unit]
Description=Send PTP SYNC messages to $EN0
After=phc2sys-$EN0.service

[Service]
Type=simple
ExecStart=/usr/sbin/ptp4l -i $EN0 -f /etc/linuxptp/hsb-ptp.conf

[Install]
WantedBy=multi-user.target
EOF
```

```
sudo chmod u+x $PTP4L_SERVICE
sudo systemctl enable ptp4l-$EN0.service
sudo systemctl start ptp4l-$EN0.service
```

16. Log in to NVIDIA GPU Cloud (NGC).
    - Register for an NGC account at https://catalog.ngc.nvidia.com/
    - Create an API key at https://ngc.nvidia.com/setup/api-key
    - Use the API key to log in to **nvcr.io**

```
$ docker login nvcr.io
Username: $oauthtoken
Password: <Your token key to NGC>
WARNING! Your password will be stored unencrypted in /home/<user>/.docker/config.json.
Configure a credential helper to remove this warning. See
https://docs.docker.com/engine/reference/commandline/login/#credentials-store

Login Succeeded
```

Note:

1. For high-bandwidth applications, such as 4K video acquisition, isolate the network receiver core to ensure optimal performance. Set processor affinity for the example program to the isolated core to improve performance and reduce latency. By default, the sensor bridge software runs the time-critical background network receiver process on core 3. Ensure core 3 is isolated from Linux scheduling so that no other processes run on it without explicit user assignment, thereby improving reliability and performance.

6.3.1.3. Building the Holoscan Sensor Bridge Demo Container

The MIPI IMX258 camera reference design is based on the HSB release version 2.5.0.

1. Fetch the HSB source code version 2.5.0 from Github:
```
git clone https://github.com/nvidia-holoscan/holoscan-sensor-bridge -b 2.5.0
```
2. Build the HSB demo container for iGPU (default for AGX Orin).
```
cd holoscan-sensor-bridge
sh docker/build.sh --igpu
```

6.3.1.4. Applying Patch to Support the IMX258 Camera Module

1. Place the patch file **lattice_sensor_bridge_2.5.0.patch** in the same directory level as the **holoscan-sensor-bridge** directory.
2. Apply the patch using the following command:
```
patch -p0 < lattice_sensor_bridge_2.5.0.patch
```
3. Verify that **linux_imx258_player.py** exists after applying **lattice_sensor_bridge_2.5.0.patch** to confirm the patch was applied correctly:
```
ls holoscan-sensor-bridge/examples/linux_imx258_player.py
```
4. Rebuild the HSB demo container using the following command:
```
cd holoscan-sensor-bridge
sh docker/build.sh --igpu
```

6.3.2. Jetson AGX Thor Developer Kit

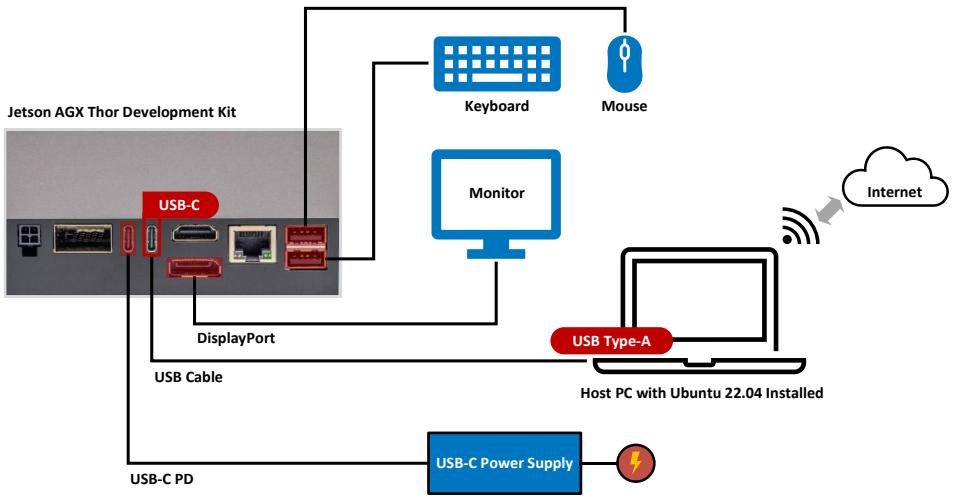


Figure 6.14. Hardware Setup for Flash Jetson AGX Thor

6.3.2.1. Flashing the Jetson AGX Thor using the SDK Manager

1. Make sure the hardware setup is done as shown in Figure 6.14, also make sure the Ubuntu Host PC is powered up and internet connection is enabled.
2. Power up the AGX Thor using the USB-C power adapter and make sure the AGX Thor can boot up to the operating system. If the AGX Thor has never flashed before, it won't boot up to the operating system and needs to be set to recovery mode.

Recovery mode step:

a. Ensure the AGX Thor is powered OFF. Verify that the LED indicator is OFF.
b. Connect the Type-C power cable to the AGX Thor. The power supply must be ON.
c. Press and hold the **Recovery Button** (see Figure 6.15 for location).
d. While holding the **Recovery Button**, press the Power Button.
e. Release both buttons simultaneously.

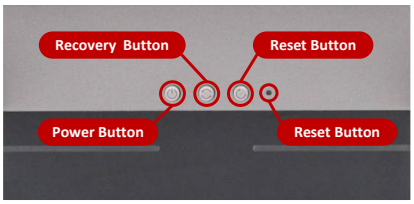


Figure 6.15. AGX Thor Recovery, Reset, and Power Button

Note: Run all commands in this section from the terminal of the Ubuntu host PC.

3. In Ubuntu Host PC, open a terminal window and execute the below commands to download the SDK Manager.

```
wget https://developer.download.nvidia.com/compute/cuda/repos/ubuntu2204/x86_64/cuda-keyring_1.1-1_all.deb
sudo dpkg -i cuda-keyring_1.1-1_all.deb
sudo apt-get update
sudo apt-get -y install sdkmanager
```

4. Run the SDK Manager command.

```
Sdkmanager
```

5. Sign up for an NVIDIA Developer account at NVIDIA Developer if you do not have one.
6. After the SDK Manager is launched, click Login as shown in Figure 6.16. A browser window will open, where you'll sign in using your NVIDIA Developer account credentials.
7. Check your email for the authentication verification link and click it to complete the login process. Once verified, the SDK Manager will launch automatically.

Figure 6.16. SDK Manager Login

8. Select **Jetson AGX Thor Development** as the **Target Hardware** (see letter **A** in Figure 6.17). Verify that the Jetson AGX Thor module is detected. If the module is not detected, repeat the Recovery mode step. Set the SDK version to **JetPack 7.0 (rev. 1)** (see letter **B** in Figure 6.17). Click **CONTINUE** to proceed to **STEP 02 – Details and License**.

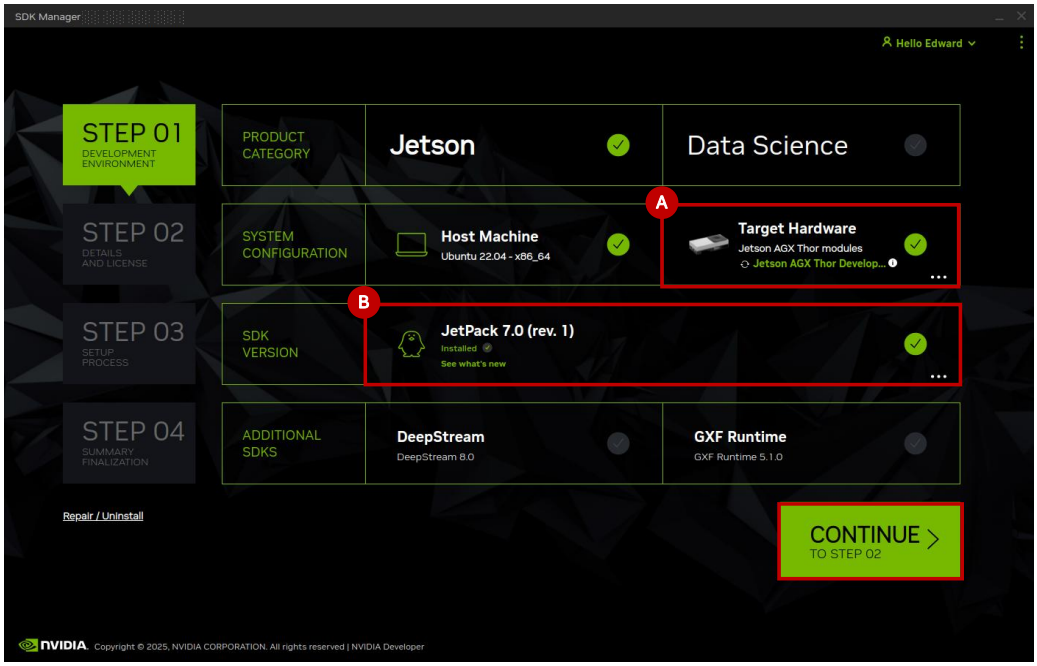


Figure 6.17. STEP 01 – Development Environment

9. In **STEP 02**, select **I accept the terms and conditions of the license agreements** as shown in Figure 6.18. Click **CONTINUE** to proceed with the installation process.

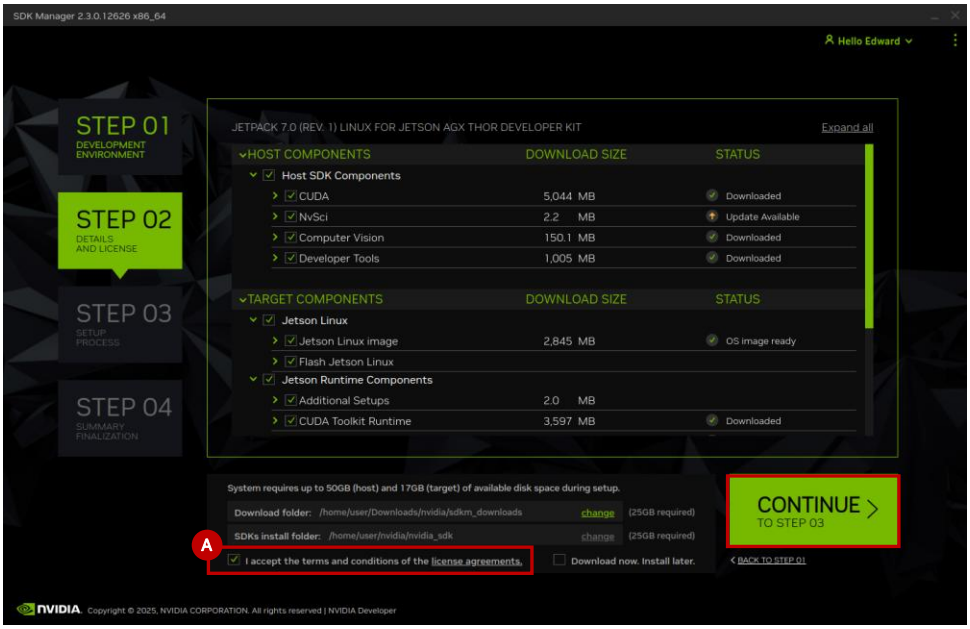


Figure 6.18. STEP 02 – Details and License

10. In STEP 03, the **SDK Manager** will prompt for a sudo password. Enter the password and click **OK**. The software download and installation process begins. The progress is shown in Figure 6.20.

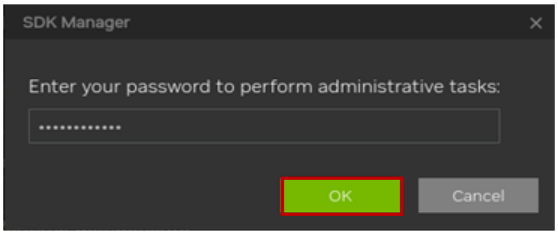


Figure 6.19. Administrative Right Request

Figure 6.20. STEP 03 – Setup Process

11. After the installation completes, the SDK Manager displays a dialog box to flash the target device. Select **Manual Setup – Jetson AGX Thor Developer Kit** (see letter **A**) in the **Recovery mode setup** as shown in Figure 6.21 to begin flashing the target device. Refer to the Recovery mode step for details.

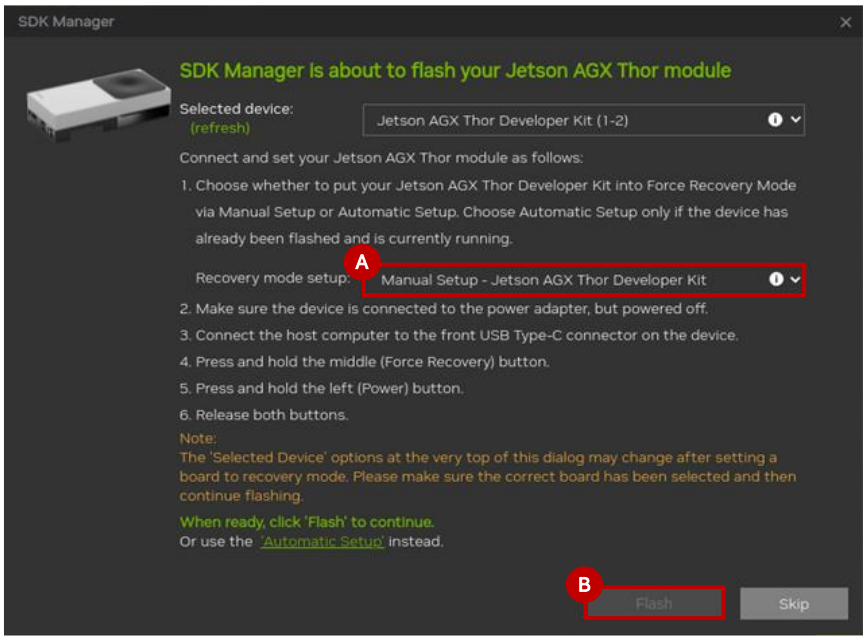


Figure 6.21. Recovery Mode Selection

12. In the setup configuration screen, select **Pre-Config** under the **OEM Configuration** (letter **A**) as shown in Figure 6.22. Enter the desired **username** (letter B) and **password** (letter **C**) to create the new user account for AGX Thor. Leave the **Storage Device** setting as the default. Click **Flash** to begin the flashing process.

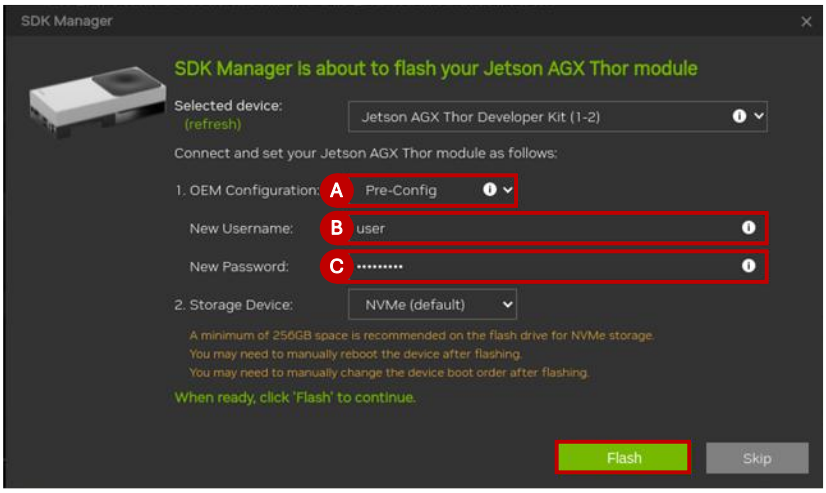


Figure 6.22. Pre-flash Operation Setup

13. After flashing is complete, a full reboot is required (power off, then power on the Jetson AGX Thor, see the power button location in Figure 6.15).
14. Allow the SDK Manager to detect the device and begin the initial setup process. When the AGX Thor reaches the operating system login screen, enter the created **username** (letter **A**) and **password** (letter **B**) as shown in Figure 6.23. Click **Install** to start installing the SDK component.

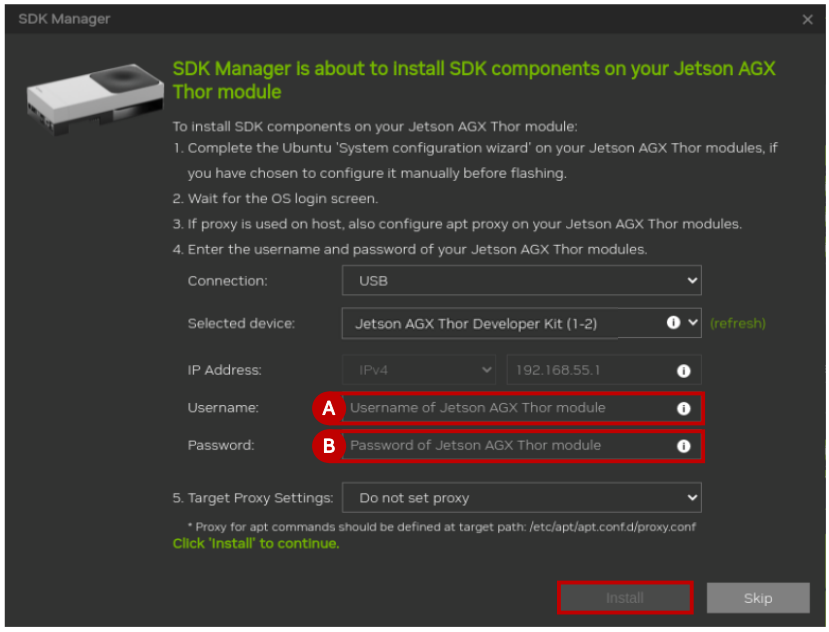


Figure 6.23. Post-flash Installation Dialog

15. After the SDK component installation completes, the **STEP 04 – Summary Finalization** panel appears Review any warnings or errors displayed in the summary panel. Click **FINISH AND EXIT** to complete the installation process.

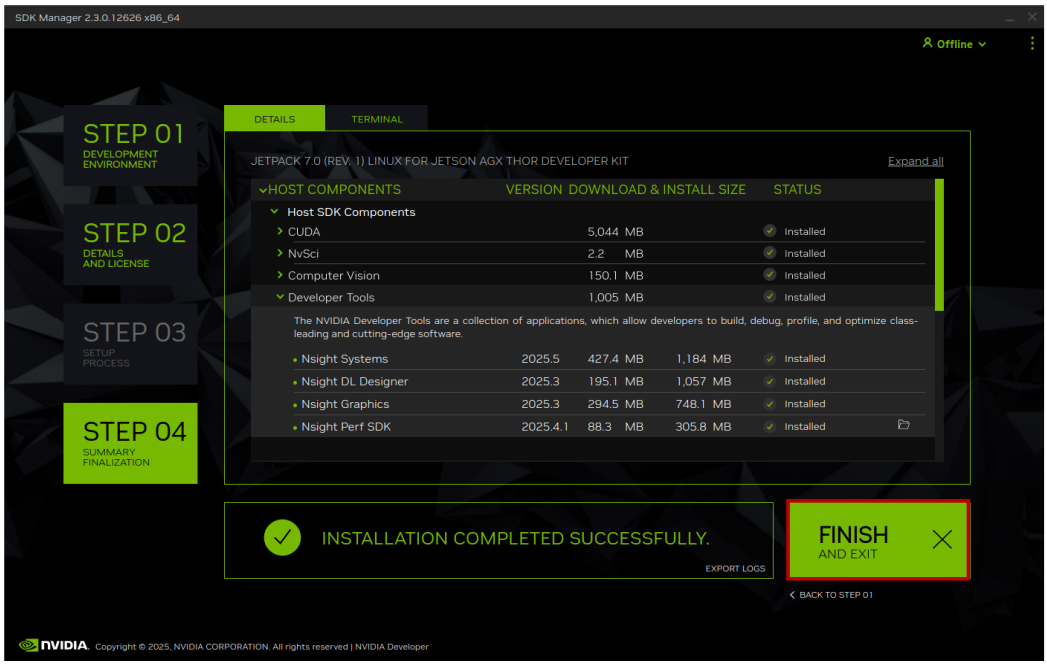


Figure 6.24. STEP 04 – Summary Finalization

6.3.2.2. Configuring the AGX Thor Developer Kit

Note: All commands in this section must be executed in the AGX Thor terminal and only need to be performed once.

1. Install the Holoscan SDK.
```
sudo apt update
sudo apt install holoscan=3.7.0-2
```
2. Install the Holoscan Sensor Bridge dependencies.
```
sudo apt install -y git-lfs cmake libfmt-dev libssl-dev libcurlpp-dev libyaml-cpp-dev
libibverbs-dev python3-dev
```
3. Add the user to the Docker subsystem.
```
sudo usermod -aG docker $USER
```
4. Increase the Linux network receive buffer size.
```
echo 'net.core.rmem_max = 31326208' | sudo tee /etc/sysctl.d/52-hololink-rmem_max.conf
sudo sysctl -p /etc/sysctl.d/52-hololink-rmem_max.conf
```
5. Isolate a processor core from the Linux kernel when running Linux socket-based examples:
Open **/boot/extlinux/extlinux.conf.** for editing
```
sudo apt update
sudo apt install nano
sudo nano /boot/extlinux/extlinux.conf
```
6. Add the setting **`isolcpus=2`** to the end of the line that begins with APPEND.
Your file should resemble the following:
```
TIMEOUT 30
DEFAULT primary

MENU TITLE L4T boot options

LABEL primary
    MENU LABEL primary kernel
    LINUX /boot/Image
    ...
    APPEND ${cbootargs} ...<other-settings>... isolcpus=2
```
Save and exit by pressing **Ctrl + O**, then Enter, followed by **Ctrl + X**.

Note: *The sensor bridge applications can run the network receiver process on a different core by setting the environment variable* ***HOLOLINK_AFFINITY*** *to the desired core. (Complete Steps 1–6 and the procedure in* Building the Holoscan Sensor Bridge Demo Container *before continuing with Steps 7–12).*

The command below is shown for demonstrating the use of HOLOLINK_AFFINITY and is not required for system setup.
```
HOLOLINK_AFFINITY=0 python3 examples/linux_imx258_player.py
```
7. Enable the network interface (assuming a camera IP address 192.168.0.2).
```
EN0=mgbe0_0
sudo nmcli con add con-name hololink-$EN0 ifname $EN0 type ethernet ip4 192.168.0.101/24
sudo nmcli connection modify hololink-$EN0 +ipv4.routes 192.168.0.2/32
sudo nmcli connection up hololink-$EN0
```
8. Reboot the AGX Thor to apply changes.
```
sudo reboot
```

9. Enable PTP for **$EN0** to synchronize timestamps in received data with the host system time. Install the **linuxptp** tool, then create a systemd service to run **phc2sys** at boot, ensuring the clock in **$EN0** is synchronized with the system clock.

```
sudo apt update && sudo apt install -y linuxptp
EN0=mgbe0_0
PHC2SYS_SERVICE=/etc/systemd/system/phc2sys-$EN0.service
cat <<EOF | sudo tee $PHC2SYS_SERVICE >/dev/null
[Unit]
Description=Copy system time to $EN0
Requires=NetworkManager.service
After=NetworkManager.service
After=timemaster.service

[Service]
Type=simple
ExecStartPre=timeout 3m bash -c "until [ \"\$(nmcli -g GENERAL.STATE device show $EN0)\" =
\"100 (connected)\" ]; do sleep 1; done"
ExecStart=/usr/sbin/phc2sys -c $EN0 -s CLOCK_REALTIME -O 0 -S 0.0001

[Install]
WantedBy=multi-user.target
EOF
```

10. Configure the service to run at startup, and start it.

```
sudo chmod u+x $PHC2SYS_SERVICE
sudo systemctl enable phc2sys-$EN0.service
sudo systemctl start phc2sys-$EN0.service
```

11. Run **ptp4l** to send PTP SYNC messages to **$EN0**.

```
cat <<EOF | sudo tee /etc/linuxptp/hsb-ptp.conf >/dev/null
# This configuration is appropriate for NVIDIA Holoscan sensor bridge
# applications, where PTP messages are sent over L2 and a 1/2 second interval.
[global]
logSyncInterval -1
logMinDelayReqInterval -1
network_transport L2
EOF
```

12. Create a systemd service to run **ptp4l.**

```
PTP4L_SERVICE=/etc/systemd/system/ptp4l-$EN0.service
cat <<EOF | sudo tee $PTP4L_SERVICE >/dev/null
[Unit]
Description=Send PTP SYNC messages to $EN0
After=phc2sys-$EN0.service

[Service]
Type=simple
ExecStart=/usr/sbin/ptp4l -i $EN0 -f /etc/linuxptp/hsb-ptp.conf

[Install]
WantedBy=multi-user.target
EOF

sudo chmod u+x $PTP4L_SERVICE
sudo systemctl enable ptp4l-$EN0.service
sudo systemctl start ptp4l-$EN0.service
```

6.3.2.3. Building the Holoscan Sensor Bridge Demo Container

1. Fetch the Holoscan Sensor Bridge source code from NVIDIA Github.
   ```
   git clone https://github.com/nvidia-holoscan/holoscan-sensor-bridge -b 2.5.0
   ```
2. Navigate to the directory at the same level where the `holoscan-sensor-bridge` repository is cloned, copy the patch file **lattice_sensor_bridge_2.5.0.patch** into this directory, and apply the patch to support IMX258 camera module.
   ```
   patch -p0 < lattice_sensor_bridge_2.5.0.patch
   ```
3. Verify that **linux_imx258_player.py** exists after applying **lattice_sensor_bridge_2.5.0.patch** to confirm that the patch was applied correctly.
   ```
   ls holoscan-sensor-bridge/examples/linux_imx258_player.py
   ```
   Expected output is as follows:
   ```
   holoscan-sensor-bridge/examples/linux_imx258_player.py
   ```
4. Log in to NVIDIA GPU Cloud (NGC) using the browser on AGX Thor.
   - Register for a developer account for NGC at https://catalog.ngc.nvidia.com/
   - Create an API key at: https://ngc.nvidia.com/setup/api-key
   - Use the API key to log in to **nvcr.io.** Run the command *docker login nvcr.io*
     ```
     docker login nvcr.io
     Username: $oauthtoken
     Password: <Your token key to NGC>
     WARNING! Your password will be stored unencrypted in /home/<user>/.docker/config.json.
     Configure a credential helper to remove this warning. See
     https://docs.docker.com/engine/reference/commandline/login/#credentials-store

     Login Succeeded
     ```
5. Rebuild the Holoscan Sensor Bridge demo container using the following command.
   ```
   cd holoscan-sensor-bridge
   sh docker/build.sh --igpu
   ```
6. After the demo container has been built, start the Docker container:
   ```
   xhost +
   sh docker/demo.sh
   ```
7. When the demo container prompt appears, run the IMX258 streaming demo.
   ```
   python examples/linux_imx258_player.py
   ```

6.4. Testing the System

This section provides details of the reference design testing on the CertusPro-NX Versa Board with NVIDIA AGX Orin/Thor GPU Host connected.

6.4.1. Test Setup on the CertusPro-NX Versa Board

6.4.1.1. Programming the Bit File

This section outlines the steps for uploading the *.bit* file. There are two methods to update the reference design firmware into the CertusPro-NX Versa board.

1. Local firmware update via USB interface.

   Flash the firmware directly into the board using a USB connection, independent of the Holoscan ecosystem. This method is ideal for initial setup, debugging, and hands-on development.
2. Remote firmware update via Ethernet

   Update the firmware remotely over an Ethernet connection using the Holoscan ecosystem. This method is suited for field updates and production environments, where remote access and automation are essential.

The following sections describes in detail the steps of uploading the *.bit* file using the two methods.

Local Firmware Update through USB Interface

1. Connect the board to the PC using a mini-USB Type-A cable, as shown in Figure 6.25. Connect the power adaptor to the board power port and turn the switch **ON.** The board is now ready to be programmed.

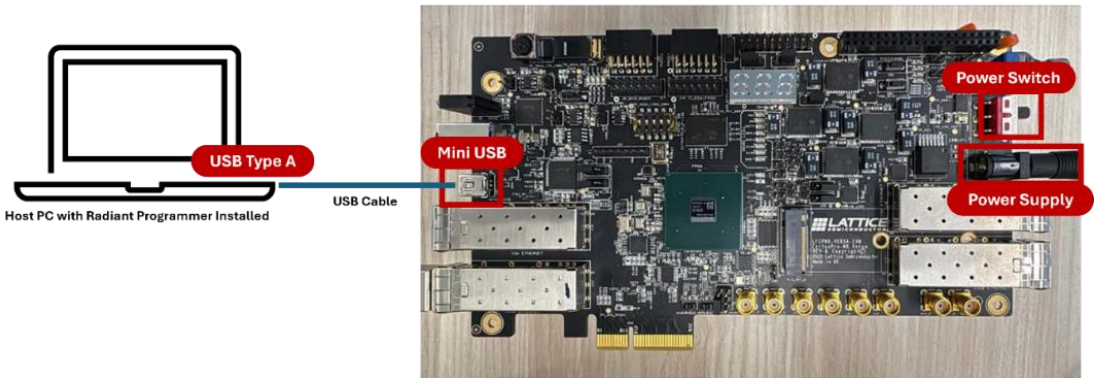


Figure 6.25. Hardware Setup for Bit File Programming

2. Click the Radiant Programmer icon ( ) if the project is already open in the Lattice Radiant software, otherwise, launch the standalone Radiant Programmer. Enter the **Project Location**, **Project Name**, then click **OK**.

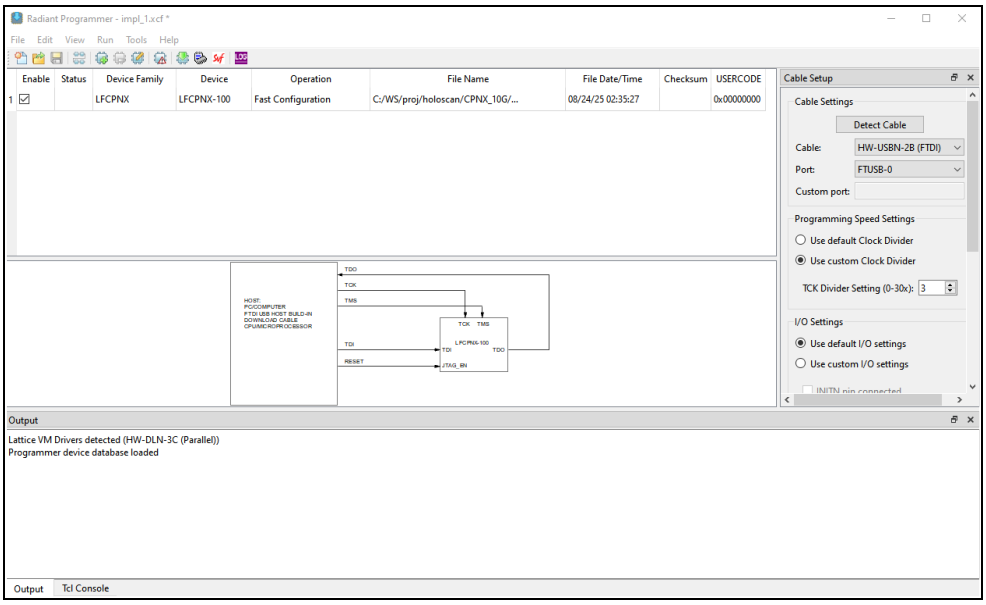


Figure 6.26. Radiant Programmer Window

3. Click **Detect Cable** in the cable setup section, select **FTUSB-0**. Then click **OK** to proceed.

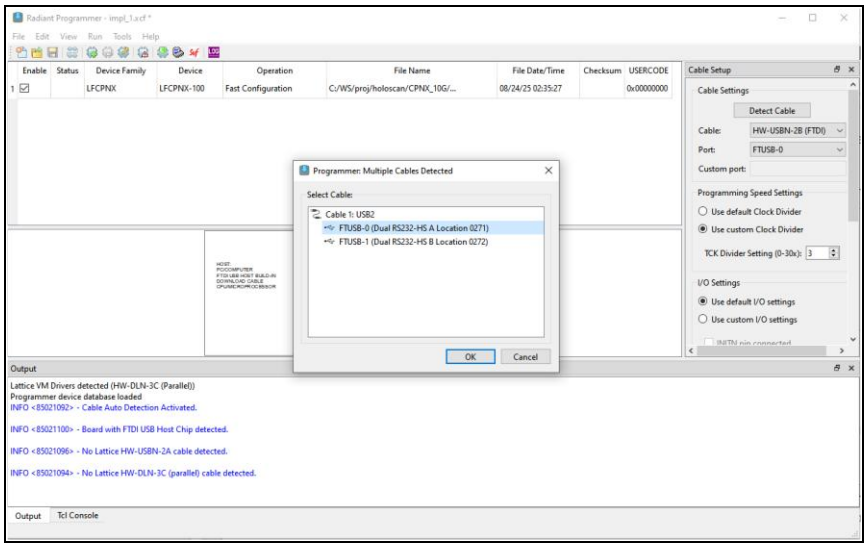


Figure 6.27. Select Cable Settings

4. Select the appropriate SPI flash configuration to flash directly to external SPI flash. Refer to Figure 6.28 for the expected settings. Click the **…** button under the file name bar and choose the bitstream file to program.

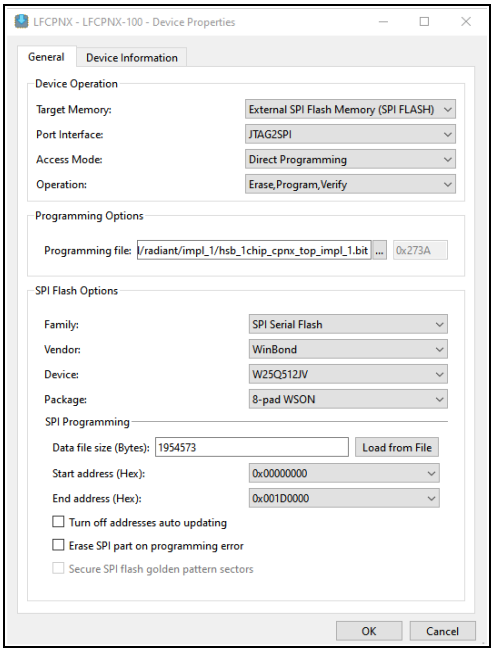


Figure 6.28. Load Bitstream File

5. Click the **Program Device** toolbar icon to load the bitstream into the board, as shown in Figure 6.29.

Figure 6.29. Program Device Toolbar Icon

6. Verify that the programming status is **Operation: successful** in the output window, as shown in Figure 6.30. To activate the flashed bitstream, power cycle the CertusPro-NX Versa board by switching it **OFF**, then **ON**.

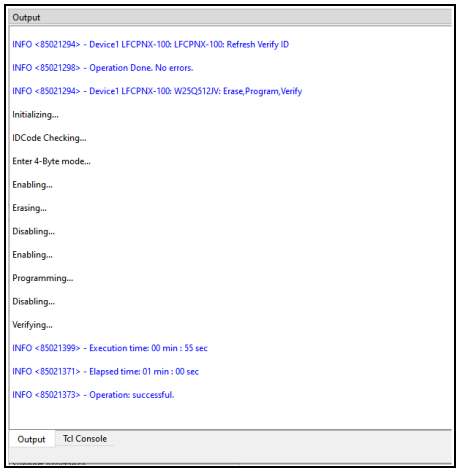


Figure 6.30. Message on Successful Programming

Remote Firmware Update through Ethernet

Before using this method note the following prerequisites:

- If you are using the CertusPro-NX Versa board for the first time, perform a Local Firmware Update through USB. After the initial update, you may use the remote firmware update via Ethernet for future updates.
- For firmware changes involving a switch between 10GbE and 1GbE[1] bitstreams on the same board, use the Local Firmware Update through USB.
- Before proceeding, complete the steps in Applying Patch to Support the IMX258 Camera Module.

If all prerequisites are met, follow the steps below:

1. Connect the AGX Orin/Thor ethernet port to the CertusPro-NX Versa board 10GbE/1GbE ethernet port (SFP Module). Refer to Figure 6.1 for the setup.
2. Select and copy the following 10GbE/1GbE[1] FPGA bitstream file into the Holoscan-Sensor-Bridge directory .
   - Bitstream file supporting 10GbE Ethernet: fpga_cpnx_versa_0106_2511.bit
   - Bitstream file supporting 1GbE Ethernet: fpga_cpnx_versa_0205_2511.bit
3. Open the terminal on the AGX Orin.
4. Change directory to the Holoscan-Sensor-Bridge directory .
   ```
   cd holoscan-sensor-bridge
   ```
5. Update the FPGA bitstream for ethernet 10GbE or 1GbE[1] using the command below. The process takes 20 to 30 minutes to complete.
   - Using bitstream that supports 10GbE Ethernet:
     ```
     program_lattice_cpnx_versa scripts/manifest_cpnx_versa_10g.yaml
     ```
   - Using bitstream that supports 1GbE[1] Ethernet:
     ```
     program_lattice_cpnx_versa scripts/manifest_cpnx_versa_1g.yaml
     ```

6. Wait for the process to complete. When prompted, power cycle the Versa board, then Press **Enter** to exit the program. Refer to Figure 6.31 for the expected output.

```
INFO spi_flash_base.cpp:169 status tid=0xa0 -- CPNX: verify address=0x100000
INFO spi_flash_base.cpp:169 status tid=0xa0 -- CPNX: verify address=0x110000
INFO spi_flash_base.cpp:169 status tid=0xa0 -- CPNX: verify address=0x120000
INFO spi_flash_base.cpp:169 status tid=0xa0 -- CPNX: verify address=0x130000
INFO spi_flash_base.cpp:169 status tid=0xa0 -- CPNX: verify address=0x140000
INFO spi_flash_base.cpp:169 status tid=0xa0 -- CPNX: verify address=0x150000
INFO spi_flash_base.cpp:169 status tid=0xa0 -- CPNX: verify address=0x160000
INFO spi_flash_base.cpp:169 status tid=0xa0 -- CPNX: verify address=0x170000
INFO spi_flash_base.cpp:169 status tid=0xa0 -- CPNX: verify address=0x180000
INFO spi_flash_base.cpp:169 status tid=0xa0 -- CPNX: verify address=0x190000
INFO spi_flash_base.cpp:169 status tid=0xa0 -- CPNX: verify address=0x1A0000
INFO spi_flash_base.cpp:169 status tid=0xa0 -- CPNX: verify address=0x1B0000
INFO spi_flash_base.cpp:169 status tid=0xa0 -- CPNX: verify address=0x1C0000
INFO spi_flash_base.cpp:169 status tid=0xa0 -- CPNX: verify address=0x1D0000
You must now physically power cycle the sensor bridge device.
Press <Enter> to continue:
root@ubuntu-agx:/home/agx/hsb/holoscan-sensor-bridge-2.2.0#
```

Figure 6.31. Console Output — Remote Firmware Update

7. Power cycle the Versa board by switching it **OFF**, and then **ON** to activate the newly flashed bitstream .

Note:

1. Only Jetson AGX Orin supports 1GbE Ethernet

6.4.1.2. Programming the Golden FPGA Bitstream with a Jump Table

To enable dual-boot operation, you must include both a primary FPGA bitstream (the default boot image) and a golden FPGA bitstream (a reliable fallback for recovery). You generate a PROM file by combining the primary and golden bitstreams with the required jump table. Use this PROM file to program the external SPI flash device.

1. Generate the PROM file.
   a. Open the Lattice Radiant Programmer.
   b. In Radiant Programmer, select **Tools > Deployment Tool**. The window shown in Figure 6.32 opens.

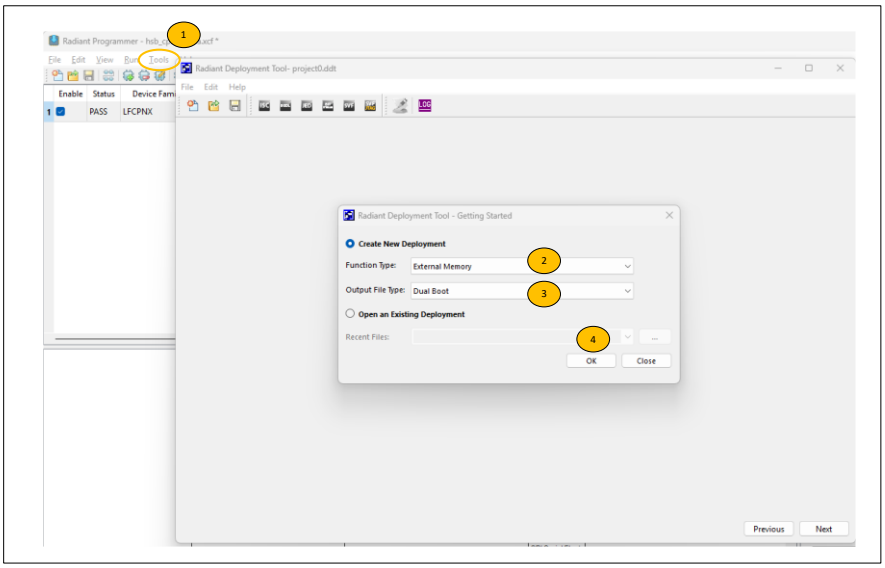


Figure 6.32. Radiant Deployment Tool – Getting Started

   c. Set Function to External Memory and Output File Type to Dual Boot, and then click OK.
   d. Add your primary and golden bitstream files, regardless of orientation.

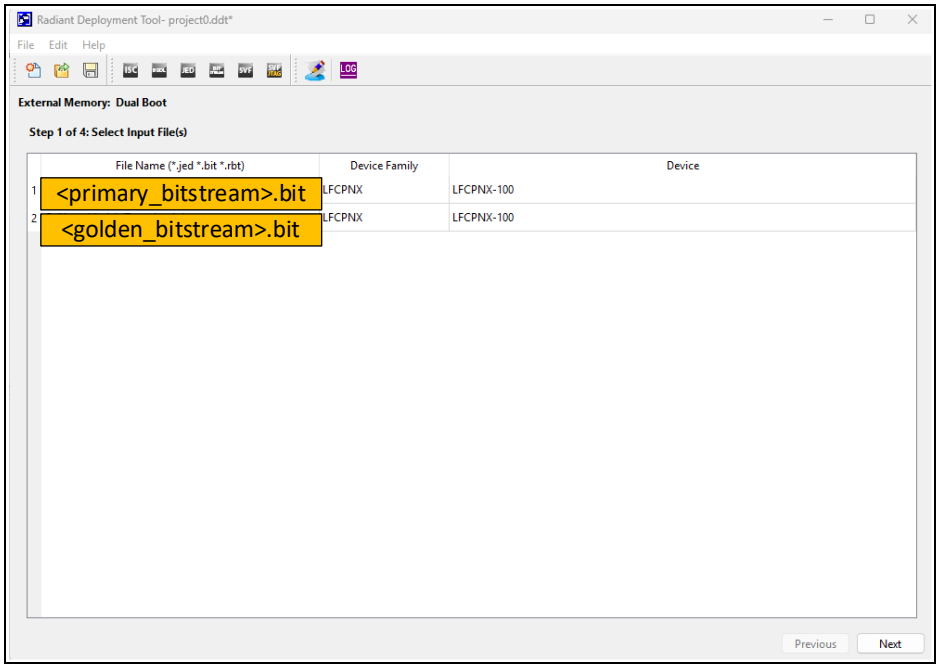


Figure 6.33. Select Input File

e. Configure the dual-boot option as required; ensure the golden and primary FPGA bitstream files are correctly selected.

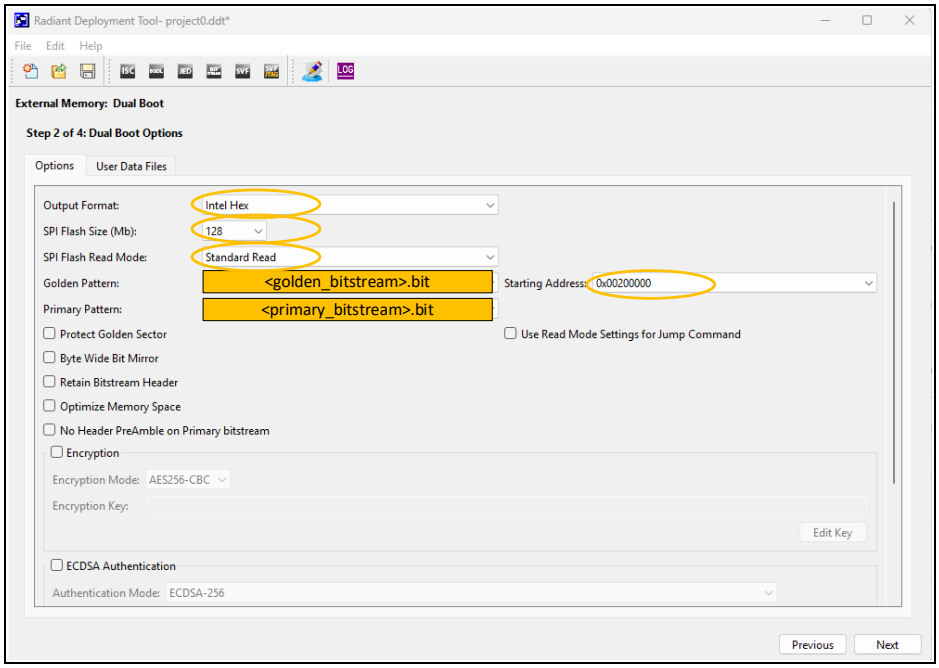


Figure 6.34. Dual Boot Options

f. Select the output file name and the save location.

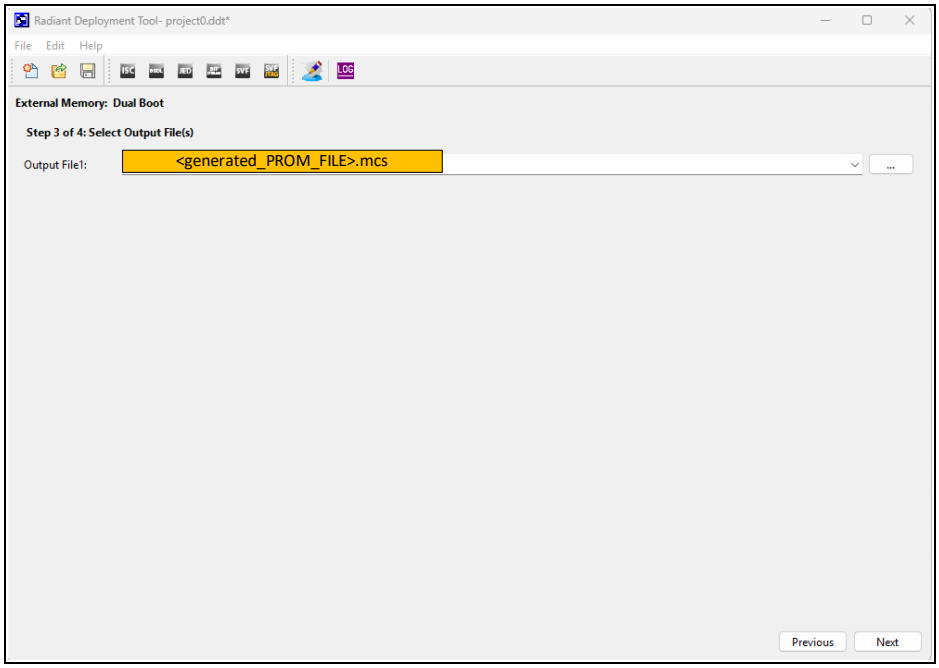


Figure 6.35. Select Output File

g. Generate the PROM file and confirm that the log shows a successful generation message.

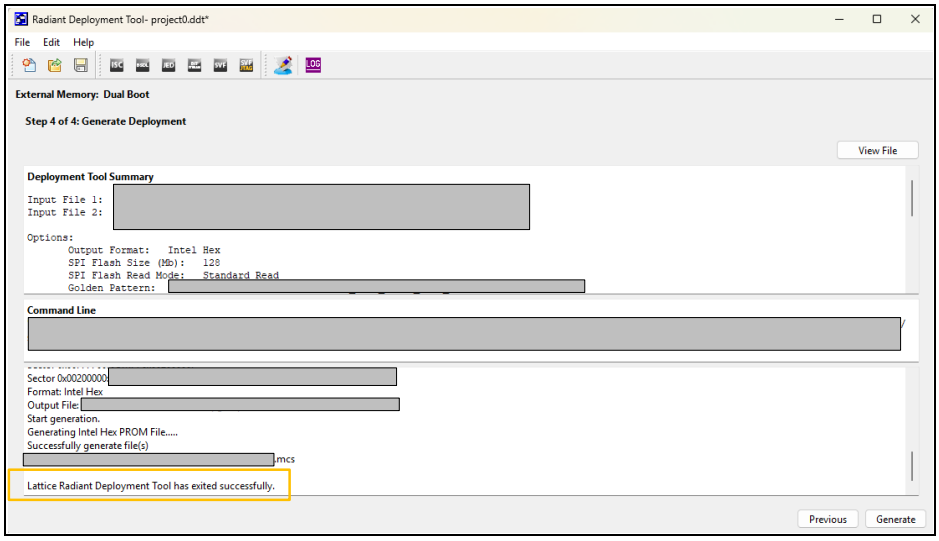


Figure 6.36. Generate Deployment

2. Program the PROM (.mcs) file.

   Programming the PROM file is the same as programming the bitstream file described in Local Firmware Update through USB Interface section. The only difference is that the input is the PROM file with the *.mcs* extension.

6.4.1.3. Testing Camera Video Streaming

1. Run the Holoscan Sensor Bridge demo container.
```
cd /<path>/<to>/<holoscan-sensor-bridge>
xhost +
sh docker/demo.sh
```
2. Run the camera video streaming example .

   This example will be streaming from the camera and display the video on AGX Orin.

   Note: Once Step 1 is executed in the AGX Orin terminal, the demo container starts, the command prompt will switch to the environment inside the container.
3. Run the video streaming demo for IMX258 camera using the following commands:
   - When using 10GbE Ethernet:
     ```
     python examples/linux_imx258_player.py
     ```
   - When using 1GbE[1] Ethernet:
     ```
     python examples/linux_imx258_player.py --camera-mode=1
     ```

Note:
1. Only Jetson AGX Orin supports 1GbE Ethernet

Figure 6.37 shows the camera video streaming test setup. The video is streamed by the NVIDIA host and captured in an office environment under lighting conditions ranging from 140 lux to 135 lux. The test environment is identical for both 1GbE[1] and 10GbE Ethernet configurations. Image quality remains consistent across both.

The primary objective of this reference design is to establish a robust and reliable bridge between the HSB interfaces and the NVIDIA host. Image tuning is not included. This process typically involves defining image quality parameters, configuring processing pipelines, and optimizing the image signal processor (ISP)—tasks that are highly specific to the camera sensor and require dedicated resources.

Note:
1. Only Jetson AGX Orin supports 1GbE Ethernet

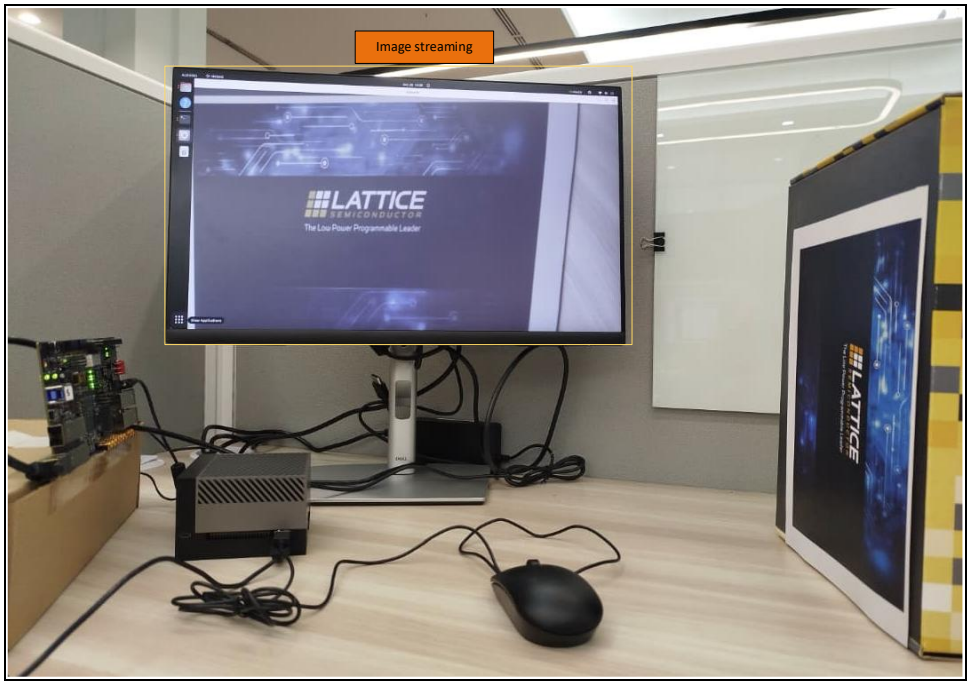


Figure 6.37. Camera Video Streaming Test Setup

6.4.2. Test Setup on the CertusPro-NX Sensor-to-Ethernet Bridge Board

6.4.2.1. Programming the Bit File

This section outlines the steps for uploading the .bit file. There are two methods to update the reference design firmware into the CertusPro-NX Sensor-to-Ethernet Bridge board.

1. Local firmware update through USB interface.

Flash the firmware directly into the board using a USB connection, independent of the Holoscan ecosystem. This method is ideal for initial setup, debugging, and hands-on development.

2. Remote firmware update over Ethernet.

Update the firmware remotely over an Ethernet connection using the Holoscan ecosystem. This method is suited for field updates and production environments, where remote access and automation are essential.

The following sections describes in detail the steps of uploading the *.bit* file using both methods.

Local Firmware Update through JTAG

1. Use the Lattice Radiant Programmer to program the board. Launch it as a standalone tool or from a Lattice Radiant project. Set up the hardware as shown in Figure 6.38, and connect the Lattice Programming Cable to header J22 (Figure 6.39).

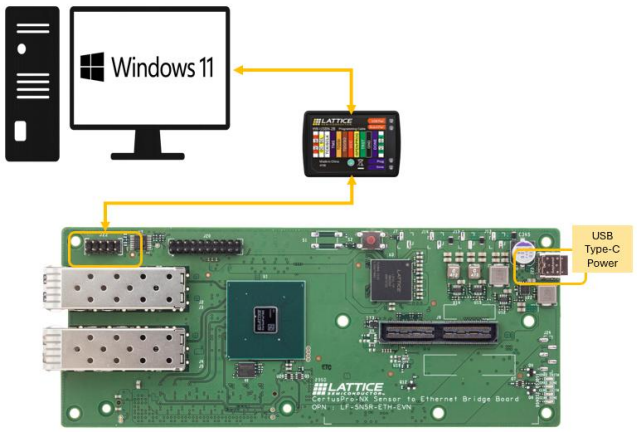
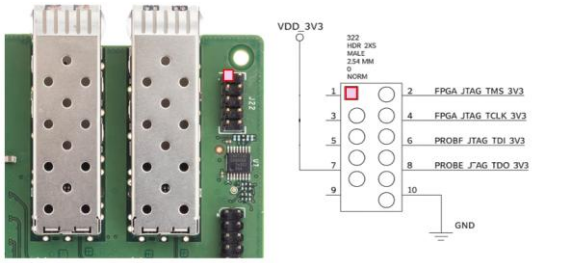


Figure 6.38. Bit File Programming Hardware Setup



LF-SNSR-ETH-EVN	J22 NET NAME	Lattice Programming Cable	Cable Color
J22.2	FPGA_JTAG_TMS_3V3	TMS	Purple
J22.4	FPGA_JTAG_TCLK_3V3	TCK/SCLK	White
J22.6	PROBE_JTAG_TDI_3V3	TDI/SI	Orange
J22.7	VDD_3V3	VCC	Red
J22.8	PROBE_JTAG_TDO_3V3	TDO/SO	Brown
J22.10	GND	GND	Black

Figure 6.39. Lattice Programming Cable Pin Configuration

2. Power on the board by connecting a USB Type-C power source.
3. Start a programming session by launching the tool and running a board scan (Figure 6.40).

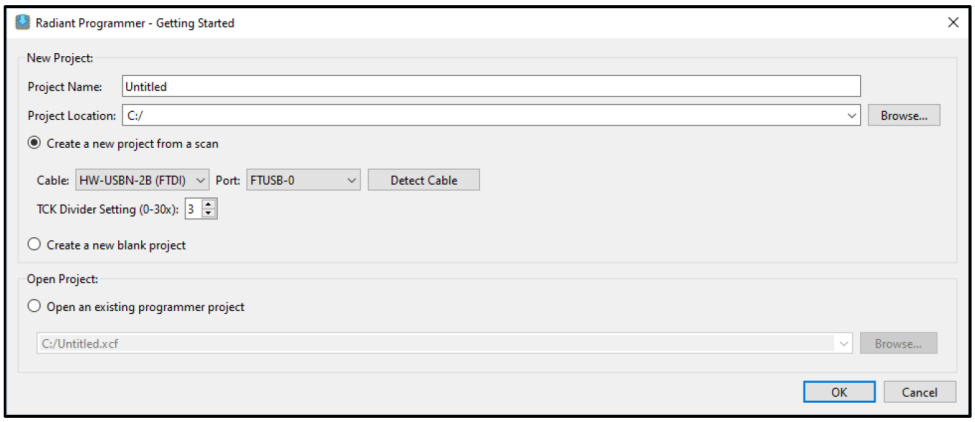


Figure 6.40. Radiant Programmer – Getting Started

4. When the board is detected, the window shown in Figure 6.41 opens. This interface allows you to enter the file name.

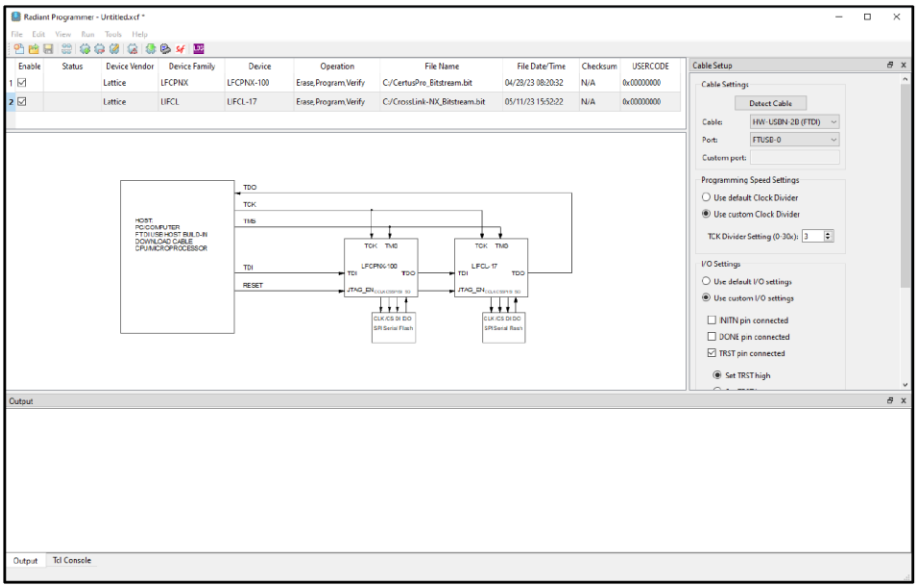


Figure 6.41. External Flash Configuration

5. Double-click the Operation field and select the appropriate programming mode. In this example, select Erase, Program, Verify for External SPI Flash Memory (SPI flash) (Figure 6.42 and Figure 6.43).

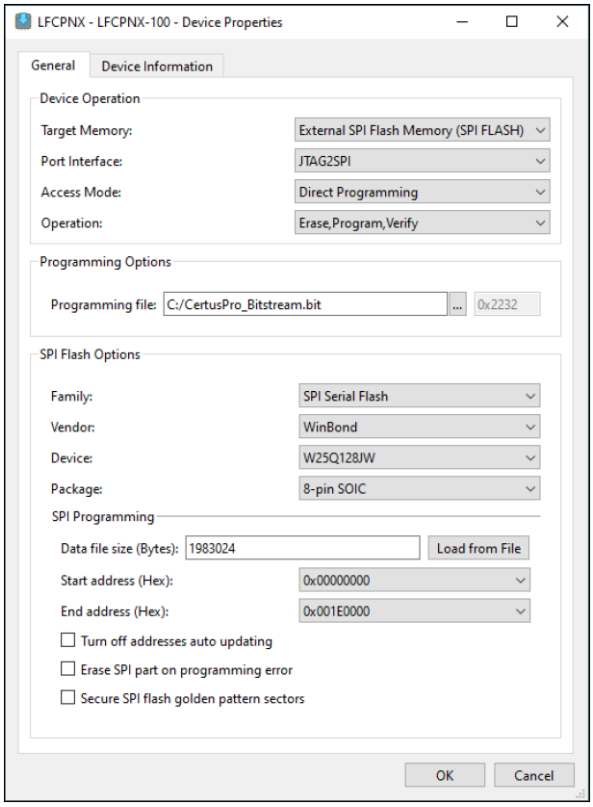


Figure 6.42. External Flash Memory (SPI flash) Device Properties – CertusPro-NX Device

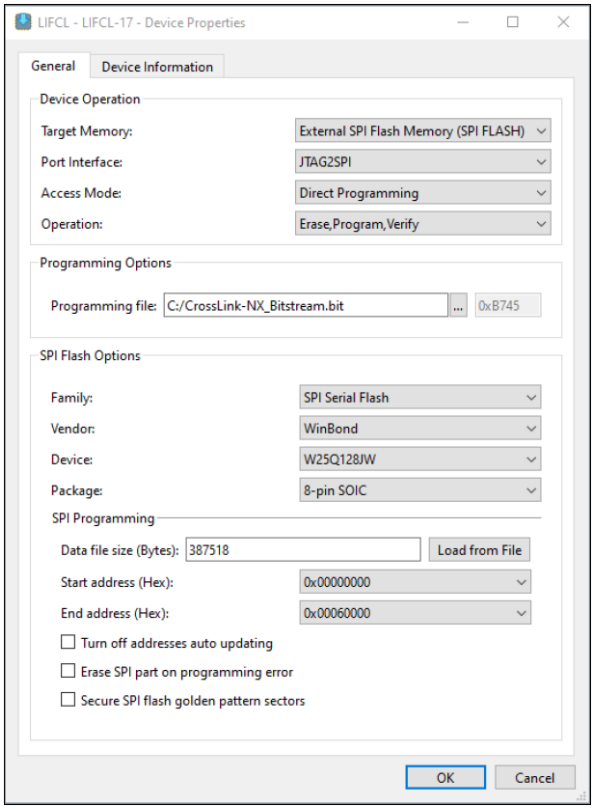


Figure 6.43. External Flash Memory (SPI flash) Device Properties – CrossLink-NX Device

6. Back in the main window, click Program to program both flashes on the CertusPro-NX Sensor-to-Ethernet Bridge board.
7. Verify the programming result in the Output console at the bottom of Lattice Radiant Programmer. You should see **Operation: Successful** (Figure 6.44).

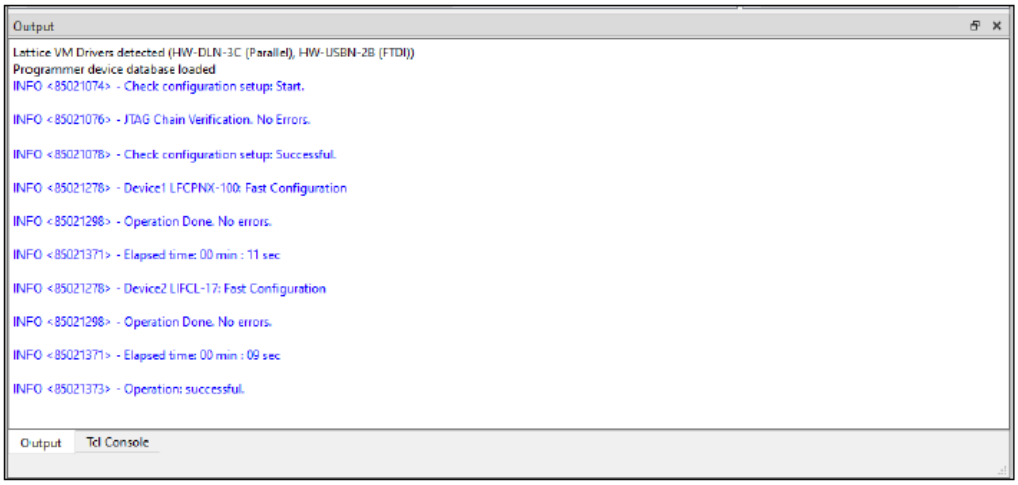


Figure 6.44. Output Window

Remote Firmware Update through Ethernet

Before using this method note the following prerequisites:

- If you are using the CertusPro-NX Sensor-to-Ethernet Bridge Board for the first time, perform a Local Firmware Update through JTAG.
- After the initial update, you may use the remote firmware update through Ethernet for future updates.

If all prerequisites are met, follow the steps below:

1. Connect the AGX Orin Ethernet port to the CertusPro-NX Sensor-to-Ethernet Bridge board's 10GbE Ethernet port (SFP module). See Figure 6.4 for the setup.
2. Select and copy the following 10GbE FPGA bitstream into the holoscan-sensor-bridge directory.
   Bitstream that supports 10GbE Ethernet: fpga_cpnx_2chip_0001_2511.bit
3. Open a terminal on the AGX Orin.
4. Change to the holoscan-sensor-bridge directory.
   ```
   cd holoscan-sensor-bridge
   ```
5. Update the FPGA bitstream for 10GbE Ethernet using the following command. The process takes 20 to 30 minutes to complete.

   Using the bitstream that supports 10GbE Ethernet:
   ```
   program_lattice_cpnx100 scripts/manifest_cpnx_2chip_10g.yaml
   ```
6. Wait for the process to complete. When prompted, power-cycle the Sensor-to-Ethernet Bridge board, then press Enter to exit the program. See Figure 6.45 for the expected output.

```
INFO spi_flash_base.cpp:169 status tid=0xa0 -- CPNX: verify address=0x100000
INFO spi_flash_base.cpp:169 status tid=0xa0 -- CPNX: verify address=0x110000
INFO spi_flash_base.cpp:169 status tid=0xa0 -- CPNX: verify address=0x120000
INFO spi_flash_base.cpp:169 status tid=0xa0 -- CPNX: verify address=0x130000
INFO spi_flash_base.cpp:169 status tid=0xa0 -- CPNX: verify address=0x140000
INFO spi_flash_base.cpp:169 status tid=0xa0 -- CPNX: verify address=0x150000
INFO spi_flash_base.cpp:169 status tid=0xa0 -- CPNX: verify address=0x160000
INFO spi_flash_base.cpp:169 status tid=0xa0 -- CPNX: verify address=0x170000
INFO spi_flash_base.cpp:169 status tid=0xa0 -- CPNX: verify address=0x180000
INFO spi_flash_base.cpp:169 status tid=0xa0 -- CPNX: verify address=0x190000
INFO spi_flash_base.cpp:169 status tid=0xa0 -- CPNX: verify address=0x1A0000
INFO spi_flash_base.cpp:169 status tid=0xa0 -- CPNX: verify address=0x1B0000
INFO spi_flash_base.cpp:169 status tid=0xa0 -- CPNX: verify address=0x1C0000
INFO spi_flash_base.cpp:169 status tid=0xa0 -- CPNX: verify address=0x1D0000
You must now physically power cycle the sensor bridge device.
Press <Enter> to continue:
root@ubuntu-agx:/home/agx/hsb/holoscan-sensor-bridge#
```

Figure 6.45. Console Output – Remote Firmware Update

7. Power-cycle the Sensor-to-Ethernet Bridge board: turn it off, then on to activate the newly flashed bitstream.

6.4.2.2. Programming the Golden FPGA Bitstream with a Jump Table

To enable dual-boot operation, you must include both a primary FPGA bitstream (the default boot image) and a golden FPGA bitstream (a reliable fallback for recovery). You generate a PROM file by combining the primary and golden bitstreams with the required jump table. Use this PROM file to program.

1. Generate the PROM file.
   a. Open the Lattice Radiant Programmer.
   b. In Radiant Programmer, select **Tools > Deployment Tool**. The window shown in Figure 6.46 opens.

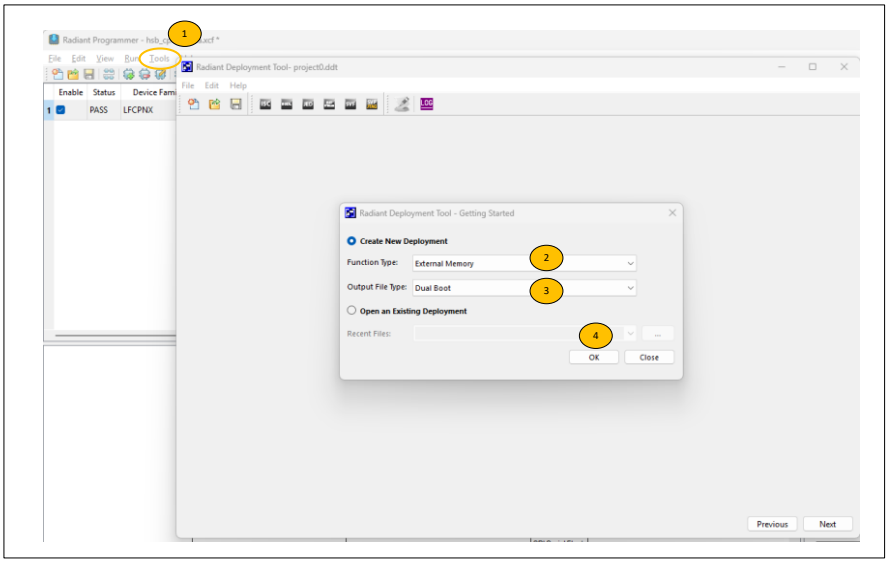


Figure 6.46. Radiant Deployment Tool – Getting Started

   c. Set Function to External Memory and Output File Type to Dual Boot, and then click OK.
   d. Add your primary and golden bitstream files, regardless of orientation.

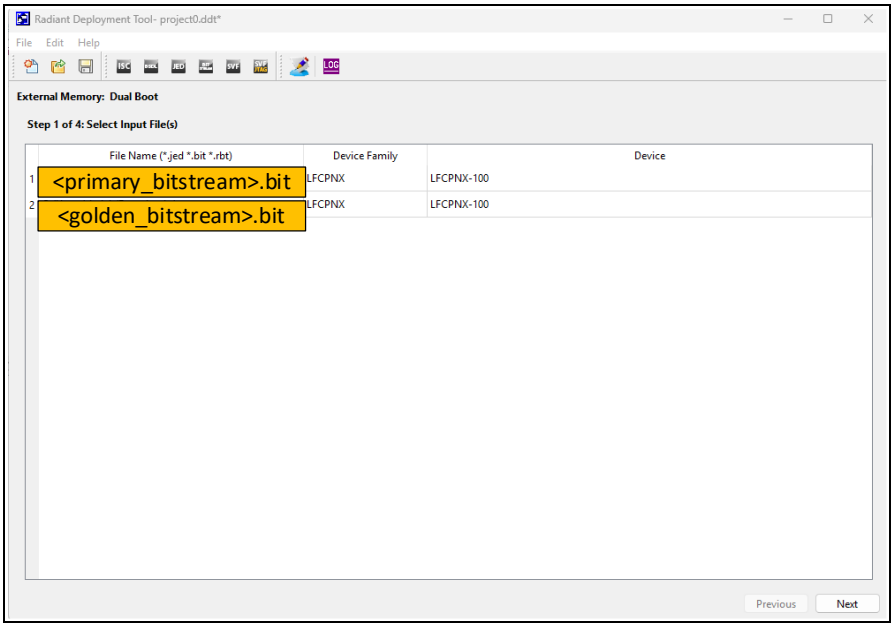


Figure 6.47. Select Input File

e. Configure the dual-boot option as required; ensure the golden and primary FPGA bitstream files are correctly selected.

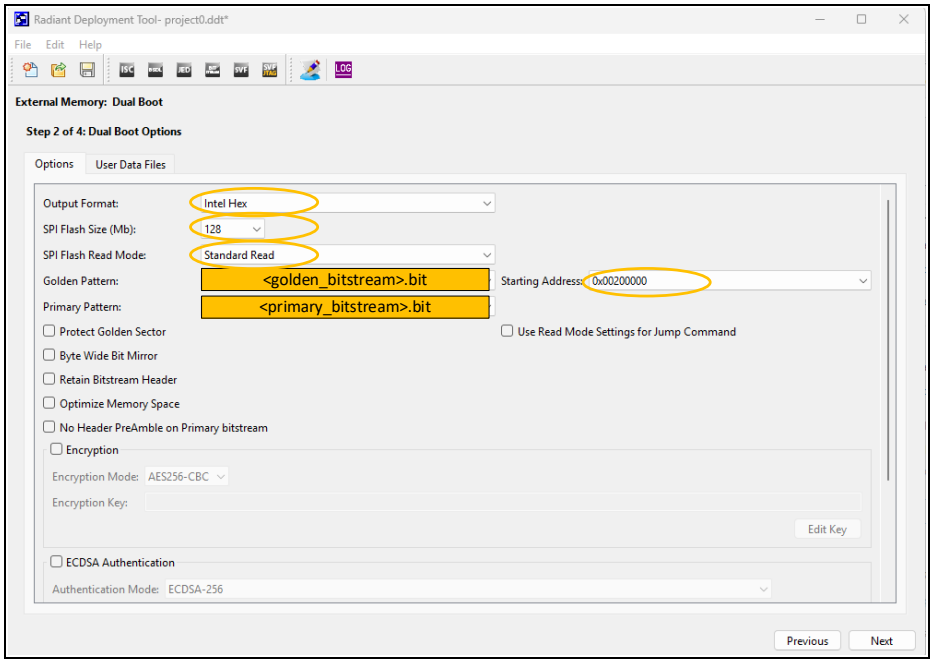


Figure 6.48. Dual Boot Options

f. Select the output file name and the save location.

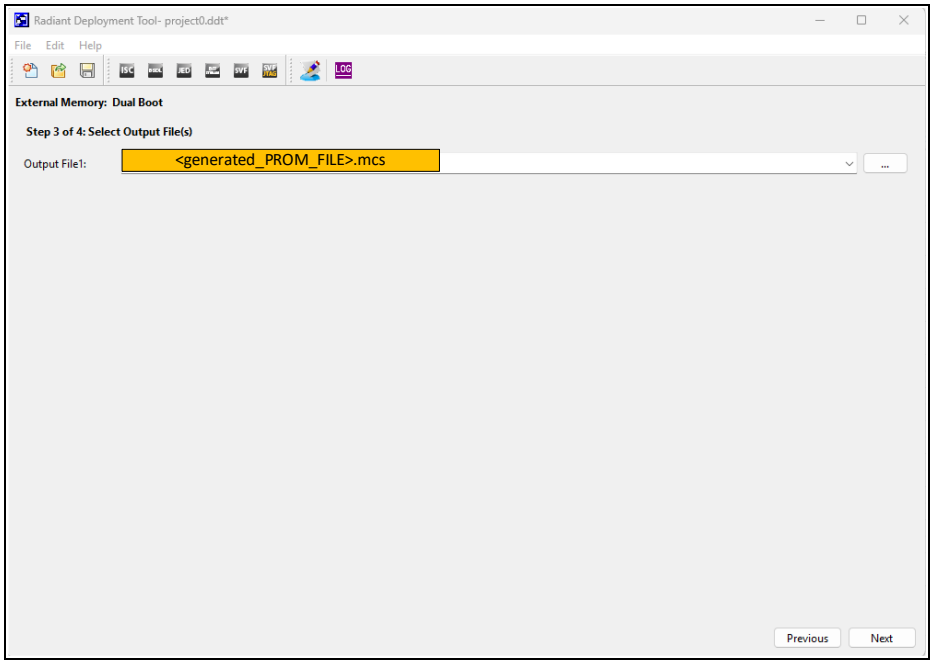


Figure 6.49. Select Output File

g. Generate the PROM file and confirm that the log shows a successful generation message.

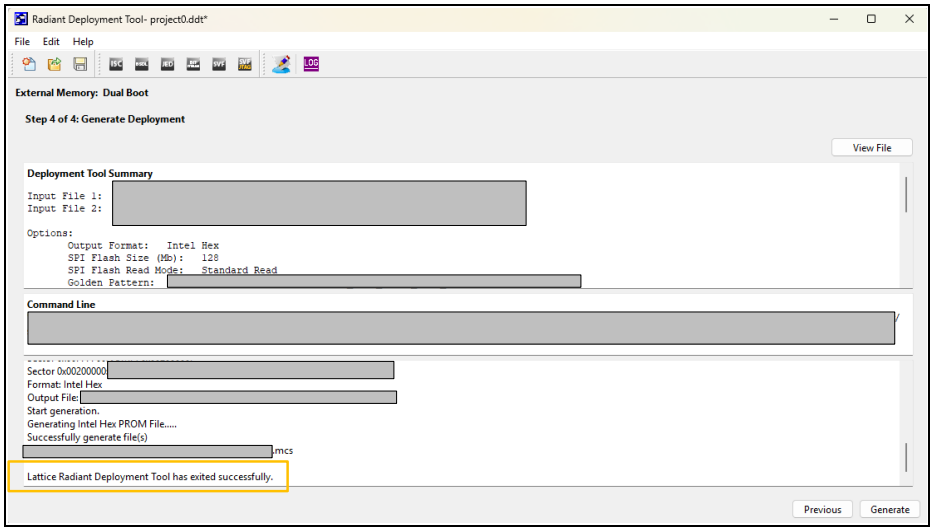


Figure 6.50. Generate Deployment

2. Program the PROM (.mcs) file.

   Programming the PROM file is the same as programming the bitstream file described in the Local Firmware Update through JTAG section. The only difference is that the input is the PROM file with the .mcs extension.

6.4.2.3. Testing Camera Video Streaming

1. Run the Holoscan Sensor Bridge demo container.
```
cd /<path>/<to>/<holoscan-sensor-bridge>
xhost +
sh docker/demo.sh
```
2. Run the camera video streaming example.

   This example will be streaming from the camera and display the video on AGX Orin.

   Note: Once Step 1 is executed in the AGX Orin terminal, the demo container starts, the command prompt will switch to the environment inside the container.
3. Run the video streaming demo for the camera using the following commands:
   - For 10GbE Ethernet using single camera:
     ```
     python examples/linux_imx274_player.py
     ```
   - For 10GbE Ethernet using dual camera
     ```
     python examples/linux_single_network_stereo_imx274_player.py
     ```

Figure 6.51 shows the camera video streaming test setup. The video is streamed by the NVIDIA host and captured in an office environment under lighting conditions ranging from 140 lux to 135 lux. The test environment is identical for 10GbE Ethernet configurations. Image quality remains consistent across both.

The primary objective of this reference design is to establish a robust and reliable bridge between the HSB interfaces and the NVIDIA host. Image tuning is not included. This process typically involves defining image quality parameters, configuring processing pipelines, and optimizing the image signal processor (ISP)—tasks that are highly specific to the camera sensor and require dedicated resources.

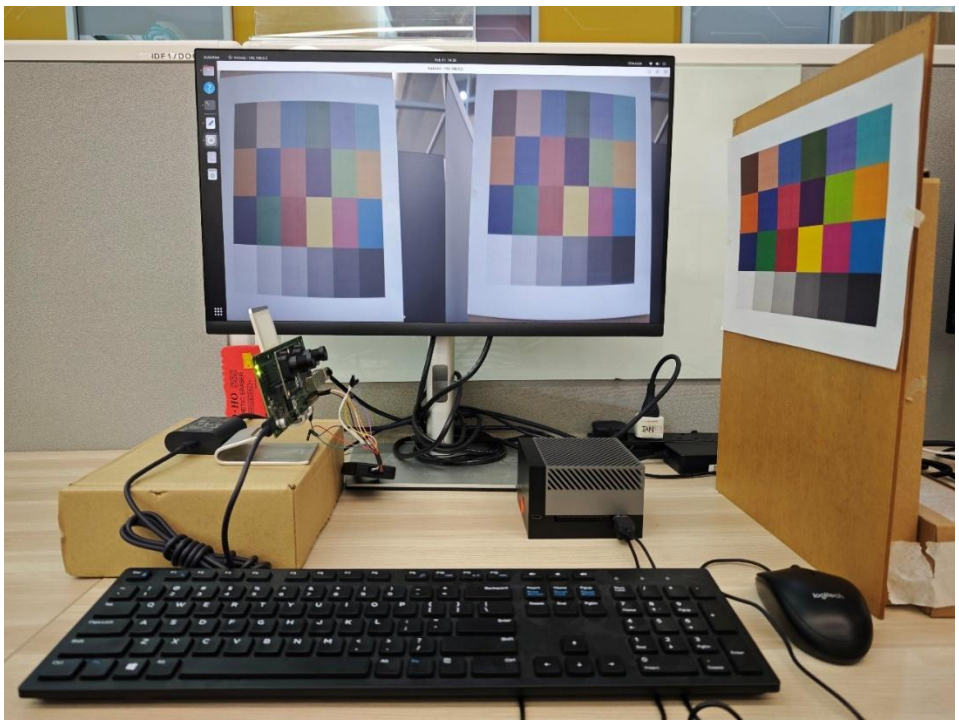


Figure 6.51. Dual IMX274 Camera Video Streaming Test Setup

7. Resource Utilization

The section shows the resource utilization of the reference design for the CertusPro-NX FPGA (LFCPNX-100-9LFG672I) device using the Synplify Pro tool in the Lattice Radiant software version 2025.2.0.48.0. Refer to the Compiling the Reference Design section for configuration details. Note that changes in design attributes may affect resource utilization, and values may vary over time due to feature updates, bug fixes, or other modifications.

7.1. Resource Utilization Using the CertusPro-NX Versa Board

7.1.1. Resource Utilization with Ethernet 1GbE

Table 7.1 shows one camera sensor interface configured with four MIPI lanes at 720 Mbps, paired with a single-port 1GbE Ethernet host interface.

Table 7.1. Logic Consumption for each Instance Available in the Reference Design

Instance name	LUT4 Logic	LUT4 Distributed RAM	LUT4 Ripple Logic	PFU Registers	DSP MULT	EBR
multicam_top (camera sensor interface)	2,213	0	256	1,871	0	9
Hololink_top (Hololink IP)	9,857	420	2,776	15,344	2	40
Ethernet_inst (Ethernet 1GbE- host interface)	3,125	18	910	3,463	0	5
Clk_rst	2	0	0	38	0	0
Miscellaneous	276	48	212	873	0	0
Total	15473	486	4,154	21,589	2	54

Note: Other submodules are categorized as miscellaneous in this table.

Table 7.2 compares the reference designs logic consumption with the available resources of the CertusPro-NX (LFCPNX-100-9LFG672I) device, based on the configuration described in Table 7.1.

Table 7.2. Comparison between Reference Design Utilization and CertusPro-NX Resources Available

	LUT	PFU registers	DSP Mult	EBR
LFCPNX-100 device logic resource	79,872	79,872	156	208
Reference design logic resource consumed	20,113	21,589	2	54
Reference design logic resource consumed (%)	25.18	27.03	1.28	25.96

From the place-and-route report, the device SLICE utilization summary after final SLICE packing is 77% used (31,036 out of 39,936 slices). The F_{MAX} used is 125 MHz.

7.1.2. Resource Utilization with Ethernet 10GbE

Table 7.3 shows one camera sensor interface configured with four MIPI lanes at a lane rate of 720 Mbps, and a single-port 10GbE Ethernet host interface.

Table 7.3. Logic Consumption for each Instance Available in the Reference Design

Instance name	LUT4 Logic	LUT4 Distributed RAM	LUT4 Ripple Logic	PFU Registers	DSP MULT	EBR
multicam_top (camera sensor interface)	2,312	0	248	1,981	0	8
Hololink_top (Hololink IP)	11,732	468	2,682	16,945	2	36
Ethernet_inst (Ethernet 10GbE- host interface)	3,945	0	110	2,976	0	4
Clk_rst	4	0	0	38	0	0
Miscellaneous	403	0	212	943	0	0
Total	18396	468	3,252	22,883	2	48

Note: Other submodules are categorized as miscellaneous in this table.

Table 7.4 compares the reference design logic consumption with the available resources of the CertusPro-NX (LFCPNX-100-9LFG672I) device, based on the configuration described in Table 7.3.

Table 7.4. Comparison between Reference Design Utilization and CertusPro-NX Resources Available

	LUT	PFU registers	DSP Mult	EBR
LFCPNX-100 device logic resource	79,872	79,872	156	208
Reference design logic resource consumed	22,116	22,883	2	48
Reference design logic resource consumed (%)	27.69	28.65	1.28	23.08

From the place-and-route report, the device SLICE utilization summary after the final SLICE packing is 85% used (34, 337 out of 39,936 slices). The FMAX used is 156.25 MHz.

7.2. Resource Utilization Using the CertusPro-NX Sensor-to-Ethernet Bridge Board

7.2.1. Resource Utilization with Ethernet 10GbE

Table 7.5 reports resource utilization only for the CertusPro-NX FPGA. The CrossLink-NX (LIFCL-17) FPGA is treated as external; its resource usage is not included here. Table 7.6 compares the reference design's logic usage with the available resources of the CertusPro-NX (LFCPNX-100-9LFG672C), using the configuration in Table 7.5.

Table 7.5. Logic Consumption for each Instance Available in the Reference Design

Instance name	LUT4 Logic	LUT4 Distributed RAM	LUT4 Ripple Logic	PFU Registers	DSP MULT	EBR
cam_sensor_rcvr[0] (LVDS DDR RX interface)	1,050	0	58	766	0	3
cam_sensor_rcvr[1] (LVDS DDR RX interface)	1,038	0	58	766	0	3
Hololink_top (Hololink IP)	24,058	2,820	3,774	31,462	2	62
Ethernet_inst (Ethernet 10GbE- host interface X2)	8,140	0	220	6,694	0	8
Clk_rst	4	0	0	38	0	0
Miscellaneous	949	48	328	1,729	0	0
Total	35,235	2,868	4,438	41,455	2	76

Note: Other submodules are categorized as miscellaneous in this table

Table 7.6. Comparison between Reference Design Utilization and CertusPro-NX Resources Available

	LUT	PFU registers	DSP Mult	EBR
LFCPNX-100 device logic resource	79,872	79,872	156	208
Reference design logic resource consumed	42,541	41,455	2	76
Reference design logic resource consumed (%)	53.26	51.90	1.28	36.54

From the place-and-route report, the device SLICE utilization summary after the final SLICE packing is 90% used (35,941 out of 39,936 slices). The F_{MAX} used is 156.25MHz.

8. Debug Methodology

This section outlines the recommended steps for debugging the camera video streaming setup in the Holoscan Sensor Bridge reference design. By following this procedure, you can verify system functionality and identify potential issues during integration and testing.

8.1. CertusPro-NX Versa Board

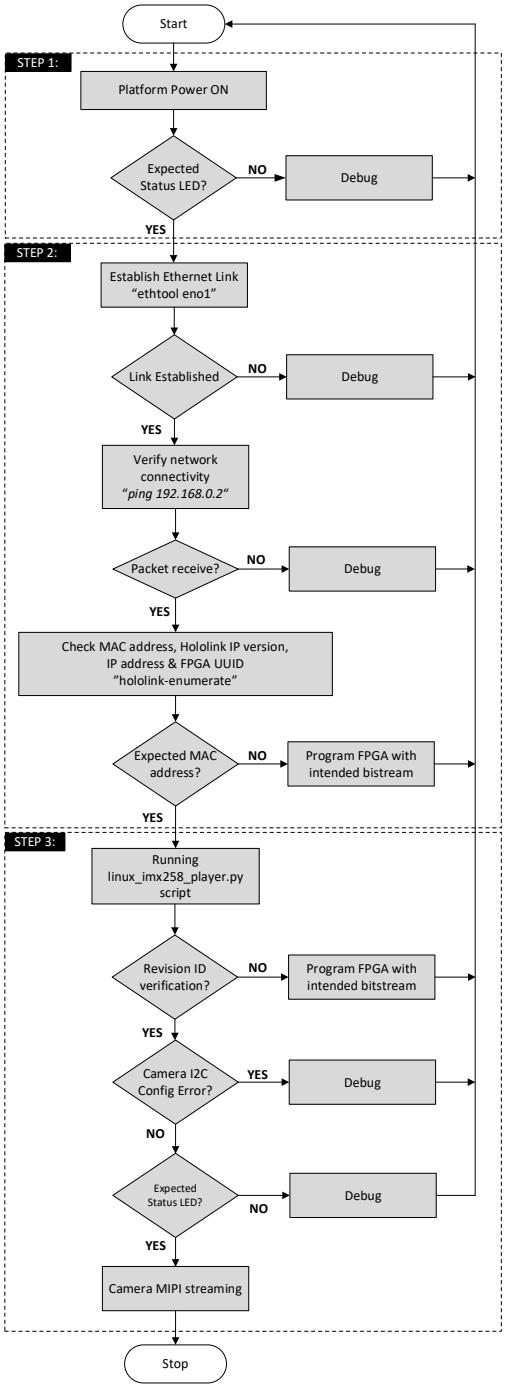


Figure 8.1. Debug Methodology Flow Chart For RD

8.1.1. Powering Up the Board

1. Power cycle the board after programming.
   After programming the FPGA firmware into the external SPI flash, fully power down the platform, then power it back up. This power cycle ensures the FPGA correctly loads and configures the new firmware.
2. Verify LED status.
   After powering up, check the status LEDs on the board. Refer to Figure 8.2 for LED locations. These LEDs indicate the board operational status. Table 8.1 explains each LED behavior and meaning.
   Note: This step assumes the HSB Docker container is already set up on the host system.

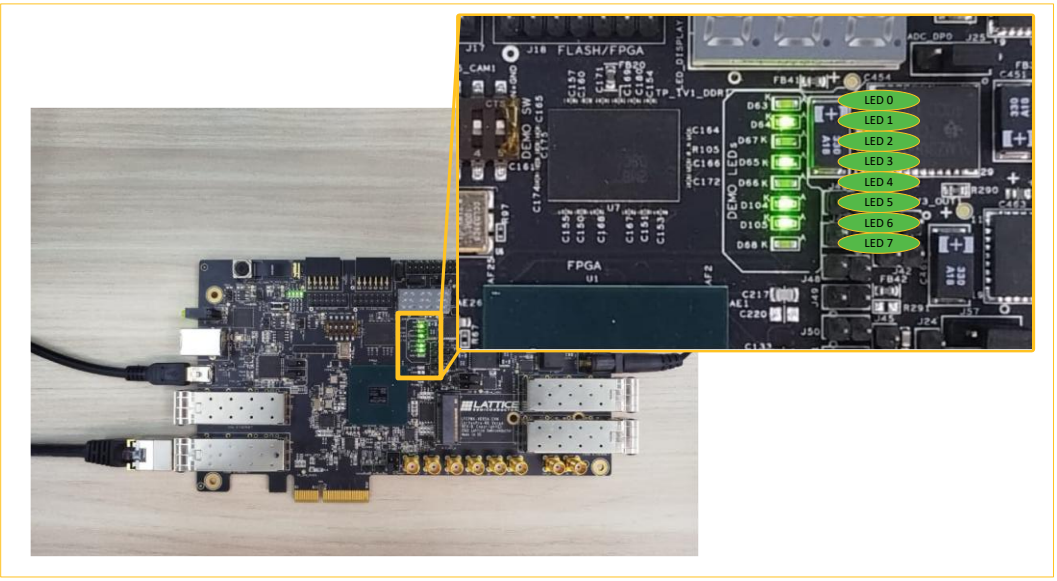


Figure 8.2. Position of the LED on CertusPro-NX Versa Board

Table 8.1 shows the LED status upon power-up.

Table 8.1. LED Status upon Board Power-up

LED	Connected Signal	Board Power UP
LED0	pcs_clk_heart_beat	LED toggles
LED1	hif_clk_heart_beat	LED toggles
LED2	byte_clk_heart_beat	OFF
LED3	plat_rst_n (platform reset)	ON
LED4	sif_rst	OFF
LED5	sw_sen_rst	ON
LED6	cam_rst_n	ON
LED7	hif_rst	OFF

8.1.1.1. Troubleshooting Common Issues

- **Issue A: No status LEDs turn on at power-up**.
  - Workaround 1: Check that the CertusPro-NX Versa board power supply is connected and the 12 V switch is turned on.
  - Workaround 2: Power cycle the board using 12 V switch.
  - Workaround 3: Reprogram the FPGA to confirm the correct bitstream is used.
  - Workaround 4: If the issue persists, submit a technical support case through Lattice Technical Support.

- **Issue B: LED is not toggling**.
  Possible cause: Ethernet IP configuration issue.
  - Workaround 1: Regenerate the Ethernet IP with the correct settings. Recompile and reprogram the FPGA device with the newly compiled FPGA bitstream.
  - Workaround 2: If the issue persists, submit a technical support case through Lattice Technical Support.
- **Issue C: Reset status LED behave unexpectedly**.
  Possible cause: Custom changes to HDL source code or software patches.
  - Review your modifications to the reference design HDL source code and any applied software patches.

8.1.2. Verifying the Ethernet Connection

1. Check the Ethernet link status.
   On the host terminal, run *ethtool eno1* command. This verifies whether the Ethernet link is established, and confirms that the link speed is as expected. If successful, the terminal will display the link status, as shown in Figure 8.3.

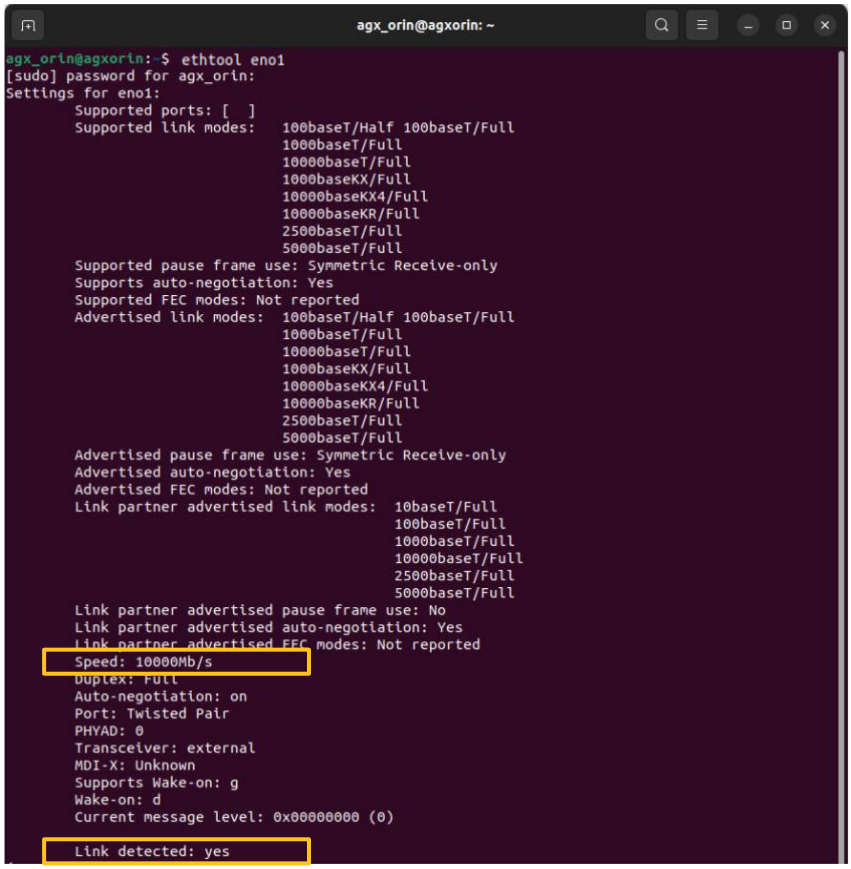


Figure 8.3. Ethernet Link Establishment Status

2. Test the Ethernet connectivity.
   Run *ping 192.168.0.2* command on the host terminal. A successful response confirms that the network connection is active. You should see messages indicating that packets are being received. Refer to Figure 8.4 for an example of successful ping response from the evaluation board.

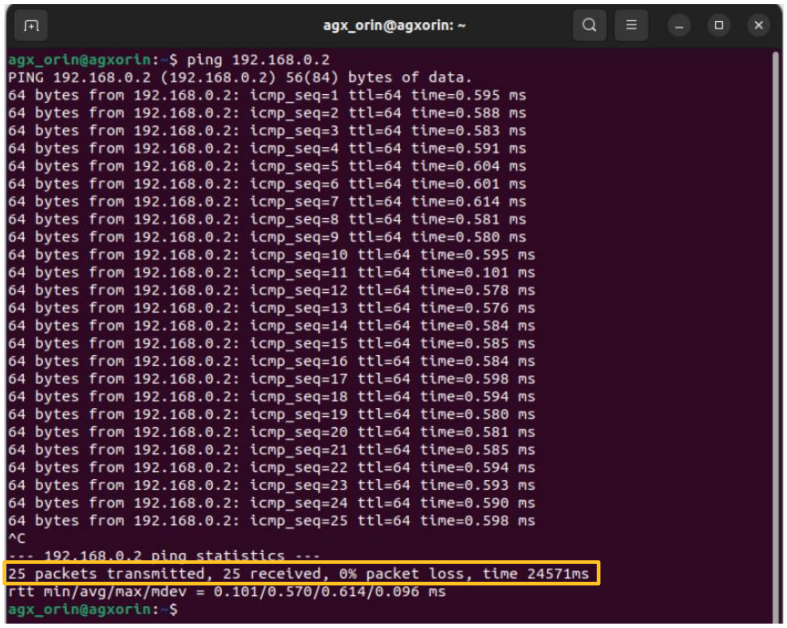


Figure 8.4. Data Packet Received by Host

3. Verify the device information.
   On the host HSB container prompt, run *hololink-enumerate* command. This command displays the MAC address, Hololink IP version, IP address, and FPGA UUID. See Figure 8.5 for a sample output.

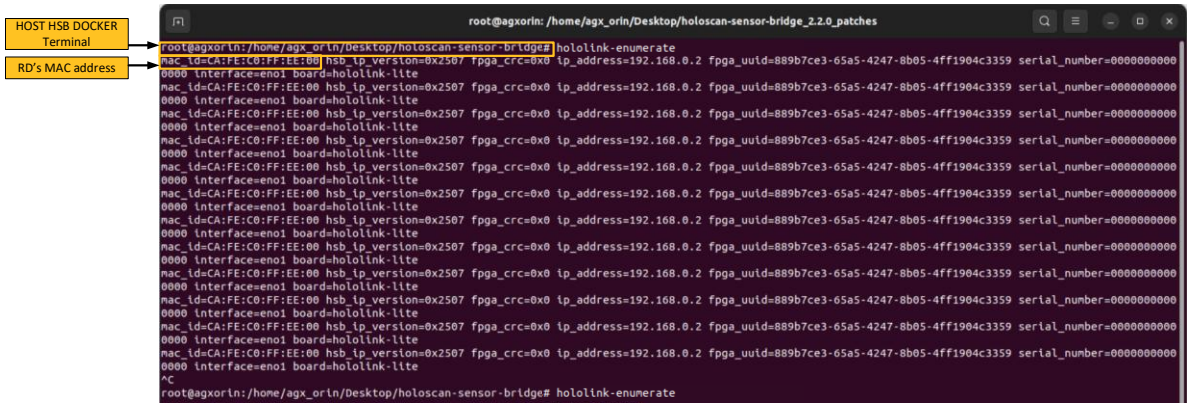


Figure 8.5. Sample Output

8.1.2.1. Troubleshooting Connection Issues

If you encounter issues during steps 1 or 2, try the following:

- Workaround 1: Ensure the SFP module is securely locked into the SFP cage.
- Workaround 2: Confirm that the LAN cable is properly connected to both the SFP module and the host LAN port. If the connection is correct, the LAN indicator light should be **ON**, as shown in Figure 8.6.

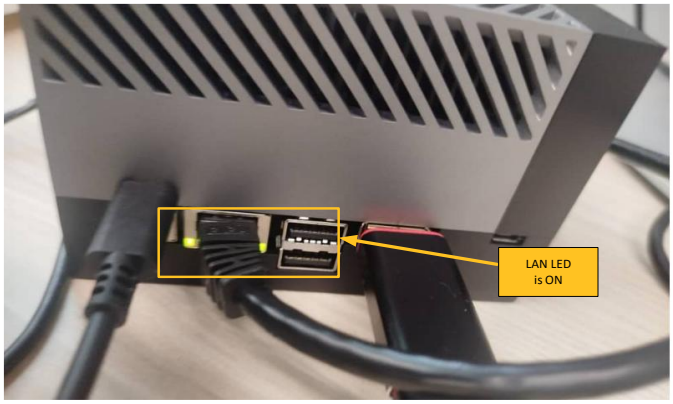


Figure 8.6. LAN Light Indication on Host

8.1.3. Running the Streaming Script (linux_imx258_player.py)

8.1.3.1. Preparing the Streaming Script

Run the script. Follow the steps in the Camera Video Streaming Test section to run the *linux_imx258_player.py* command on the host HSB docker container prompt.

8.1.3.2. Monitoring the Output of the Streaming Script

Once the script is running, observe the following:

1. Verify the Revision ID.
   Check the log for the Revision ID to confirm the FPGA firmware version. Figure 8.7 shows the Revision ID version from the host HSB docker container prompt, which represents the bitstream version for the CertusPro-NX with 10GbE Ethernet.

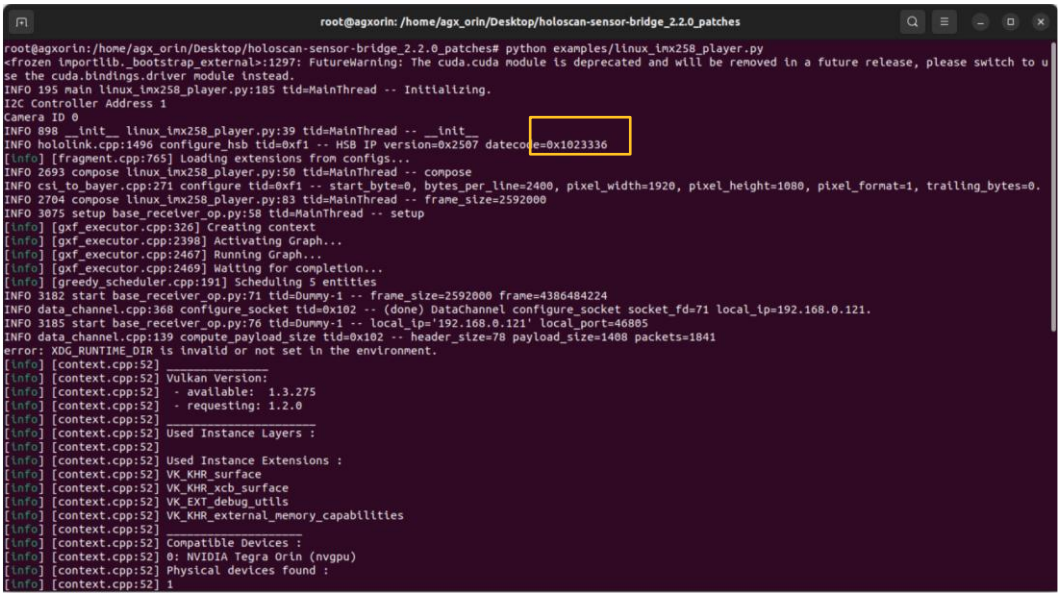


Figure 8.7. Revision ID Version

2. Check the camera for I2C configuration errors.
   Look for any I2C configuration errors in the log, when the *linux_imx258_player.py* script is executed. Figure 8.8 shows an example of a failed camera I2C configuration.

Figure 8.8. Camera I2C Configuration Fail Log

3. Observe the status LED.
   Refer to Table 8.2 for expected LED behavior. The byte clock heartbeat LED should toggle, indicating that the camera sensor is transmitting MIPI data.

Table 8.2. Expected Status LED Behavior when running linux_imx258_player.py.script

LED	Connected Signal	MIPI camera streaming
LED0	pcs_clk_heart_beat	LED toggles
LED1	hif_clk_heart_beat	LED toggles
LED2	byte_clk_heart_beat	LED toggles
LED3	plat_rst_n (platform reset)	ON
LED4	sif_rst	OFF
LED5	sw_sen_rst	ON
LED6	cam_rst_n	ON

4. Confirm MIPI Camera Streaming
   If no errors are detected, the MIPI camera stream should display successfully on the host monitor.

8.1.3.3. Troubleshooting Common Issues

- **Issue A: Revision ID version mismatch.**
  - Workaround: Reprogram the HSB board with the correct FPGA bitstream version.
- **Issue B: Camera I2C Configuration error.**
  - Workaround 1: Ensure the *IMX258* camera sensor is properly connected.
  - Workaround 2: If you are using your own reference design HDL code, verify that the camera reset signal is not asserted.
  - Workaround 3: If you are using your own software patch, confirm the I2C configuration port is correctly targeted.
  - Workaround 4: If you are using your own software patch, ensure the camera sensor register settings are correct.

8.2. CertusPro-NX Sensor-to-Ethernet Bridge Board

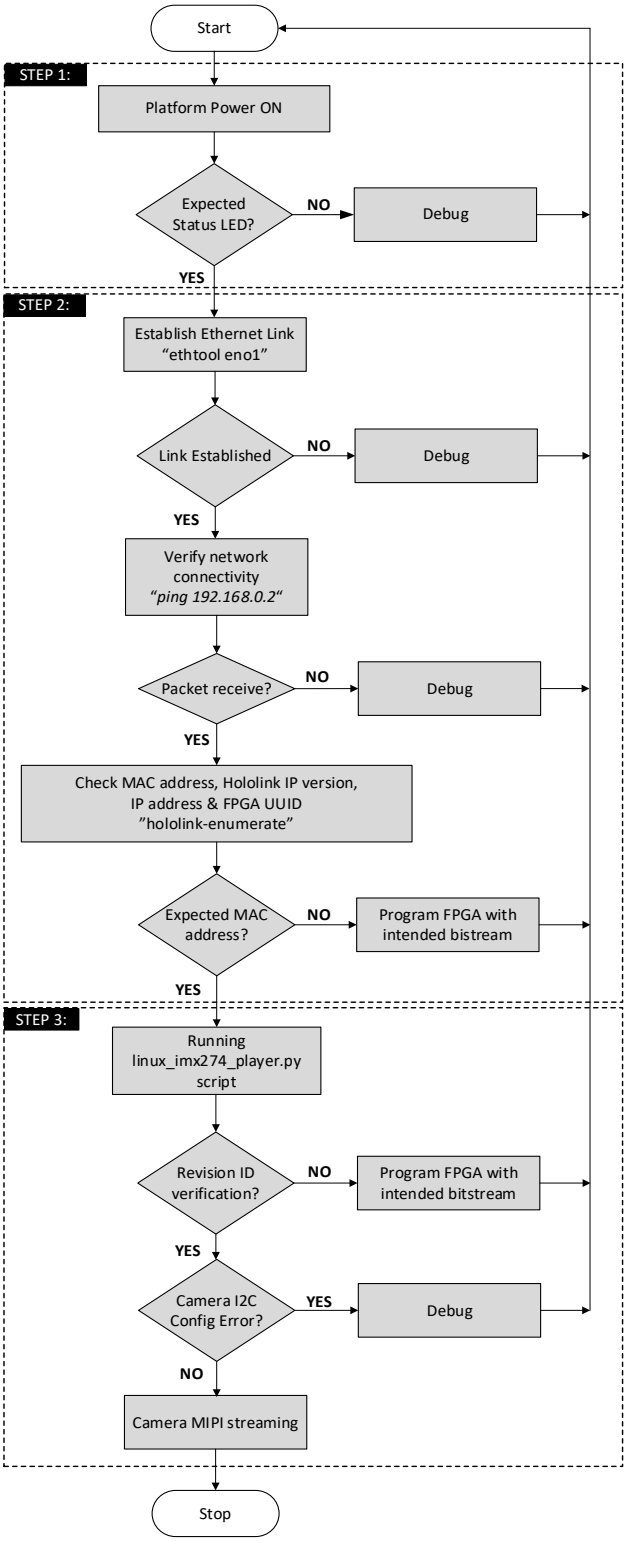


Figure 8.9. Debug Methodology Flow Chart For RD

8.2.1. Powering Up the Board

1. Power cycle the board after programming the FPGA bitstream into the external SPI flash.
   After programming the FPGA firmware into the external SPI flash, fully power down the platform, then power it back up. This power cycle ensures the FPGA correctly loads and configures the new firmware.
2. Verify LED status.
   After powering up, check the status LEDs on the board. Refer to Figure 8.10 for LED locations. These LEDs indicate the board operational status. Table 8.3 explains each LED behavior and meaning.
   Note: This step assumes the HSB Docker container is already set up on the host system.

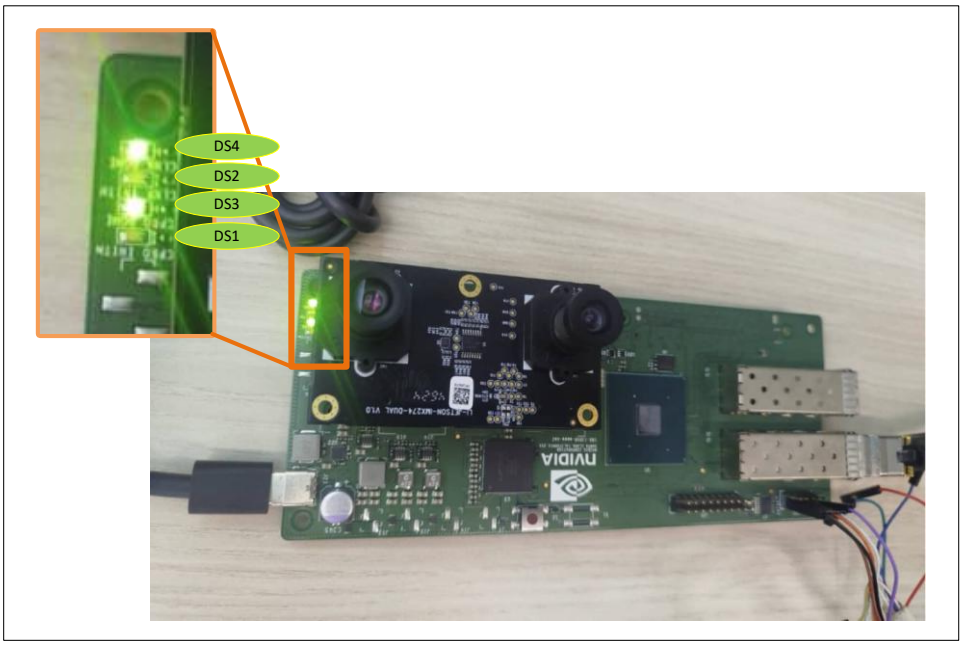


Figure 8.10. Position of the Status LED on CertusPro-NX Sensor-to-Ethernet Bridge Board

Table 8.3 shows the LED status upon power-up.

Table 8.3. LED Status upon Board Power-up

LED	Connected Signal	Board Power UP
DS1	CPRO INITN	OFF
DS2	CLNK INITN	OFF
DS3	CPRO DONE	ON
DS4	CLNK DONE	ON

Use the INITN status pin to monitor errors during configuration. After configuration completes successfully, DONE asserts and the FPGA enters User Mode.

8.2.1.1. Troubleshooting Common Issues

- **The status LEDs do not behave as described in** Table 8.3.
  - Workaround 1: Check that the CertusPro-NX Sensor-to-Ethernet Bridge Board power supply is connected and is turned on.
  - Workaround 2: Power cycle the board.
  - Workaround 3: Reprogram the FPGA to confirm the correct bitstream is used.
  - Workaround 4: If the issue persists, submit a technical support case through Lattice Technical Support.

8.2.2. Verifying the Ethernet Connection

1. Check the Ethernet link status.
   On the host terminal, run *ethtool eno1* command. This verifies whether the Ethernet link is established, and confirms that the link speed is as expected. If successful, the terminal will display the link status, as shown in Figure 8.11.

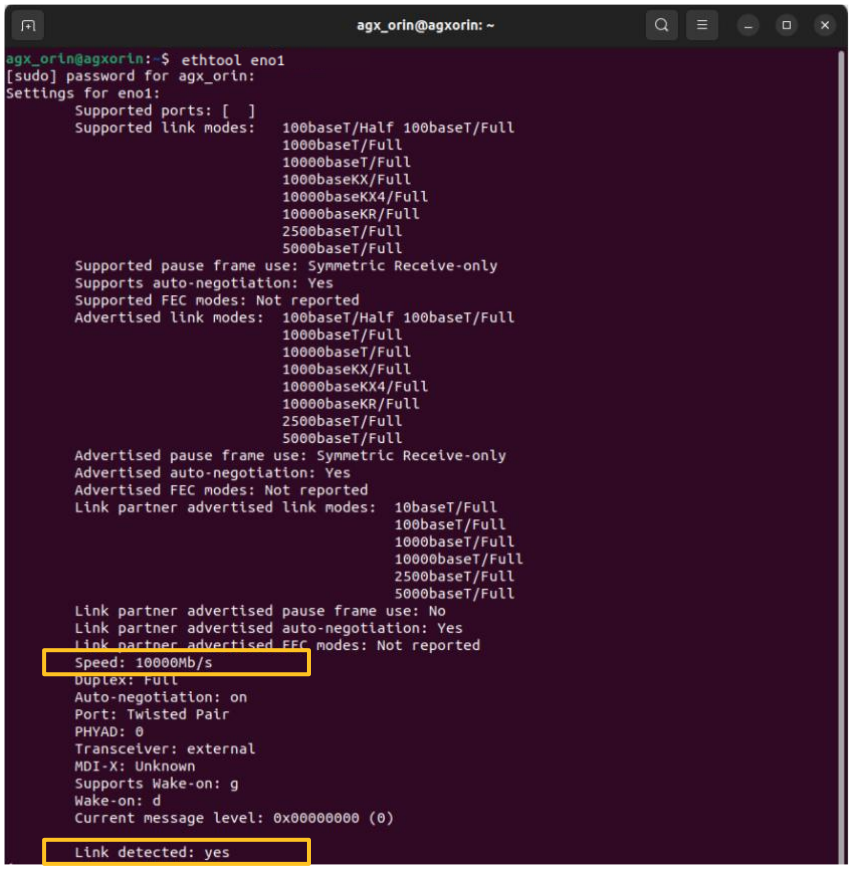


Figure 8.11. Ethernet Link Establishment Status

2. Test the Ethernet connectivity.
   Run *ping 192.168.0.2* command on the host terminal. A successful response confirms that the network connection is active. You should see messages indicating that packets are being received. Refer to Figure 8.12 for an example of successful ping response from the evaluation board.

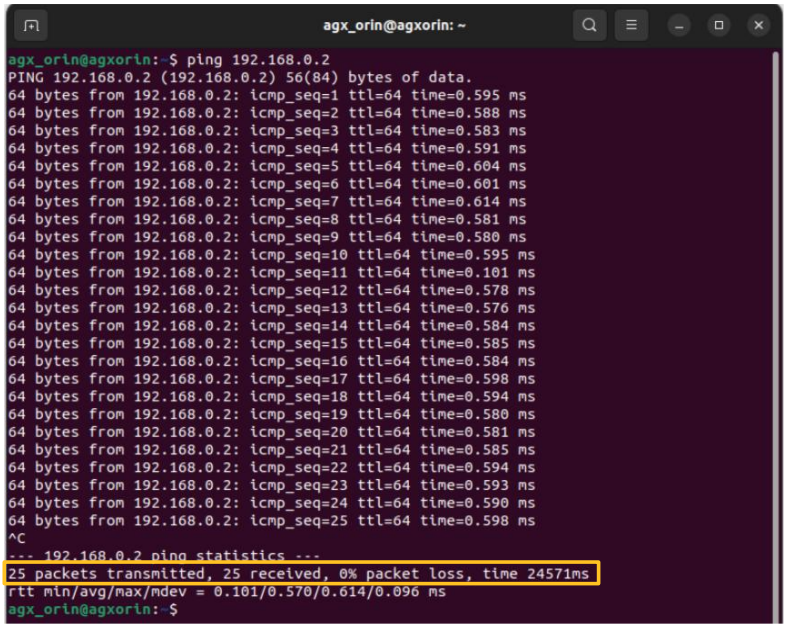


Figure 8.12. Data Packet Received by Host

3. Verify the device information.
   On the host HSB container prompt, run *hololink-enumerate* command. This command displays the MAC address, Hololink IP version, IP address, and FPGA UUID. See Figure 8.13 for a sample output.

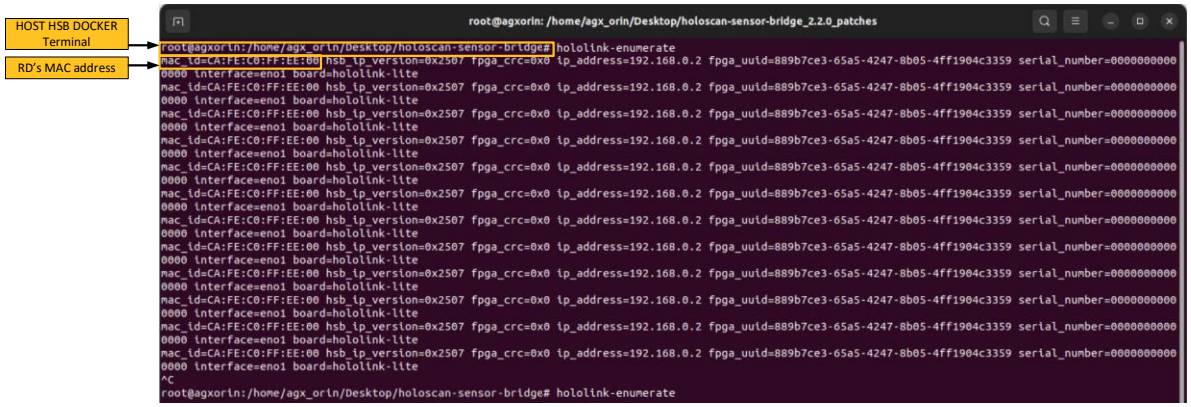


Figure 8.13. Sample Output

8.2.2.1. Troubleshooting Connection Issues

If you encounter issues during steps 1 or 2, try the following:

- Workaround 1: Ensure the SFP module is securely locked into the SFP cage.
- Workaround 2: Confirm that the LAN cable is properly connected to both the SFP module and the host LAN port. If the connection is correct, the LAN indicator light should be on, as shown in Figure 8.14.

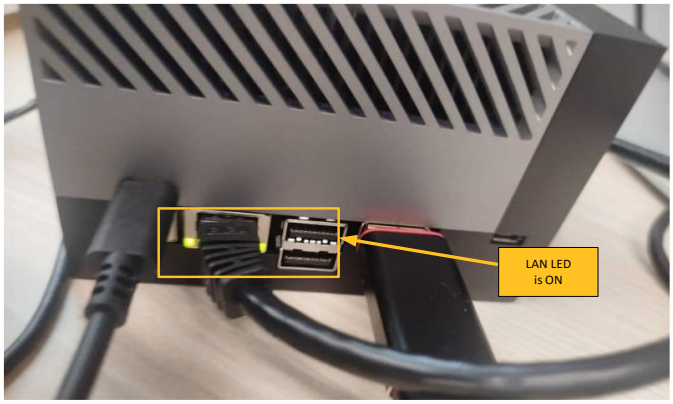


Figure 8.14. LAN Light Indication on Host

8.2.3. Running the Streaming Script (linux_imx274_player.py)

8.2.3.1. Preparing the Streaming Script

Run the script. Follow the steps in the Camera Video Streaming Test section to run the *linux_imx274_player.py* command on the host HSB docker container prompt.

8.2.3.2. Monitoring the Output of the Streaming Script

Once the script is running, observe the following:

1. Verify the Revision ID.
   Check the log for the Revision ID to confirm the FPGA firmware version. Figure 8.15 shows the Revision ID version from the host HSB docker container prompt, which represents the bitstream version for the CertusPro-NX with 10GbE Ethernet.

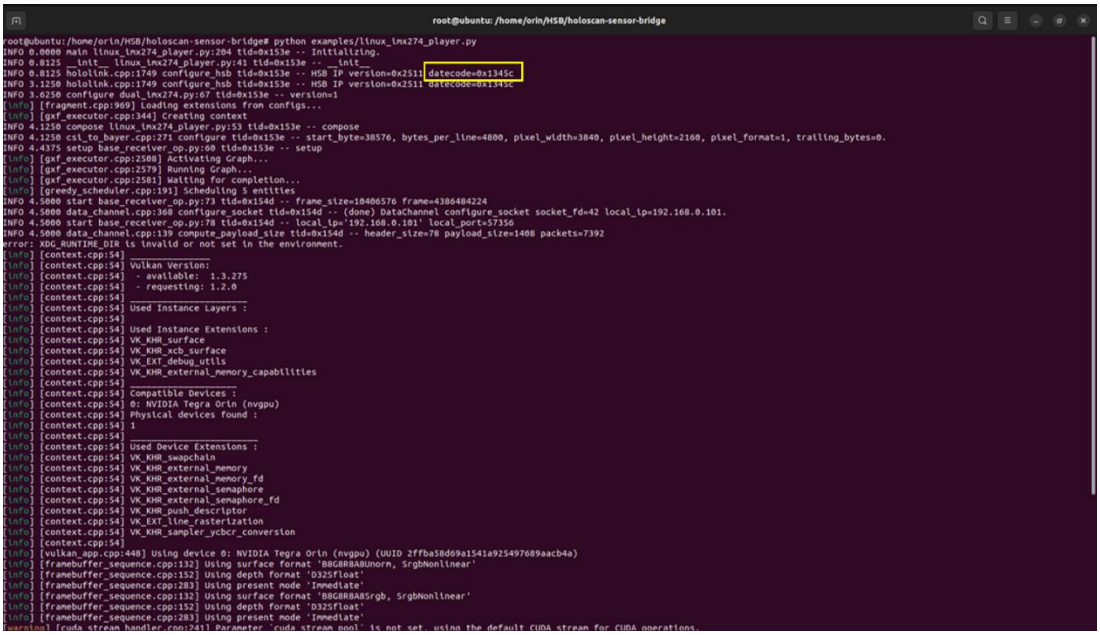


Figure 8.15. Revision ID Version

2. Check the camera for I2C configuration errors.
   Look for any I2C configuration errors in the log, when the *linux_imx274_player.py* script is executed. Figure 8.16 shows an example of a failed camera I2C configuration.

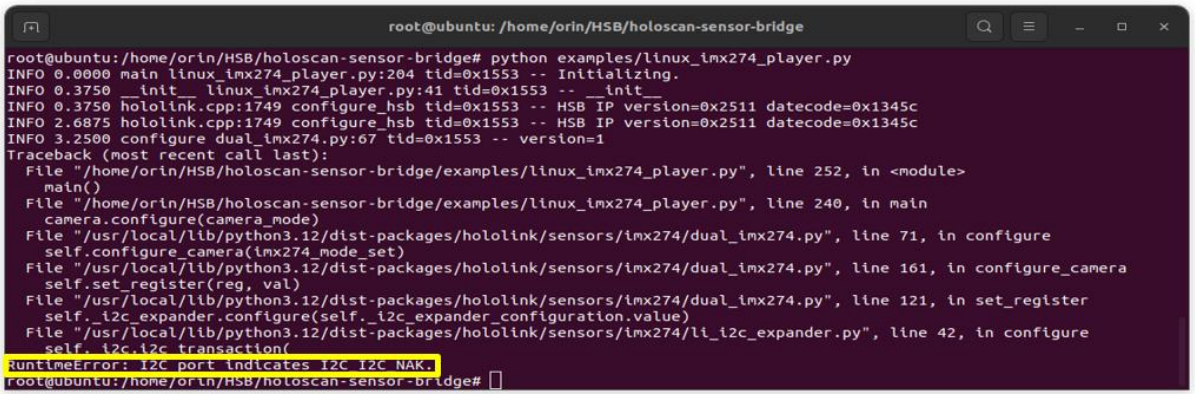


Figure 8.16. Camera I2C Configuration Fail Log

3. Confirm MIPI Camera Streaming.
   If no errors are detected, the MIPI camera stream should display successfully on the host monitor.

8.2.3.3. Troubleshooting Common Issues

- **Issue A: Revision ID version mismatch.**
  - Workaround: Reprogram the HSB board with the correct FPGA bitstream version.
- **Issue B: Camera I2C Configuration Error.**
  - Workaround 1: Ensure the *IMX274* camera sensor is properly connected.
  - Workaround 2: If you are using your own reference design HDL code, verify that the camera reset signal is not asserted.
  - Workaround 3: If you are using your own software patch, confirm the I2C configuration port is correctly targeted.
  - Workaround 4: If you are using your own software patch, ensure the camera sensor register settings are correct.

Appendix A: Known Issues

1. When using certain types of 1000BASE-T RJ-45 SFP module, the network link may fail to establish, and no link LED activity is observed during this condition.
2. When using certain types of 10GBASE-T SFP+ modules, the network link may fail to establish, and no link LED activity is observed during this condition. Additionally, the Ethernet MAC may reset unexpectedly. This issue has been identified and is scheduled to be addressed in a future software release.

References

- CertusPro-NX Versa Board User Guide (FPGA-EB-02053)
- CertusPro-NX Sensor to Ethernet Bridge Board User Guide (FPGA-EB-02069)
- CSI-2/DSI D-PHY Receiver IP Core - User Guide (FPGA-IPUG-02081)
- Multi-Boot User Guide for Nexus Platform (FPGA-TN-02145)
- CertusPro-NX Versa Board web page
- CertusPro-NX Sensor-to-Ethernet Bridge Board web page
- CertusPro-NX Versa Holoscan Kit web page
- CSI-2/DSI D-PHY Receiver IP Core web page
- CSI-2/DSI D-PHY Transmitter IP Core web page
- NVIDIA Holoscan - NVIDIA Docs NVDIA Holoscan Docs Hub
- NVIDIA Jetson Developer Kits web page
- Lattice Radiant FPGA design software
- Lattice Radiant Software User Guide
- Lattice Insights for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, please refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 1.3, April 2026

Section	Change Summary
All	• Corrected HSB SDK version from *2.5.0-EA* to *2.5.0.* • Minor editorial fixes.
Introduction	• Updated Tri-speed Ethernet version to *2.1.0* in Table 1.2. Summary of CertusPro-NX Versa Board with NVIDIA Jetson AGX Thor. • Updated LVDS DDR Receiver version to *1.7.0* in Table 1.3. Summary of CertusPro-NX Sensor-to-Ethernet Bridge Board with NVIDIA Jetson AGX Orin.

Functional Description	• Updated the following *key components* in the Ethernet 10GbE Support with 10GBase-T SFP+ Transceiver section.
	  • Updated encoding/decoding to support *64b/66b schemes*.
	  • Removed *1GbE* support in the SFP+ transceiver module.

Implementing the Reference Design	• Updated the Test Setup on the CertusPro-NX Versa Board section.
	  • Updated the reference of step 2 to *Local Firmware Update through USB Interface* in the Programming the Golden FPGA Bitstream with a Jump Table subsection.
	• Updated the Test Setup on the CertusPro-NX Sensor-to-Ethernet Bridge Board section.
	  • Updated the reference of step 2 to *Local Firmware Update through JTAG* in the Programming the Golden FPGA Bitstream with a Jump Table subsection.

Revision 1.2, March 2026

Section	Change Summary
All	• Changed the document title from *CertusPro-NX Versa Board – Customizable HSB Sensor Interfaces* to *Customizable HSB Sensor Interfaces on Lattice CertusPro-NX Platforms.* • Added the *CertusPro-NX Sensor-to-Ethernet Bridge Board platform* in this document.
Abbreviations in This Document	Added CMOS, DDR, Hex, PMA, and PROM in this section.
Introduction	Reworked section content.
Directory Structure and File Overview	Reworked section content.
Functional Description	Reworked section content.
Customizing the Reference Design	Reworked section content.
Compiling the Reference Design	Reworked section content.
Implementing the Reference Design	Reworked section content.
Resource Utilization	• Updated the resource utilization values for CertusPro-NX Versa Board. • Added resource utilization for CertusPro-NX Sensor-to-Ethernet Bridge Board.
Debug Methodology	Reworked section content.
Appendix A. Known Issues	Added known issue regarding *10GBASE-T SFP+ modules*.
References	Added the following: • CertusPro-NX Versa Board User Guide (FPGA-EB-02053) • CertusPro-NX Sensor to Ethernet Bridge Board User Guide (FPGA-EB-02069) • Multi-Boot User Guide for Nexus Platform (FPGA-TN-02145) • CertusPro-NX Versa Board web page • CertusPro-NX Sensor-to-Ethernet Bridge Board web page • CertusPro-NX Versa Holoscan Kit web page • NVIDIA Jetson Developer Kits web page

Revision 1.1, March 2026

Section	Change Summary
All	• Updated Hololink IP version from *2507* to *2511*. • Added Thor platform.

Introduction	• Added the *Thor* platform in this section.
	• Updated the following in Table 1.1. Summary of the Reference Design
	  • Lattice Radiant software version to *2025.2.0.48.0*.
	  • NVIDIA Holoscan SDK from *3.3.0* to *3.7.0*.
	  • HSB SDK from *2.2.0* to *2.5.0-EA.*
	• Added the following in Table 1.1. Summary of the Reference Design
	• Added *Host Software* (*AGX Thor).*
	  • Added AGX Thor cable 100G QSFP28 to 4×25G SFP28 Breakout Active Optical Cable (AOC).

Functional Description	Updated Holoscan Sensor Bridge version from *2.2.0* to *2.5.0-EA* in the Hololink IP Overview section.
Customizing the Reference Design	• Added a disclaimer in this section that the screenshots are for reference only. • Updated the GitHub link in the Hololink IP section.
Compiling the Reference Design	• Added a disclaimer in this section that the screenshots are for reference only. • Updated Lattice Radiant software version to *2025.2.0.48.0* in the Configuring the Lattice Radiant Software to Compile the Reference Design section.
Implementing the Reference Design on the CertusPro-NX Versa Board	• Added hardware and software requirements for NVIDIA Thor. • Updated the HSB SDK version to *2.5.0-EA.* • Added Figure 6.3. Setup with AGX Thor for 10G Ethernet. • Added NVIDIA Platform Host Setup section and moved the Jetson AGX Orin Developer Kit under this section. • Minor updates on the commands in the Configuring the AGX Orin Developer Kit section. • Added the Jetson AGX Thor Developer Kit section. • Added a note indicating that only Jetson AGX Orin supports 1G Ethernet in the Remote Firmware Updated via Ethernet section and in the Camera Video Streaming Test section.
Resource Utilization	• Reworked Table 7.1. Logic Consumption for each Instance Available in the Reference Design and in Table 7.3. Logic Consumption for each Instance Available in the Reference Design. • Reworked Table 7.2. Comparison between Reference Design Utilization and CertusPro-NX Resources Available and Table 7.4. Comparison between Reference Design Utilization and CertusPro-NX Resources Available. • Updated the *SLICE packaging percentage* in this section.

Revision 1.0, November 2025

Section	Change Summary
All	Initial release.

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