SERDES Reference Clock

Introduction

This document discusses the ORT82G5, ORT42G5, ORSO82G5 and ORSO42G5 FPSC devices [1] reference clock input characteristics and the selection/interconnection of the external reference clock source. The reference clock signal quality is critical to SERDES high speed signal interfaces, as is demonstrated in Appendix A. Clock signal jitter can cause jitter generation at the transmit data output port and affect jitter tolerance of receiver data input port. Care must be taken in the selection and connection of the reference clock source to obtain optimum jitter performance. Several possible commercial oscillator manufacturers are identified and alternative interconnections circuits are presented.

Reference Clock Input Characteristics

The ORT82G5, ORT42G5, ORSO82G5 and ORSO42G5 provide two separate REFCLK differential inputs, to allow device operation under two different clock domains. Each REFCLK input port services four of the eight available SERDES channels. Each differential input port has an internal differential amplifier with significant common-mode signal rejection characteristics. The minimum required differential input level requirement is 500 mVp-p. The maximum input is 2 Vp-p. The input common-mode voltage may be set to any level which maintains each input peak voltage between VDD and ground potential.

Clock Source Selection

A crystal oscillator or crystal oscillator-based clock source with differential output is recommended. The experiment described in Appendix A shows that reference clock signal jitter does contribute directly to SERDES transmit signal jitter. It is therefore important to select a clock source with low jitter characteristics. The source should contain power supply decoupling (internal and/or external) and ideally be located on the same circuit board as the SERDES device.

A number of crystal oscillator products on the market are compatible with the ORT82G5, ORT42G5, ORSO82G5 and ORSO42G5. Several are listed in the table below.

*Table 1. Crystal Oscillator Products Compatible with the ORT82G5, ORT42G5, ORSO82G5 and ORSO42G5 Devices*

Vendor	Model	Output	Comments
Connor Winfield [6]	P123	LVPECL	small size SMD package
Epson [3]	EG-2101CA	PECL	SMD package, 50ppm
MF Electronics [5]	M2980	LVPECL	thru-hole/ gull-wing pkg, low jitter specified
Saronix [2]	SDS3811	LVDS	SMD package, to 20ppm
Vectron [4]	XO-480	LVPECL or LVDS	SMD package, to 10ppm

Interconnection Circuit Alternatives

A differential output interconnection to the ORT82G5, ORT42G5, ORSO82G5 and ORSO42G5 is recommended to minimize the conversion of system common mode noise into clock signal jitter. This is achieved by taking advantage of the common-mode rejection of the internal differential receiver. If the source signal is shared with other devices or inputs on the circuit board, it is recommended that high speed differential buffering be provided to distribute a dedicated differential output signal to each device reference clock input.
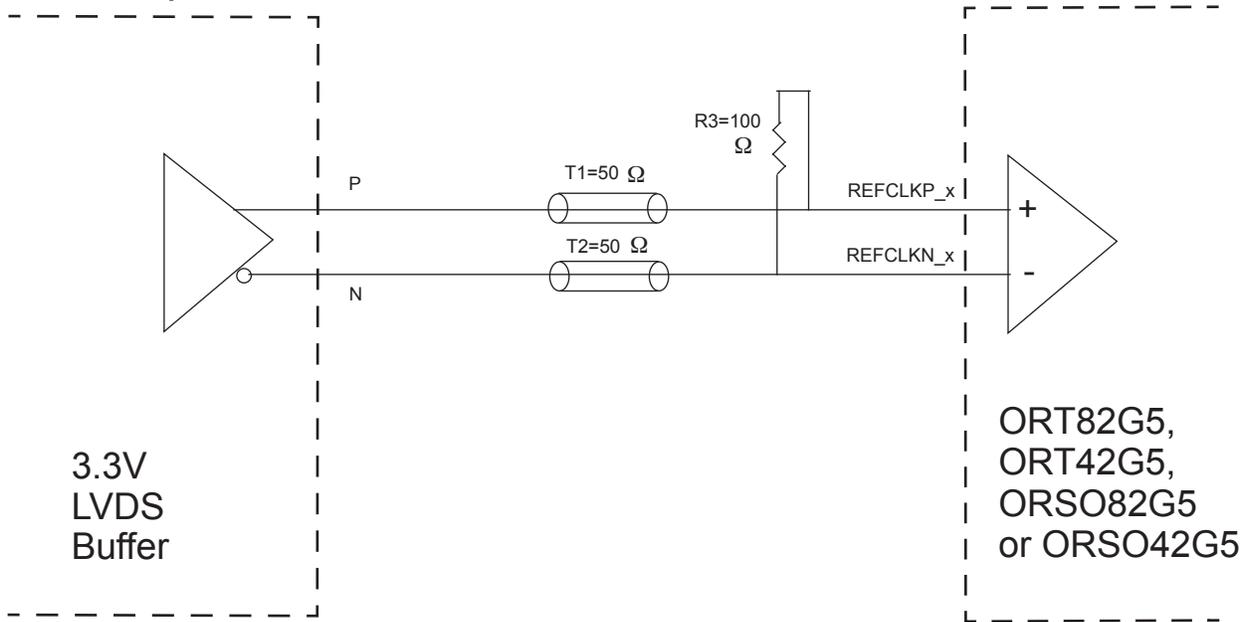
The recommended interconnection of a 3.3V LVPECL Reference Clock source to the Quad SERDES input port is shown in Figure 1.

Figure 1. DC Coupled LVPECL Interface
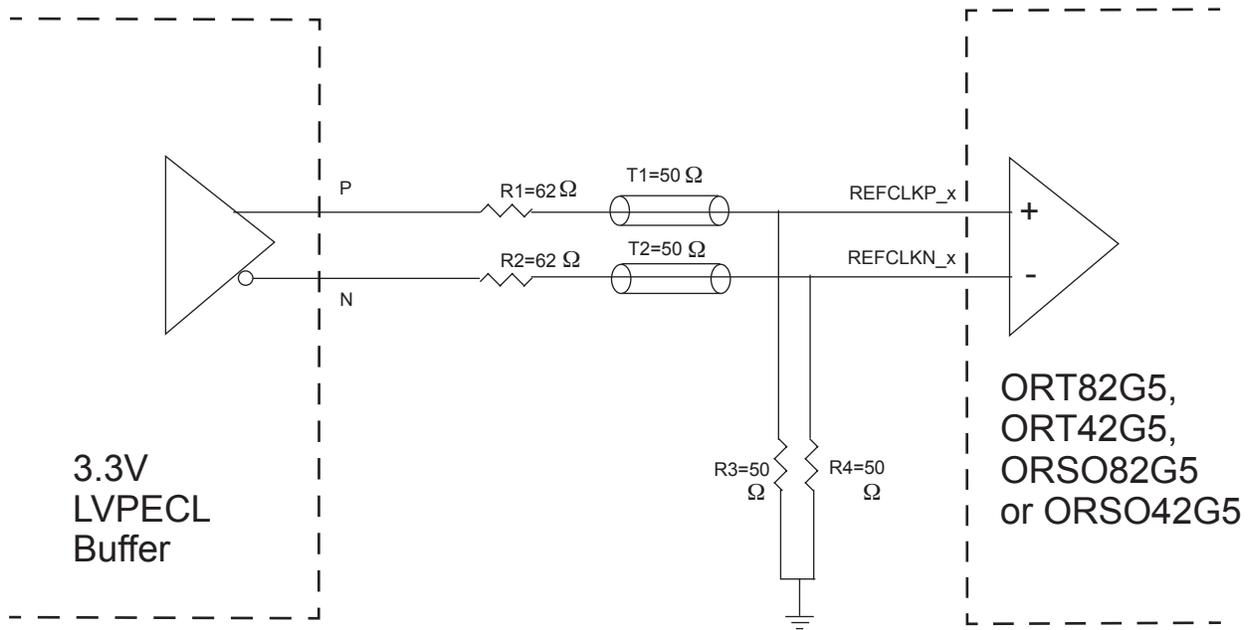
The dc coupling scheme from the 3.3V LVPECL clock signal buffer output allows a minimal number of discrete components in the interconnection circuit.

Figure 2. DC-Coupled LVDS Interface

The standard LVDS output dc voltage is compatible with the ORT82G5, ORT42G5, ORSO82G5 and ORSO42G5 RefClk input, allowing a very simple interface circuit. The single termination resistor should minimize the possibility of system generated EM noise coupling into the reference clock signal.

Figure 3. AC-Coupled PECL Interface
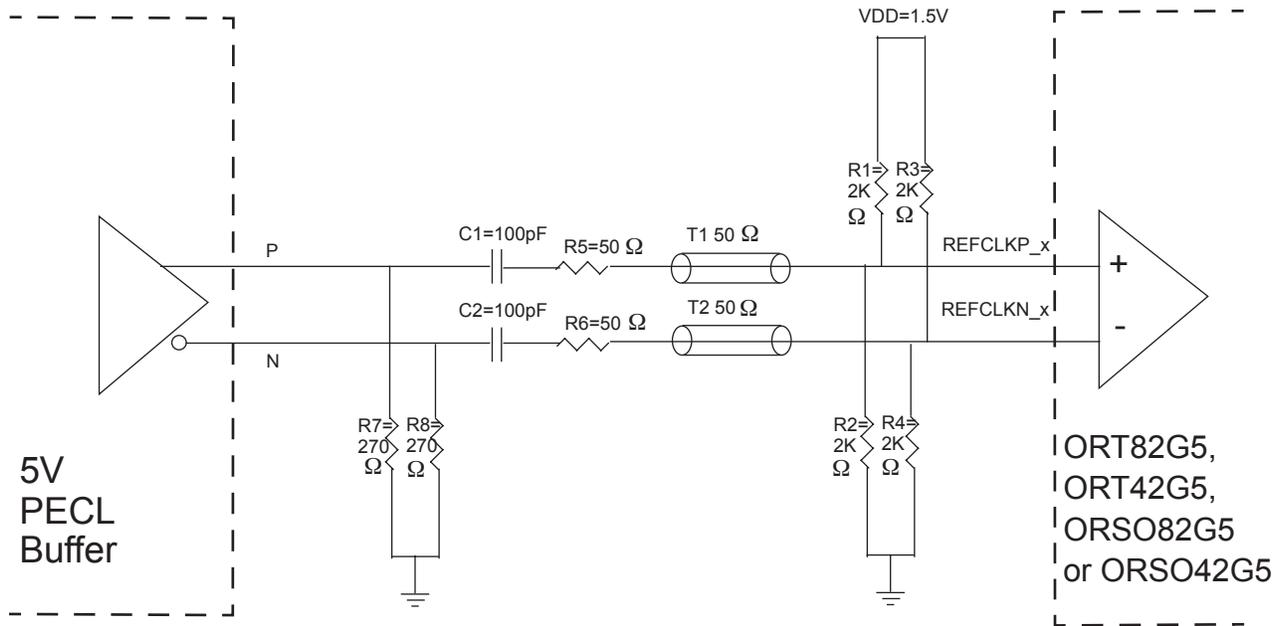
A conventional ECL source terminated configuration is used with ac coupling. Resistive voltage divider biasing of the Reference Clock input pins must be provided.

Applications where SERDES jitter performance is not critical may consider using single-ended reference clock interconnections. Such interconnections have been successfully used in laboratory testing. For these cases, external biasing and capacitive bypassing of the unused input must be provided. These applications may also choose to drive both reference clock ports of the ORT82G5, ORT42G5, ORSO82G5 or ORSO42G5 with a single clock source output. Care must be taken to minimize trace lengths between the transmission line, line termination resistors, and Reference Clock input pins.

PCB Layout Recommendations

To minimize differential clock signal noise and jitter at the ORT82G5, ORT42G5, ORSO82G5 and ORSO42G5 device input, the T1/T2 transmission line connection path should have the following characteristics:

- adjacent stripline point-to-point 50 ohm transmission lines or coupled adjacent lines with 100 ohm differential characteristic impedance

- matched length, to within 0.05 inch (1.27mm)

- cross-talk coupling to other signal traces on the PCB minimized

- stripline implementation

- The discrete components in Figures 1 and 3 should be placed according to the following recommendations:

- PCB connection trace lengths should be kept as short as possible.

- Corresponding components on the P and N signal sides should be placed close to each other, to minimize system coupled differential noise.

Conclusion

The ORT82G5, ORT42G5, ORSO82G5 and ORSO42G5 SERDES jitter performance is sensitive to the external reference clock signal jitter. For best performance, a differential transmission line clock signal should be used. Interconnection circuits for several oscillator output formats were recommended and described. Careful PCB layout with some specific recommendations was presented. Several possible oscillator vendors were identified.

References

1. ORCA ORT82G5 and ORT42G5 Data Sheet

2. Saronix, http://www.saronix.com/

3. Epson Electronics America, http://www.eea.epson.com/go/products/displayCategory?categoryId=EEA.QD.Crystal_Oscillators

4. Vectron International, http://www.vectron.com/

5. MF Electronics, http://www.mfelectronics.com/products/xo/

6. Connor Winfield, http://www.conwin.com

7. ORCA ORSO82G5 and ORSO42G5 Data Sheet

Appendix A - SERDES Jitter Sensitivity

A simple experiment was performed in the laboratory to determine the effect of reference clock input jitter on ORT82G5, ORT42G5, ORSO82G5 and ORSO42G5 SERDES transmit jitter. Sinusoidial jitter was injected onto the reference clock signal, while observing SERDES output signal jitter. DCA measured eye-diagram waveforms of the data output signal and reference clock input signal are shown in the following 4 figures. Figure 4 is with no jitter added. Figures 5, 6, and 7 are with sinusoidial jitter added to the reference clock signal. The frequency of the jitter signal is indicated in each of these figures. Note that in all four Figures, a density function of the reference clock transitions (horizontal axis crossing, at the center level) is shown.

Figure 4. Transmit Data Output & Ref Clk Eye-Diagrams with No Jitter Added
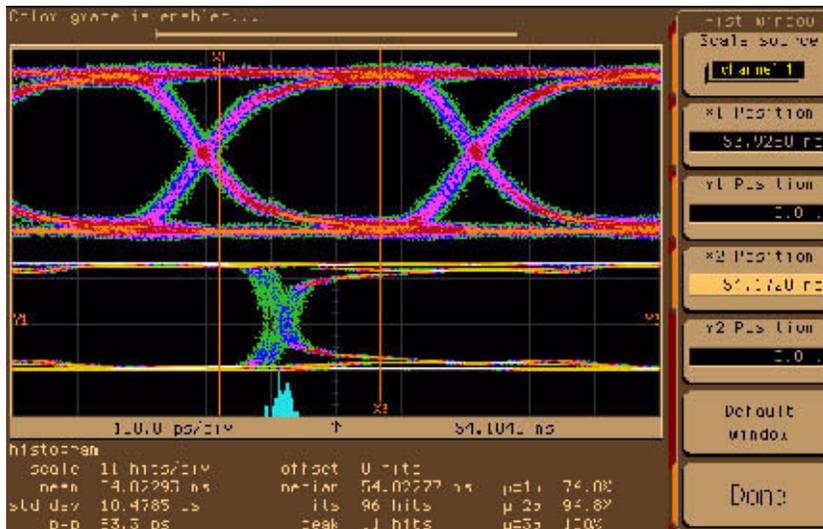
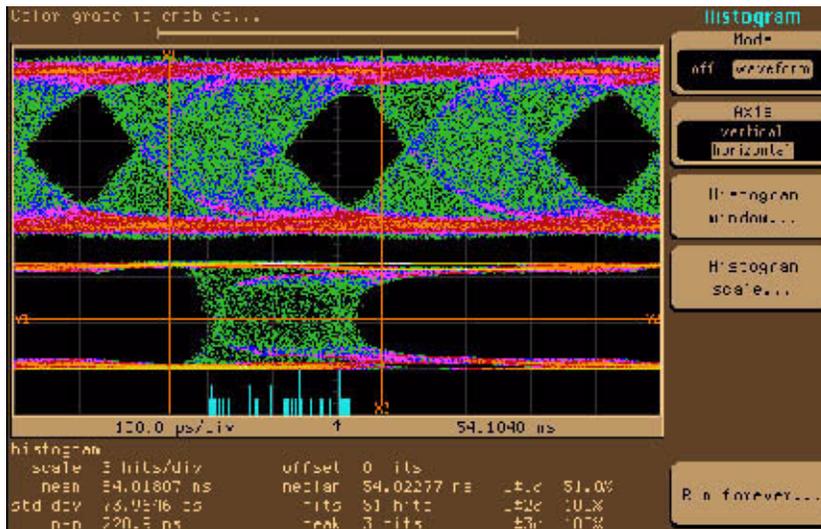*Figure 5. Transmit Data Output & Ref Clk Eye-Diagrams with 10 KHz Jitter Added*

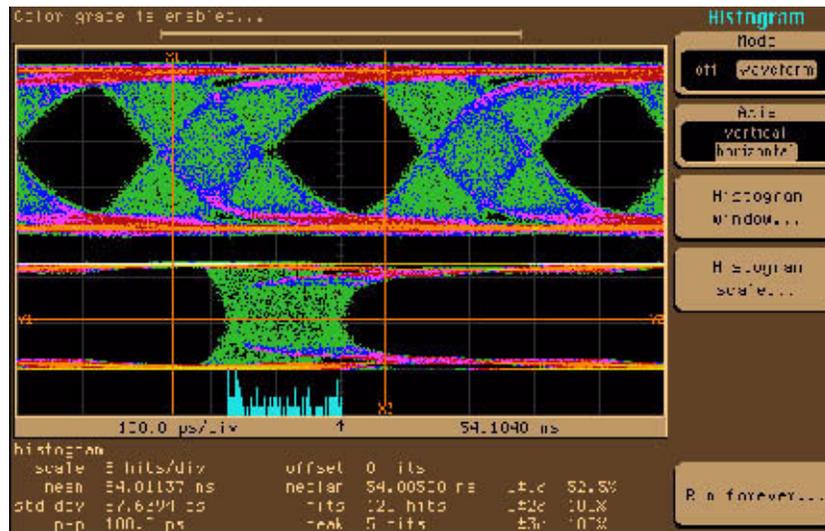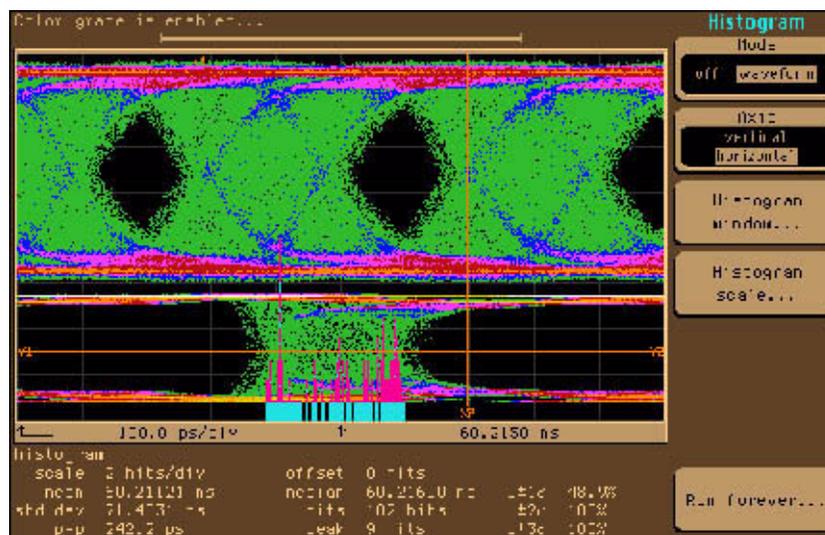*Figure 6. Transmit Data Output & Ref Clk Eye-Diagrams with 100 KHz Jitter Added*

Figure 7. Transmit Data Output & Ref Clk Eye-Diagrams with 500 KHz Jitter Added

Discussion

Comparing Figure 4 to Figure 5, it can been seen that adding jitter to the reference clock signal causes an increase in transmitter output signal jitter. Observing the amount of jitter on the two waveforms in Figures 5 through Figure 7, it can be seen they are approximately the same. The conclusion drawn from this experiment is that there is a 1 to 1 jitter transfer from the reference clock signal to the transmit output signal. This is an expected result which will apply to jitter frequencies below about 5 MHz (the closed loop bandwidth of the SERDES transmit clock PLL).