MachXO sysCLOCK Design and Usage Guide

September 2011 **Technical Note TN1089**

Introduction

As clock distribution and clock skew management become critical factors in overall system performance, the Phase Locked Loop (PLL) is increasing in importance for digital designers. Lattice incorporates its sysCLOCK™ PLL technology in the MachXO™ device family to help designers manage clocks within their designs. The PLL components in the MachXO device family use the same PLL as the LatticeECP™, LatticeEC™ and LatticeXP™ families.

The number of PLLs for each device are listed in Table 10-1.

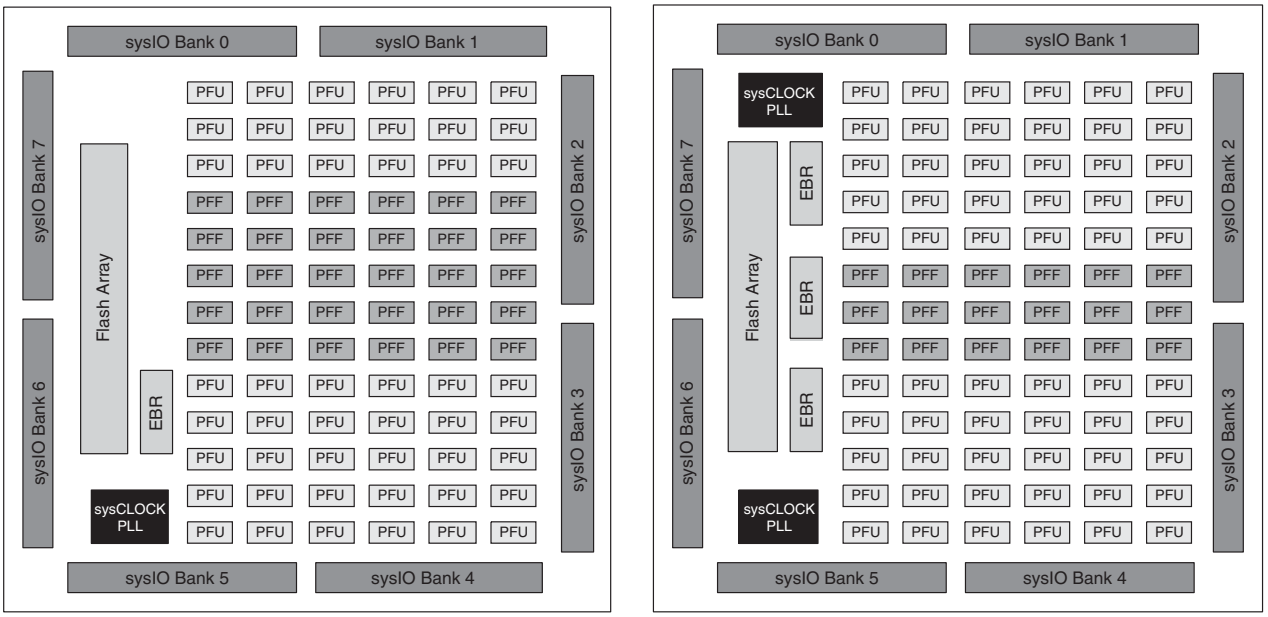
Table 10-1. MachXO Family and PLLs

	MachXO256	MachXO640	MachXO1200	MachXO2280
Number of PLLs	0	0	1	2

MachXO Top Level View

Figure 10-1 shows a chip-level view of the MachXO1200 and MachXO2280.

Figure 10-1. Top Level View of MachXO1200 and MachXO2280

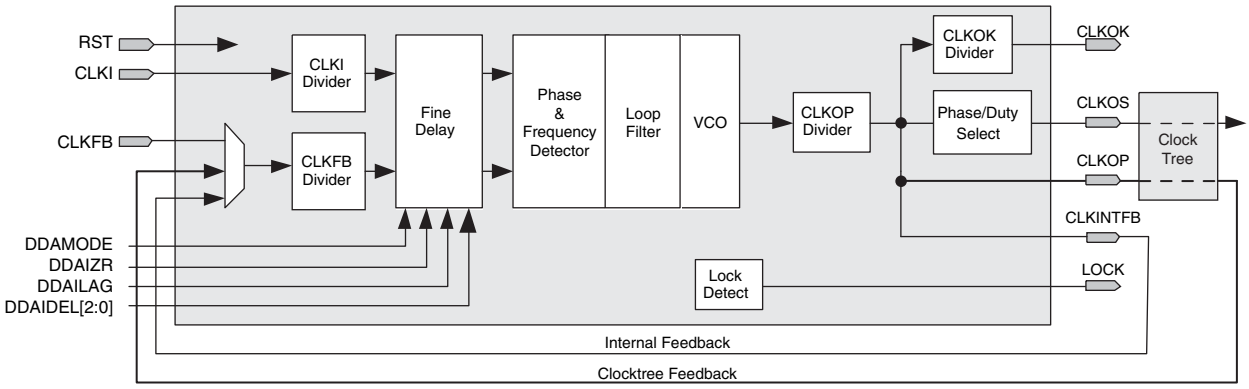


MachXO1200 **MachXO2280**

sysCLOCK PLL

This technical note describes the features and functions of the PLLs and their configuration in the ispLEVER® design tool. Figure 10-2 shows the block diagram of the PLL.

Figure 10-2. PLL Block Diagram



Features

- Clock synthesis
- Phase shift/duty cycle selection
- Internal, clock tree and external feedback
- Dynamic delay adjustment
- No external components required
- Lock detect output

Functional Description

PLL Divider and Delay Blocks

Input Clock (CLKI) Divider

The CLKI divider is used to control the input clock frequency into the PLL block. The divider setting directly corresponds to the divisor of the output clock. The input and output of the input divider must be within the input and output frequency ranges specified in the MachXO Family Data Sheet.

Feedback Loop (CLKFB) Divider

The CLKFB divider is used to divide the feedback signal. Effectively, this multiplies the output clock, because the divided feedback must speed up to match the input frequency into the PLL block. The PLL block increases the output frequency until the divided feedback frequency equals the input frequency.The input and output of the feedback divider must be within the input and output frequency ranges specified in the MachXO Family Data Sheet.

Delay Adjustment

The delay adjust circuit provides programmable clock delay. The programmable clock delay allows for step delays in increments of 250ps (nominal) for a total of 2.00ns lagging or leading. The time delay setting has a tolerance. See the MachXO Family Data Sheet for details. Under this mode, CLKOP, CLKOS and CLKOK are identically affected. The delay adjustment has two modes of operation:

Static Delay Adjustment: In this mode, the user-selected delay is configured at power-up.

Dynamic Delay Adjustment (DDA): In this mode, a simple bus is used to configure the delay. The bus signals are available to the general purpose FPGA.

Output Clock (CLKOP) Divider

The CLKOP divider serves the dual purposes of squaring the duty cycle of the VCO output and scaling up the VCO frequency into the 420MHz to 840MHz range to minimize jitter. Refer to Table for CLKOP Divider values.

CLKOK Divider

The CLKOK divider feeds the global clock net. It divides the CLKOP signal of the PLL by the value of the divider. It can be set to values of 2, 4, 6,....126,128.

PLL Inputs and Outputs

CLKI Input

The CLKI signal is the reference clock for the PLL. It must conform to the specifications in the MachXO Family Data Sheet in order for the PLL to operate correctly. The CLKI can be derived from a dedicated dual-purpose pin or from routing.

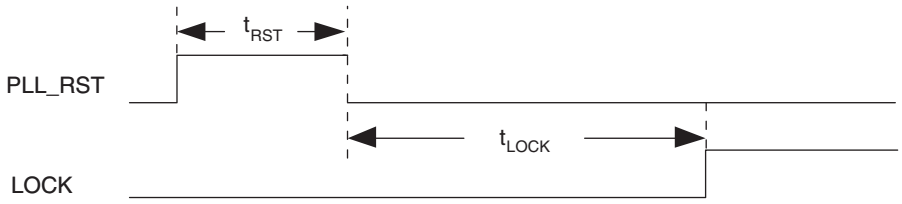
RST Input

The PLL reset occurs under two conditions. At power-up an internal power-up reset signal from the configuration block resets the PLL. The user controlled PLL reset signal RST is provided as part of the PLL module that can be driven by an internally generated reset function or a pin. This RST signal resets all internal PLL counters. When RST goes inactive, the PLL will start the lock-in process, and will take the t_{LOCK} time to complete the PLL lock.

Note: The use of RST is mandatory. RST must be asserted to start the PLL locking process or to re-start the locking process after losing lock.

Figure 10-3 shows the timing diagram of the RST input.

Figure 10-3. RST Input Timing Diagram



CLKFB Input

The feedback signal to the PLL, which is fed through the feedback divider, can be derived from the Primary Clock net (CLKOP), a dedicated dual-purpose pin, directly from the CLKOP divider (CLKINTFB) or from general routing. External feedback allows the designer to compensate for board-level clock alignment.

CLKOP Output

The sysCLOCK PLL main clock output, CLKOP, is a signal available for selection as a primary clock.

CLKOS Output with Phase and Duty Cycle Select

The sysCLOCK PLL auxiliary clock output, CLKOS, is a signal available for selection as a primary clock. The CLKOS is used when phase shift and/or duty cycle adjustment is desired. The programmable phase shift allows for different phase in increments of 45° to 315°. The duty select feature provides duty select in 1/8th of the clock period.

CLKOK Output with Lower Frequency

The CLKOK is used when a lower frequency is desired. It is a signal available for selection as a primary clock.

Dynamic Delay Control I/O Ports

Refer to Table 10-4 for detailed information.

LOCK Output

The LOCK output provides information about the status of the PLL. After the device is powered up and the input clock is valid, the PLL will achieve lock within the specified lock time. Once lock is achieved, the PLL lock signal will be asserted. If, during operation, the input clock or feedback signals to the PLL become invalid, the PLL will lose lock. However, when the input clock completely stops, the LOCK output will remain in its last state, since it is inter-

nally registered by this clock. It is recommended to assert PLL RST to re-synchronize the PLL to the reference clock. The LOCK signal is available to the FPGA routing to implement generation of RST. ModelSim® simulation models take two to four reference clock cycles from RST release to LOCK high.

PLL Attributes

The PLL utilizes several attributes that allow the configuration of the PLL through source constraints. This section details these attributes and their usage.

FIN
The input frequency can be any value within the specified frequency range based on the divider settings.

CLKI_DIV, CLKFB_DIV, CLKOP_DIV, CLKOK_DIV
These dividers determine the output frequencies of each output clock. The user is not allowed to input an invalid combination; determined by the input frequency, the dividers, and the PLL specifications.

FREQUENCY_PIN_CLKOP, FREQUENCY_PIN_CLKOK
These output clock frequencies determine the divider values.

FDEL
The FDEL attribute is used to pass the Delay Adjustment step associated with the Output Clock of the PLL. This allows the user to advance or retard the Output Clock by the step value passed multiplied by 250ps (nominal). The step ranges from -8 to +8 resulting the total delay range to +/- 2ns.

PHASEADJ
The PHASEADJ attribute is used to select Coarse Phase Shift for CLKOS output. The phase adjustment is programmable in 45° increments.

DUTY
The DUTY attribute is used to select the Duty Cycle for CLKOS output. The Duty Cycle is programmable at 1/8 of the period increment.

FB_MODE
There are three sources of feedback signals that can drive the CLKFB Divider: Internal, CLKOP (Clock Tree) and User Clock. CLKOP (Clock Tree) feedback is used by default. Internal feedback takes the CLKOP output at CLKOP Divider output before the Clock Tree to minimize the feedback path delay. The User Clock feedback is driven from the dedicated pin, clock pin or user specified internal logic.

DELAY_CNTL
This attribute is designed to select the Delay Adjustment mode. If the attribute is set to “DYNAMIC” the delay control switches between Dynamic and Static depending upon the input logic of DDAMODE pin. If the attribute is set to “STATIC”, Dynamic Delay inputs are ignored in this mode.

CLKOK Output with Lower Frequency
The CLKOK is used when a lower frequency is desired. It is a signal available for selection as a primary clock.

MachXO PLL Primitive Definitions

A PLL primitive is used for MachXO PLL implementation. The definitions of the PLL I/O ports are shown in Table 10-2. Figure 10-4 shows the MachXO PLL primitive library symbol. The EHXPLLC includes all features available in the PLL including Dynamic Delay Adjustment.

Figure 10-4. MACHXO PLL Primitive Symbols

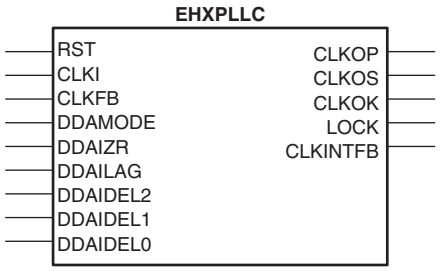


Table 10-2. MachXO PLL I/O Definitions

Signal	I/O	Description
CLKI	I	General routing or dedicated global clock input pad.
CLKFB	I	From general routing, clock tree, internal feedback from CLKOP or dedicated external feedback pad.
RST	I	"1" to reset PLL counters.
CLKOP	O	PLL output clock to clock tree (no phase shift).
CLKOS	O	PLL output clock to clock tree (phase shifted/duty cycle changed).
CLKOK	O	PLL output to clock tree (CLKOK divider, low speed, output).
LOCK	O	"1" indicates PLL LOCK to CLKI, asynchronous signal.
CLKINTFB	O	Internal feedback source. CLKOP divider output before CLOCK TREE.
DDAMODE	I	DDA Mode. "1" Pin control (dynamic), "0": Fuse Control (static).
DDAIZR	I	DDA Delay Zero. "1": delay = 0, "0": delay = on.
DDAILAG	I	DDA Lag/Lead. "1": Lead, "0": Lag.
DDAIDEL[2:0}	I	DDA delay.

PLL Attributes Definitions

The MachXO PLL utilizes several attributes that allow the configuration of the PLL through source constraints. This section details these attributes and their usage.

Table 10-3. MachXO PLL User Attributes

Attributes	MM GUI Access	Attribute Name	Preference Editor Support	Value	Default Value
CLKI Frequency (MHz)	Y	FIN	N	Note 6	100
CLKI Frequency (MHz)	Y	FREQUENCY_PIN_CLKI	N	Note 6	100
CLKOP Frequency (MHz)	Y	FREQUENCY_PIN_CLKOP	N	Note 6	100
CLKOK Frequency (MHz)	Y	FREQUENCY_PIN_CLKOK	N	Note 6	50
CLKOP Frequency Tolerance (%)	Y		N	0.0,0.1,0.2,0.5,1.0,2.0,5.0,10.0	0.0
CLKI Divider Setting	Y	CLKI_DIV[4]	N	1 to 16	1
CLKFB Divider Setting	Y	CLKFB_DIV	N	1 to 16	1
CLKOP Divider Setting	Y	CLKOP_DIV	N	Note 3	8 (Note 2)
CLKOK Divider Setting	Y	CLKOK_DIV	N	2,4,6,..,126,128	2
Fine Delay Adjust	N	FDEL[7]	Y	-8 to 8	0
Coarse Phase Shift Selection (O)	Y	PHASEADJ	N	0, 45, 90...315	0

Table 10-3. MachXO PLL User Attributes (Continued)

Attributes	MM GUI Access	Attribute Name	Preference Editor Support	Value	Default Value
Duty Cycle Selection (1/8 Increment)	Y	DUTY	N	1 to 7	4
Delay Control	Y	DELAY_CNTL[1]	N	DYNAMIC/STATIC	STATIC
Feedback Mode	Y	Note 5	N	INTERNAL/CLKOP/UserClock	CLKOP
CLKOS Select	Y		N		
CLKOK Select	Y		N		

1. DYNAMIC This mode switches delay control between Dynamic and Static depending upon the input logic of DDAMODE pin.
   STATIC This mode sets the delay control to Static Control.
2. CLKOP_DIV value is calculated to maximize the f_{VCO} within the specified range based on FIN, CLKOP_FREQ in conjunction with CLKI_DIV and CLKFB_DIV values.
3. The CLKOP Divider values are 2, 4, 6, 8,…30, 32 if CLKOS is unused and 2, 4, 8, 16, 32 if CLKOS is used.
4. All divider settings are user transparent in Frequency Mode. These are user attributes in Divider Mode.
5. CLKFB source:
   INTERNAL: CLKINTFB (internal feedback path is used).
   CLKOP: Primary Clock net feedback node of CLKOP.
   User Clock:
   - General routing (includes FPGA logic or general I/O)
   - Primary Clock net (includes user connecting CLKOP to CLKFB internally to the chip, or the use of a device clock pin)
   - Dedicated PLL feedback pin
6. Refer to the MachXO Family Data Sheet for current specifications.
7. This attribute is not available in the IPexpress GUI. After reviewing the trace report file, users can determine the amount of delay that will best fit the clocking in their design. Further information on FDEL settings is described in the following section.

FDEL Settings

There are four ways the user can enter the desired FDEL value.

1. Although the FDEL entry is not available in the IPexpress GUI, the module generated by IPexpress includes the attribute with default value “0”. Users can replace it with a desired value.

   Example of source code with default FDEL value:

   ```
   attribute FDEL of ehxpll_mod_0_0 : label is "0";
   generic map (…
      FDEL=>"0",
      …
      ")
   ```

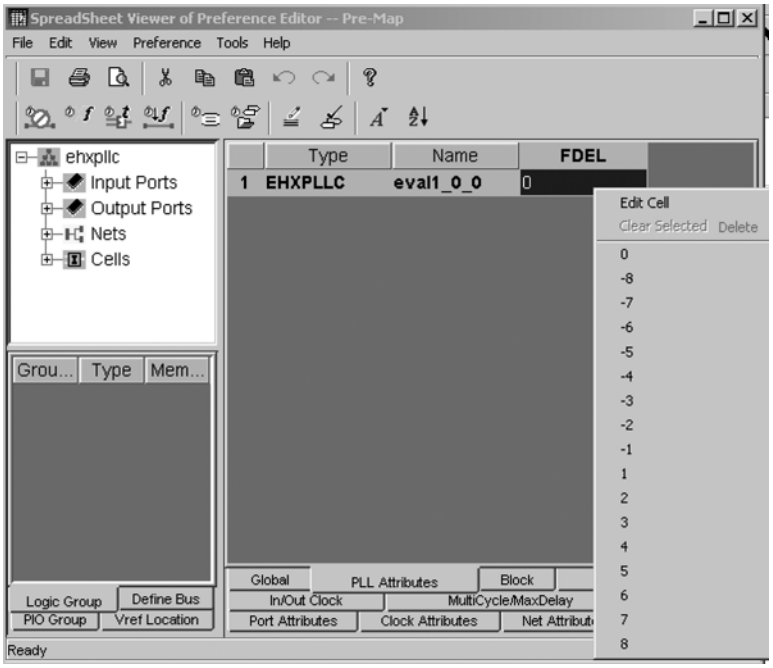
2. Preference File: User may specify the preference in the Preference file.

   Example:

   ```
   ASIC "FDEL_CODE_0_0" TYPE "EHXPLLB" FDEL="-2"  ;
   ```

3. Pre-Map Preference Editor: Users can enter the FDEL value in the Pre-Map Preference Editor as shown in Figure 10-5. Figure 10-5 shows the Pre-Map Preference Editor in the ispLEVER software. To see a similar screen shot for Lattice Diamond™ software, go to Appendix A, Figure 10-16.

Figure 10-5. Pre-Map Preference Editor



Dynamic Delay Adjustment

The Dynamic Delay Adjustment is controlled by the DDAMODE input. When the DDAMODE input is set to “1”, the delay control is done through the inputs, DDAIZR, DDAILAG and DDAIDEL(2:0). For this mode, the attribute “DELAY_CNTL” must be set to “DYNAMIC”. Table 10-4 shows the delay adjustment values based on the attribute/input settings.

In this mode, the PLL may come out of lock due to the abrupt change of phase. RST must be asserted to re-lock the PLL. Upon de-assertion of RST, the PLL will start the lock-in process and will take the t_{LOCK} time to complete the PLL lock.

Table 10-4. Delay Adjustment

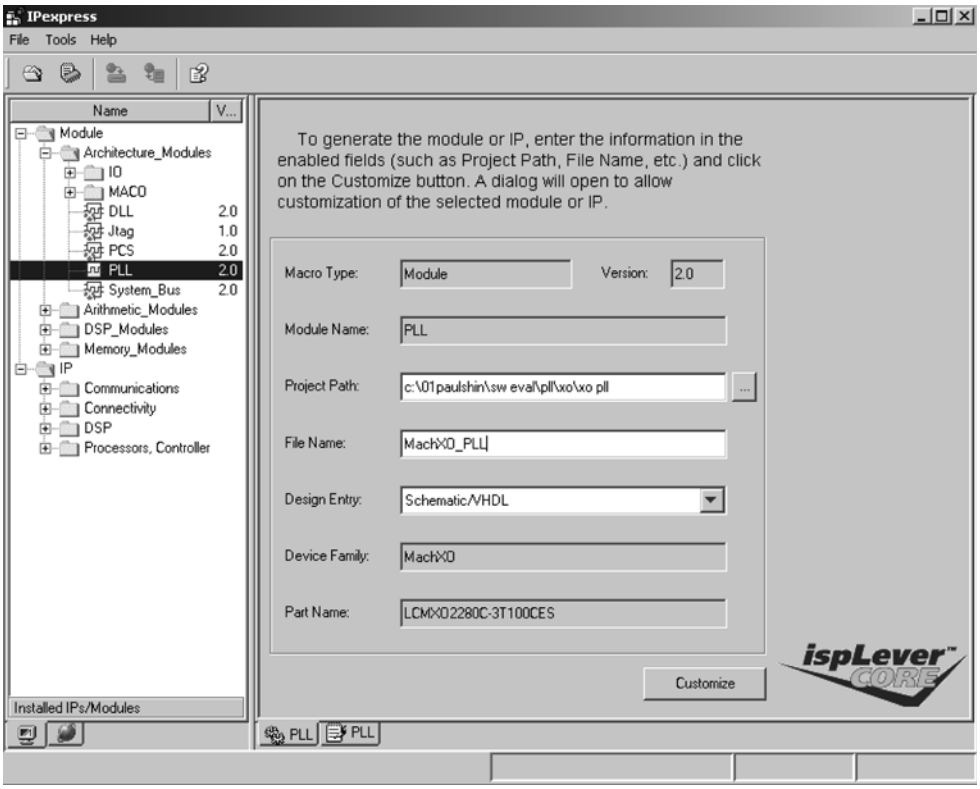
DDAMODE = 1: Dynamic Delay Adjustment			Delay 1 Tdly = 250 ps (Nominal)	DDAMODE = 0
DDAIZR	DDAILAG	DDAIDEL[2:0]		Equivalent FDEL Value
0	1	111	Lead 8 Tdly	-8
0	1	110	Lead 7 Tdly	-7
0	1	101	Lead 6 Tdly	-6
0	1	100	Lead 5 Tdly	-5
0	1	011	Lead 4 Tdly	-4
0	1	010	Lead 3 Tdly	-3
0	1	001	Lead 2 Tdly	-2
0	1	000	Lead 1 Tdly	-1
1	Don't Care	Don't Care	no delay	0
0	0	000	Lag 1 Tdly	1
0	0	001	Lag 2 Tdly	2
0	0	010	Lag 3 Tdly	3
0	0	011	Lag 4 Tdly	4
0	0	100	Lag 5 Tdly	5
0	0	101	Lag 6 Tdly	6
0	0	110	Lag 7 Tdly	7
0	0	111	Lag 8 Tdly	8

MachXO PLL Usage in IPexpress

The MachXO PLL is fully supported by IPexpress in ispLEVER and Diamond design software.

Figure 10-6 shows the main window when PLL is selected. To see screen shots of IPexpress in the Diamond software environment, see Appendix A, Figure 10-17. The only entry required in this window is the module name. Other entries are set to the project settings. The user may change these entries as desired. After entering a module name, click on Customize to open the Configuration Tab window, as shown in Figure 10-7.

Figure 10-6. IPexpress Main Window



Configuration Tab

The Configuration Tab lists all user accessible attributes with default values set. Upon completion of entries, click on Generate to generate source and constraint files. The user may choose to use the .lpc file to load parameters.

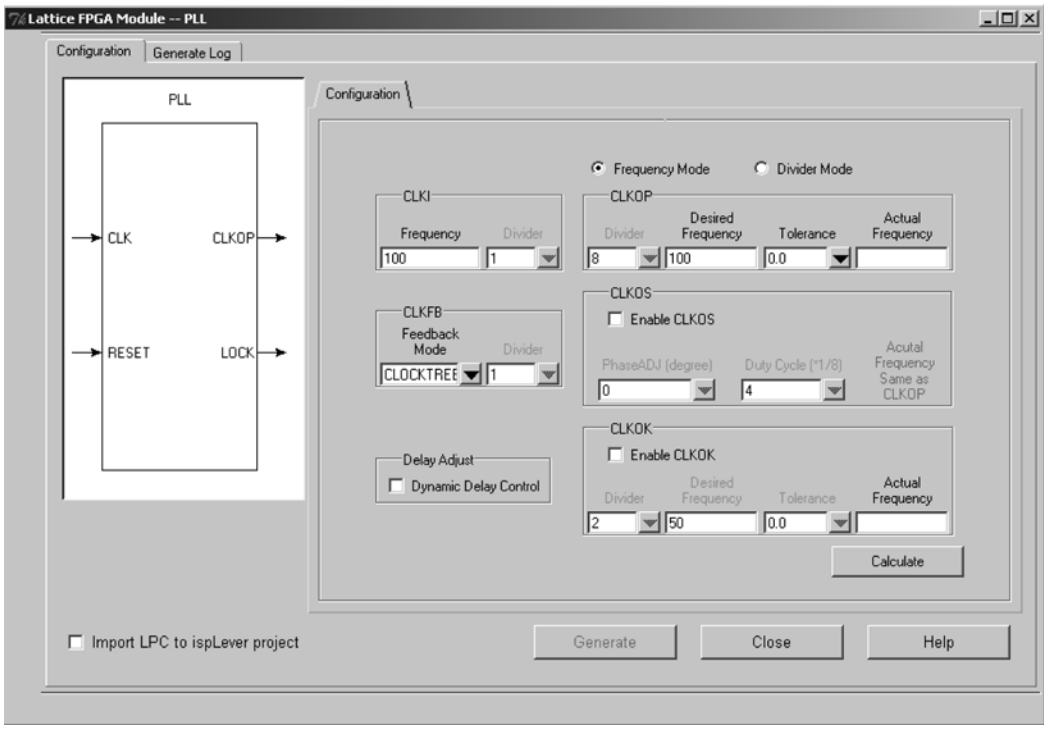
Mode

There are two modes for configuring the PLL in the Configuration Tab, Frequency Mode and Divider Mode.

Frequency Mode

In this mode, the user enters input and output clock frequencies and the software calculates the divider settings for user. If the output frequency the user entered is not achievable, the nearest frequency will be displayed in the Actual text box. After input and output frequencies are entered, clicking the Calculate button will display the divider values. Figure 10-7 shows the Frequency Mode configuration tab.

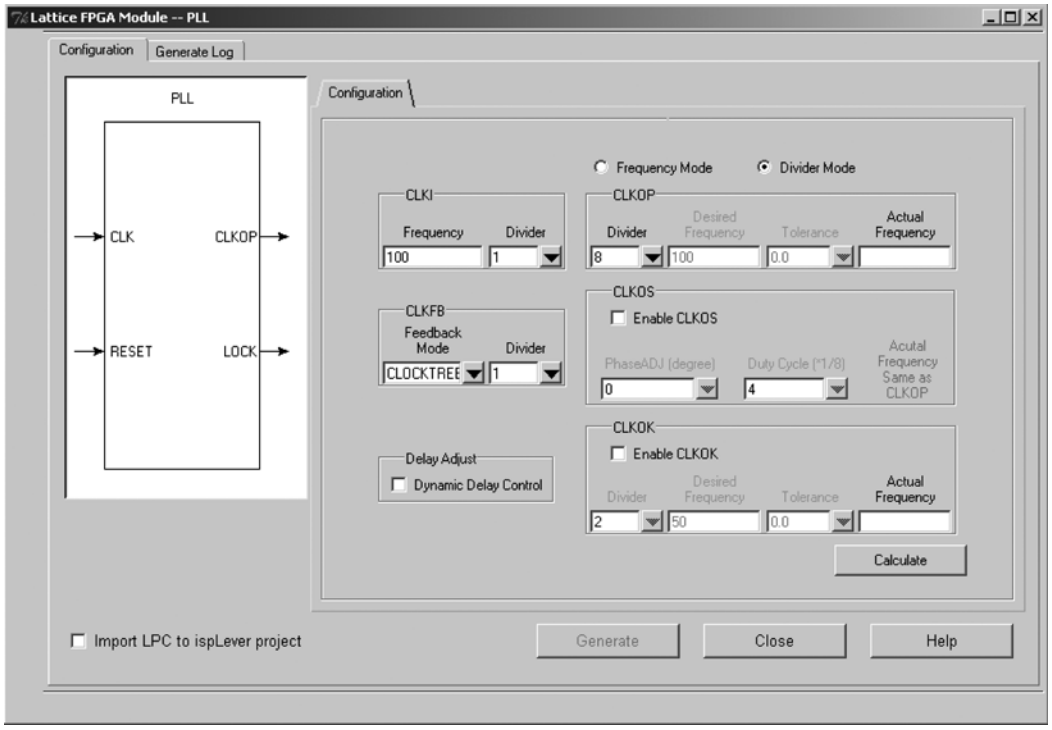
Figure 10-7. MachXO PLL Configuration Tab (Frequency Mode) Screen Capture (also see Diamond screen shot, Appendix A, Figure 10-18)



Divider Mode

In this mode, the user sets the divider settings with input frequency. The user must choose the CLKOP Divider value to maximize the f_{VCO} to achieve optimum PLL performance. After input frequency and divider settings are complete, clicking the Calculate button will display the frequencies. Figure 10-8 shows the Divider Mode Configuration tab.

Figure 10-8. MachXO PLL Configuration Tab (Divider Mode) - also see Diamond screen shot, Appendix A, Figure 10-19



Frequency Programming in Divider Mode for Advanced Users

Table 10-5. Frequency Limits

Parameter	Value
f_{IN}	Refer to the MachXO Family Data Sheet for frequency data.
f_{OUT}	Refer to the MachXO Family Data Sheet for frequency data.
f_{OUTK}	Refer to the MachXO Family Data Sheet for frequency data.
f_{VCO} (Hz)	Refer to the MachXO Family Data Sheet for frequency data.
CLKI Divider	1 to 16
CLKFB Divider	1 to 16
CLKOP Divider	2, 4, 8, 16, 32 (CLKOS used) 2, 4, 6, 8,... 28, 30, 32 (CLKOS not used)
CLKOK Divider	2, 4, 6, 8,..,126, 128
Maximum (N*V)	32
f_{PFD} (f_{IN}/M) (Hz)	Refer to the MachXO Family Data Sheet for frequency data.

Equations for generating Divider Settings and Output Frequency Ranges for Divider Mode Users
The divider names are abbreviated with legacy names as follows:

CLKI DIVIDER: M
CLKFB DIVIDER: N
CLKOP DIVIDER: V
CLKOK DIVIDER: K

f_{VCO} Constraint

From the loop:
$f_{OUT} = f_{IN} * (N/M)$ . . . . . (1)

From the loop:
$f_{VCO} = f_{OUT} * V$ . . . . . (2)

Substitute (1) in (2) yields:
$f_{VCO} = f_{IN} * (N/M) * V$ . . . . . (3)

Arrange (3):
$f_{IN} = (f_{VCO} /(V*N))*M$ . . . . . (4)

From equation (4):
$f_{INMIN} = ((f_{VCOMIN} /(V*N))*M$ . . . . . (5)
$f_{INMAX} = (f_{VCOMAX}/(V*N))*M$ . . . . . (6)

f_{PFD} Constraint

From the loop:
$f_{PFD} = f_{IN}/M$ . . . . . (7)
$f_{IN} = f_{PFD} *M$
$f_{INMIN} = f_{PFDMIN} *M = 25 * M$, (assume $f_{PFDMIN} = 25$) . . . . . (8)

So, equation (5) becomes:
$f_{INMIN} = ((f_{VCOMIN} /(V*N))*M$, if below 25 * M round up to 25 * M . . . . . (9)

From the loop:

$f_{INMAX} = f_{PFDMAX} *M = 420 * M$ . . . . . (10)
Assume f_{INMAX} =420

So, equation (6) becomes:
$f_{INMAX} = (f_{VCOMAX}/(V*N))*M$, if above 420 round down to 420 . . . . . (11)

From equation (1):
$f_{OUTMIN} = f_{INMIN}*(N/M)$, if below 25 * N round up to 25 * N . . . . . (12)
$f_{OUTMAX} = f_{INMAX}*(N/M)$, if above 420 round down to 420 . . . . . (13)

$f_{OUTKMIN} = f_{OUTMIN}/K$
$f_{OUTKMAX} = f_{OUTMAX}/K$

Example: When CLKOS is Not Used

Assume: f_{IN} = 40 MHz, M = 2, N = 3, V = 4

Then:
$f_{OUT} = 40 * 3/2 = 60$ . . . . . within range
$f_{VCO} = 60 * 4 = 240$ . . . . . out of range

f_{PFD} = 40 / 2 = 20 or 60 / 3 = 20 . . . . . .out of range

Assume M =1

Then:

f_{OUT} = 40*3/1 = 120. . . . . .within range
f_{VCO} = 120 * 4 = 480 . . . . . within range but not an optimum value
f_{PFD} = 40 /1 or 120 /3 = 40 . . . . . .within range

In this case, V = 6 will satisfy all conditions.

f_{VCO} = 120*6 = 720 < 840

Oscillator (OSCC)

There is a dedicated oscillator in the MachXO device whose output is made available for user.

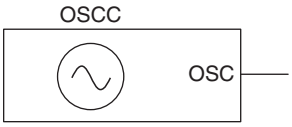
The oscillator frequency range is 18 to 26 MHz. The output of the oscillator can also be routed as an input clock to the clock tree. The oscillator frequency output can be further divided by internal logic (user logic) for lower frequencies, if desired. The oscillator is powered down when not in use.

Primitive Name: OSCC

Table 10-6. OSCC Port Definition

I/O	Name	Description
Output	OSC	Oscillator Clock Output

Figure 10-9. Oscillator Primitive Symbol (OSCC)



Oscillator Usage with VHDL - Example

```
COMPONENT OSCC
        PORT (OSC:OUT   std_logic);
END COMPONENT;

begin

OSCInst0: OSCC
        PORT MAP (
         OSC    =>  osc_int
         );
```

Clock/Control Distribution Network

The MachXO family provides global clocks: four primary clocks and four secondary clocks. These global signals are generated from four 16:1 muxes as shown in Figure 10-10 and Figure 10-11. The available clock sources for the MachXO256 and MachXO640 devices are four dual function clock pins and 12 internal routing signals. The available clock sources for the MachXO2280 devices are four dual function clock pins, six internal routing signals and six PLL outputs.

Dual function I/Os are provided for clocking usage. These I/Os are used as user programmable I/O pins when not in use as PLL or clock pins.

PCLK PIO (Primary Clock Pads)
There are two PCLK PIOs on top and two PIOs on bottom, for a total of four pins for each MachXO device. These pads connect directly to the global clock network.

PLL PIO
There are two pad pairs (one pad pair on the upper side and one pair on the lower side) for the MachXO2280 and one pad pair for the MachXO1200.

PLLFB PIO
Two pad pairs (one pad pair on the upper side and one pair on the lower side) for the MachXO2280 and one pad pair for the MachXO1200.

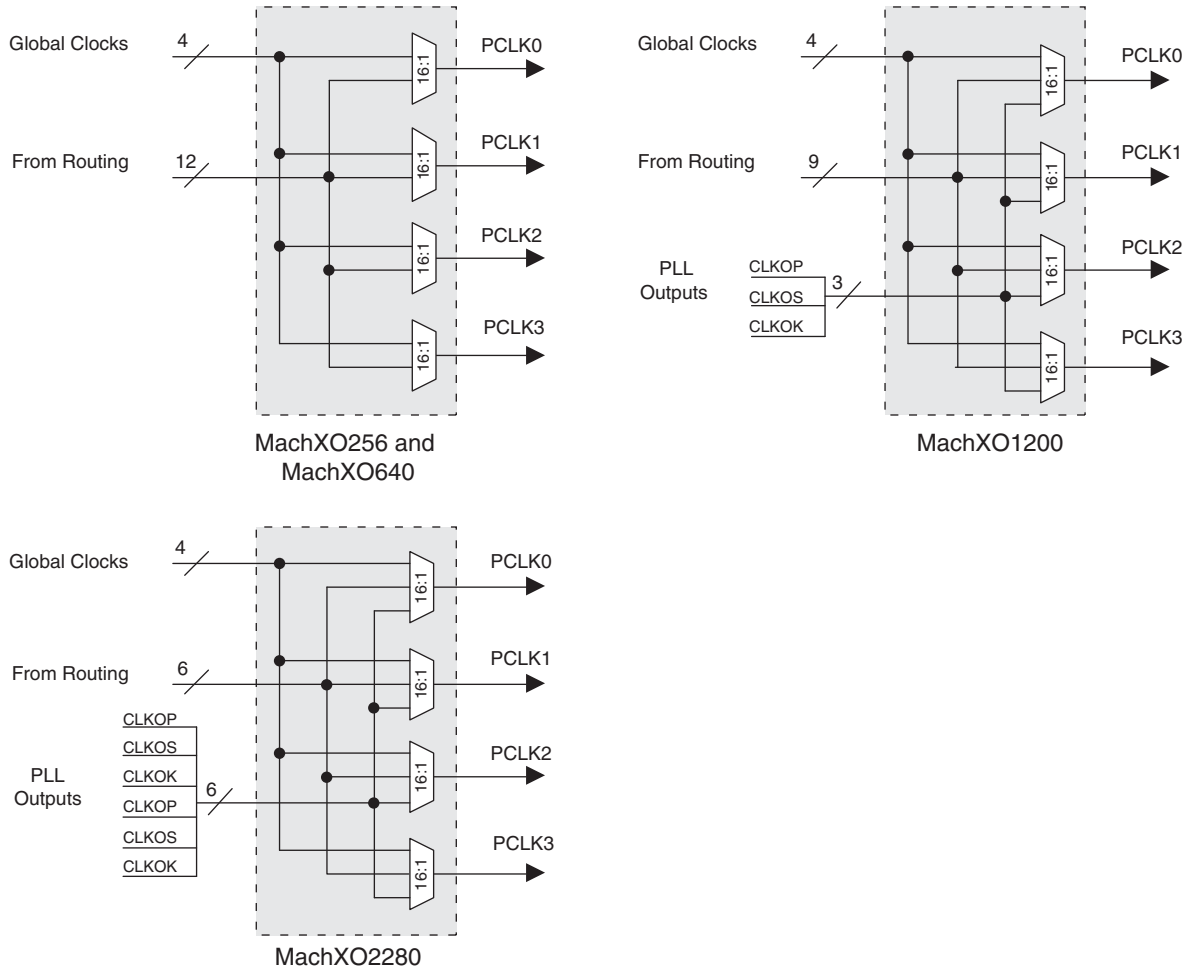
Primary Clock Mux Connectivity

The Primary Clock Mux input sources include:

- Primary clock input pins.
- PLL outputs
- From routing

The Primary Clock Mux outputs feed four clock input switch boxes in a PFU.

Figure 10-10. Primary Clock Net



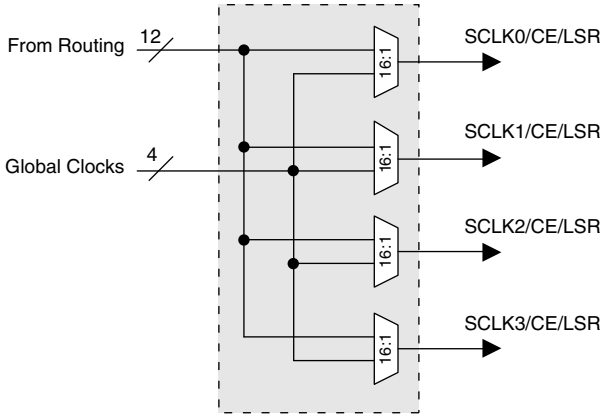
Secondary Clock/CE/LSR Mux Connectivity

The Secondary Clock/CE/LSR Mux input sources include:

- Primary Clock input pins
- From routing

The Secondary Clock/CE/LSR Mux outputs feed four clock input switch boxes and eight control input switch boxes in each PFU. Each slice includes one clock input switch box and two control input switch boxes, one for CE (Clock Enable) and the other for LSR (Local Set/Reset).

Figure 10-11. Secondary Clock/Control Net (All MachXO)



Primary Clock and Secondary Clock/CE/LSR Distribution Network

The Clock Input Switch Box and Control Input Switch Box are described in Figure 10-12 and Figure 10-13. Figure 10-14 shows the entire connectivity of the MachXO clock distribution network for each PFU.

Figure 10-12. Clock Switch Mux to Each PFU Slice

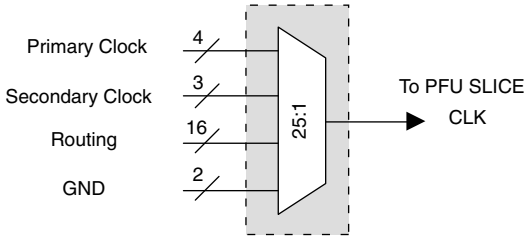


Figure 10-13. Control Switch Mux to Each PFU Slice

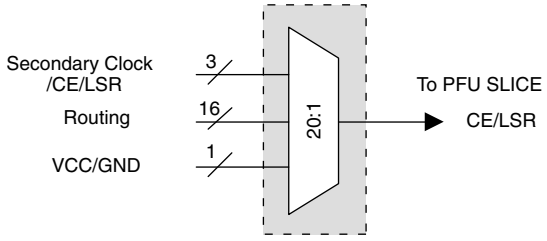
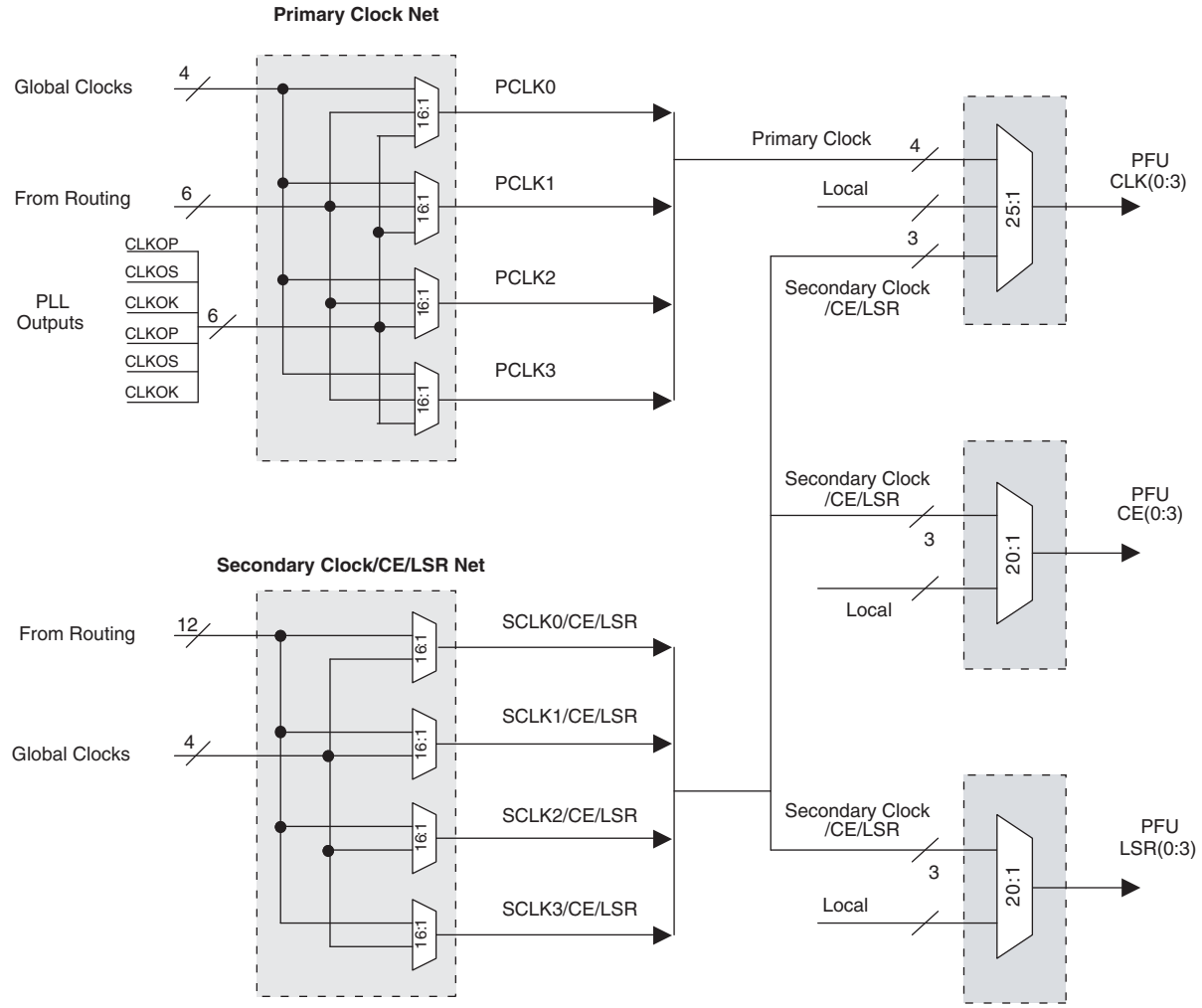


Figure 10-14. Primary Clock and Secondary Clock/CE/LSR Distribution



Maximum Number of Secondary Clocks Available

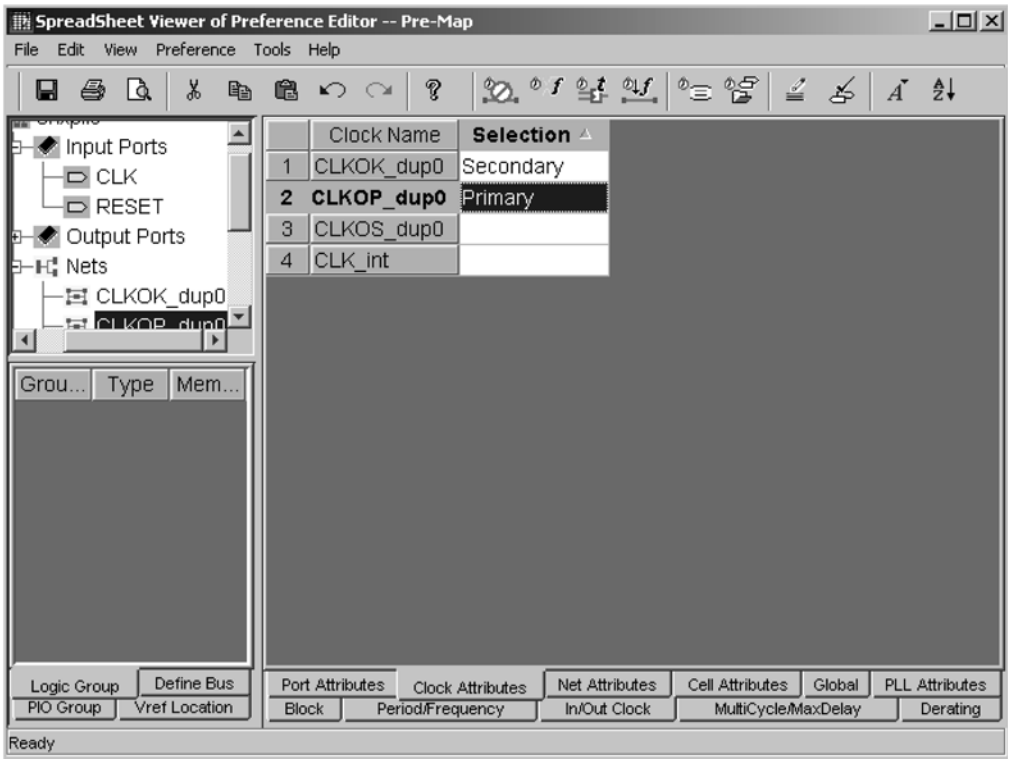
As illustrated in Figure Figure 10-14, there are four secondary clock nets in the clock distribution network but only three of them are reaching the clock input mux at PFU. This limits the number of total secondary clocks available to three.

Post Map Preference Editor Usage

Fine delay adjustment can be entered in the Post-Map Preference Editor after “Place and Run” to determine the required timing for the system design.

The Clock Preference assignments are also entered in the Post-Map Preference Editor. Figure 10-15 shows an example screen shot. To see a similar screen shot for Diamond design software, go to Appendix A, Figure 10-20.

Figure 10-15. Post-Map Preference Editor Example



Technical Support Assistance

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Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
July 2005	01.0	Initial release.
October 2005	01.1	OSC frequency range changed.
		Total number of secondary clocks available is 3.
		ispLEVER GUI screen shot updated for version 5.1.
		References to MM/IP Manager replaced with IPexpress
		CLKOS/CLKOK select attributes added.
September 2006	01.2	Minor corrections.
February 2010	01.3	Reconciled LOCK description among MachXO, LatticeXP2, LatticeECP2/M and LatticeECP3.
October 2010	01.4	Updated for Lattice Diamond software support.
September 2011	01.5	Removed text section: “PCB Layout Recommendations for VCCPLL and GNDPLL if Separate Pins are Available”.

Appendix A. Lattice Diamond Design Software Screen Shots

Figure 10-16. Pre-Map Preference Editor in Diamond

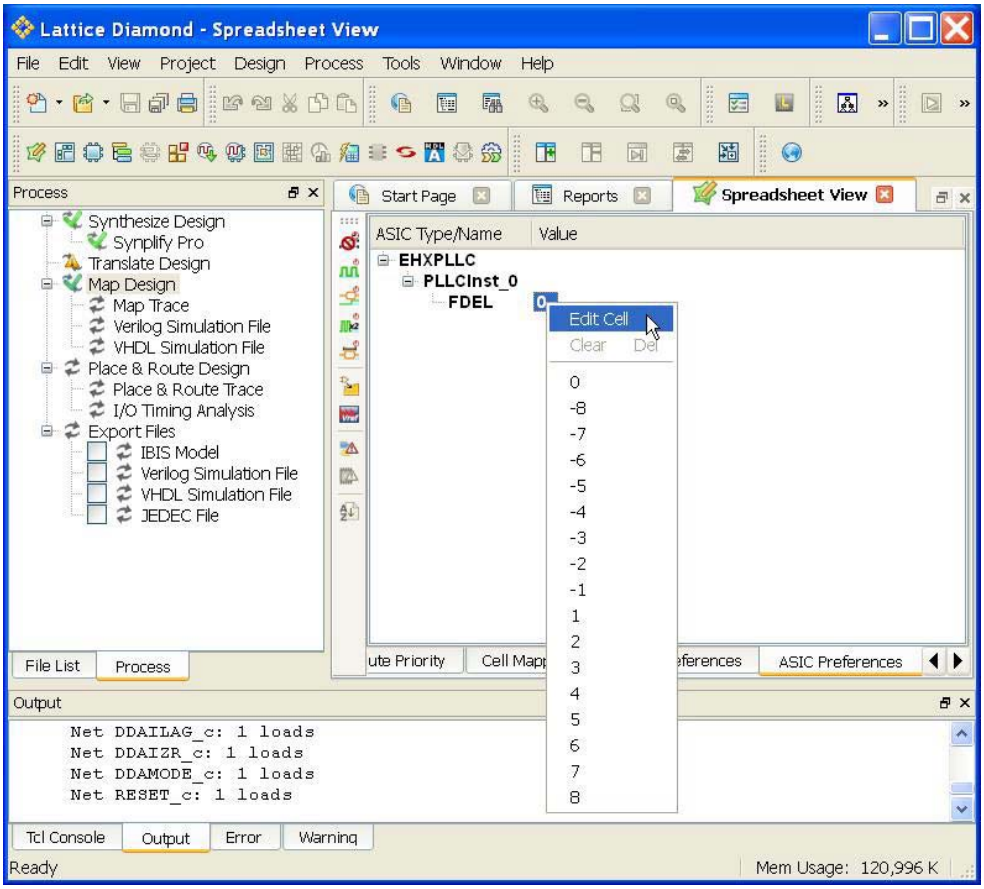

Figure 10-17. IPexpress Main Window in Diamond

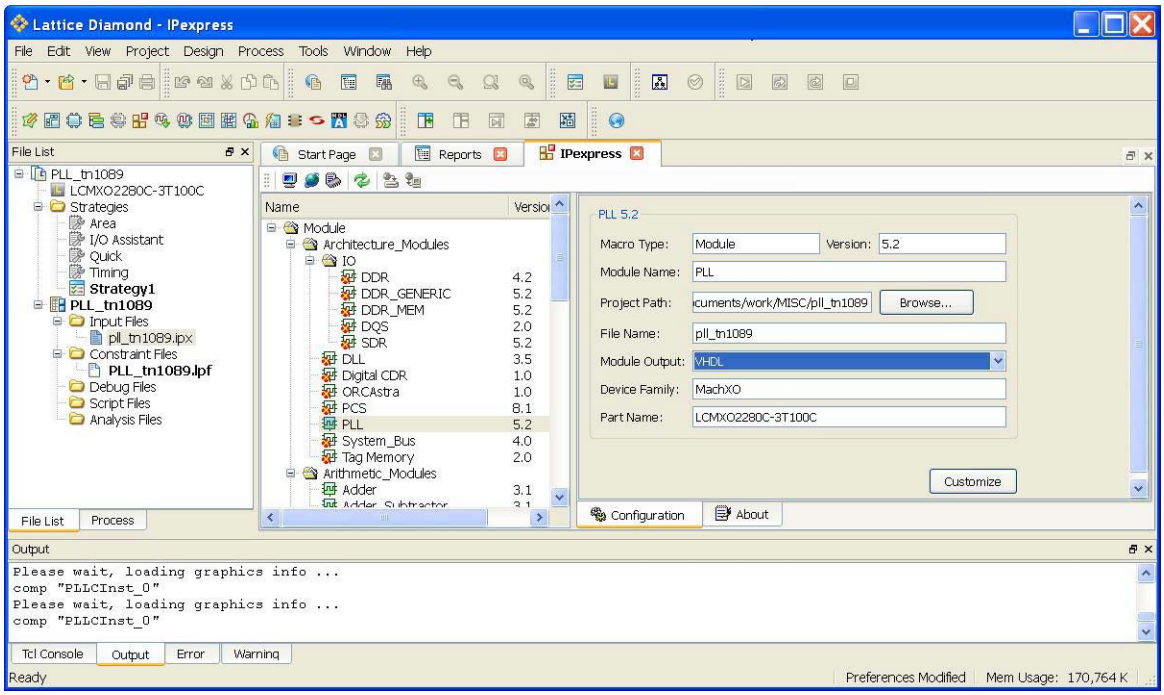

Figure 10-18. MachXO PLL Configuration Tab (Frequency Mode) in Diamond

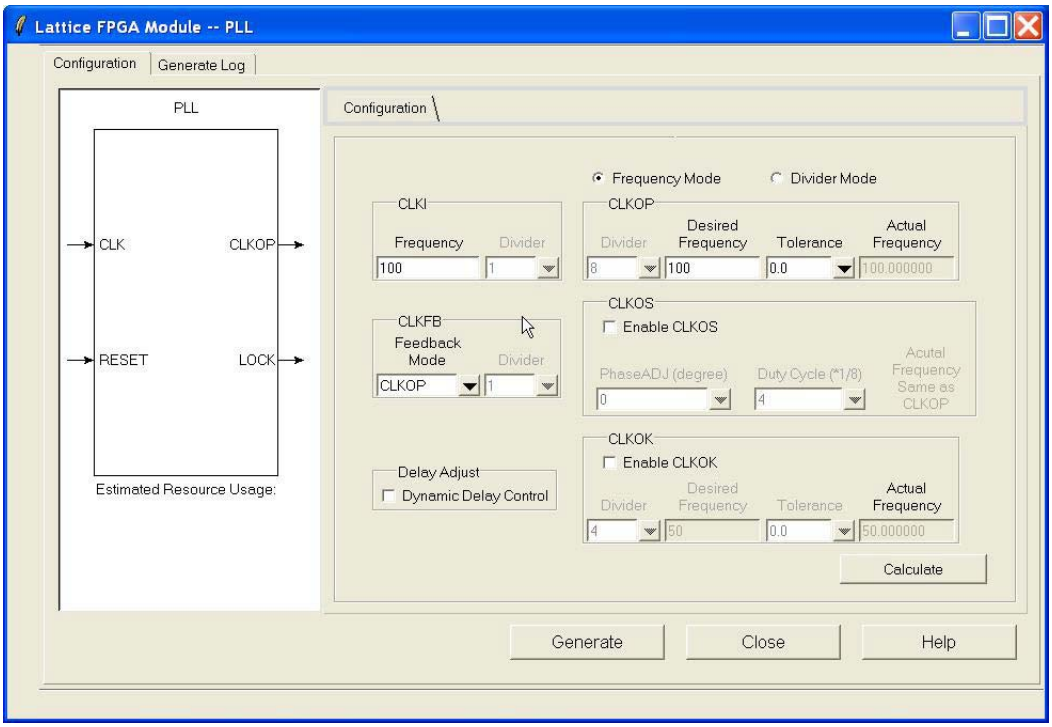

Figure 10-19. MachXO PLL Configuration Tab (Divider Mode) in Diamond

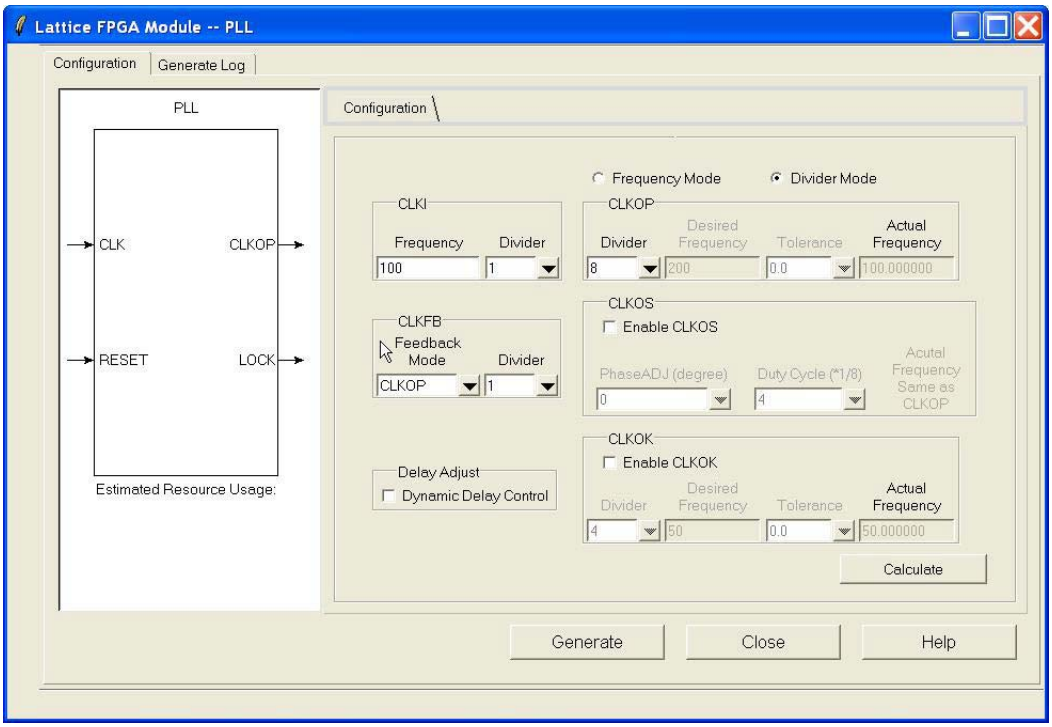

Figure 10-20. Post-Map Preference Editor Example in Diamond