LatticeXP sysCONFIG Usage Guide

September 2008 **Technical Note TN1082**

Introduction

The memory in the LatticeXP™ FPGAs is built using Flash cells, along with SRAM cells, so that configuration memory can be loaded automatically at power-up, or at any time the user wishes to update the device. In addition to "instant-on" capability, on-chip Flash memory greatly increases design security by getting rid of the external configuration bitstream; while maintaining the ease of use and reprogrammability of an SRAM-based FPGA.

While an external device is not required, the LatticeXP does support several external configuration modes. The available external configuration modes are:

- Slave Serial
- Master Serial
- Slave Parallel
- ispJTAG™ (1149.1 interface)

This guide will cover all the configuration options available for the LatticeXP.

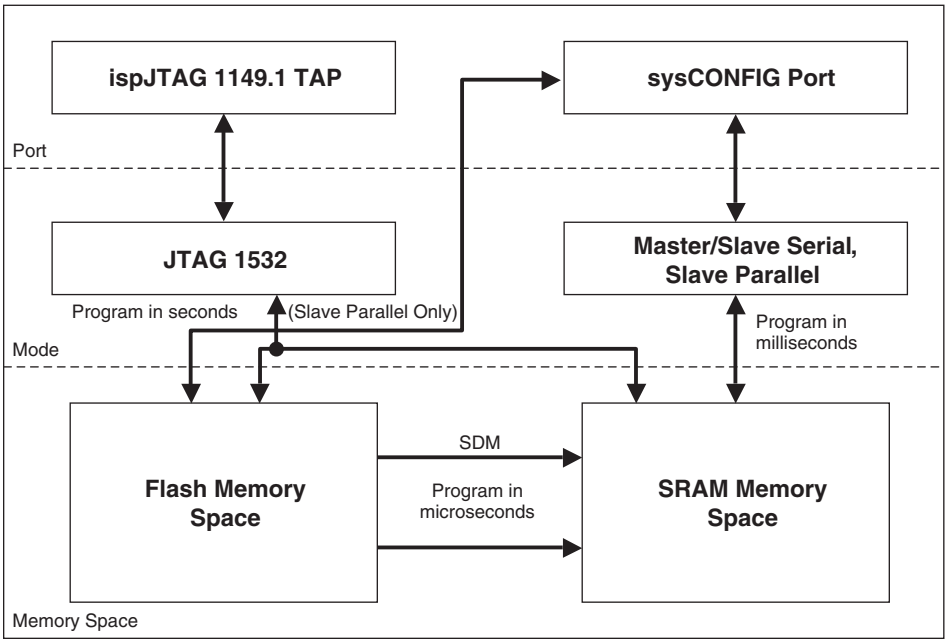
Programming Overview

The LatticeXP contains two types of memory, SRAM and Flash (refer to Figure 13-1). SRAM contains the FPGA configuration, essentially the "fuses" that define the circuit connections; Flash provides an internal storage space for the configuration data.

The SRAM can be configured using JTAG, one of the external configuration modes, or by using the data stored in on-chip Flash. The configuration process consists of SRAM initialization (clear the RAM and the address pointers), loading the SRAM with the configuration data, and setting the FPGA into user mode (waking up the FPGA).

On-chip Flash can be programmed by using JTAG or by using the external Slave Parallel port. JTAG Flash programming can be performed any time the device is powered up. The Slave Parallel port uses the sysCONFIG™ pins and can program the Flash directly or in the background. Direct programming takes place during config mode, background programming during user mode. The FPGA enters config mode at power up, when the PROGRAMN pin is pulled low, or when a refresh command is issued via JTAG; it enters user mode when it wakes up, i.e. when the device begins running user code. These two programming modes, direct and background, will be referred to in this document as Flash Direct and Flash Background.

Figure 13-1. Programming Block Diagram



Configuration Pins

The LatticeXP supports two types of sysCONFIG pins, dedicated and dual-purpose. The dual-purpose pins are available as extra I/O pins if they are not used for configuration.

Two configuration mode pins, along with a programmable option, control the dual-purpose configuration pins. The configuration mode pins (CFG) are generally hard wired on the PCB and determine which configuration mode will be used; the programmable option is accessed via preferences in Lattice ispLEVER® design software, or as HDL source file attributes, and allows the user to protect the configuration pins from accidental use by the user or the place-and-route software. The LatticeXP devices also support ispJTAG for configuration, including transparent readback, and for JTAG testing. The following sections describe the functionality of the sysCONFIG and JTAG pins. Note that JTAG and ispJTAG will be used interchangeably in this document. Table 13-1 is provided for reference.

Table 13-1. Configuration Pins for the LatticeXP Device

Pin Name	I/O Type	Pin Type	Mode Used
CFG[1:0]	Input, weak pull-up	Dedicated	All
PROGRAMN	Input, weak pull-up	Dedicated	All
INITN	Bi-Directional Open Drain, weak pull-up	Dedicated	All
DONE	Bi-Directional Open Drain with weak pull-up or Active Drive	Dedicated	All
CCLK	Input or Output	Dedicated	All
DIN	Input, weak pull-up	Dual-Purpose	Serial
DOUT/CSON	Output	Dual-Purpose	Serial or Parallel
CSN	Input, weak pull-up	Dual-Purpose	Parallel
CS1N	Input, weak pull-up	Dual-Purpose	Parallel
WRITEN	Input, weak pull-up	Dual-Purpose	Parallel
BUSY	Output, tri-state, weak pull-up	Dual-Purpose	Parallel
D[0:7]	Input or Output	Dual-Purpose	Parallel
TDI	Input, weak pull-up	JTAG	

Table 13-1. Configuration Pins for the LatticeXP Device (Continued)

Pin Name	I/O Type	Pin Type	Mode Used
TDO	Output	JTAG	
TCK	Input with Hysteresis	JTAG	
TMS	Input, weak pull-up	JTAG	

Note: Weak pull-ups consist of a current source of 30uA to 150uA. The pull-ups for CFG and PROGRAMN track V_{CC} (core); the pull-ups for TDI and TMS track V_{CCJ}; all other pull-ups track the V_{CCIO} for that pin.

Dedicated Pins

Following is a description of the dedicated sysCONFIG pins for the LatticeXP device. These pins are used to control or monitor the configuration process. These pins are used for non-JTAG programming sequences only. The JTAG pins will be explained later in the ispJTAG Pins section of this document.

CFG[1:0]

The Configuration Mode pins, CFG[1:0], are dedicated inputs with weak pull-ups. The CFG pins are used to select the configuration mode for the LatticeXP, i.e. what type of device the LatticeXP will configure from. At Power-On-Reset (POR), or when the PROGRAMN pin is driven low, and depending on the configuration mode selected, different groups of dual-purpose pins will be used for device configuration.

Table 13-2. LatticeXP Configuration Modes

Configuration Mode	CFG[1]	CFG[0]
Slave Serial	0	0
Master Serial	0	1
Slave Parallel	1	0
Self Download Mode (SDM)	1	1

When both CFG pins are high the device will configure itself by reading the data stored in on-chip Flash; this is referred to as SDM, or Self Download Mode. See the Self-Download section of this document for more information regarding SDM.

PROGRAMN

The PROGRAMN pin is a dedicated input with a weak pull-up. This pin is used to initiate a non-JTAG SRAM configuration sequence. A high to low signal applied to PROGRAMN sets the device into configuration mode. The PROGRAMN pin can be used to trigger configuration at any time. If the device is using JTAG then PROGRAMN will be ignored until the device is released from JTAG mode.

PROGRAMN should not be low externally during power-up. It should be driven high or rising with the power supply via an external pullup resistor. Once all power supplies have reached minimum levels, PROGRAMN may be used to initiate the configuration process.

If the CFG pins are not both high (not in SDM) then the configuration sequence will proceed using the selected configuration port. If both CFG pins are high (SDM), and the Flash has been programmed, then the configuration sequence will proceed using the data in on-chip Flash.

If both CFG pins are high (SDM), and the Flash has not been programmed, the configuration sequence will pause and wait for the Flash done bit to be programmed. Once the Flash has been programmed, and PROGRAMN is brought high, the configuration sequence will continue.

INITN

The INITN pin is a dedicated bi-directional open drain pin with a weak pull-up. INITN is capable of driving a low pulse out as well as detecting a low pulse driven in.

During SRAM configuration from an external device INITN going low indicates that the SRAM is being initialized; INITN going high indicates that the FPGA is ready to accept configuration data. To delay configuration the INITN pin can be held low externally. The device will not enter configuration mode as long as the INITN pin is held low. After configuration has started INITN is used to indicate a bitstream error. The INITN pin will be driven low if the calculated CRC and the configuration data CRC do not match; DONE will then remain low and the LatticeXP will not wake up.

During SRAM configuration from on-chip Flash INITN is not used or monitored and is driven low.

When programming on-chip Flash the INITN pin is only used to indicate an error during erase or program. If an error occurs INITN will be driven low. During Flash Direct programming an error will prevent the FPGA from configuring from the Flash, during Flash Background programming an error will not affect the configuration already running in SRAM.

DONE

The DONE pin is a dedicated bi-directional open drain with a weak pull-up (default), or an actively driven pin. DONE will be driven low when the device is in configuration mode and the internal DONE bit is not programmed. When the INITN and PROGRAMN pins go high (or in the case of SDM just PROGRAMN goes high), and the internal DONE bit is programmed, the DONE pin will be released (or driven high, if it is an actively driven pin). The DONE pin can be held low externally and, depending on the wake-up sequence selected, the device will not become functional until the DONE pin is externally brought high.

Reading the DONE bit is a good way for an external device to tell if the FPGA is configured.

When using JTAG to configure SRAM the DONE pin is driven by the boundary scan cell, so the state of the DONE pin has no meaning during JTAG configuration.

CCLK

CCLK is a dedicated bi-directional pin; direction depends on whether a Master or Slave mode is selected. If a Master mode is selected via the CFG pins, the CCLK pin will become an output pin; otherwise CCLK is an input pin.

If the CCLK pin becomes an output, the internal programmable oscillator is connected to the CCLK and is driven out to slave devices. CCLK will stop 120 clock cycles after the DONE pin is brought high and the device wake-up sequence completed. The extra clock cycles ensure that enough clocks are provided to wake-up other devices in the chain. When stopped, CCLK becomes an input (tri-stated output). CCLK will restart (become an output) on the next configuration initialization sequence.

The MCCLK_FREQ parameter (see ispLEVER software documentation) controls the CCLK master frequency (see Table 13-3). Until changed during configuration CCLK will be 2.5 MHz. One of the first things loaded during configuration is the MCCLK_FREQ parameter; once this parameter is loaded the frequency changes to the selected value using a glitchless switch. Care should be exercised not to exceed the frequency specification of the slave devices or the signal integrity capabilities of the PCB layout.

Table 13-3. Master Clock Frequency Selections

CCLK (MHz)	CCLK (MHz)	CCLK (MHz)
2.5	13	45
4.3	15	51
5.4	20	55
6.9	26	60
8.1	30	130
9.2	34	-
10.0	41	-

Note: Default is the lowest frequency, 2.5 MHz.

Table 13-4. Maximum Configuration Bits

Density	Bitstream Size (Mb)
LFXP3	1
LFXP6	1.6
LFXP10	2.8
LFXP15	4
LFXP20	4.9

Table 13-5. SDM Pin Usage

Configuration Mode	SDM (Self Download Mode)			
CFG[1:0]	[1, 1]			
Flash Programming Mode	Direct	Background	Direct	Background
Port	sysCONFIG		ispJTAG[1]	
Pins	CCLK, CSN, CS1N, WRITEN, D[0:7]		TAP	
User I/O States	Tristate	User	BSCAN	User
PROGRAMN	↓	Keep at High	Keep At High[2]	
BUSY	Status	Status	Not Used	
INITN	Pass/Fail	Pass/Fail	Not Used[3]	
DONE	Done	Not Used	Keep at High[4]	
PERSISTENT Bit	Don't Care	ON	Don't Care	

1. ispJTAG can be used to program the Flash regardless of the state of the CFG pins, however only if the device is in SDM can Flash be used to configure SRAM
2. The state of the PROGRAMN pin is ignored by the device during JTAG Flash programming but the pin should be held high as a low will inhibit Flash to SRAM data transfer.
3. The state of the INITN pin is ignored by the device during JTAG Flash programming but the pin should be allowed to float high using the internal pull-up.
4. The state of the DONE pin is ignored by the device during JTAG Flash programming but the pin should be allowed to float high using the internal pull-up as a low can keep the device from waking up.

Table 13-6. Pins Used for Memory Access

CFG Pins			On-Chip Flash	SRAM	
1	0	CFG Mode	Write or Read[2]	Write From	Readback[2, 3]
X[1]	X[1]	JTAG	TAP	TAP	TAP
1	1	SDM	sysCONFIG	On-Chip Flash	sysCONFIG
1	0	Slave Parallel	N/A[4]	sysCONFIG	sysCONFIG
0	1	Master Serial	N/A[4]	sysCONFIG	N/A[5]
0	0	Slave Serial	N/A[4]	sysCONFIG	N/A[5]

1. The ispJTAG port is always available independent of the CFG setting.
2. Readback can only be disabled by programming the security bit.
3. Set the PERSISTENT bit to ON to retain the sysCONFIG port for background readback.
4. Flash access is not allowed in this mode.
5. SRAM readback is not allowed in this mode.

Programming Sequence

There are three types of programming, SRAM, Flash Direct, and Flash Background. This section goes through the process for each showing how the dedicated pins are used.

SRAM: When not using SDM (Self Download Mode, on-chip Flash) to program SRAM the sequence begins when the internal power-on reset (POR) is released or the PROGRAMN pin is driven low (see Figure 13-2). The LatticeXP then drives INITN low, tri-states the I/Os, and initializes the internal SRAM and control logic. When this is

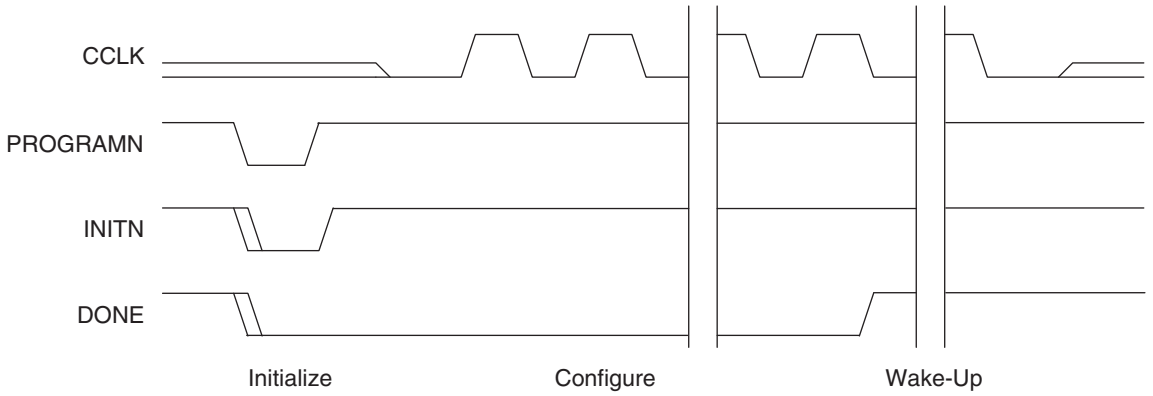
complete, if PROGRAMN is high, INITN will be released. If INITN is held low externally the LatticeXP will wait until it goes high. When INITN goes high the LatticeXP begins looking for the configuration data preamble on the selected configuration port, as determined by the CFG pins.

Once configuration is complete the internal DONE bit is set, the DONE pin goes high, and the FPGA wakes up (enters user mode). If a CRC error is detected when reading the bitstream INITN will go low, the internal DONE bit will not be set, the DONE pin will stay low, and the LatticeXP will not wake up.

When using SDM to program SRAM the sequence is similar but INITN is not used or monitored (INITN is driven low). The sequence begins when the internal power-on reset (POR) is released or the PROGRAMN pin is driven low (see Figure 13-2). The LatticeXP then tri-states the I/Os and initializes the internal SRAM and control logic. When initialization is complete the LatticeXP begins loading configuration data from on-chip Flash.

As with non-SDM, once configuration is complete the internal DONE bit is set, the DONE pin goes high, and the FPGA wakes up (enters user mode).

Figure 13-2. SRAM Configuration Timing Diagram



Flash Direct: Flash Direct programming is possible using the Slave Parallel port if both CFG pins are high (SDM). Serial ports may not be used to program the Flash. Flash Direct is only valid if the DONE pin is low (the SRAM is blank).

The sequence begins when the PROGRAMN pin is driven low. The LatticeXP tri-states the I/Os, and initializes the internal SRAM and control logic. The LatticeXP waits for WRITEN and both CSN and CS1N pins to go low and then looks for the programming preamble followed by the erase, program, and verify commands. Data is written and read on the D[0:7] pins.

Once the Flash is programmed the PROGRAMN pin can be brought high to start the transfer from Flash to SRAM.

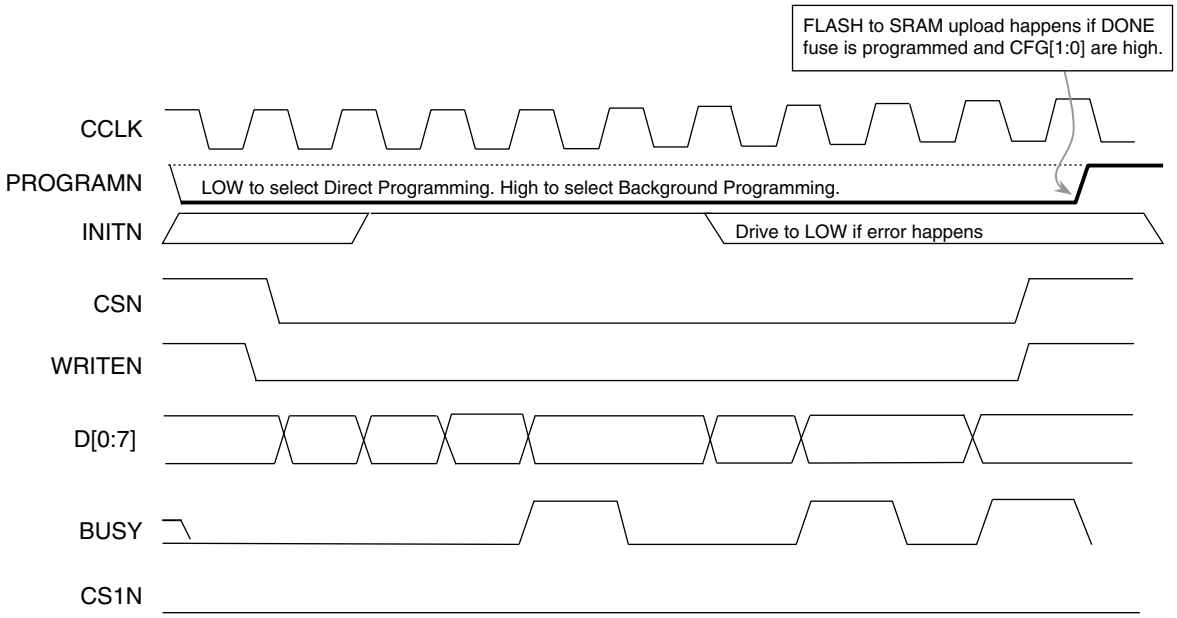
Flash Background: Flash Background programming is possible using the Slave Parallel port if both CFG pins are high (SDM). Serial ports may not be used to program the Flash. Flash Background will not disturb the FPGA's present configuration.

Flash Background programming may be used in both config mode and user mode (Done bit = 0 or 1). To support Flash Background programming in user mode the PERSISTENT bit must be set to ON.

When WRITEN goes low, and CSN and CS1N are low, the FPGA will wait for the preamble and then look for the proper commands. A low on INITN indicates an error during a Flash erase or program. Data is written and read on the D[0:7] pins.

After programming the Flash the user may toggle the PROGRAMN pin to transfer the Flash data to SRAM.

Figure 13-3. Flash Programming Timing Diagram



Dual-Purpose sysCONFIG Pins

The following is a list of the dual-purpose sysCONFIG pins. These pins are available as general purpose I/O (GPIO) after configuration. If a dual-purpose pin is to be used both for configuration and as a GPIO, the user must adhere to the following:

- The I/O type must remain the same. For example, if the pin is a 3.3V CMOS pin (LVCMOS33) during configuration it must remain a 3.3V CMOS pin as GPIO.
- The user must select the correct CONFIG_MODE setting and set the PERSISTENT bit to OFF in order to use the dual-purpose sysCONFIG pins as GPIO after configuration. These settings can be found in the ispLEVER Design Planner (formerly called the Preference Editor).
- The user is responsible for insuring that no internal or external logic will interfere with device configuration.

Also, if slave parallel configuration mode is not being used then one or both of the parallel port chip selects (CSN, CS1N) must be high or tri-stated during configuration.

After configuration, these pins, if not used as GPIO, are tri-stated and weakly pulled up.

DIN
DIN (data input) is a dual-purpose input with a weak pull-up. DIN is used for the serial bitstream configurations.

DOUT/CSON
The DOUT/CSON is a dual-purpose output that is used in Chain Mode (daisy chaining). This pin can be used in serial or parallel modes and has two uses.

For serial and parallel configuration modes, when BYPASS Chain Mode is selected, this pin will become DOUT. In a serial configuration mode, when the device becomes fully configured, a BYPASS instruction will be executed and the data on DIN will be presented on the DOUT pin through a bypass register. In this way the serial data is passed to the next device. In parallel configuration mode the data will be serialized and then presented on DOUT; D[0] (MSb) will be shifted out first followed by D[1], D[2] and so on to D[7] (LSb).

For parallel configuration mode, when FLOW_THROUGH Chain Mode is selected, this pin will become Chip Select Out (CSON). In FLOW_THROUGH Chain Mode, when the device is fully configured (the internal DONE bit goes

high), the Flow-Through instruction will be executed and the CSON pin will be driven low to enable the next device's chip select pin.

The DOUT/CSON bypass register will drive out a high upon power up and continue to do so until the execution of the Bypass or Flow-Through instruction within the bitstream.

Chain Mode is not supported when configuring from internal Flash (SDM).

CSN and CS1N
Both CSN and CS1N are active low input pins with weak pull-ups and are used in parallel mode only. These inputs are OR'ed and used to enable the D[0:7] data pins to receive or output a byte of data.

In non-SDM, when CSN or CS1N are high, the D[0:7], INITN, and BUSY pins are tri-stated. CSN and CS1N are interchangeable when controlling the D[0:7], INITN, and BUSY pins.

When SDM is selected and CSN or CS1N are high, the D[0:7], INITN, and BUSY pins are tri-stated. If the Flash has not been programmed a high on both CSN and CS1N will cause the LatticeXP to drive the INITN pin low to reset the internal FPGA configuration circuitry. The LatticeXP will then monitor D[0:7] waiting for the configuration preamble. CSN and CS1N are interchangeable when controlling the D[0:7], INITN, and BUSY pins.

During configuration or programming through the parallel sysCONFIG interface, CSN and SCIN should remain low during the entire process. Deassertion of either of these signals will interrupt the process, requiring a new cycle to properly transfer the data.

If SRAM or Flash will need to be accessed while the device is in user mode (the DONE pin is high) then the PERSISTENT preference must be set to ON in order to preserve these pins as CSN and CS1N.

WRITEN
The WRITEN pin is an active low input with a weak pull-up and used for parallel mode only. The WRITEN pin is used to determine the direction of the data pins D[0:7]. The WRITEN pin must be driven low when a byte of data is to be clocked into the device and driven high when data is to be read from the device.

If SRAM or Flash will need to be accessed while the part is in user mode (the DONE pin is high) then the PERSISTENT preference must be set to ON in order to preserve this pin as WRITEN.

BUSY
In parallel mode the BUSY pin is a tri-stated output with a weak pull-up. The BUSY pin will be driven low by the LatticeXP device only when it is ready to receive a byte of data from the D[0:7] pins or a byte of data is ready for reading. The BUSY pin can be used to support asynchronous peripheral mode (handshaking). This pin is used to indicate that the LatticeXP needs extra time to execute a command.

If SRAM or Flash will need to be accessed while the part is in user mode (the DONE pin is high) then the PERSISTENT preference must be set to ON in order to preserve this pin as BUSY.

D[0:7]
The D[0:7] pins support slave parallel mode only. The D[0:7] pins are tri-statable bi-directional I/O pins used for data write and read. When the WRITEN signal is low, and the CSN and CS1N pins are low, the D[0:7] pins become data inputs. When the WRITEN signal is driven high, and the CSN and CS1N pins are low, the D[0:7] pins become data outputs. If either CSN or CS1N is high D[0:7] will be tri-state. D[0] is the most significant bit and D[7] is the least significant bit.

If SRAM or Flash will need to be accessed while the part is in user mode (the DONE pin is high) then the PERSISTENT preference must be set to ON in order to preserve these pins as D[0:7].

Care must be exercised during read back of EBR or PFU memory. It is up to the user to ensure that reading these RAMs will not cause data corruption, i.e. these RAMs may not be read while being accessed by user code.

ispJTAG Pins

The ispJTAG pins are standard IEEE 1149.1 TAP (Test Access Port) pins. The ispJTAG pins are dedicated pins and are always accessible when the LatticeXP device is powered up. When programming the SRAM via ispJTAG the dedicated programming pins, such as DONE, cannot be used to determine programming progress. This is because the state of the boundary scan cell will drive the pin, per JTAG 1149.1, rather than normal internal logic.

TDO
The Test Data Output pin is used to shift out serial test instructions and data. When TDO is not being driven by the internal circuitry, the pin will be in a high impedance state.

TDI
The Test Data Input pin is used to shift in serial test instructions and data. An internal pull-up resistor on the TDI pin is provided. The internal resistor is pulled up to $V_{CCJ.}$

TMS
The Test Mode Select pin controls test operations on the TAP controller. On the falling edge of TCK, depending on the state of TMS, a transition will be made in the TAP controller state machine. An internal pull-up resistor on the TMS pin is provided. The internal resistor is pulled up to $V_{CCJ.}$

TCK
The test clock pin, TCK, provides the clock to run the TAP controller, which loads and unloads the data and instruction registers. TCK can be stopped in either the high or low state and can be clocked at frequencies up to the frequency indicated in the device data sheet. The TCK pin supports the value is shown in the DC parameter table of the data sheet. The TCK pin does not have a pull-up. A pull-down on the PCB of 4.7 K is recommended to avoid inadvertent clocking of the TAP controller as V_{CC} ramps up.

Optional TRST
Test Reset, TRST, in not supported on the LatticeXP device.

VCCJ
JTAG V_{CC} (V_{CCJ}) supplies independent power to the JTAG port to allow chaining with other JTAG devices at a common voltage. V_{CCJ} must be connected even if JTAG is not used. This voltage may also power the JTAG download cable. Valid voltage levels are 3.3V, 2.5V, 1.8V, 1.5V, and 1.2V.

Please see *In-System Programming Design Guidelines for ispJTAG Devices,* available on the Lattice web site at www.latticesemi.com, for further JTAG chain information.

Configuration and JTAG Voltage Levels

All of the control pins and programming pins default to LVCMOS. CFG and PROGRAMN are linked to V_{CC} (core); TCK, TDI, TDO, and TMS track V_{CCJ}; all other pins track the V_{CCIO} for that pin.

Configuration Modes and Options

The LatticeXP device supports several configuration modes, utilizing serial or parallel data inputs, as well as self-configuration. On power up, or upon driving the PROGRAMN pin low, the CFG[1:0] pins are sampled to determine the mode that will be used to configure the LatticeXP device. The CFG pins are generally hard wired on the PCB and determine which port the device will use to retrieve its configuration data. CONFIG_MODE is a programmable option accessed via preferences in Lattice ispLEVER design software, or as HDL source file attributes, and allow the user to protect the configuration pins from accidental use by the user or the place-and-route software.

Table 13-7 shows the mode, CFG[1:0], and the software CONFIG_MODE parameter. The following sections breakdown each configuration mode.

Table 13-7. Configuration Modes for the LatticeXP

Configuration Mode	CFG[1]	CFG[0]	CONFIG_MODE[1]	Chain Mode[2]
Slave Serial (no overload option)	0	0	Slave_Serial	Disable
Slave Serial (Bypass ON)	0	0	Slave_Serial	Bypass
Master Serial (no overload option)	0	1	Master_Serial	Disable
Master Serial (Bypass ON)	0	1	Master_Serial	Bypass
Slave Parallel (no overload option)	1	0	Slave_Parallel	Disable
Slave Parallel (Bypass ON)	1	0	Slave_Parallel	Bypass
Slave Parallel (Flow Through ON)	1	0	Slave_Parallel	Flowthrough
Self Download Mode (SDM)	1	1	None/Slave_Parallel[4]	Disable
ispJTAG (1149.1 interface)	X[3]	X[3]	None[5]	

1. CONFIG_MODE can be found in the ispLEVER Preference Editor.
2. CHAIN_MODE can be found in the ispLEVER bitgen options (right-click on Generate Bitstream Data and click on Properties).
3. The ispJTAG interface is always on.
4. If ispJTAG is used exclusively to access the on-chip Flash and SRAM select None, if Slave Parallel is used to access the Flash and/or the SRAM select Slave_Parallel.
5. The None selection indicates that no dual-purpose pins are reserved for configuration. This is the default.

Configuration Options

Several configuration options are available for each CONFIG_MODE.

- When daisy chaining multiple FPGA devices a configuration overflow option is provided. Configuration data overflow occurs once the first FPGA has completed its download, the remaining data in the configuration storage device is then output through the first FPGA to subsequent FPGAs. Configuration data overflow is not supported when using SDM.
- When using a master clock, the master clock frequency can be set.
- A security bit is provided to prevent SRAM or Flash readback.

By setting the proper parameters in the Lattice ispLEVER design software the selected configuration options are set in the generated bitstream. As the bitstream is loaded into the device the selected configuration options take effect. These options are described in the following sections.

Bypass Overflow Option

The Bypass overflow option can be used in serial and parallel device daisy chains. When the first device has completed configuration data download, and the Bypass option preference is selected, data coming into the device configuration port on the sysCONFIG pins will overflow serially out of DOUT and into the DIN pin of the next slave serial device. The Bypass option is selected in ispLEVER by right-clicking on Generate Bitstream Data and clicking on Properties.

In serial configuration mode, once all of the configuration data has been loaded into the first device, the Bypass option connects the DIN pin to DOUT pin via a bypass register. The bypass register is initialized with a ‘1’ at the beginning of configuration.

In parallel configuration mode, once all of the configuration data has been loaded into the first device, the Bypass option causes the data coming from D[0:7] to be serially shifted to DOUT. The serialized data is shifted to DOUT through the bypass register. D[0] of the byte wide data will be shifted out first followed by D[1], D[2] and so on.

Once the Bypass option starts, the device will remain in Bypass until the wake up sequence completes.

Flow-Though Overflow Option

The Flow-Through overflow option is used in parallel mode only. The Flow-Through option causes the CSON pin to go low when the FPGA has received all of its configuration data, driving the chip select on the next device in the daisy chain so that it will start reading configuration data from D[0:7]. The Flow Through Option will also tri-state the

D[0:7], INITN, and BUSY pins, once all of the configuration data has been received, in order to prevent interference with other devices in the daisy chain.

Once the Flow-Through option starts, the device will remain in Flow-Through until the wake up sequence completes.

Master Clock
If the CFG pins indicate that this is a Master device the CCLK pin will become an output with the frequency set by the user. The default Master Clock Frequency is 2.5 MHz.

The user can determine the Master Clock frequency by setting the MCCLK_FREQ preference in the Lattice ispLEVER design software. One of the first things loaded during configuration is the MCCLK_FREQ parameter; once this parameter is loaded the frequency changes to the selected value using a glitchless switch. Care should be exercised not to exceed the frequency specification of the slave devices or the signal integrity capabilities of the PCB layout. See Table 13-3 for available options.

Security Bit
Setting the security bit prevents readback of the SRAM and Flash from JTAG or the sysCONFIG pins. When the security bit is set the only operations available are erase and write. The security bit is updated as the last operation of SRAM configuration or Flash programming. By using on-chip Flash, and setting the security bit, the user can create a very secure device.

The security bit is accessed via the Preference Editor in ispLEVER design software.

More information on device security can be found in the document *FPGA Design Security Issues: Using the ispXPGA Family of FPGAs to Achieve High Design Security,* available on the Lattice Semiconductor web site at www.latticesemi.com.

Slave Serial Mode

Configuration Mode	CFG[1]	CFG[0]	CONFIG_MODE	Chain Mode
Slave Serial (no overload option)	0	0	Slave_Serial	Disable
Slave Serial (Bypass ON)	0	0	Slave_Serial	Bypass

The CCLK pin becomes an input and data at DI is clocked on the rising edge of CCLK. After the device is fully configured, if the Bypass option has been set, data sent to DI will be presented to the next device via the DOUT pin as shown in Figure 13-4.

Master Serial Mode

Configuration Mode	CFG[1]	CFG[0]	CONFIG_MODE	Chain Mode
Master Serial (no overload option)	0	1	Master_Serial	Disable
Master Serial (Bypass ON)	0	1	Master_Serial	Bypass

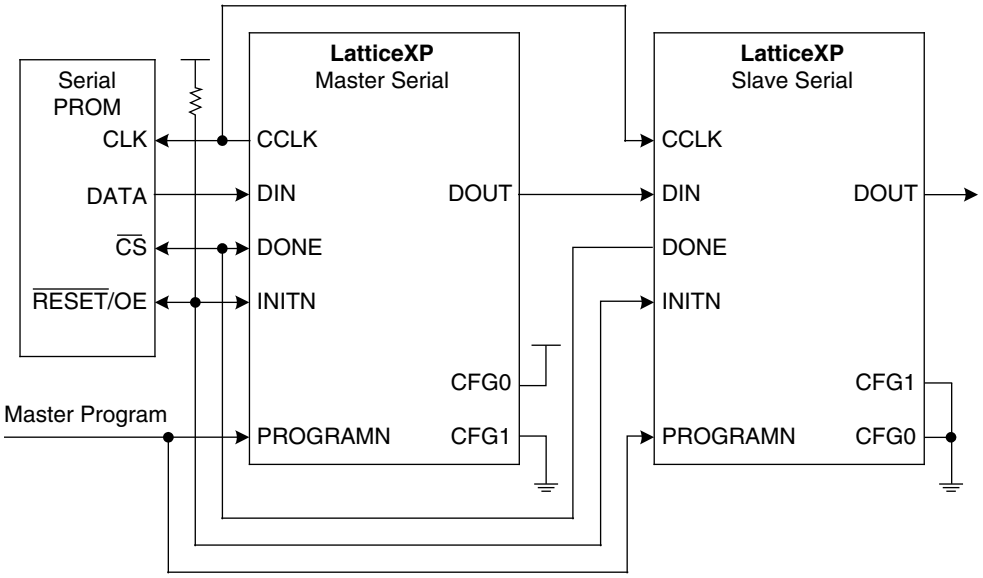
In Master Serial mode the device will drive CCLK out to the Slave Serial devices in the chain and the serial PROM that will provide the bitstream. The Master device accepts the data at DIN on the rising edge of CCLK. The Master Serial device starts driving CCLK at the beginning of the configuration and continues to drive CCLK until the external DONE pin is driven high and an additional 100 to 500 clock cycles have been generated. The CCLK frequency on power up defaults to 2.5 MHz. The master clock frequency default remains unless a new clock frequency is loaded from the bitstream.

If a Master Serial device is daisy chained with Slave Serial devices the Bypass option should be used so that overflow configuration data is directed to the DOUT pin.

Figure 13-4 shows a serial daisy chain. The daisy chain allows multiple Lattice FPGA devices to be configured using one configuration storage device. The center device operates in Master Serial with the Bypass option set

while the other Lattice FPGA devices in the daisy chain operate in Slave Serial mode. The RESET/OE pin of the PROM is driven by INITN while the Chip Select pin is driven by the DONE pin of the devices.

Figure 13-4. Master and Slave Serial Daisy Chain



Slave Parallel Mode

Configuration Mode	CFG[1]	CFG[0]	CONFIG_MODE	Chain Mode
Slave Parallel (no overload option)	1	0	Slave_Parallel	Disable
Slave Parallel (Bypass ON)	1	0	Slave_Parallel	Bypass
Slave Parallel (Flow Through ON)	1	0	Slave_Parallel	Flowthrough

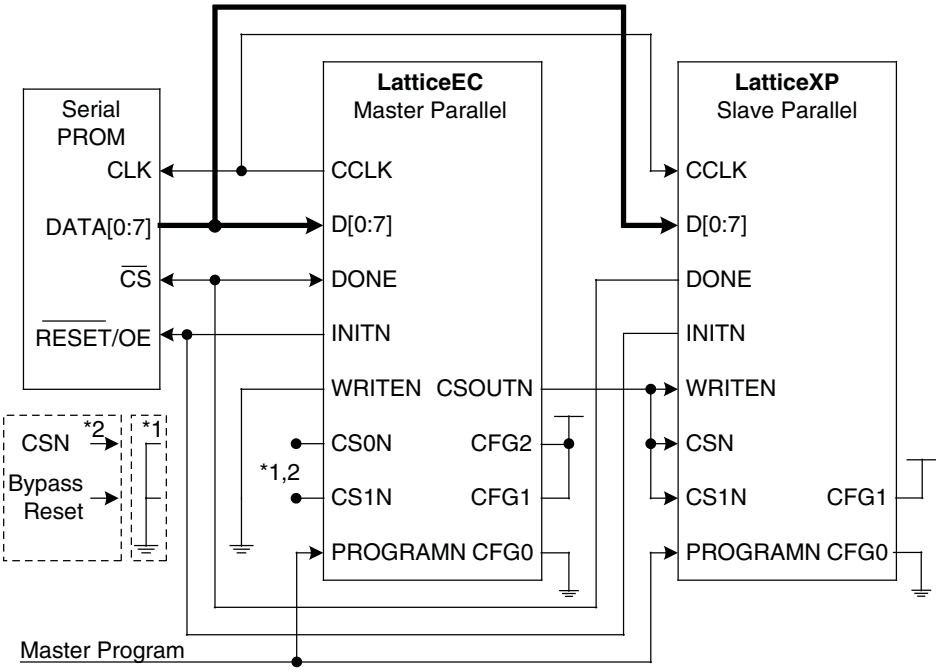
In Slave Parallel mode a host system sends the configuration data in a byte-wide stream to the device. The CCLK, CSN, CS1N, and WRITEN pins are driven by the host system. The Slave Parallel configuration mode allows multiple devices to be chained in parallel, as shown in Figure 13-5.

WRITEN, CSN, and CS1N must be held low to write to the device; data is input from D[0:7]. Slave Parallel mode can also be used for readback of the internal configuration. By driving the WRITEN pin low, and CSN and CS1N low, the device will input the readback instructions on the D[0:7] pins; WRITEN is then driven high and data read on D[0:7]. In order to support readback the PERSISTENT bit in ispLEVER's Preference Editor must be set to ON.

The Slave Parallel mode can support two types of overflow, Bypass and Flow-Through. If the Bypass option is set, after the first device has received all of its configuration data, the data presented to the D[0:7] pins will be serialized and bypassed to the DOUT pin. If the Flow-Through option is set, after the first device has received all of its configuration data, the CSON signal will drive the following parallel mode device's chip select low as shown in Figure 13-5.

To support asynchronous configuration, where the host may provide data faster than the FPGA can accept it, Slave Parallel mode can use the BUSY signal. By driving the BUSY signal high the Slave Parallel device tells the host to pause sending data. See Figure 13-6.

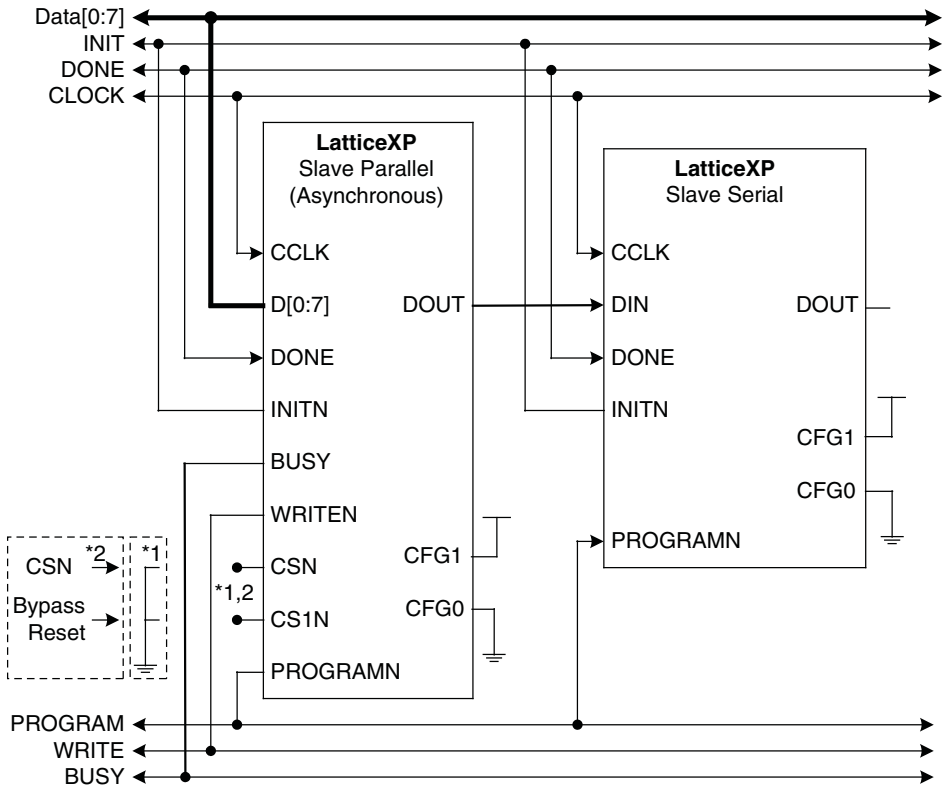
Figure 13-5. Master and Slave Parallel Daisy Chain



*1 Both CS pins can be held or driven low

*2 An option that allows the Bypass and Flow-Through option to be reset

Figure 13-6. Asynchronous Usage of Slave Parallel Configuration Mode



*1 Both CS pins can be held or driven low

*2 An option that allows the Bypass and Flow-Through option to be reset

Figure 13-6 shows an asynchronous peripheral write sequence using the Bypass option. To send configuration data to a device, the WRITEN signal has to be asserted. During the write cycle, the BUSY signal provides handshaking between the host system and the LatticeXP device. When BUSY is low the device is ready to read a byte of data at the next rising edge of CCLK. The BUSY signal is set high when the device reads the data and the device requires extra clock cycles to process the data.

Self Download Mode

Configuration Mode	CFG[1]	CFG[0]	CONFIG_MODE	Chain Mode
Self Download Mode (SDM)	1	1	None/Slave_Parallel	Disable

Self Download Mode (SDM) allows the FPGA to configure itself without using any external devices, and because the bitstream is not exposed this is also a very secure configuration mode. The user may access on-chip Flash using ispJTAG or the slave parallel port on the sysCONFIG pins.

JTAG may access the on-chip Flash any time the device is powered up, without disturbing device operation. JTAG may also read and write the configuration SRAM. If access to the on-chip Flash and SRAM is limited to JTAG then CONFIG_MODE should be set to None, freeing the dual-purpose pins for use as general purpose I/O.

The slave parallel port can also be used to access on-chip Flash. If the slave parallel port is used then CONFIG_MODE should be set to Slave_Parallel. WRITEN, CSN, and CS1N must be held low to write to on-chip Flash; data is input from D[0:7]. The slave parallel port can also be used for readback of both Flash and SRAM. By driving the WRITEN pin low, and CSN and CS1N low, the device will input the readback instructions on the D[0:7] pins; a bit in the read command will determine if the read is directed to Flash or SRAM. In order to support readback while the device is in user mode (the DONE pin is high) the PERSISTENT bit in ispLEVER's Preference Editor must be set to ON.

SDM does not support overflow.

ispJTAG Mode

Configuration Mode	CFG[1]	CFG[0]	CONFIG_MODE	Chain Mode
ispJTAG (1149.1 interface)	X	X	None	

The LatticeXP device can be configured through the ispJTAG port. The ispJTAG port is always on and available, regardless of the configuration mode selected. A CONFIG_MODE of None can be selected in the Lattice ispLEVER design software to tell the place and route tools that the JTAG port will be used exclusively, i.e. the serial and parallel ports will not be used. Setting the CONFIG_MODE to None allows software to use all of the dual-purpose pins as general purpose I/Os.

ISC 1532

Configuration through the ispJTAG port conforms to the IEEE 1532 Standard. The Boundary Scan cells take control of the I/Os during any 1532 mode instruction. The Boundary Scan cells can be set to a pre-determined value whenever using the JTAG 1532 mode. Because of this the dedicated pins, such as DONE, cannot be relied upon for valid configuration status.

Transparent Readback
The ispJTAG Transparent Readback mode allows the user to read the content of the device SRAM or Flash while the device remains in a functional state. Care must be exercised when reading EBR and distributed RAM, as it is possible to cause conflicts with accesses from the user design (causing possible data corruption).

The I/O and non-JTAG configuration pins remain active during a Transparent Readback. The device enters the Transparent Readback mode through a JTAG instruction.

Boundary Scan and BSDL Files
BSDL files for this device can be found on the Lattice web site at www.latticesemi.com. The boundary scan ring covers all of the I/O pins, as well as the dedicated and dual-purpose sysCONFIG pins.

Power Save Mode
An I/O Power Save mode option is available for the LatticeXP device and will deactivate portions of the I/O cell drivers. This is only valid when using comparator type inputs pins (pins that use VREF), like HSTL, SSTL, etc.

Power Save mode limits some of the functionality of Boundary Scan. For Boundary Scan testing it is recommended that the I/O Power Save mode be set to OFF so that all of the I/Os will be fully functional.

Wake Up Options

When configuration is complete (the SRAM has been loaded), the device should wake up in a predictable fashion. The following selections determine how the device will wake up. Two synchronous wake up processes are available. One automatically wakes the device up when the internal Done bit is set regardless of whether the DONE pin is held low externally or not, the other waits for the DONE pin to be driven high before starting the wake up process. The DONE_EX preference determines whether the external DONE pin will control the synchronous wake up.

Wake Up Sequence

Table 13-8 provides a list of the wake up sequences supported by the LatticeXP.

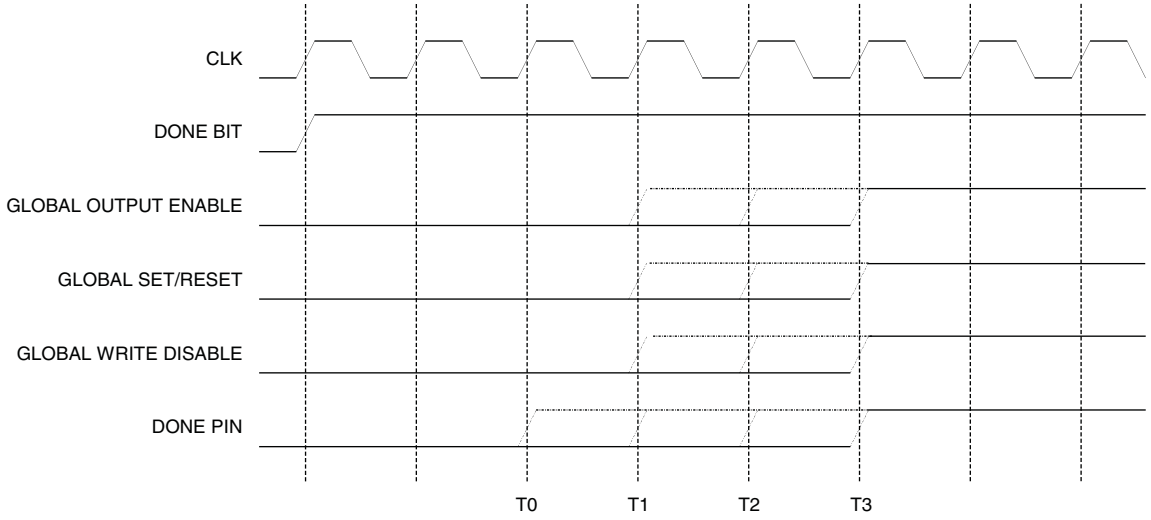
Table 13-8. Wake Up Sequences Supported by LatticeXP

Sequence	Phase T0	Phase T1	Phase T2	Phase T3
1	DONE	GOE, GWDIS, GSR		
2	DONE		GOE, GWDIS, GSR	
3	DONE			GOE, GWDIS, GSR
4	DONE	GOE	GWDIS, GSR	
5	DONE	GOE		GWDIS, GSR
6	DONE	GOE	GWDIS	GSR
7	DONE	GOE	GSR	GWDIS
8		DONE	GOE, GWDIS, GSR	
9		DONE		GOE, GWDIS, GSR
10		DONE	GWDIS, GSR	GOE
11		DONE	GOE	GWDIS, GSR
12			DONE	GOE, GWDIS, GSR
13		GOE, GWDIS, GSR	DONE	
14		GOE	DONE	GWDIS, GSR
15		GOE, GWDIS	DONE	GSR
16		GWDIS	DONE	GOE, GSR
17		GWDIS, GSR	DONE	GOE
18		GOE, GSR	DONE	GWDIS
19			GOE, GWDIS, GSR	DONE
20		GOE, GWDIS, GSR		DONE

Table 13-8. Wake Up Sequences Supported by LatticeXP (Continued)

Sequence	Phase T0	Phase T1	Phase T2	Phase T3
21 (Default)		GOE	GWDIS, GSR	DONE
22		GOE, GWDIS	GSR	DONE
23		GWDIS	GOE, GSR	DONE
24		GWDIS, GSR	GOE	DONE
25		GOE, GSR	GWDIS	DONE

Figure 13-7. Wake Up Sequence to Internal Clock



Synchronous to Internal Done Bit

If the LatticeXP device is the only device in the chain, or the last device in a chain, the wake up process should be initiated by the completion of the configuration. Once the configuration is complete, the internal Done bit will be set and then the wake up process will begin.

Synchronous to External DONE Signal

The DONE pin can be selected to delay wake up. If DONE_EX is true then the wake up sequence will be delayed until the DONE pin is high. The device will then follow the WAKE_UP sequence selected.

Software Selectable Options

In order to control the configuration of the LatticeXP device beyond the default settings, software preferences are used. Table 13-9 is a list of the preferences with their default settings.

Table 13-9. Software Preference List for the LatticeXP

Preference Name	Default Setting [List of All Settings]
PERSISTENT	OFF [off, on]
CONFIG_MODE	NONE[SLAVE_PARALLEL, SLAVE_SERIAL, MASTER_SERIAL, NONE]
DONE_OD	ON [off, on]
DONE_EX	OFF [off, on]
MCCLK_FREQ	Lowest Frequency (see Table 13-3)
CONFIG_SECURE	OFF [off, on]
WAKE_UP	21 (DONE_EX = off) 4 (DONE_EX = on)
PWRSAVE	OFF [off, on]

PERSISTENT Bit

In order to use the sysCONFIG port while in user mode to read SRAM or Flash memory, the PERSISTENT bit must be set to ON. PERSISTENT = ON preserves all of the sysCONFIG pins so the FPGA can be accessed by an external device at any time. PERSISTENT = ON lets the software know that all of the dual-purpose configuration pins are reserved and NOT available for use by the fitter or the user. PERSISTENT = ON reserves all of the dual-purpose sysCONFIG pins, without regard to CONFIG_MODE.

Configuration Mode

The device knows which physical sysCONFIG port will be used by reading the state of the CFG[1:0] pins, but the fitter software also needs to know which port will be used. The fitter cannot sample the configuration pins so the user must tell the fitter by selecting the proper CONFIG_MODE. CONFIG_MODE tells the fitter which sysCONFIG pins are not available for use as user I/O.

There are several additional configuration options, such as overflow, that are set by software. These options are selected by clicking Properties under Generate Bitstream Data in ispLEVER. If either overflow option is selected, then the DONE_EX and WAKE_UP selections will be set to correspond (see Table 13-10). Refer to the Configuration Modes and Options section of this document for more details.

Table 13-10. Overflow Option Defaults

Overflow Option	DONE_EX Preference	WAKE_UP Preference
Off	Off (Default)	Default 21 (user selectable 1 through 25)
Off	On	Default 21 (user selectable 1 through 25)
On (either)	On (automatically set by software)	Default 4 (User selectable 1 through 7)

DONE Open Drain

The “DONE_OD” preference allows the user to configure the DONE pin as an open drain pin. The “DONE_OD” preference is only used for the DONE pin. When the DONE pin is driven low, internally or externally, this indicates that configuration is not complete and the device is not ready for the wake up sequence. Once configuration is complete, with no errors, and the device is ready for wake up, the DONE pin must be driven high. For other devices to be able to control the wake up process an open drain configuration is needed to avoid contention on the DONE pin. The “DONE_OD” preference for the DONE pin defaults to ON. The DONE_OD preference is automatically set to ON if the DONE_EX preference is set to ON. See Table 13-11 for more information on the relationship between DONE_OD and DONE_EX.

DONE External

The LatticeXP device can wake up on its own after the Done bit is set or wait for the DONE pin to be driven high externally. Set DONE_EX = ON to delay wake up until the DONE pin is driven high by an external signal synchro-

nous to the clock; select OFF to synchronously wake up when the internal Done bit is set and ignore any external driving of the DONE pin. The default is DONE_EX = OFF. If DONE_EX is set to ON, DONE_OD will be set to ON. If an external signal is driving the DONE pin it should be open drain as well (an external pull-up resistor may need to be added). See Table 13-11 for more information on the relationship between DONE_OD and DONE_EX.

Table 13-11. Summary of DONE pin Preferences (Preferences)

DONE_EX	Wake Up Process	DONE_OD
OFF	External DONE ignored	User selected
ON	External DONE low delays	Set to Default (ON)

Master Clock Selection

When the user has determined that the LatticeXP will be a master configuration device (by properly setting the CFG[1:0] pins), and therefore provide the source clocking for configuration, the CCLK pin becomes an output with the frequency set by the value in MCCLK_FREQ. At the start of configuration the device operates at the default Master Clock Frequency of 2.5 MHz. Some of the first bits in the configuration bitstream are MCCLK_FREQ, once these are read the clock immediately starts operating at the user-defined frequency. The clock frequency is changed using a glitchless switch.

Security

When CONFIG_SECURE is set to ON, NO read back operation will be supported through the sysCONFIG or ispJTAG port of the general contents. The ispJTAG DeviceID area is readable and not considered securable. Default is OFF.

Wake Up Sequence

The WAKE_UP sequence controls three internal signals and the DONE pin. The DONE pin will be driven after configuration and prior to user mode. See the Wake Up Sequence section of this document for an example of the phase controls and information on the wake up selections. The default setting for the WAKE_UP preference is determined by the DONE_EX setting.

Wake Up with DONE_EX = Off (Default Setting)
The WAKE_UP preference for DONE_EX = OFF (default) supports the user selectable options 1 through 25, as shown in Table 13-8. If the user does not select a wake-up sequence, the default, for DONE_EX = OFF, will be wake-up sequence 21.

Wake Up with DONE_EX = On
The WAKE_UP preference for DONE_EX = ON supports the user selectable options 1 through 7, as shown in Table 13-8. If the user does not select a wake-up sequence, the default will be wake-up sequence 4.

Start_Up Clock Selection

Once the FPGA is configured, it enters the start-up state, which is the transition between the configuration and operational states. This sequence is synchronized to a clock source, which defaults to CCLK when sysCONFIG is used, or TCK when JTAG is used.

If desired, a user-defined clock source can be used instead of CCLK/TCK. You need to specify this clock signal, and instantiate the STRTUP library element in your design. The example shown below shows the proper syntax of instantiating the STRTUP library element.

Verilog:

```
STRTUP u1 (.UCLK(<clock_name>)) /* synthesis syn_noprune=1 */;
```

VHDL:

```
   component STRTUP
      port(STRTUP: in STD_ULOGIC );
   end component;

   attribute syn_noprune: boolean ;
   attribute syn_noprune of STRTUP: component is true;
   begin
u1: STRTUP port map (UCLK =><clock name>);
```

INBUF

The I/O INBUF option will disable all unused input buffers to save power. INBUF mode limits some of the functionality of Boundary Scan. For Boundary Scan testing it is recommended that the I/O Power Save mode be set to ON so that all of the I/Os will be fully functional.

Technical Support Assistance

Hotline: 1-800-LATTICE (North America)
+1-503-268-8001 (Outside North America)
e-mail: techsupport@latticesemi.com
Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
February 2005	01.0	Initial release.
March 2005	01.1	Changed Figure 12-1 to make it more understandable
		Changed Table 12-5 to make it more understandable
		Changed CFG[0:1] to CFG[1:0]
		Added msb, lsb references to D[0:7]
		Added Max Config Bits Table
July 2005	01.2	Changed INITN description, INITN is low during SDM configuration
September 2005	01.3	Added information on how to use the sysCONFIG dual-purpose pins as GPIO.
February 2006	01.4	Removed "pull-up" from TDO signal.
August 2007	01.5	Nomenclature for Power Save feature changed to INBUF.
September 2007	01.6	Updated Dual-Purpose sysCONFIG Pins text section.
March 2008	01.7	Updated PROGRAMN text section.
		Updated CSN and SC1N text section.
		Updated Bypass Overflow Option text section.
		Updated Flow-Through Overflow Option text section.
		Updated Slave Parallel Mode text section.
July 2008	01.8	Updated LatticeXP Device Preference List table.
		Updated Wake-Up Sequence to Internal Clock waveform.
		Replaced Wake-up Clock Selection text section with new Start_Up Clock Selection text section.
September 2008	01.9	Updated CCLK text section.