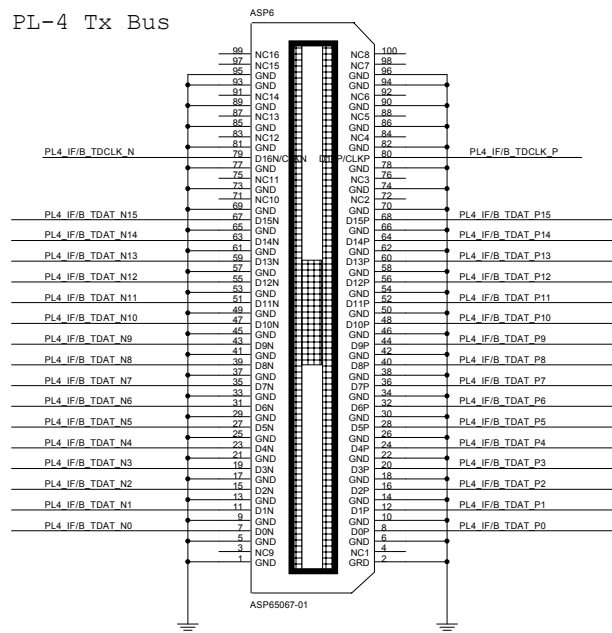




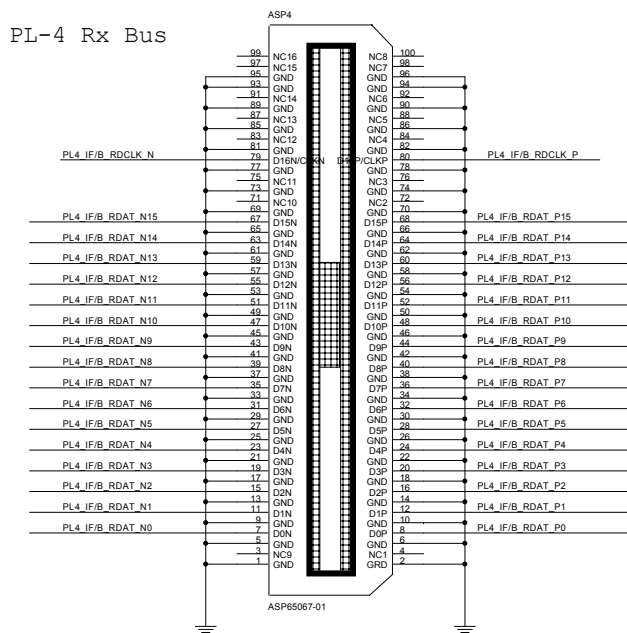
To  
ORSPI

PL-4 Tx Bus

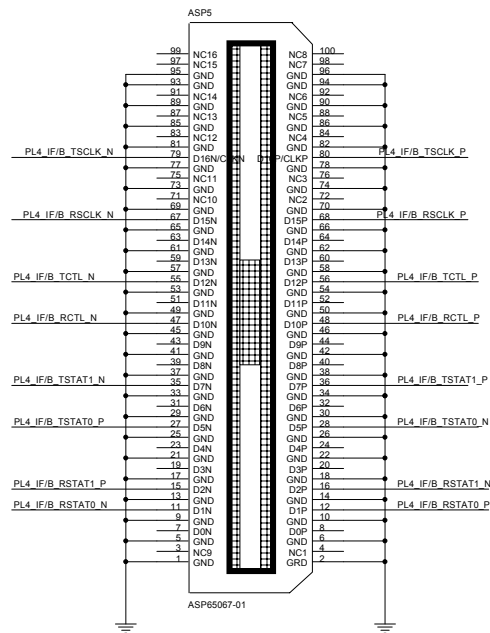


From  
ORSPI

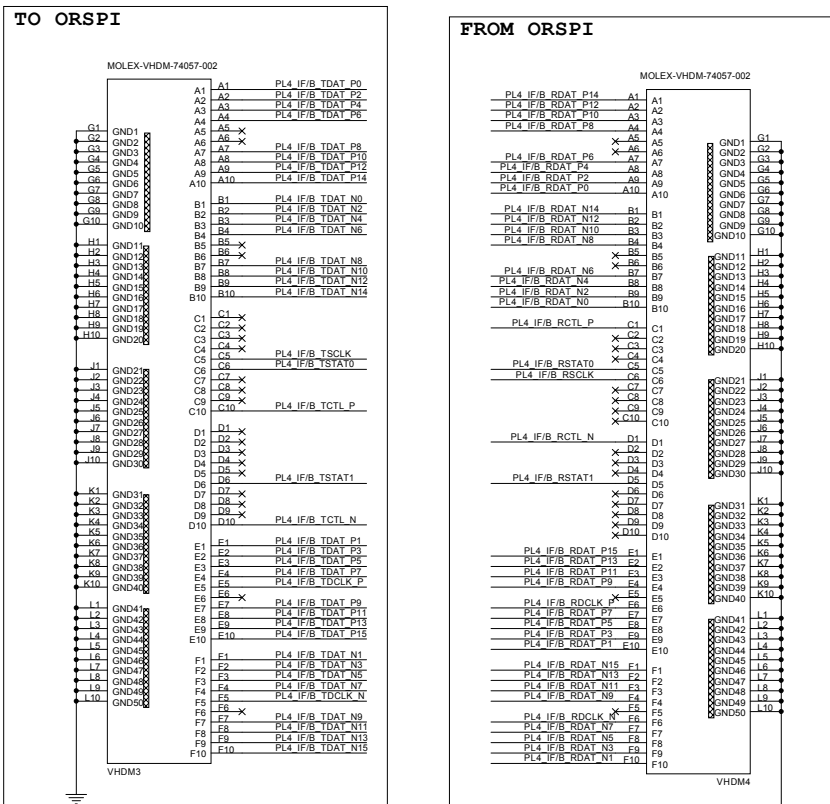
PL-4 Rx Bus



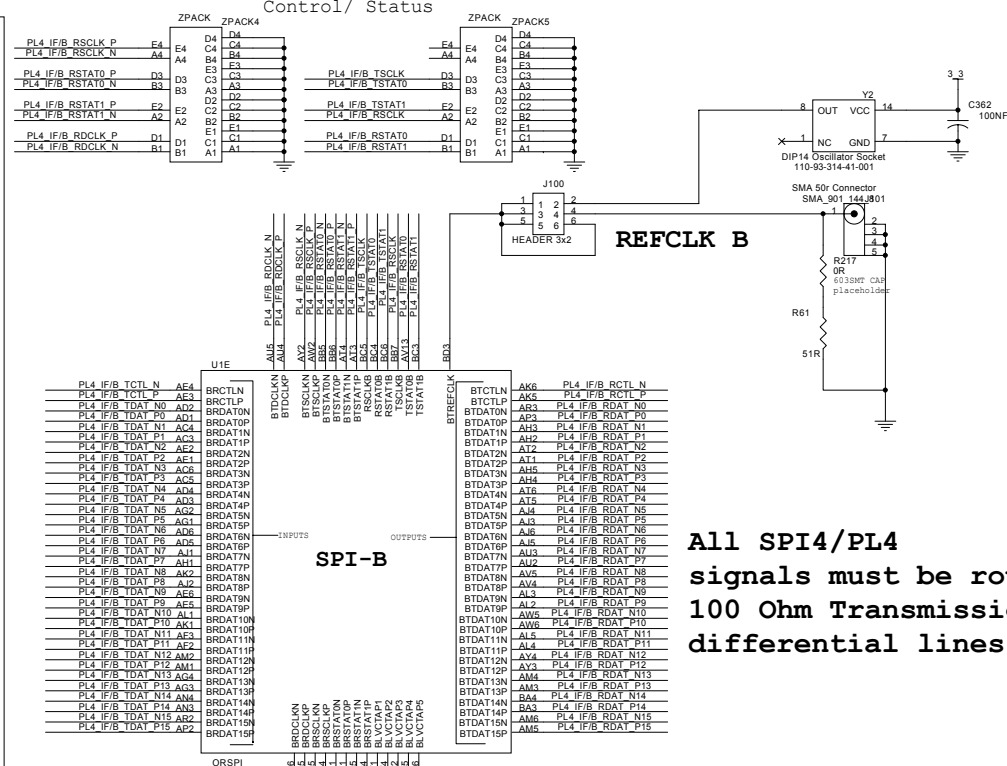
Control/ Status



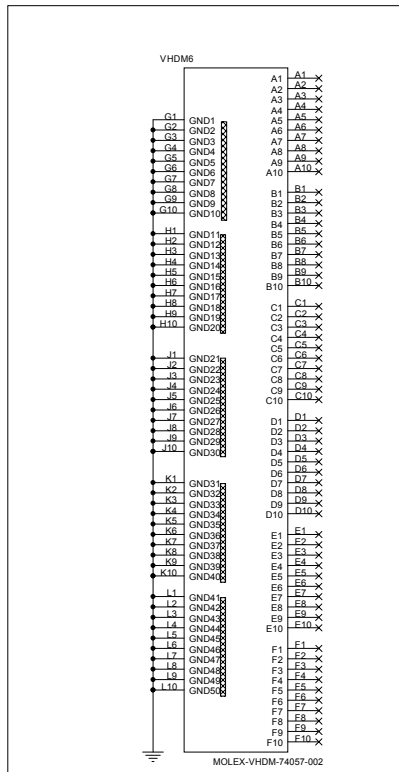
TO ORSPI



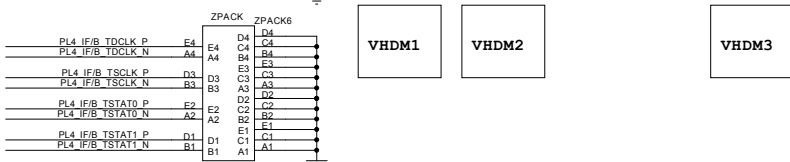
Control/ Status



All SPI4/PL4  
signals must be routed  
100 Ohm Transmission  
differential lines

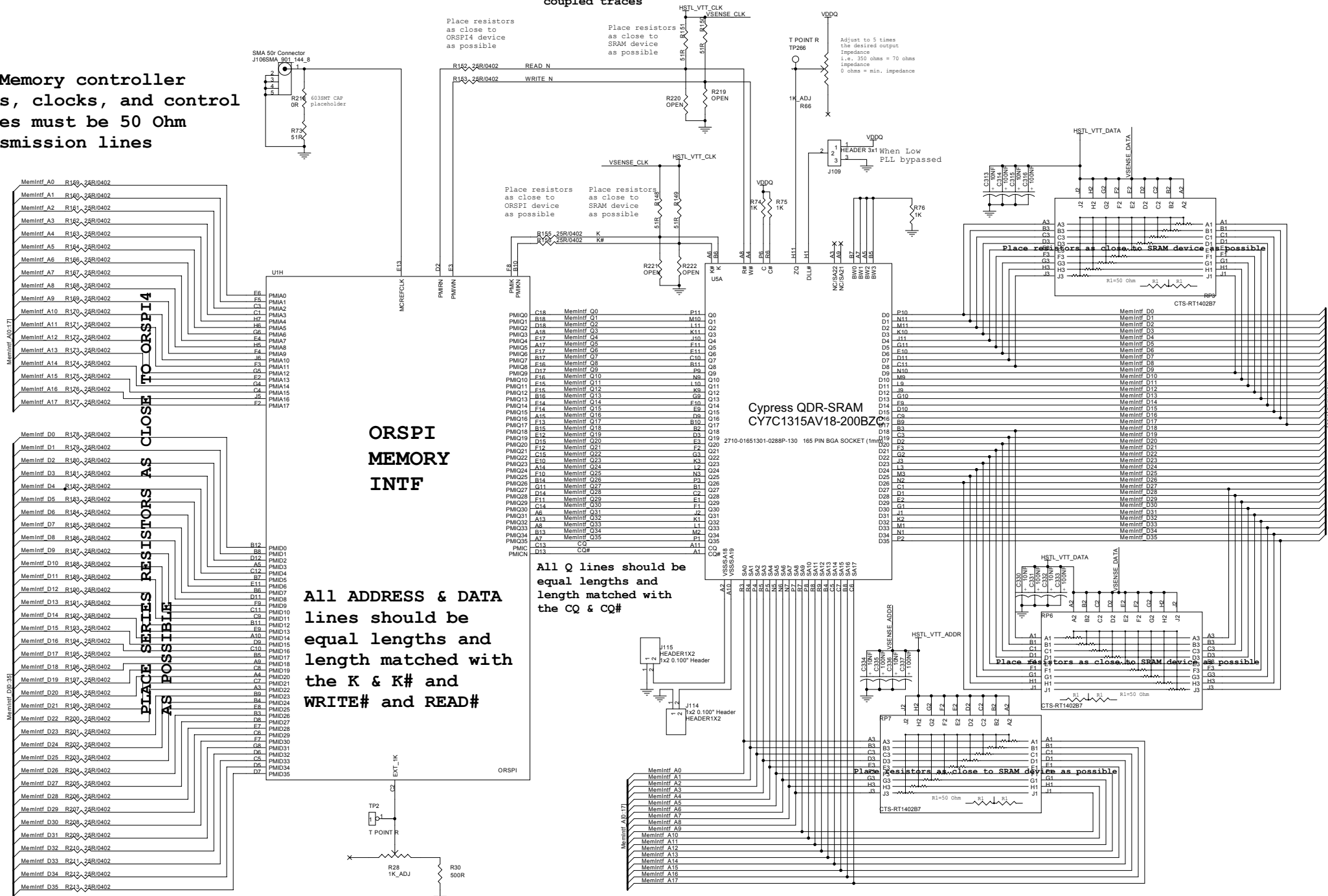


Control/ Status

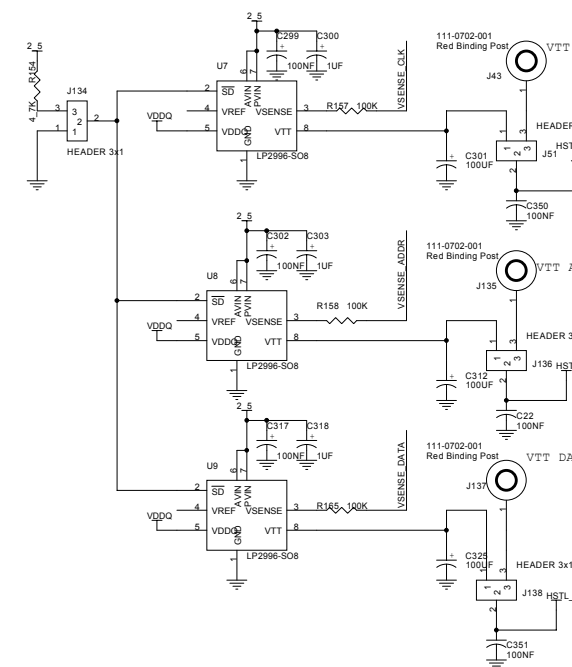




ALL Memory controller  
buses, clocks, and control  
traces must be 50 Ohm  
Transmission lines



```
ROUTE VSENSE[1:3] TO DEVICE
```



HSTL\_1 Class I,  
50 Ohm parallel terminated output  
load, and optional  
HSTL\_1 Class II, 25 Ohm source series  
resistor.

