

## Introduction

Contained in this package is information that will assist you in evaluating and verifying your ORSPI4 designs using the Lattice ORSPI4 Evaluation Board and the ORCAstra system bus control panel.

This evaluation board supports a number of testing and evaluation setups for the ORSPI4. This document covers some common types of evaluation testing that can be performed on the ORSPI4 device, including:

- SPI-4 Dynamic Alignment Mode
- SERDES RAW (non-8b/10b) Mode
- SERDES 8b/10b Mode

The tests include transmitter eye diagram measurement, SPI-4 and 8b/10b near-end loop-backs and SERDES-only (non 8b/10b), 8b/10b and aligned 8b/10b far-end loop-back. All of the described evaluation setups will use the ORSPI4\_ceval\_v1.bit bitstream. This bitstream is available for download at [www.latticesemi.com](http://www.latticesemi.com). A unique ORCAstra macro is used to configure the device for each test.

## PC and Evaluation Board Setup

This document assumes the ORCAstra application and bitstream programming software (ispVM<sup>®</sup>) are installed on a PC. It also assumes the baseline board configuration listed below. (The user is also encouraged to experiment with other configurations.)

- All jumpers should be in their default position and default programming in the ispPAC-POWR1208 as described in the *ORCA ORSPI4 Evaluation Board User's Guide*. This will apply power in the recommended sequence and provide 3.3V VDDIO to all banks.
- ispDOWNLOAD<sup>®</sup> cable (pDS4102-DL2) connected to the Parallel port of the PC and to the ispVM connector on the board (J29). The pDS4102-DL2 is included with the Lattice evaluation board. Alternately, a HW-USB-1A ispDOWNLOAD cable can be used.)
- ORCAstra connected to the parallel or USB port on the PC and the ORCAstra Interface DB-25 or USB connector on the board (J132).
- Pins 2 and 4 connected on J100. This selects the Y2 oscillator as the source of SMA J101.
- J101 connected to the J10 FPGA clock input SMA via cable. See Figure 4.
- J7/J11 FPGA SMA output connected to the External SERDES Reference Clock SMA connectors (J88/J89) via cables. This provides a clock for the SERDES operation. See Figure 4.
- J6 FPGA SMA output connected to the ATREFLCK SMA input at the connector J95 via cable. This provides a clock to the SPI-4 macro of the ORSPI4. See Figure 4.
- Pins 3 and 4 connected on J94. This selects SMA J95 as the source of ATREFCLK.
- All the switches on SW5 should be set to a logic level "1" (1.5V) towards the ORSPI4 chip.
- External power should be provided from the Molex cable and power module.

In addition, the following design-specific jumpers (for the SERDES application) need to be added. Note that references to "left" or "right" positions on switches SW16-Cx are made with the assumption that the Lattice logo is in the lower left side when looking at the board:

- Jumper pins 13 and 14 on J124. This is an error injection signal (inj\_err\_n) to switch SW16-C4. Flipping the switch from "left" to "right" and back injects errors in the transmit direction of the FPGA path to the SERDES.

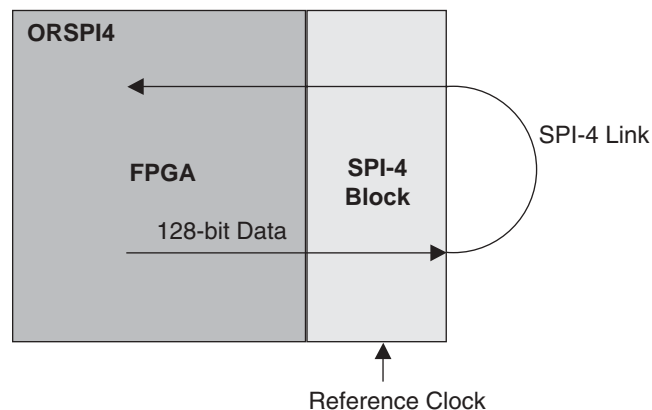
- Jumper pins 16 and 17 on J124. This connects the input “clear\_errors\_n” signal to switch SW16-C3. Flipping SW16-C3 from the “left” to the “right” position clears the “prbserror”(D11-1) and “pkterror”(D11-4) LEDs described below.
- Jumper pins 19 and 20 on J124. This connects the “farendlba” input signal to switch SW16-C2. When SW16-C2 is in the “left” position, channel A is in far end loop-back mode.
- Jumper pins 22 and 23 on J124. This connects the “farendlbb” input signal to switch SW16-C1. When SW16-C1 is in the “left” position, channel B is in far end loop-back mode.
- Jumper pins 26 and 27 on J124. This connects the PRBS error checker signal to the D11-1 LED. The design can be programmed to check  $2^7-1$  PRBS data on either of channels A or B in the FPGA. D11-1 will glow and remain lit anytime PRBS errors are detected. To clear D11-1, SW16-C3 needs to be flipped from the “left” to the “right” position.
- Jumper pins 35 and 36 on J124. This connects the 8b/10 packet error checker signal to the D11-4 LED. The design can be programmed to check a predefined 8b/10 packet data (generated on the transmit side of A and B) on either of channels A or B in the FPGA. D11-1 will glow and remain lit anytime packet errors are detected. To clear D11-4, SW16-C3 needs to be flipped from the “left” to the “right” position.

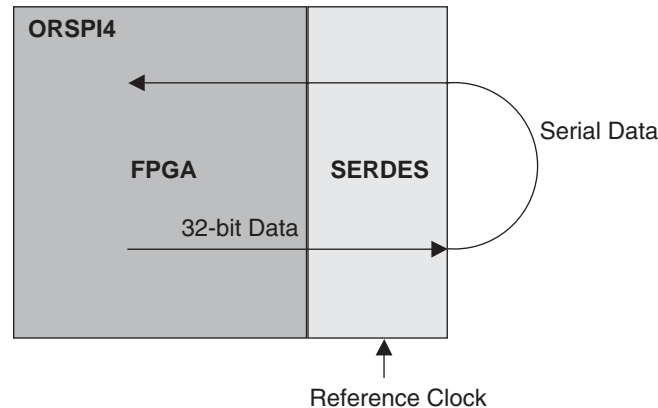
Please refer to Figure 4 for information on how the above SERDES related signals are connected in the FPGA.

## Loop-back Description

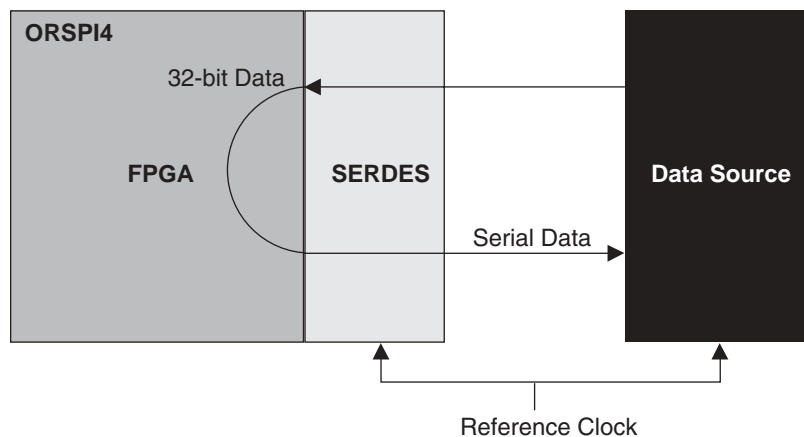
Three types of high-speed loop-backs are discussed in this technical note: SPI4 Near-End Loop-back, SERDES Near End Loop-back and Far-End Loop-back. Near-End Loop-Back (NELB) is defined as the data path from the FPGA Transmit into the SERDES (or SPI4 Macro) and back through the SERDES (or SPI4 Macro) to the FPGA Receive as shown in Figure 1 and Figure 2. The actual loop-back connection is made internally at the interfaces to transmit and receive CML buffers of the ORSPI4 device.

**Figure 1. Near-End Loop-back for SPI4 Operation**



**Figure 2. Near-End Loop-back for SERDES Operation**

Far-End Loop-back (FELB) is defined as the data path from the SERDES input, to the parallel data and back out the SERDES as shown in Figure 3. Three different internal FELB path options are discussed, SERDES-only, 8b/10b and aligned 8b/10b.

**Figure 3. Far-End Loop-back**

## ORSPI4\_CEVAL\_V1 Bitstream

The ORSPI4\_ceval\_v1.bit design has been created as a base for all the described evaluation setups for the ORSPI4 device. As shown in Figure 4, the design takes advantage of:

- Four SERDES channels available on the board for SERDES demo
- ORSPSPI4 Macro SPIA for SPI-4 demo

The ORSPI4\_ceval\_v1 bitstream and the ORCAstra macros used in the tests are available at:

[www.latticesemi.com/products/devtools/software/orcastra/index.cfm](http://www.latticesemi.com/products/devtools/software/orcastra/index.cfm)

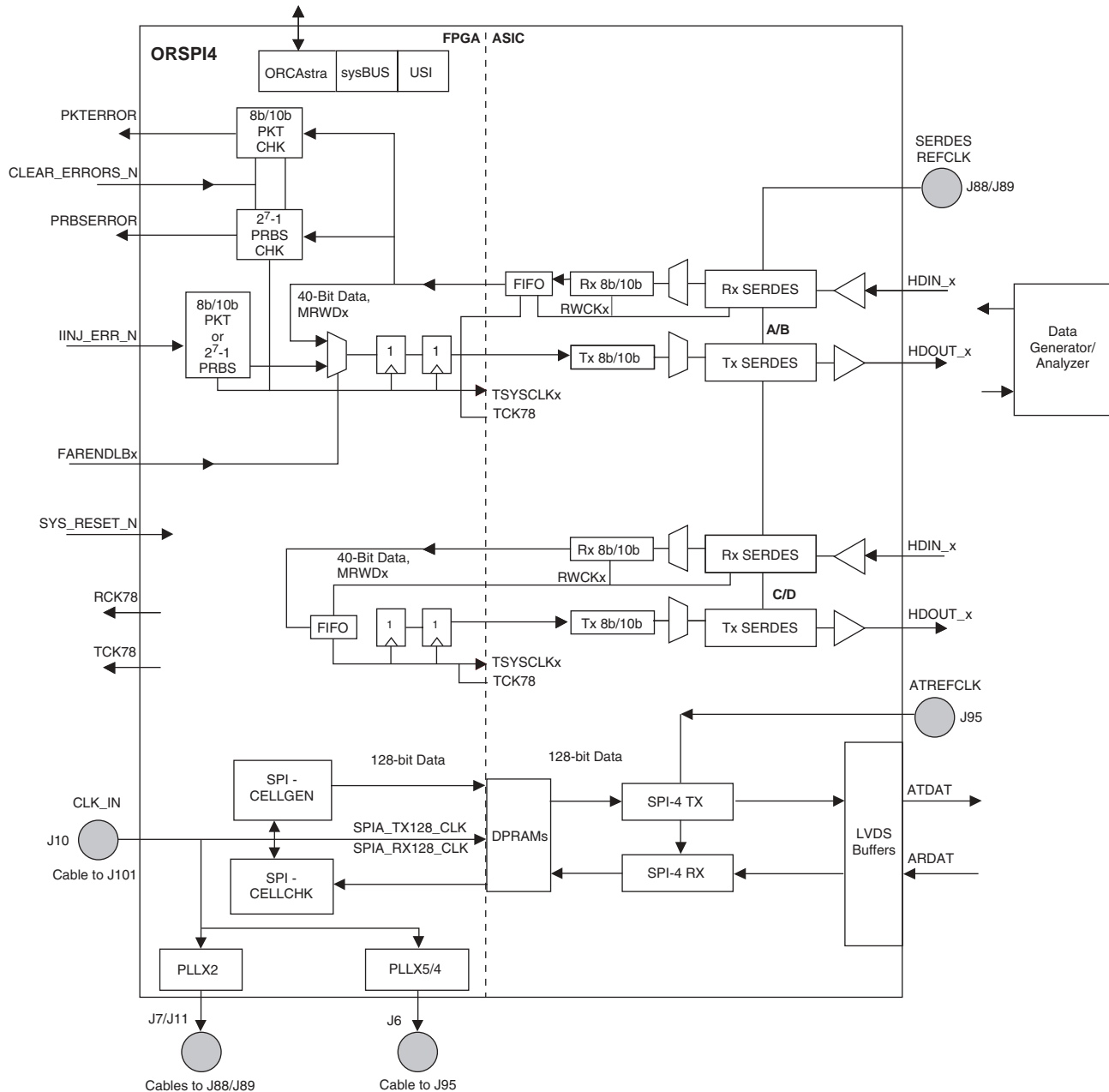
A global active low FPGA signal (sys\_reset\_n) is used to reset most of the FPGA logic. That signal is connected to the SW2 push-button on the board.

The clocking scheme is as shown in Figure 4 (please verify all connections below):

- The on-board 77.76MHZ (Y2) oscillator drives SMA pin J10 into the FPGA. This is performed by adding a jumper between pins 2 and 4 on J100, then connecting a cable between SMA J101 and SMA J10.
- Internally, the input clock drives

- The SPIA FPGA clock domain
- An X2 PLL. The output of this PLL drives the LVPECL differential outputs on SMA J7/J11. Cables then connect these outputs to the SERDES differential REFCLK inputs at J88 and J89.
- An X5/4 PLL. The output of this PLL drives the J6 SMA output. A cable then connect J6 to the SPIA REFCLK input (ATREFCLK) at J95. A jumper also needs to be connected between pins 3 and 4 on J94.

**Figure 4. ORSPI4\_ceval\_v1 Design**



Either a PRBS 2<sup>7</sup>-1 or predefined 8b/10b generator in the FPGA logic can supply the transmit data source for all SERDES tests. Channels A and B can be used in a transmit-only mode to observe the transmit eye diagram, or can be used for loop-back testing.

Channels A and B use the FIFO in the Embedded Core for clock domain crossing. Dual channel alignment can be performed on these two channels. The FIFO can also be bypassed. In this case, the source of TCK78 needs to be set in register 30821 depending on whether channel A or C is being looked at.

In channels C and D, the clock domain crosses the FIFO in the FPGA logic. These channels can be used in SERDES-only mode or in 8b/10b mode.

For SPI-4 tests, PRBS  $2^7-1$  data is provided to the core in 128-bit format. A single SPI-4 port design is used to demonstrate the Far-end Loop-back function for SPI-4 operation.

## Transmit Eye Diagram

One of the most fundamental evaluations that can be performed with the ORSPI4 Evaluation Board is observation and measurement of the data eye generated by the device. The ORSPI4 device's major modes will produce 8b/10b encoded, SPI-4 encapsulated, or PRBS  $2^7-1$  data eye. The same experimental setup can be used for Near-end Loop-back tests. Other data pattern eye diagrams can be measured using Far-end Loop-back setups discussed later in this document.

In the SERDES application example, either channel A or B can be used to evaluate a data eye. In 8b/10b mode, both channels use the 8b/10b transmit encoding block. IN PRBS  $2^7-1$  mode, the 8b/10b transmit encoder is bypassed. The data eye can then be observed on the A or B HDOUT CML pins.

In the SPI-4 application example, a SPIA macro is used to evaluate the data eye. PRBS  $2^7-1$  data is sent in 128-bit format using only one virtual SPI-4 port. The Near-end Loop-back can be performed internally or externally using a loop-back board.

## Transmit Eye Diagram Set-up Requirements

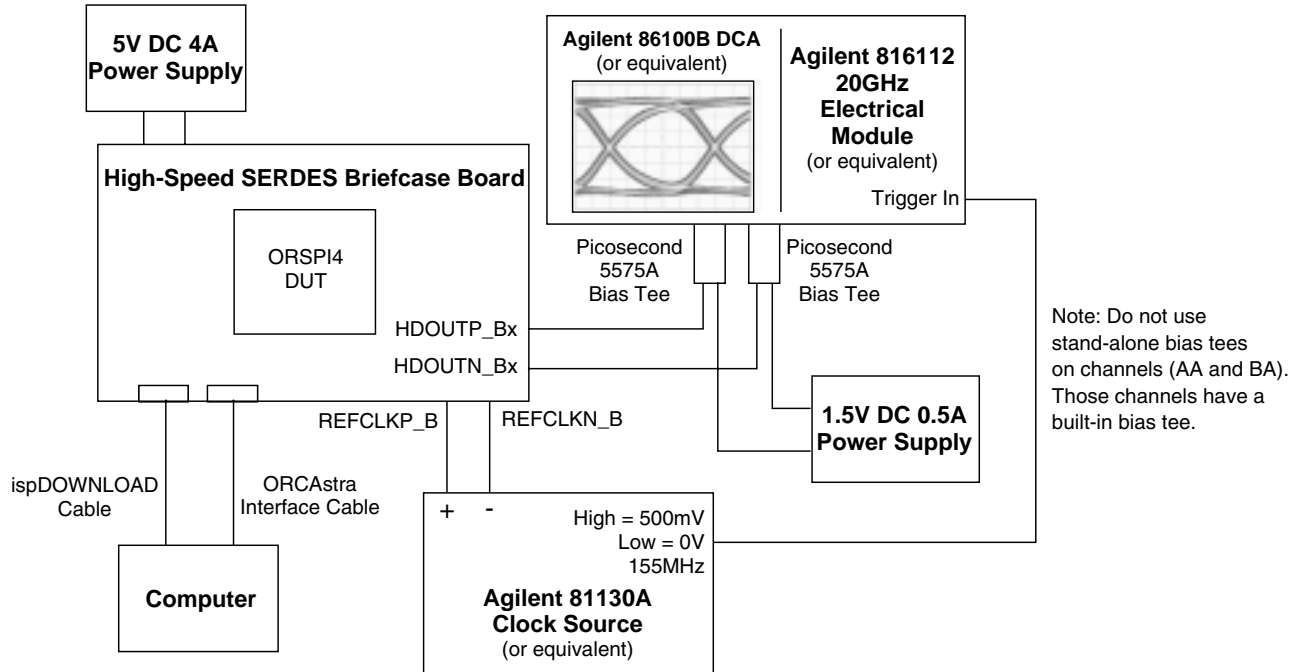
You will need the following to complete this evaluation:

- ORSPI4 Evaluation Board configured as described earlier.
- ORSPI4\_ceval\_v1.bit bitstream and bitstream programming devices (ispDOWNLOAD cable and ispVM running on a PC).
- ORCAstra GUI application in the ORSPI4 view (from the Options Menu)
- ORCAstra configuration files
  - For SERDES: 8b10b.fp1 for 8b/10b, raw\_a.fp1 for PRBS, pktA.fpm for 8b/10b, prbsA.fpm for PRBS
  - For SPI-4: Enable\_Interrupts
  - Basic\_Setup, Baseline, Training, Setup\_Cal\_Mem, Enable\_FPGA\_Data, Clear\_Error\_Count and Inject\_Error
- Measurement instruments:
  - For SERDES: Scope to view data eye and high-speed SMA cables (50ohm up to 3.0Gb/s) with bias-tee's at the input to the scope.
  - For SPI-4: Scope to view data eye and 50-ohm SMA coax cables.
- Clock sources:
  - For SERDES: Clock Source capable of driving a CML input clock (77.76-156.25MHz) and SMA cables from the clock source to the evaluation board and to the trigger input of the scope. (Note: The eye measurements could alternately be made using a Serial Data Analyzer. In that case no trigger connection is required.)
  - For SPI-4: LVTTTL clock source for the ATREFCLK running between 87.5 MHz and 112.5 MHz, and LVTTTL FPGA clock source running at approximately 80MHz.
- 5V DC wall power supply.

- 1.5V DC supply for the bias-T's.

A typical setup is shown in Figure 5.

**Figure 5. Transmit Eye Diagram Setup for SERDES Application**



## SERDES Transmit Eye Diagram Test Procedures (8b/10b Data Eye)

1. Connect the system as shown in Figure 6. The scope SMA cables should be connected to the HDOUTP\_x and HDOUTN\_x SMA connectors on the board.
2. Power-up the system
3. Start the clock generator and provide a nominal 156.25MHz CML reference clock.
4. Download the ORSPI4\_ceval\_v1.bit bitstream into the ORSPI4.
5. Open Configuration 8b10b.fp1 using the pull down menu in the ORCAstra application. This will setup the A and B channels in an 8b/10b mode
6. Run the pktA.fpm macro using the pull down menu in the ORCAstra application. This macro will enable channels A and B to transmit 8b/10b packets
7. Make sure that SW16-C1 and SW16-C2 are in the “right” position to prevent far end loop-back on channels A and B
8. Observe the 8b/10b encoded data eye on the scope.

Now that the eye is present, the system can be manipulated to improve and/or distort the eye diagram. The ORCAstra software can be used to change the pre-emphasis settings for the CML output buffer, change the half-amplitude setting for the CML output buffer, change the half-rate setting for the TX SERDES channel, or change the frequency of the incoming reference clock. The TX SERDES channel can also be powered down using the ORCAstra application.

Note: To obtain a valid eye diagram measurement, both outputs of the CML buffer must be connected to the same load. A difference in the loading of the P and the N outputs of the CML buffer will degrade the measured data eye.

## SERDES Near-End Loop-Back (8b/10b Data Eye)

In addition to the steps performed above to observe an 8b/10b eye, it is possible to perform an internal loop-back on either channel A or B and verify the 8b/10b packet checker functionality.

In addition to the steps shown in the Transmit Eye Diagram Test Procedures (8b/10b Data Eye) section. The following steps enable checking channel A for 8b/10b packet in near end loop-back:

1. Check the TESTEN check box for channel A (or write Data=41, address =30004) in the ORCAstra GUI. This sets channel A in internal loop-back while still enabling the data output to observe an eye on A.
2. Press the SW2 button to reset the FPGA logic.
3. Run the pktA.fpm macro using the pull down menu in the ORCAstra application. This macro will enable channels A and B to transmit 8b/10b packets and allows checking of 8b/10b packets using channel A.
4. Observe LED D11-4 (packet errors LED). If this LED is on, then previous packet errors were seen. The LED needs to be cleared to see if it latches any additional errors. Move SW16-C3 to the "left" position, then to the "right" position. D11-4 should be cleared by now.
5. If D11-4 is not cleared, then repeat steps 3 and 4.

In addition to the steps shown in the Transmit Eye Diagram Test Procedures (8b/10b Data Eye) section, the following steps enable checking channel B for 8b/10b packet in near-end loop-back:

1. Check the TESTEN check box for channel B (or write Data=41, address =30014) in the ORCAstra GUI. This sets channel B in internal loop-back while still enabling the data output to observe an eye on B.
2. Press the SW2 button to reset the FPGA logic.
3. Run the pktB.fpm macro using the pull down menu in the ORCAstra application. This macro will enable channels A and B to transmit 8b/10b packets and allows checking of 8b/10b packets using channel B.
4. Observe LED D11-4 (packet errors LED). If this LED is on, then previous packet errors were seen. The LED needs to be cleared to see if it latches any additional errors. Move SW16-C3 to the "left" position, then to the "right" position. D11-4 should be cleared by now.
5. If D11-1 is not cleared, repeat steps 3 and 4.

## SERDES Transmit Eye Diagram Test Procedures (PRBS 2<sup>7</sup> Data Eye)

1. Connect the system as shown in Figure 4. The scope SMA cables should be connected to the HDOUTP\_x and HDOUTN\_x SMA connectors on the board.
2. Power-up the system
3. Start the clock generator and provide a nominal 156.25MHz CML reference clock.
4. Download the ORSPI4\_ceval\_v1.bit bitstream into the ORSPI4.
5. Open Configuration raw.fp1 using the pull down menu in the ORCAstra application. This will set up the A and B channels in SERDES-only mode.
6. Run the prbsA.fpm macro using the pull down menu in the ORCAstra application. This macro will set up the A and B channels in SERDES-only mode and transmit PRBS2<sup>7</sup> packets.

7. Make sure that SW16-C1 and SW16-C2 are in the “right” position to prevent far end loop-back on channels A and B.
8. Observe the PRBS data eye on the scope.

Now that the eye is present, the system can be manipulated to improve and/or distort the eye diagram. The ORCAstra software can be used to change the pre-emphasis settings for the CML output buffer, change the half-amplitude setting for the CML output buffer, change the half-rate setting for the TX SERDES channel, or change the frequency of the incoming reference clock. The TX SERDES channel can also be powered down using the ORCAstra application.

Note: To obtain a valid eye diagram measurement, both outputs of the CML buffer must be connected to the same load. A difference in the loading of the P and the N outputs of the CML buffer will degrade the measured data eye.

## SERDES Near End Loop-Back (PRBS 2<sup>7</sup>-1 Data Eye)

In addition to the steps performed above to observe a 2<sup>7</sup>-1 eye, it is possible to perform an internal loop-back on either channel A or B and verify the 2<sup>7</sup>-1 PRBS checker functionality.

In addition to the steps shown under the Transmit Eye Diagram Test Procedures (PRBS 2<sup>7</sup>-1 Data Eye) section, the following steps enable checking channel A for PRBS 2<sup>7</sup>-1 in near-end loop-back:

1. Open Configuration raw.fp1 using the pull-down menu in the ORCAstra application. This will set up the A and B channels in SERDES-only mode.
2. Check the TESTEN check box for channel A (or write Data=41, address =30004) in the ORCAstra GUI. This sets channel A in internal loop-back while still enabling the data output to observe an eye on A.
3. Press the SW2 button to reset the FPGA logic.
4. Run the prbsA.fpm macro using the pull down menu in the ORCAstra application. This macro will enable channels A and B to transmit PRBS 2<sup>7</sup>-1 and allows checking of PRBS 2<sup>7</sup>-1 using channel A. It also sets channel A as the source of TCK78.
5. Observe LED D11-1 (PRBS 2<sup>7</sup>-1 errors LED). If this LED is on, then previous packet errors were seen. The LED needs to be cleared to see if it latches any additional errors. Move SW16-C3 to the “left” position, then to the “right” position. D11-1 should be cleared by now.
6. If D11-1 is not cleared, then repeat steps 4 and 5.

In addition to the steps shown under the Transmit Eye Diagram Test Procedures (PRBS 2<sup>7</sup>-1 Data Eye) section, the following steps enable checking channel B for PRBS 2<sup>7</sup>-1 in near end loop-back:

1. Open Configuration raw.fp1 using the pull down menu in the ORCAstra application. This will set up the A and B channels in SERDES-only mode.
2. Check the TESTEN check box for channel B (or write Data=41, address =30014) in the ORCAstra GUI. This sets channel B in internal loop-back while still enabling the data output to observe an eye on B.
3. Press the SW2 button to reset the FPGA logic.
4. Run the prbsB.fpm macro using the pull down menu in the ORCAstra application. This macro will enable channels A and B to transmit PRBS 2<sup>7</sup>-1 and allows checking of PRBS 2<sup>7</sup>-1 using channel B. It also sets channel B as the source of TCK78.
5. Observe LED D11-1 (PRBS 2<sup>7</sup>-1 errors LED). If this LED is on, then previous packet errors were seen. The LED needs to be cleared to see if it latches any additional errors. Move SW16-C3 to the “down” position, then to the “up” position. D11-1 should be cleared by now.



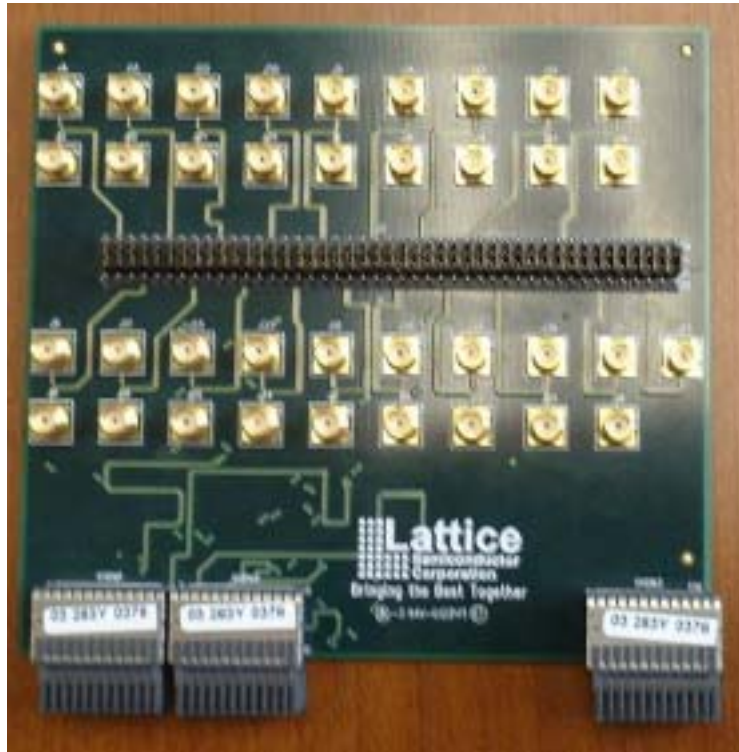
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6. If D11-1 is not cleared, then repeat steps 4 and 5.

## Transmit Eye Diagram and Near-End loop-back Test Procedures (SPI-4 Data Eye)

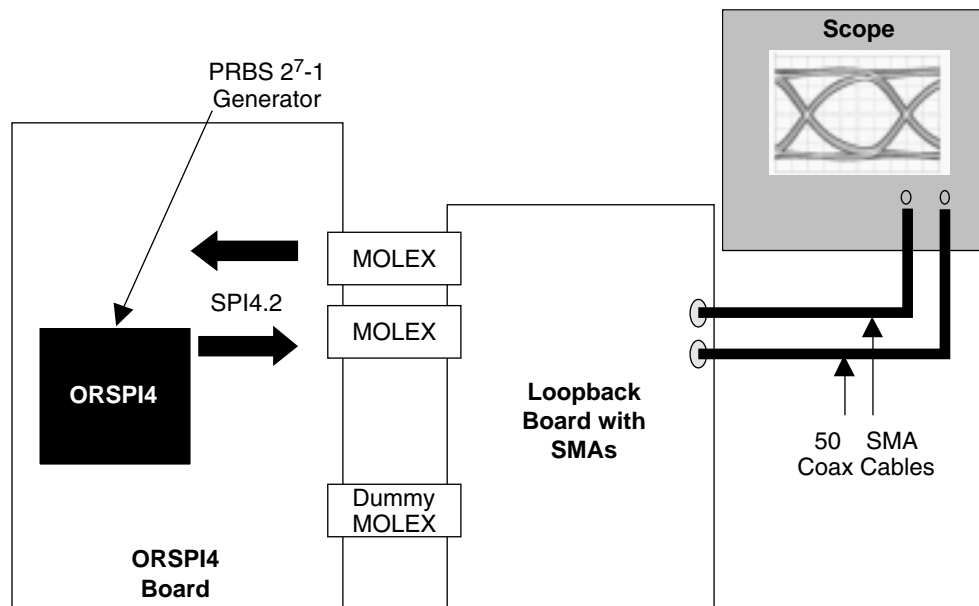
The following procedure must be followed to test near-end loop-back and generate a SPI4 data eye.

1. From screen (View) 2 of the ORSPI4 ORCASTRA GUI, open the Macro Window from the “Custom Programmability” Menu Item.
  2. Open the supplied Macro “Enable\_Interrupts” and click on “Run”. This will enable the following ORSPI4 core interrupts:
    - a. DPRAM RX FIFO Interrupts: Register 30912
      - i. OVERRUN
      - ii. UNDERRUN
    - b. SPI4.2 Interrupts: Register 30913
      - i. Loss of Lock for High Speed PLL
      - ii. Baseline Done
      - iii. Baseline Error
      - iv. Dynamic Alignment or De-skew Done
      - v. Dynamic Alignment Error
      - vi. Training Patterns Detected
      - vii. Loss of alignment due excess consecutive DIP4 errors
      - viii. TX status for having too many consecutive DIP2 errors
    - c. DIP4 and DIP2 Errors Interrupts Enable: Register 30914
      - i. Illegal Control Word
      - ii. DIP4 Error
      - iii. DIP2 Error
      - iv. Asynchronous FIFO (in the High Speed block) overrun.
  3. After the interrupts are enabled the visual indication can be seen on the screen by clicking the “Poll All” button. The check marks corresponding to all of the interrupts will light up in white. These check marks indicate that the interrupts were enabled. If the background light (red or green) is also lit, this indicates the instantaneous status of that specific interrupt.
  4. Open the macro “Basic\_Setup” and click on “Run”. This macro sets up the following configuration:
    - a. TX and RX DPRAMs in 128 bit aggregation mode and no partitions
    - b. TX DPRAMs FIFO\_FULL level and RX DPRAM FIFO\_EMPTY level
    - c. TX and RX Calendar Length to 1
    - d. TX and RX Calendar\_M to 10
    - e. MAX\_BURST1 to “1F” and MAX\_BURST2 to “0F”
  5. Open the macro “Baseline” and click on “Run”. This macro performs the baseline operation essential for the high-speed blocks to internally align.
  6. Open the macro “Training” and click on “Run”. This macro enables the training to be detected by the receiver.
  7. Click on the “Poll All” button again and ensure register 3091C reads “54” indicating:
    - a. PLL is locked to the clock
    - b. Baseline and training completed without errors
    - c. Training patterns are still being detected
  8. If this does not happen, either baseline or training was not successful and the above procedure needs to be repeated. The details of the start-up procedure are given in the ORSPI4 Data Sheet and should be referenced for a more thorough understanding of the required start-up procedure.
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9. Open the macro "Setup\_Cal\_Mem" and click on "Run". This macro will provision the RX and TX Calendars and Port Descriptor Memories (PDM) for one virtual SPI4 Port.
10. The Calendar and PDM tables can be viewed from the ORCAstra GUI by clicking on their respective buttons. The Calendar and PDM tables are very helpful in making any necessary changes to the various fields by simply editing the field and clicking on "Write".
11. The ORSPI4 is now ready to pass data from TX to RX.
12. Open the Macro "Enable\_FPGA\_Data" and click on "Run". This macro will enable the FPGA data generator to start inputting data in to the ORSPI4 core and will also enable the data checker to start checking the RX data for errors.
13. Open the macro "Clear\_Error\_Count" and click on "Run". This macro will clear any previous error count in the Data Checker. To check if the Error count has been reset, read registers 8200 to 8203 in the GUI to ensure they are "00".
14. Open the macro "Inject\_Error" and click on "Run". This macro will insert a single PRBS error in the TX Data stream. To check if the Error count was incremented with an error, read registers 8200 to 8203 in the GUI again.
15. The above test can be repeated to insert and detect more errors with or without running the "Clear\_Error\_Count" script.
16. DIP4 and DIP2 errors can be inserted and detected from the ORCAstra GUI. There are check boxes on the screen 2 (View 2) corresponding to inserting DIP4 and DIP2 errors, when they are checked (selected) then errors are inserted from the ORPSI4 core and detected after the loop-back. These error counters are also located on screen 2.
17. The eye measurements can be taken from the J21 and J22 SMA pins on the loop-back board. The loop-back board supplied with the ORSPI4 briefcase board is equipped with four rows of headers that need to be appropriately jumped. In near-end loop-back mode, headers of the two middle rows are jumped as shown in Figure 6.

*Figure 6. ORSPI4 Loop-back Board Jumper Settings*

18. Unless the SMA cables are fully connected to the scope, the data may get corrupted because the cables will act as non-terminated stubs.

*Figure 7. Transmit Eye Diagram Setup for SP-4 Application*

## SERDES Far-End Loop-back

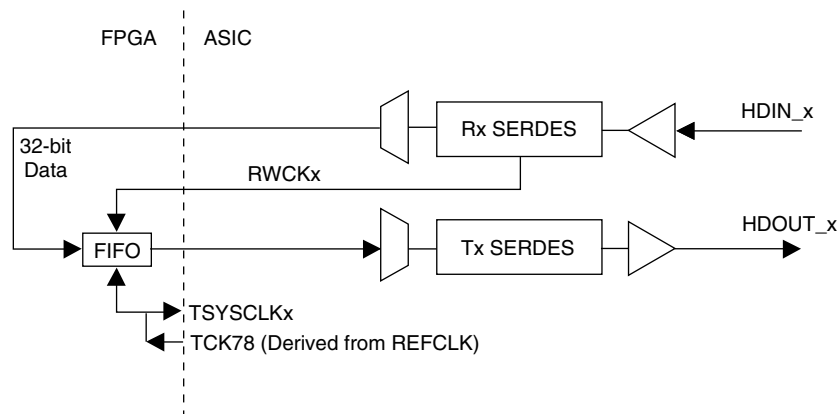
For a Far-End Loop-back (FELB) test using the ORSPI4 device, the reference clock for the ORSPI4 and for the data source must be frequency locked. This is a mandatory requirement since the ORSPI4 transmitter always uses the local reference clock.

Three types of FELB can be performed with the ORSPI4 device. Each type uses a different data path for the transmit and receive blocks of the embedded ASIC core. The three paths are SERDES-only, 8b/10b, and Aligned 8b/10b.

### SERDES-Only Tests

The active blocks in the SERDES-only data path are shown in Figure 8. Serial data is input through the CML buffer into the SERDES. Clock and data recovery is then performed, producing a 10-bit data bus and recovered clock. A MUX block then converts the 10-bit data to 40-bit data. This 40-bit data is transmitted into the FPGA. The ORSPI4\_ceval\_v1.bit design uses an asynchronous FIFO to cross clock domains to the local reference clock (REFCLK). The 40-bit data is then sent back into the embedded ASIC core, then through the MUX block to convert back to 10 bits. Finally, it is re-serialized and transmitted via the CML buffer.

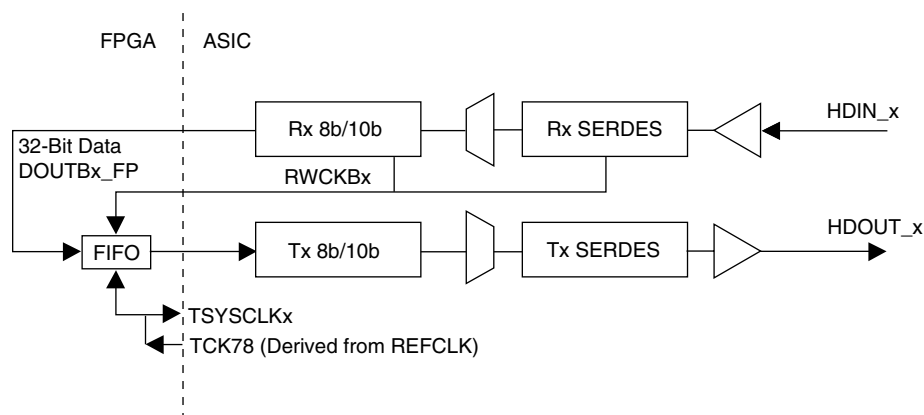
**Figure 8. SERDES Only Data Path (ORSPI4\_ceval\_v1.bit, Channel C or D)**



The SERDES-only data path can be used to evaluate any type of data pattern. The data pattern must be guaranteed to provide an adequate density of 1's for the ORSPI4 SERDES run length. For example, a Pseudo-Random Bit Stream (PRBS) test can be performed using an external data source and checker and various types of PRBS 2n-1 sequences to test the ORSPI4 device. Different types of transmit data eyes can also be observed and measured using different data patterns in this mode.

### 8b/10b Tests

The active blocks in the 8b/10b data path are shown in Figure 9. The 8b/10b data path requires 8b/10b data to be sent from an external data source to the RX input. The TX output then sends the data back to the data source for checking.

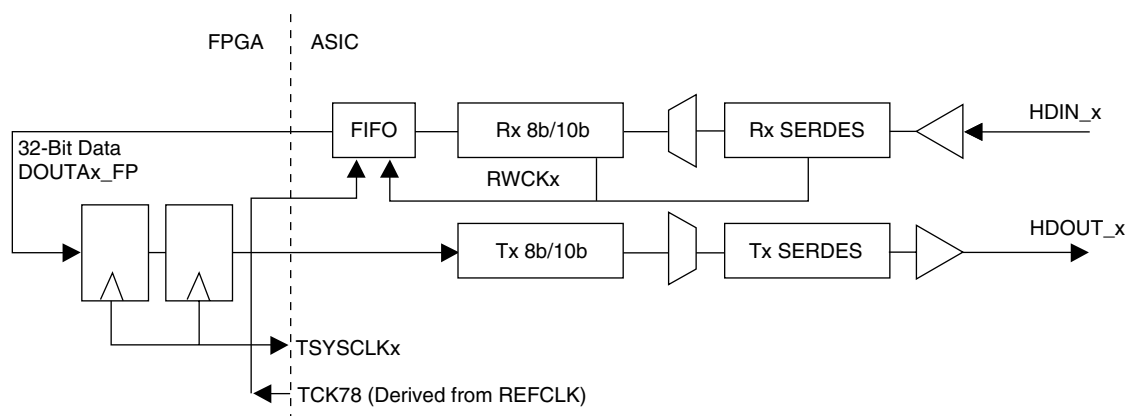
**Figure 9. 8b/10b Data Path (ORSPI4\_ceval\_v1.bit, Channel C or D)**

Serial data is input through the CML buffer into the SERDES. Clock and data recovery is then performed, producing a 10-bit data bus and recovered clock. A MUX block then converts the 10 bits of data to 40 bits of data using an alignment character (/A/ character in XAUI mode, and ordered sets in Fiber Channel mode).

The aligned 40-bit data is transmitted to the FPGA. The ORSPI4\_ceval\_v1.bit design uses an asynchronous FIFO to cross clock domains to the local reference clock (REFCLK). The data is then sent back into the embedded core as 40 bits of data (32 bits of data, 4 bits of control, and 4 bits of TBIT9). Inside the TX 8b/10b block, the 40 bits of data is sent through the MUX block, converted back to 10 bits (8b/10b decoder), serialized and transmitted via the CML buffer.

### Aligned 8b/10b Tests

The active blocks in the aligned 8b/10b data path are shown in Figure 10. The aligned 8b/10b data path requires 8b/10b data to be sent from an external data source to the RX input. The TX output sends the data back to the data source for checking.

**Figure 10. Aligned 8b/10b Data Path (ORSPI4\_ceval\_v1.bit, Channel A and B)**

Serial data is input through the CML buffer into the SERDES. Clock and data recovery is then performed, producing a 10-bits data bus and recovered clock. A MUX block then converts the 10 bits of data to 40 bits of data using an alignment character (/A/ character in XAUI mode, and ordered sets in Fiber Channel mode).

The aligned 40-bit data is then transmitted to the alignment FIFO. The alignment FIFO crosses clock domains from the recovered clock to the local reference clock (REFCLK), aligns the two channels and sends the aligned data to the FPGA.

The ORSPI4\_ceval\_v1.bit design uses two registers to clock the data back to the transmit interface to the embedded ASIC core as 40-bit data and frame pulse ((32 bits of data, 4 bits of control, and 4 bits of TBIT9) for each channel. Inside the TX block, the data is sent through the MUX block, converted back to 10 bits (8b/10b decoder), serialized and transmitted via the CML buffer.

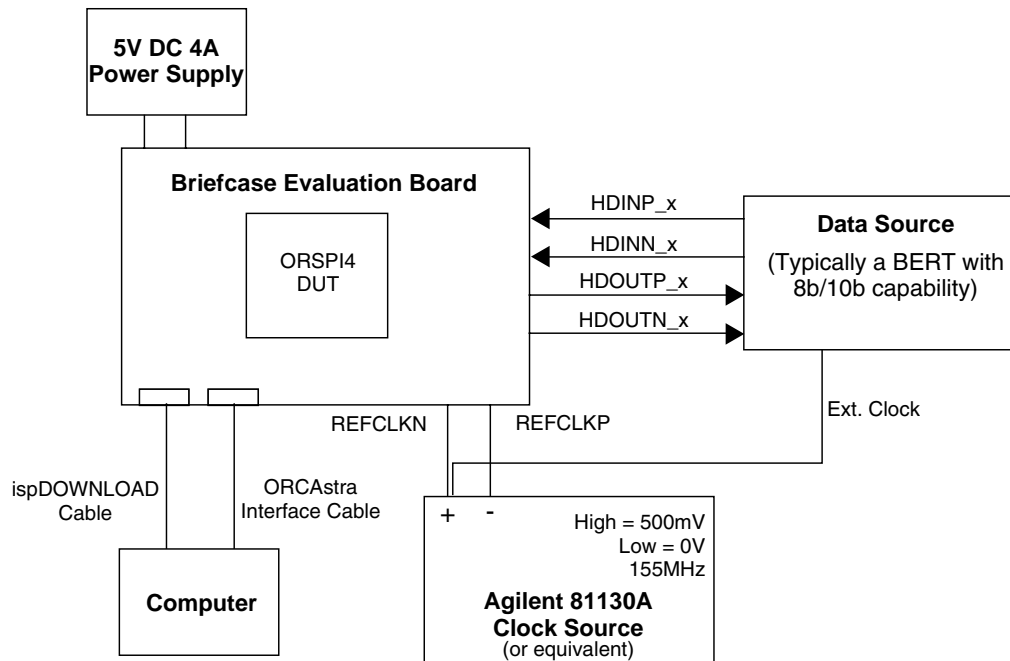
### Setup Requirements – Far-end Loop-back Testing

You will need the following to complete this evaluation:

- ORSPI4 Evaluation Board configured as described earlier
- ORSPI4\_ceval\_v1.bit bitstream and bitstream programming devices (ispDOWNLOAD cable and ispVM running on a PC).
- 5V DC wall power supply.
- Clock source capable of driving a CML input clock (77.76-156.25MHz) and SMA cables from the clock source to the evaluation board.
- ORCAstra GUI application.
- Data source with 8b/10b capability and frequency locked to the ORSPI4 reference clock. Typically this data source will also perform checks on the received data stream.

A typical test setup is shown in Figure 11.

**Figure 11. Far-End Loop-back Test Setup**



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## Test Procedures

### SERDES Only FELB (Channels C and D)

1. Connect the system as shown in Figure 11. The data SMA cables should be connected to the HDIN\_x and HDOUTN\_x SMA connectors on the board.
2. Power-up the system.
3. Start the clock generator to provide a nominal 156.25MHz CML reference clock.
4. Download the ORSPI4\_ceval\_v1.bit bitstream into the ORSPI4.
5. Open Configuration raw.fp1 using the pull down menu in the ORCAstra application. This will set up the C and D channels in SERDES-only mode.
6. Begin transmitting and analyzing data from the data source.

Note: If at any point the REFCLK or data is stopped, the SERDES channel may need to be reset to reacquire data lock. This can be done by checking and then un-checking the GSWRT check box in the ORCAstra GUI.

### 8b/10b FELB (Channels C and D)

1. Connect the system as shown in Figure 11. The data SMA cables should be connected to the HDIN\_x and HDOUTN\_x SMA connectors on the board.
2. Power-up the system.
3. Start the clock generator to provide a nominal 156.25MHz CML reference clock.
4. Download the ORSPI4\_ceval\_v1.bit bitstream into the ORSPI4.
5. Open Configuration 8b10b.fp1 using the pull down menu in the ORCAstra application. This macro will enable channels C and D in 8b/10b mode and turn on the Fibre Channel link state machine. This set-up assumes that ordered sets (ex: K28.5 Dxx.x Dxx.x Dxx.x) are received.
6. Begin transmitting and analyzing 8b/10b data from the data source.

Note: If at any point the REFCLK or data is stopped, the SERDES channel may need to be reset to reacquire data lock. This can be done by checking and then un-checking the GSWRT check box for Bx in the ORCAstra GUI.

### Aligned 8b/10b FELB (Channels A and B)

1. Connect the system as shown in Figure 11. The data SMA cables should be connected to the HDIN\_x and HDOUTN\_x SMA connectors on the board.
2. Power-up the system.
3. Start the clock generator to provide a nominal 156.25MHz CML reference clock.
4. Download the ORSPI4\_ceval\_v1.bit bitstream into the ORSPI4.
5. Open Configuration 8b10b.fp1 using the pull down menu in the ORCAstra application. This will enable channels A and B in 8b/10b mode and turn on the Fiber Channel State machine. In addition, it will enable the Alignment FIFO on A and B. This set-up assumes that ordered sets (ex: K28.5 Dxx.x Dxx.x Dxx.x) are received.
6. Set SW16-C1 and SW16-C2 in the "left" position. This sets both A and B in far-end loop-back mode.
7. Begin transmitting and analyzing 8b/10b data from the data source.

Note: If at any point the REFCLK or data is stopped, the SERDES channel may need to be reset to reacquire data lock. Check then uncheck the GSWRST check box in the ORCAstra GUI. In addition, check then uncheck the FMPU\_RESYNC1 check box for A and B in the GUI. As an indication that alignment is achieved, verify that the DEMUX\_WAS and CH248\_SYNC LEDs in the GUI are on (bright GREEN) for A and B.

## References

- Bias Tee Model 5575A, Picosecond Pulse Labs
- Picosecond Pulse Labs, Boulder CO, [www.picosecond.com](http://www.picosecond.com)

## Recommended Reading

- ORSPI4 Data Sheet
- ORCA Series 4 FPGA Data Sheet
- ispVM System Software Data Sheet
- ispDOWNLOAD Cable Data Sheet
- ORSPI4 Evaluation Board User Manual
- ORCAstra System Bus Control Panel User Manual

## Technical Support Assistance

Hotline: 1-800-LATTICE (North America)  
+1-408-826-6002 (Outside North America)  
e-mail: [techsupport@latticesemi.com](mailto:techsupport@latticesemi.com)  
Internet: [www.latticesemi.com](http://www.latticesemi.com)



## Appendix A. Function of the Bias Tee Network

### Q: What is the purpose of the bias tee and when is it needed?

The bias tee module is an enhanced DC blocking device that allows application of an external DC bias current to a device under test. It is commonly used when interfacing a high frequency device DC coupled output device to an input that does not provide the required DC bias.

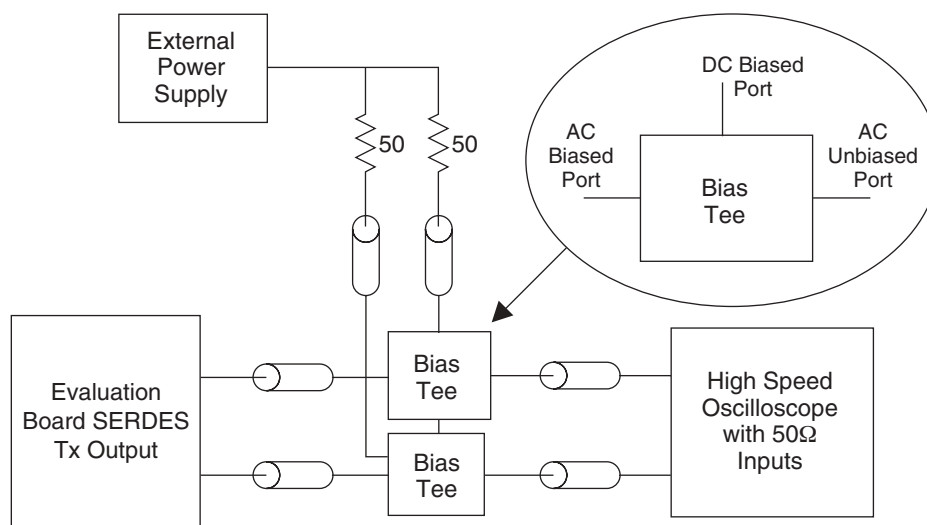
### Q: Why do the Lattice FPSC 2.5/3.125G SERDES need a bias tee?

The FPSC 2.5/3.125G SERDES high speed outputs are designed to operate into  $50\Omega$  termination impedance biased at 1.5V or 1.8V DC. (This is the internal termination provided by Lattice 2.5/3.125G SERDES inputs and other vendor CML inputs.) Since most oscilloscopes and Digital Communications Analyzers (DCAs) have  $50\Omega$  input impedance terminated to ground, they do not provide the required termination bias voltage. When this equipment is directly connected to the SERDES output, it will provide an incorrect DC bias and prevents proper output buffer operation.

Inserting the bias tee module in the SERDES output connection to the oscilloscope allows the application of the required dc bias condition and provides the dc voltage translation going into the scope. This allows the oscilloscope to display the SERDES output waveform/eye diagram under the proper termination bias conditions.

### Q: What is the proper bias tee setup for Lattice High-Speed SERDES Boards?

The connections are shown below:

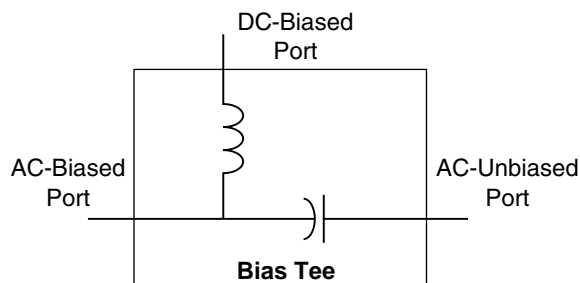


Note: The  symbol above indicates a region where shielded (SMA) cable should be used.

The bias tees may be placed anywhere in the signal path. Delay matched cables should be used insure proper P to N signal timing at the oscilloscope.

**Q: What is inside a bias tee module and how does it work?**

The bias tee module is a passive device, consisting of a capacitor and inductor, as shown below.



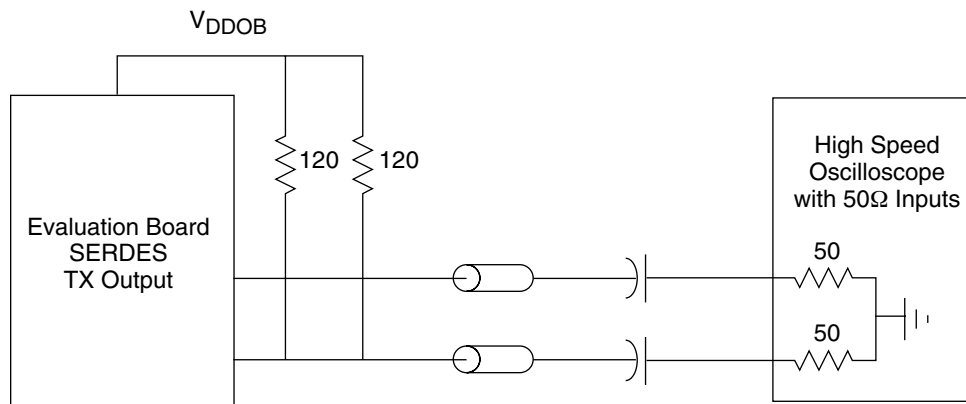
The capacitor blocks DC between the right and left signal ports. The inductor provides DC coupling/AC isolation between the upper port and the left port. The inductor is the most critical element. In practice this element consists of several inductor and resistor components very carefully assembled to provide high impedance over multiple decades of frequency. This is the key to providing low signal line reflection and low signal distortion.

Not all bias tees are the same. There are a variety of bias tees designed for specific frequency ranges and DC current levels, from several different vendors. Lattice uses a Picosecond Pulse Lab bias tee. More detailed characterization and application documents are available from this vendor. See the References section at the end of this document.

**Q: Can the SERDES output be observed without a bias tee module?**

Yes, in two different ways as shown below.

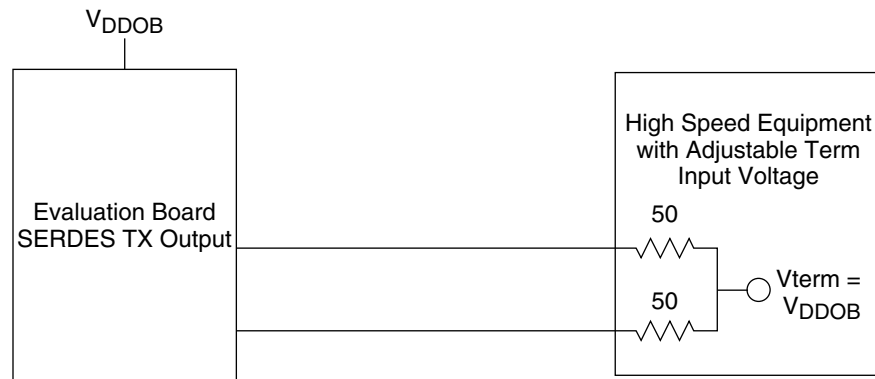
1. For AC-coupled SERDES interface applications, external shunt resistors, tied to  $V_{DDOB}$ , are suggested at the Tx output. In this case the outputs may be connected to a high speed oscilloscope without using bias tee elements. Simple coupling capacitors can be used as shown below.



Note: The  symbol above indicates a region where shielded (SMA) cable should be used.

In this interconnection the 120Ω external resistors provide the necessary DC bias to the Tx CML buffer outputs.

2. Some newer test equipment provides adjustable bias voltage on the internal  $50\Omega$  input terminations. This equipment may be directly connected to the SERDES Tx output, as shown below.



For this connection, the adjustable termination voltage should be set to the  $V_{DDOB}$  supply voltage used on the High-Speed SERDES Board (1.5V, if internal supply is being used). This is the best means of observing the Tx data output signals for DC coupled applications, since it eliminates any possible signal degradation caused by bias tee and DC blocking elements.

## References

Bias Tee Model 5575A, Picosecond Pulse Labs, Boulder CO, [www.picosecond.com](http://www.picosecond.com)