Double Data Rate (DDR) SDRAM Controller

(Non-Pipelined Version)

User's Guide

November 2004
ipug23_03

Introduction

This version of the Lattice DDR SDRAM Controller does not have pipelining, and is significantly smaller than the pipelined version. DDR (Double Data Rate) SDRAM was introduced as a replacement for SDRAM memory running at bus speeds over 75MHz. DDR SDRAM is similar in function to regular SDRAM but doubles the bandwidth of the memory by transferring data twice per cycle on both edges of the clock signal, implementing burst mode data transfer.

The DDR SDRAM Controller is a parameterized core that provides the flexibility for modifying data widths, burst transfer rates, and CAS latency settings in a design. In addition, the DDR core supports intelligent bank management, which is done by maintaining a database of "all banks activated" and the "rows activated" in each bank. With this information, the DDR SDRAM Controller decides if an active or pre-charge command is needed. This effectively reduces the latency of read/write commands issued to the DDR SDRAM.

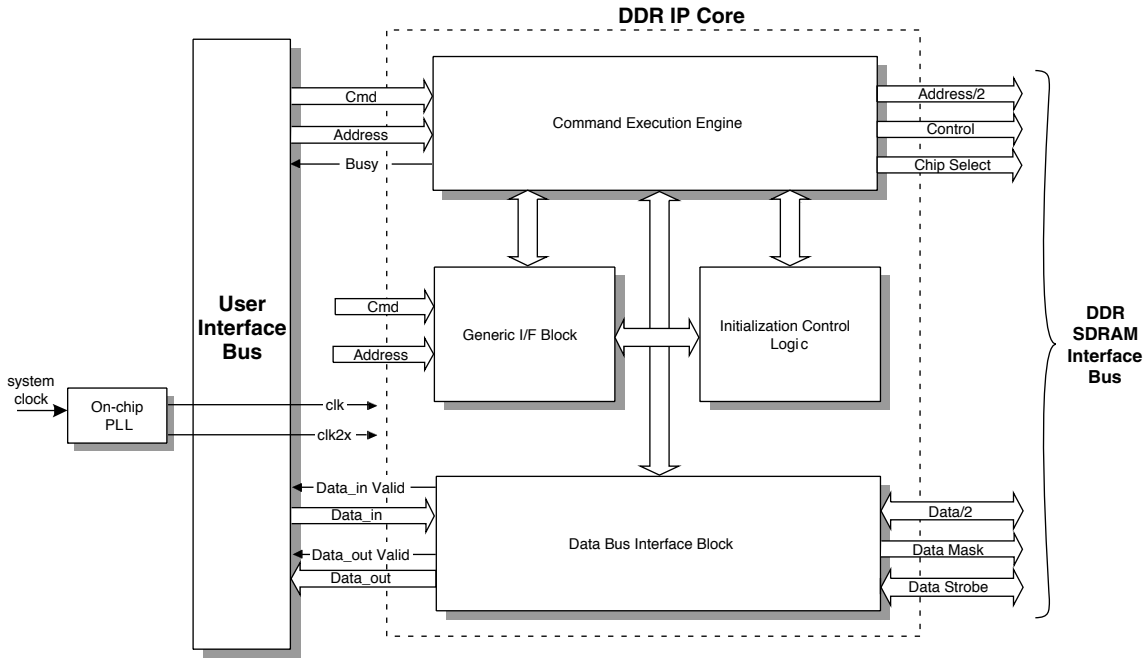
Since the DDR SDRAM Controller takes care of activating/pre-charging the banks, user only needs to issue simple read/write commands.

Features

- Performance of up to 200MHz (400 DDR)
- Interfaces to JEDEC standard DDR SDRAM
- Supports DDR SDRAM data widths of 16, 32 and 64 bits
- Supports up to eight external memory banks
- Programmable burst lengths of 2, 4, or 8
- Programmable CAS latency of 1.5, 2.0, 2.5 or 3.0
- Byte-level writing supported
- Supports Power-down and Self Refresh modes
- Automatic initialization
- Automatic refresh during Normal and Power-down modes
- Timing and settings parameters implemented as programmable registers
- Complete synchronous implementation

Block Diagram

Figure 1. DDR SDRAM Controller (non-pipelined) Block Diagram



Functional Description

The DDR SDRAM Controller block diagram (Figure 1) consists of four functional modules: the Generic Interface block, Command Execution Engine, Data Bus Interface block and the Initialization Control Logic.

Generic Interface Block

The Generic interface block contains the configuration registers: CFG0, CFG1, CFG2, and CFG3. These registers are updated when a `Load_CFG` command is received. These registers contain the programmable DDR SDRAM timing parameters and can be changed by the user to suit the DDR SDRAM memory timings being used thus giving flexibility to use any DDR SDRAM memory.

Command Execution Engine

The Command Execution Engine is the main component of the DDR SDRAM controller. This block accepts commands from the User Interface Bus and keeps a record of bank open/close status. It accepts one command at any time (non-pipelined). Once a command is received, it decides whether to open the bank, close the bank or directly execute the READ/WRITE commands and apply the appropriate DDR SDRAM commands to the DDR SDRAM memory. Table 1 shows the different user interface commands supported.

This block uses one state machine to process read/write commands received from the user interface.

This block also maintains an auto refresh counter, which refreshes the DDR SDRAM memory at the predetermined programmed intervals, even during power down.

Table 1. DDR SDRAM Controller Generic I/F Commands

Command Name	cmd[2:0]	Description
NOP	000	No operation.
READ	001	Initiate a burst read.
WRITE	010	Initiate a burst write.
LOAD CONFIG REG (Load_CFG)	011	Load controller configuration values. The controller use this command to load the CFG0/CFG1/CFG2/CFG3 registers.
LOAD MODE REG (Load_MR)	100	Load the Mode and Extended Mode register.
POWER DOWN	101	Puts the DDR SDRAM into power-down, or wake up from POWER DOWN.
SELF REFRESH	110	Start self-refresh mode or stops self-refresh mode

Data Bus Interface

The Data Bus Interface block controls the data flow between the User Generic Interface bus and DDR SDRAM Memory interface bus. The data received from memory during a read operation is converted from a double data rate to single data rate. Similarly, the data to be written into the memory is converted from a single data rate to a double data rate.

During a write operation, depending on the data mask signals, the data is written or masked by the DDR SDRAM memory.

Initialization Control Logic

When the user sets the initialization bit (Bit 7 in the configuration register CFG0) using the Load_CFG command, this block starts initialization as specified in the DDR SDRAM specification. The DDR controller initialization can only be performed after the system power is applied and the clock is running for at least 200μs. An initialization is required before any read/write command is issued to the DDR SDRAM memory.

User Interface Bus

The main function of the User Interface Bus block is to trap all transactions on the respective bus addressed to the DDR SDRAM and translate them into Generic Interface commands.

Since this bus has a burst address which is greater than the burst supported by the DDR SDRAM memory, all the interfaces have an address generator block which generates the appropriate address depending on the requested burst.

In all the interfaces the data going in and out of the bus is stored in a sync FIFO block, which is used as a storage buffer for read/write commands. During a read from the DDR SDRAM the data is sent to FIFO and is read by the User Bus Interface block. During a write the data is first written into the FIFO before actually writing this data into the DDR SDRAM.

Parameter Descriptions

The static parameters are set before the design is synthesized to a gate-level netlist. The dynamic parameters can also be set in this way, or they can be changed after the core is programmed onto a device by writing the values into the Configuration Registers. The user should consult the DDR SDRAM specifications before choosing dynamic parameters, which are dependent on the DDR SDRAM device being used.

Table 2. Static DDR SDRAM Core (non-pipelined) Parameters

Parameter	Description	Default Value
DSIZE	Defines the bus width for the data input/output port on the User Interface Bus side of the core. The selectable values are 32, 64, and 128 bits. The data width on the DDR SDRAM Interface Bus (external memory side of the core) will be half of this value. For example, if a 64-bit wide bus is needed to access the DDR memory chip, the value for DSIZE needs to be set to 128.	32 bits
RSIZE	Defines row address width.	12 bits
CSIZE	Defines column width.	11 bits
BSIZE	Defines bank width for internal chip banks. This version of the DDR SDRAM Controller is designed to work with memory chips containing four internal banks (sometimes called a quad memory array). The default value for BSIZE cannot be changed in this version of the core.	2 bits
RANK_SIZE	Defines the number of external Banks (RANKS). NOTE: an external bank is a memory chip or group of chips (such as on a DIMM) that can be accessed using the same chip select signal. RANK_SIZE = 0 (External Banks = 1) RANK_SIZE = 1 (External Banks = 2) RANK_SIZE = 2 (External Banks = 4) RANK_SIZE = 3 (External Banks = 8)	0

Table 3. Dynamic DDR Core Parameters

Parameter	Description	Default Value
INIT	Initialize DDR. Initializes the DDR SDRAM when bit is set. Set by command in register.	0
TRCD Delay	RAS to CAS Delay. This is the delay from /RAS to /CAS in number of clock cycles and is calculated using this formula INT($t_{RCD(MIN)}$ / t_{CK})*.	2
TRRD Delay	Row ACTIVE to Row ACTIVE Delay, this delay is in clock cycles and is calculated using this formula INT($t_{RRD(MIN)}$ / t_{CK})*.	2
TRFC Delay	AUTO REFRESH command period, this delay is in clock cycles and is calculated using this formula INT ($t_{RFC(MIN)}$ / t_{CK})*.	9
TRP Delay	PRECHARGE command period. This is calculated by the formula INT($t_{RP(MIN)}$ / t_{CK})*.	2
TMRD Delay	LOAD MODE REGISTER command cycle time. This is calculated by the formula INT($t_{MRD(MIN)}$ / t_{CK})*.	2
TWR Delay	Write recovery time. This is calculated by the formula INT($t_{WR(MIN)}$ / t_{CK})*.	2
TRAS Delay	ACTIVE to PRECHARGE delay. Defines the delay between ACTIVE and PRECHARGE commands. (Maximum value: 15 clock cycles)	6
TWTR Delay	WRITE to READ command delay. Defines internal write to read command delay. (Maximum value: 7 clock cycles)	1
TRC Delay	ACTIVE to ACTIVE /AUTOREFRESH command delay. Defines ACTIVE to ACTIVE/auto refresh command period delay. (Maximum value: 15 clock cycles)	8
CAS Latency	CAS Latency is a delay in clock cycles between the registration of a READ command and the first bit of output data. Valid values are 1.5, 2.0, 2.5 and 3.0.	2 (2.0 clock cycles)
Burst Length	Burst Length, this number determines the maximum number of columns that can be accessed for a given READ/WRITE and is equal to Burst Length programmed in the Mode register. Valid values are 2, 4 and 8.	2

Table 3. Dynamic DDR Core Parameters (Continued)

Parameter	Description	Default Value
Burst Type	Burst type. Defines if an interleaved or Sequential burst is required. 0 represents sequential and 1 represents interleaved burst type.	0
DSTRENGTH	Drive strength. Defines the bit 1 in Extended mode register. 0 represents normal drive strength, 1 represents a reduced drive strength (Required by some memory devices).	0
QFCFUNC	Defines bit 2 of the extended mode register, which enables or disables the QFC Function (Required by some memory devices).	0
Refresh Period	Refresh period. Defines maximum time period between AUTOREFRESH commands. It is calculated as follows. INT(t_{REF}/ t_{CK})*.	2228

*Notes:

t_{CK} = Clock cycle time
$t_{RCD(MIN)}$ = ACTIVE to READ or WRITE delay
$t_{RRD(MIN)}$ = ACTIVE (bank A) to ACTIVE (bank B) command period
$t_{RFC(MIN)}$ = AUTOREFRESH command period (min.)
$t_{RP(MIN)}$ = PRECHARGE command period
$t_{MRD(MIN)}$ = LOAD_MR command cycle time
$t_{WR(MIN)}$ = Write recovery time
t_{REF} = AUTOREFRESH command interval (max.)

Signal Descriptions

The following tables show the interface signals for the DDR SDRAM controller. The DDR SDRAM Interface signals are the same for all core configurations.

Table 4. DDR SDRAM Interface Bus Signals

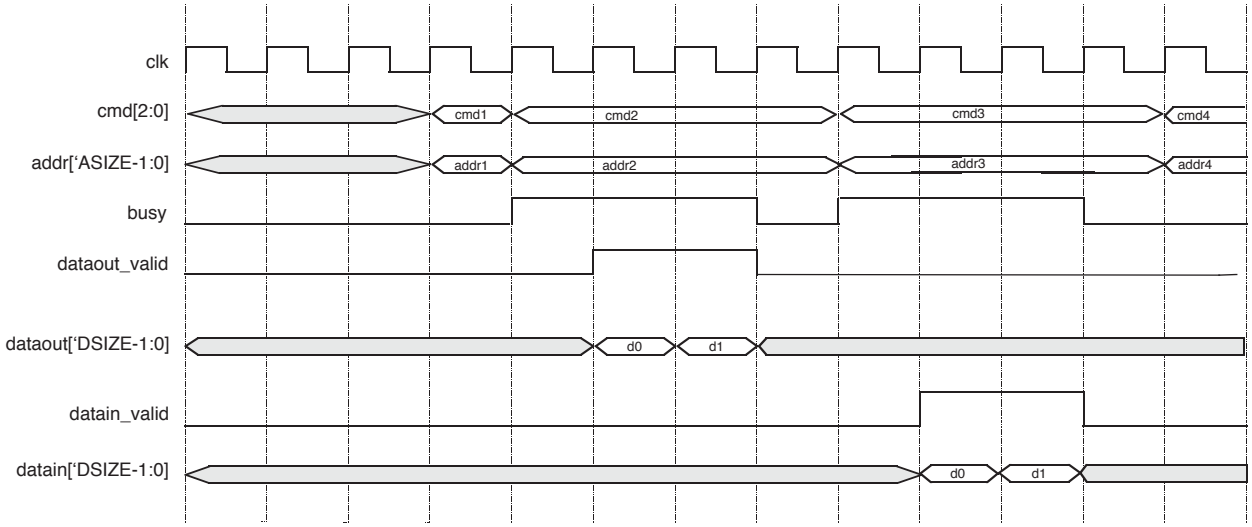
Signal Name	Direction	Active State	Description
ddr_clk	Output	N/A	DDR SDRAM Clock, derived from the system clock. **NOTE: If multiple memory banks are used (RANK_SIZE > 0), then additional clock signals will be needed at the project's top level to drive each individual memory bank.**
ddr_clk_n	Output	N/A	Inverted DDR SDRAM Clock, derived from the system clock. **NOTE: If multiple memory banks are used (RANK_SIZE > 0), then additional clock signals will be needed at the project's top level to drive each individual memory bank.**
ddr_cke	Output	High	Clock enable.
ddr_cs_n [(2^{RANK_SIZE}) - 1:0]	Output	NA	Active low chip select, which selects and deselects the DDR SDRAM external bank.
ddr_we_n	Output	Low	Write enable, defines the part of the command being entered.
ddr_cas_n	Output	Low	Column Select, defines the part of the command being entered
ddr_ras_n	Output	Low	Row select, defines the part of the command being entered.
ddr_ad[RSIZE-1:0]	Output	N/A	Row or column address lines depending whether the /RAS or /CAS is active.
ddr_ba[BSIZE-1:0]	Output	N/A	Bank address select.
ddr_dq[DSIZE/2-1:0]	In/Out	N/A	Bi-directional data bus.
ddr_dqm[DSIZE/16-1:0]	Output	N/A	Data mask signals used to mask the byte lanes for byte level write control.
ddr_dqs[DSIZE/16-1:0]	In/Out	N/A	Data strobe signals used by memory to latch the write data.

Table 5. User Interface Bus Signals

Signal Name	Direction	Active State	Description
clk	Input	N/A	System clock.
clk2x	Input	N/A	This is the doubled clock signal coming from the on-chip PLL.
reset_n	Input	Low	System reset.
cmd[2:0]	Input	N/A	Command for controller.
datain[DSIZE-1:0]	Input	N/A	Data input. DSIZE is a programmable parameter of 32, 64 or 128.
addr[ASIZE-1:0]	Input	N/A	Address for read/write. ASIZE is based on size of memory, which is derived by the following formula: ASIZE = RANK_SIZE + RSIZE + BSIZE + CSIZE
dmsel[DSIZE/8-1:0]	Input	N/A	Data Mask select.
busy	Output	High	Busy signal indicates the controller will not accept any more commands.
dataout[DSIZE-1:0]	Output	N/A	Data out.
dataout_valid	Output	High	During a read, this signal indicates when the dataout bus from the controller contains valid data.
datain_valid	Output	High	This signal indicates when the user can start sending in data through datain bus during a write.

Timing Specifications

Figure 2. Generic I/F Timing Diagram for ORCA 4



cmd1 = read, cmd2 = write, bl =2

Figure 3. Read Followed By Read (Same Bank Same Row with BL = 2)

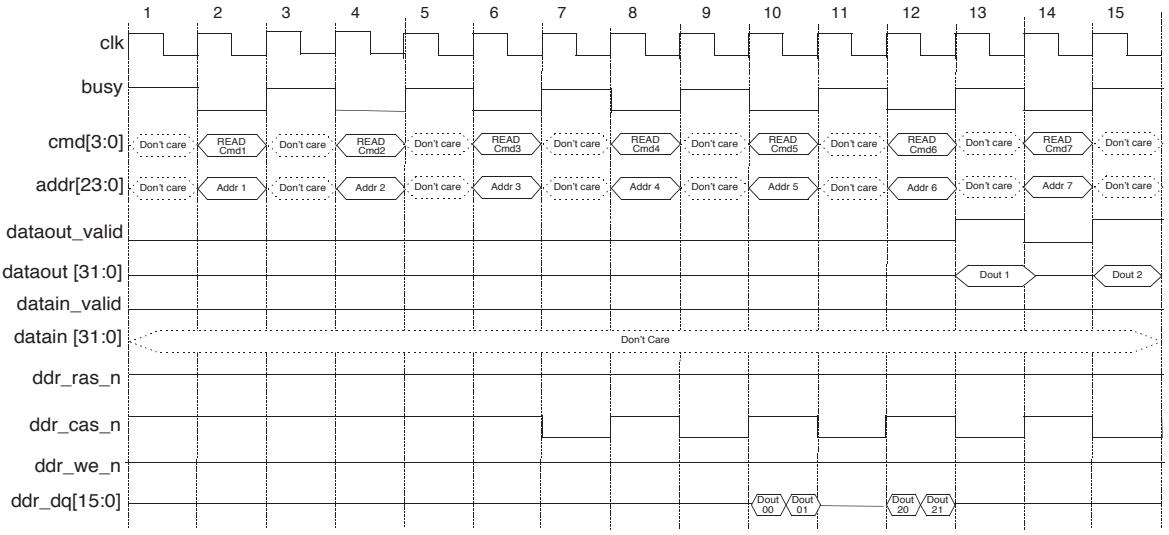


Figure 4. Read Followed By Read (Same Bank Different Row BL = 2)

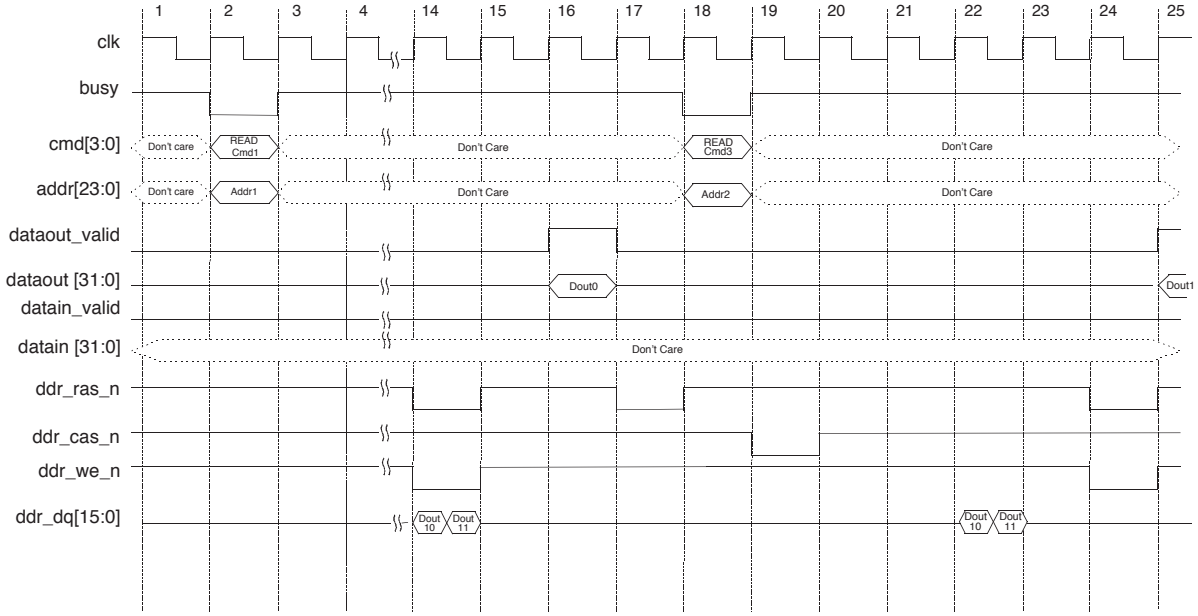


Figure 5. Read Followed By Read (Different Bank Row Open BL = 2)

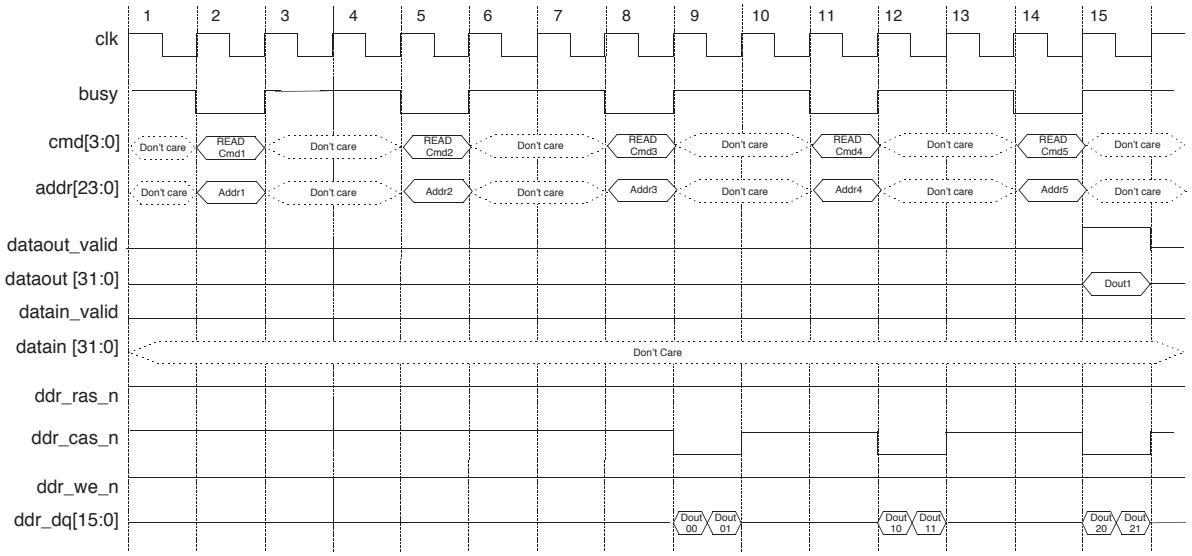


Figure 6. Read Followed By Read (Different Bank Row Closed BL = 2)

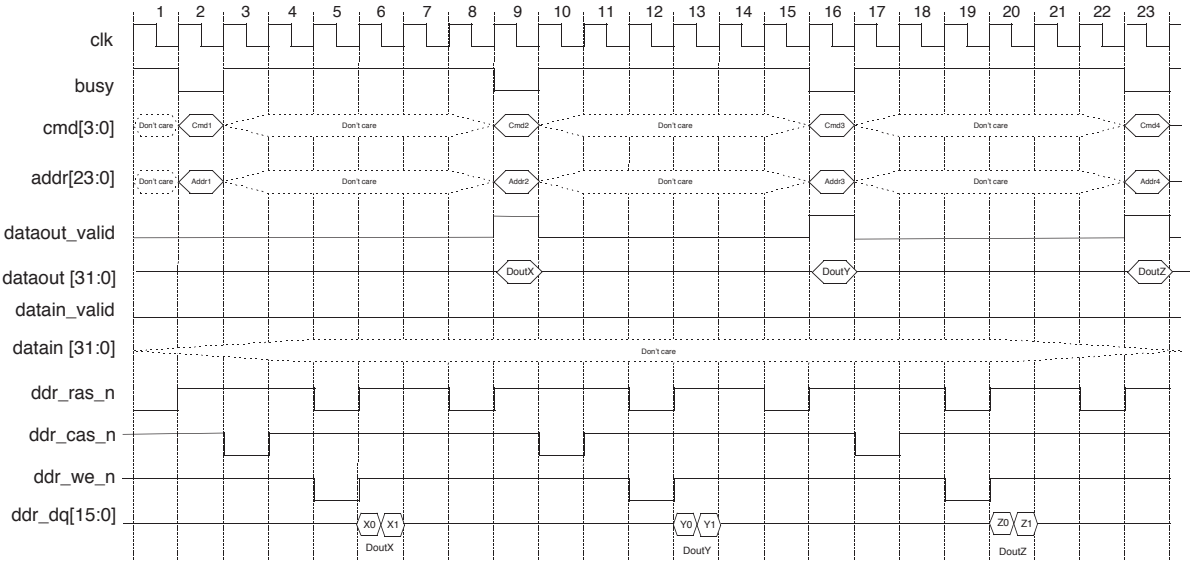


Figure 7. Read Followed By Read (Different Row Open Row Close BL = 2)

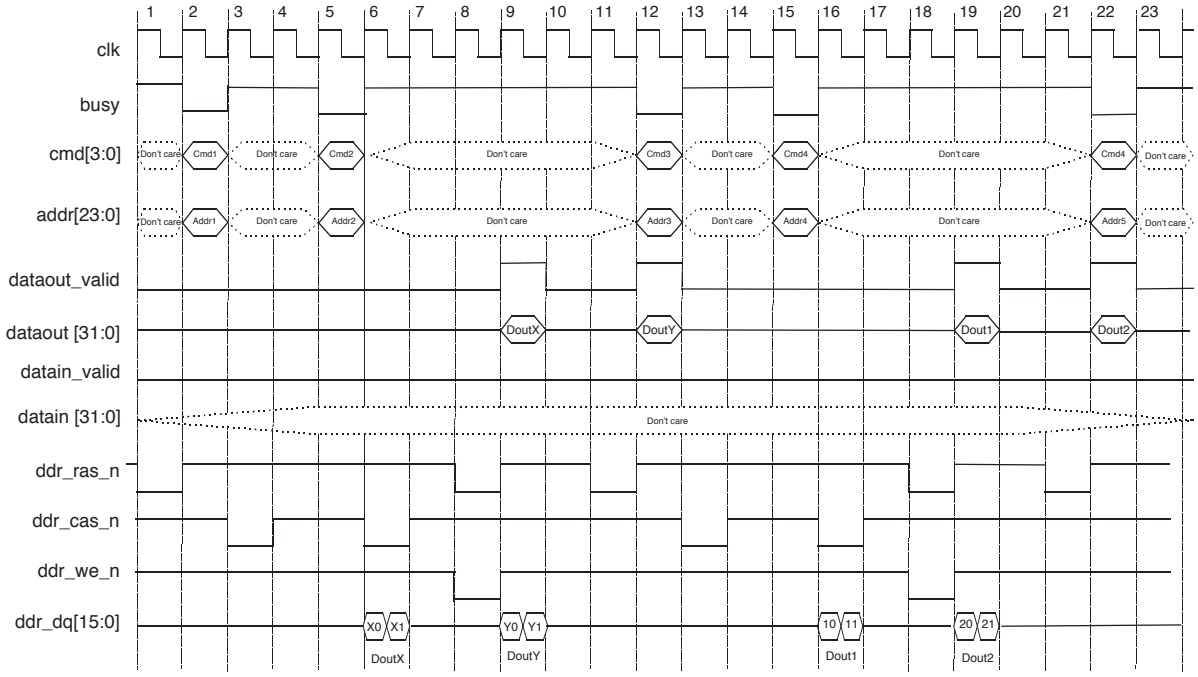


Figure 8. Write Followed By Write (Same Bank Same Row BL = 2)

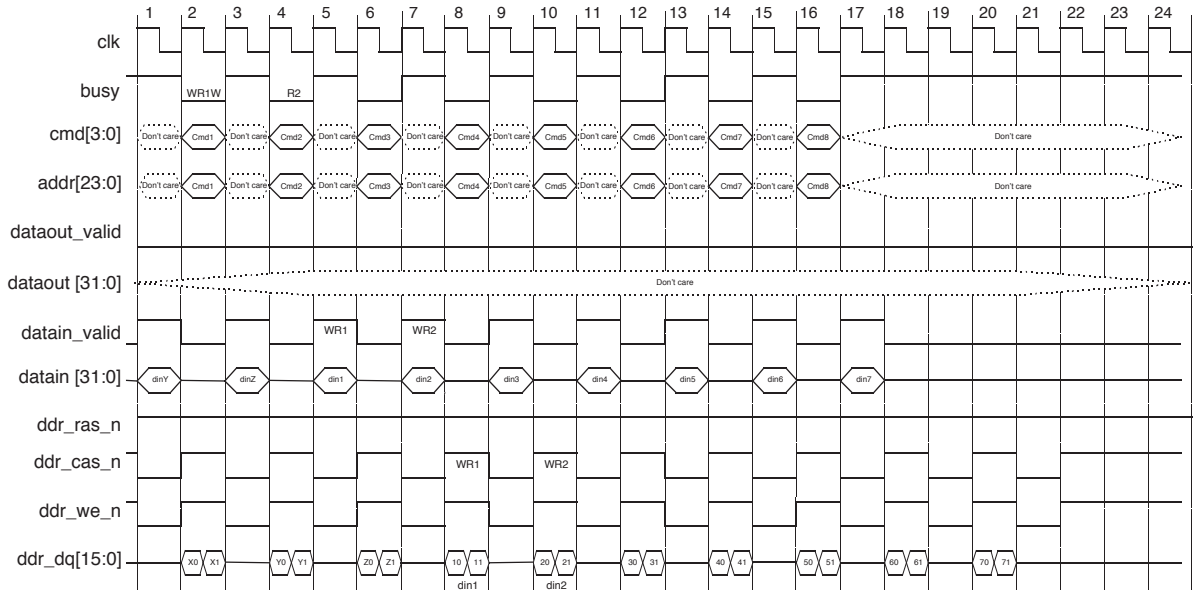


Figure 9. Write Followed By Write (Same Bank Different Row BL =2)

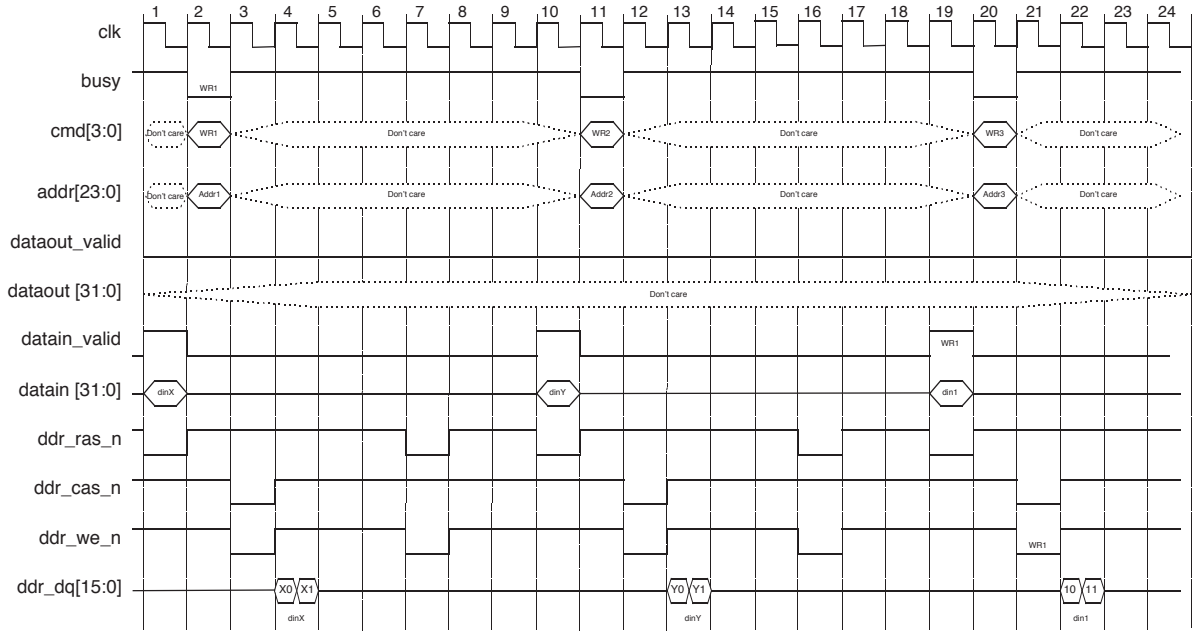


Figure 10. Write Followed By Write (Different Bank Row Open BL = 2)

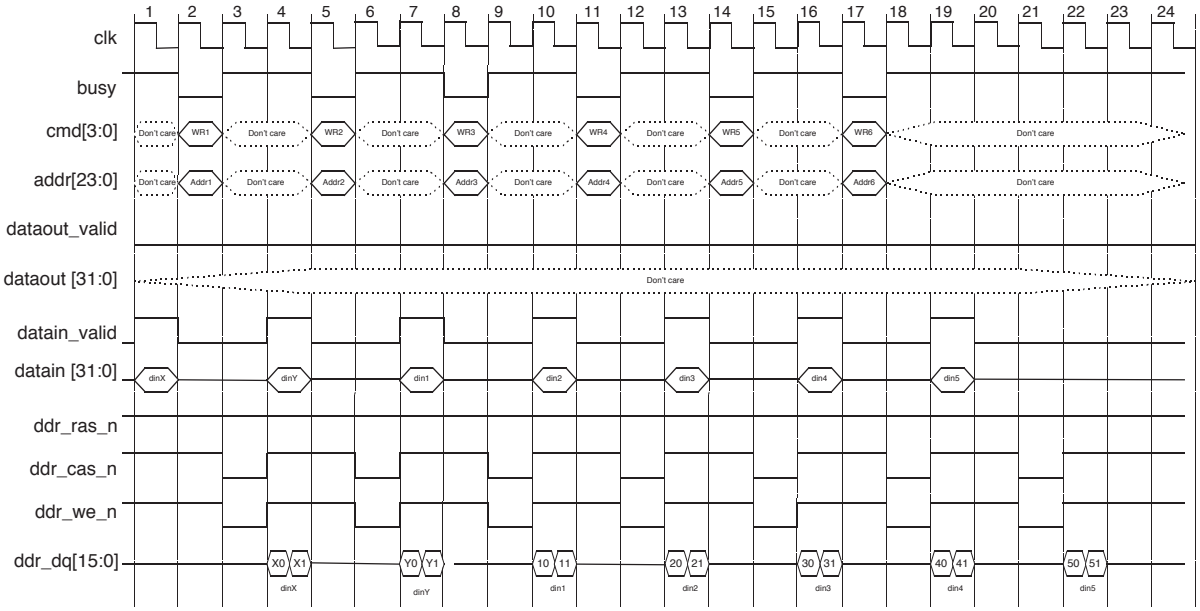


Figure 11. Write Followed By Write (Different Bank Row Close BL = 2)

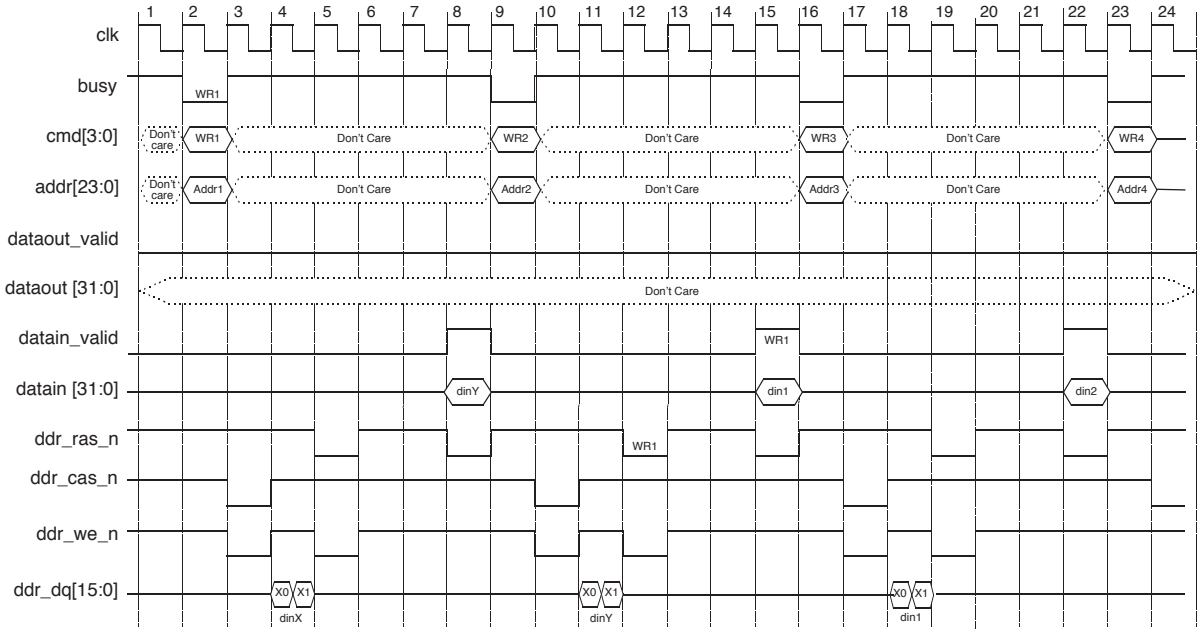


Figure 12. Write Followed By Write (Different Bank Row Open Row Close BL = 2)

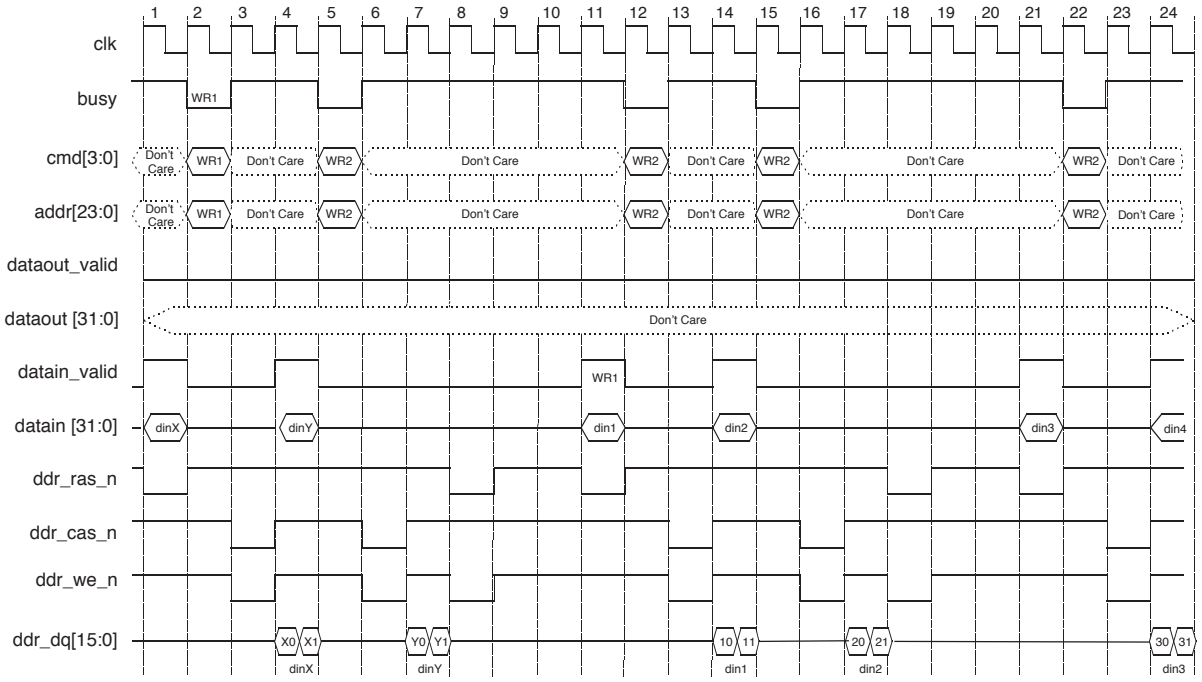


Figure 13. Power Down

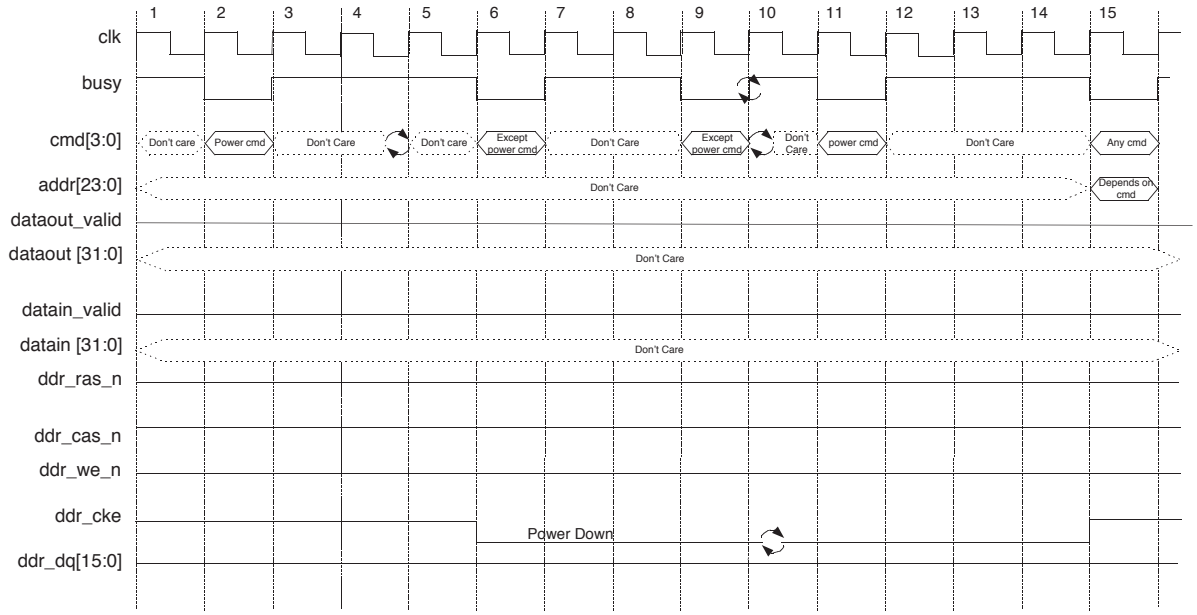
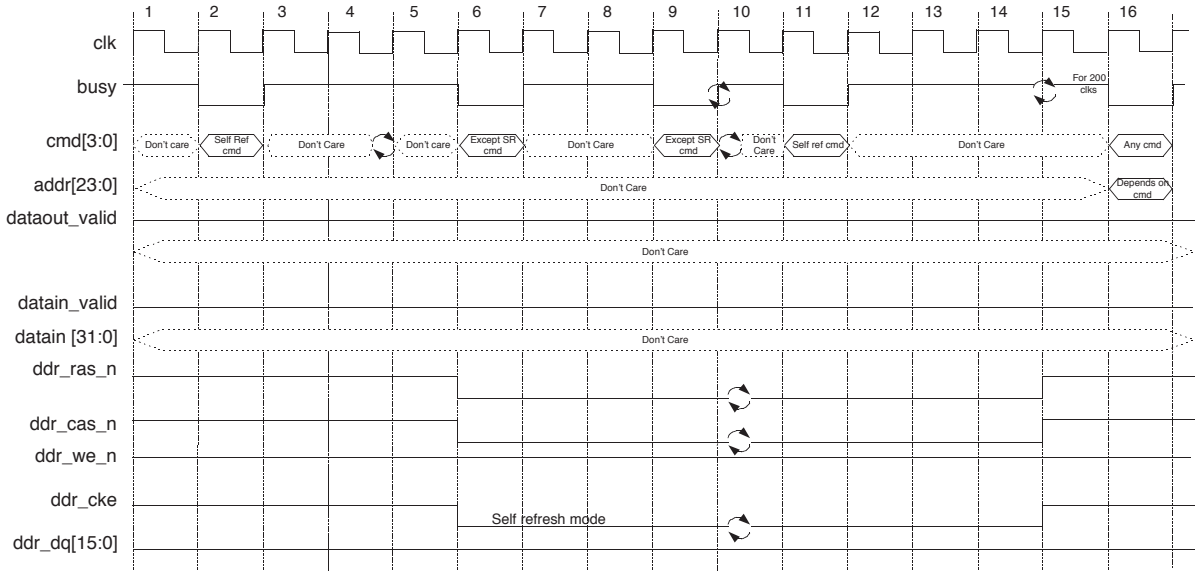


Figure 14. Self Refresh



Command Descriptions and Usage

This section describes the commands supported and their usage at the generic interface block.

NOP

This command is issued when the interface is waiting to issue commands. This command does not perform any operation on the DDR SDRAM.

Command Name	Cmd[2:0]	Addr['ASIZE-1:0]	
		Rank	Absolute Address
NOP	000	Rank Number	xxxx (Don't Care)

READ

This command is issued when a READ is required form a memory location. The address is comprised of rank number and absolute address. The absolute address is formed by the row, bank and column addresses.

This read command automatically applies ACTIVATE, READ and PRECHARGE commands to the DDR SDRAM by looking at the bank and row address.

Once a READ command is issued, the `dataout` bus will contain valid read data when the `dataout_valid` signal is high.

Command Name	Cmd[2:0]	Addr['ASIZE-1:0]	
		Rank	Row, Bank, Column
READ	001	Rank Number	Absolute Address

WRITE

This command is issued when a WRITE is required from a memory location. The address is composed of rank number and absolute address. The absolute address is formed by the row, bank and column addresses.

The WRITE command automatically applies ACTIVATE, READ and PRECHARGE commands to the DDR SDRAM by looking at the bank and row address.

After a WRITE command is issued, the controller accepts the data to be written from the `datain` bus when the `datain_valid` signal is high.

Command Name	Cmd[2:0]	Addr['ASIZE-1:0]	
		Rank	Row, Bank, Column
WRITE	010	Rank Number	Absolute Address

SELF REFRESH

The SELF REFRESH command is issued to retain the data in the DDR SDRAM. This can be issued even if the rest of the system is powered down. In this mode, the DDR SDRAM retains data without applying an external clock signal. During this command, the address is "don't care" since all the DDR SDRAM devices enter self-refresh mode.

Once the command is given, the DDR Controller enters the self-refresh mode. The DDR Controller will remain in this mode until another SELF REFRESH command is sent. All other user commands are ignored while the DDR Controller is in the self-refresh mode.

Command Name	Cmd[2:0]	Addr['ASIZE-1:0]	
		Rank	Row, Bank, Column
SELF REFRESH	110	xxxx	xxxx (Don't Care)

Load_MR

The Load_MR command is issued to program either the Mode Register or Extended Mode Register depending on the BA1:BA0 bits in the address.

BA1:BA0 = 00 Addresses the Mode Register

BA1:BA0 = 01 Addresses the Extended Mode Register

Once the Mode register is programmed, the CFG0 register in the controller is also updated

Command Name	Cmd[2:0]	Addr['ASIZE-1:0]			
		Rank	Addr['ASIZE-1:14]	Addr[13:12]	Addr[11:0]
Load_MR	100	xxxx	xxxx	BA1:BA0	A11:A0

POWER DOWN

The POWER DOWN command is issued to make the DDR SDRAM enter power down mode. The Controller automatically wakes up the DDR SDRAM, then puts the DDR SDRAM back into power down mode.

Once the command is given, the DDR Controller enters power-down mode. The power-down mode (and the DDR SDRAM) remains in power-down mode until another POWER DOWN command is sent. All other user commands are ignored while the DDR is in power-down mode.

Command Name	Cmd[2:0]	Addr['ASIZE-1:0]	
		Rank	Row, Bank, Column
POWER DOWN	101	xxxx	xxxx (Don't Care)

Load_CFG

The Load_CFG command is used to program the Controller CFG0, CFG1, CFG2 and CFG3 registers. The controller register is selected with the A1:A0 bits in the address as shown in the table below.

The Load_CFG command can be used before the initialization of the DDR Controller.

A[1:0]	Configuration Register Selected
00	CFG0
01	CFG1
10	CFG2
11	CFG3

Once the CFG0 is programmed, the Mode Register in the DDR SDRAM is also updated.

Command Name	Cmd[2:0]	Addr['ASIZE-1:0]			
		Rank	Addr['ASIZE-1:20]	Addr[19:2]	Addr[1:0]
Load_CFG	011	xxxx	xxxx	A[19:2]	A1:A0

The A[19:2] maps to the register (refer to the next section on Configuration Registers).

Configuration Registers

There are four Configuration registers in the DDR Controller: CFG0, CFG1, CFG2 and CFG3. These registers are selected using the Load_CFG command (see above). The A1 and A0 address bits determine the CFG register being addressed. A2 to A19 contain the data to be loaded into the selected register. See the description of the Load_CFG command for more information.

Configuration Register 0

The Configuration Register 0 (CFG0) is used to modify the DDR SDRAM Controller timing and behavior. Table 6 describes the contents of CFG0. When any change is made to this register, the DDR Controller automatically updates the DDR SDRAM mode register. The DDR SDRAM mode register is also updated when the DDR Controller receives a LOAD MODE REG command.

The user can program the `Burst Length`, `Burst Type`, and `CAS Latency` bits or use the default values without any programming.

After the power up condition is satisfied (all power supply and reference voltages are stable at approximately 200μs), the user triggers initialization of the DDR SDRAM by setting the INIT bit using the `Load_CFG` command. Once this bit is set, the controller starts the initialization process. The `busy` signal is held high until the initialization process is completed.

The default values for this register are set in the Verilog parameters file.

Table 6. Configuration Register 0 (CFG0)

Configuration Bits	Parameter	Description
CFG0[2:0]	Burst Length	Burst Length, valid values are 2, 4 and 8. 001b = 2 010b = 4 011b = 8 All others are reserved. Default value is `Burst Length` parameter.
CFG0[3]	Burst Type	Burst Type, Sequential / Interleaved 0 = Sequential 1 = Interleaved Default value is `Burst Type` parameter
CFG0[6:4]	CAS Latency	CAS Latency in number of clock cycles. 101b = 1.5 010b = 2.0 110b = 2.5 011b = 3.0 Default value is `CAS Latency` parameter
CFG0[7]	INIT	Initialize the DDR SDRAM when this bit is set. Default value is 0.
CFG0[19:8]	Reserved	These bits are reserved. Default value is unknown.

Configuration Register 1

The Configuration Register 1 (CFG1) is used to modify the DDR SDRAM Controller timing and behavior. The correct settings will depend on the DDR SDRAM being used with the controller. Table 7 shows the contents of CFG1.

Table 7. Configuration Register 1 (CFG1)

Configuration Bits	Parameter	Description
CFG1[2:0]	TRCD Delay	RAS to CAS Delay in number of clocks (maximum value 7 clocks). Default value is `TRCD Delay` parameter
CFG1[5:3]	TRRD Delay	Active bank A to active bank B command (maximum value 7 clocks). Default value is `TRRD Delay` parameter
CFG1[9:6]	TRFC Delay	AUTO REFRESH command delay period in number of clocks (maximum value 15 clocks). Default value is `TRFC Delay` parameter
CFG1[12:10]	TRP Delay	PRECHARGE Command period (maximum value 7 clocks). Default value is `TRP Delay` parameter
CFG1[15:13]	TMRD Delay	LOAD MODE REGISTER Command period (maximum value 7 clocks). Default value is `TMRD Delay` parameter

Table 7. Configuration Register 1 (CFG1) (Continued)

Configuration Bits	Parameter	Description
CFG1[18:16]	TWR Delay	Write recovery time (maximum value 7 clocks). Default value is TWR Delay parameter
CFG1[19]	Reserved	This bit is reserved. Default value is unknown.

Configuration Register 2

The Configuration register 2 (CFG2) contains the 16 bits used to store the Refresh Period (RP). The DDR Controller regularly issues AUTO REFRESH commands to the DDR SDRAM during normal operation mode. Table 8 shows the contents of CFG2.

Table 8. Configuration Register 2 (CFG2)

Configuration Bits	Parameter	Description
CFG2[15:0]	Refresh Period	Refresh Period (max. = t_{CK} * FFFFh). Default value is Refresh Period parameter.
CFG2[19:16]	Reserved	These bits are reserved. Default value is unknown.

Configuration Register 3

The Configuration register 3 (CFG3) is used to modify the DDR SDRAM Controller timing and behavior. The correct settings will depend on the DDR SDRAM being used with the controller. Table 9 shows the contents of CFG3.

Table 9. Configuration Register 3 (CFG3)

Configuration Bits	Parameter	Description
CFG3[3:0]	TRAS Delay	Active to pre-charge command (maximum value of 15 clocks). Default value is TRAS Delay parameter.
CFG3[6:4]	TWTR Delay	Internal write to read command delay (maximum value of 7 clocks). Default value is TWTR Delay parameter.
CFG3[10:7]	TRC Delay	Active to Active/AUTO REFRESH command delay period in number of clocks (maximum value of 15 clocks). Default value is TRC Delay parameter.
CFG3[19:11]	Reserved	These bits are reserved. Default value is unknown.

References

- DDR SDRAM Controller White Paper, Northwest Logic Design, Inc., 2000.
- DDR SDRAM Controller IP Data Sheet, Lattice Semiconductor Corp., 2001.
- Double Data Rate (DDR) SDRAM Data Sheet, Micron Technology, Inc., 2001.
- 128 M-bit Synchronous DRAM with Double Data Rate, NEC Corp., December 1998.
- DDR SDRAM Specification Version 0.3, Samsung Electronics, 2000.
- DDR SDRAM Controller Data Sheet, Lattice Semiconductor Corporation, 2002.
- ispLeverCORE™ Evaluation Tutorials, Lattice Semiconductor Corp., 2003.

Technical Support Assistance

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+1-408-826-6002 (Outside North America)
e-mail: techsupport@latticesemi.com
Internet: www.latticesemi.com

Appendix A. Specific Information for LatticeECP™ and LatticeEC™ FPGAs

DQS Detection Logic

Several signals are added to the DDR core for implementation on the LatticeECP/EC FPGAs. The DQS Detection circuit of the LatticeECP/EC devices requires the falling edge of internal signal `pio_read` to be placed within the preamble stage. It is also preferable that this falling edge be placed as early as possible in the preamble stage to account for the routing delays. The preamble state of the DQS can be detected using the CAS Latency and the round trip delay for the signals between the FPGA and the Memory device.

To place the falling edge as early as possible within the preamble state, the IP core provides `pio_read` signals with a quarter clock cycle phase difference between each other. The `pio_read` signal is generated on different phases of the clock so as to fall within the preamble window.

The signals `pio_read_dqs[0:7]` are added to the DDR core to designate the clock phase in which the `pio_read` signal will be generated. To ensure maximum flexibility in using the IP core, these signals are designed as inputs to the IP core that can be tied to desired values within the top level RTL file. The different phases of the clock can be set through four values as shown in the table below.

pio_read_dqs[0:7]	Direction	Value
`pio_read` generated on 90 deg phase shifted clk positive edge	Input	4'b0001
`pio_read` generated on clk negative edge	Input	4'b0010
`pio_read` generated on 90 deg phase shifted clk negative edge	Input	4'b0100
`pio_read` generated on clk positive edge	Input	4'b1000

Depending on the board design, if the round trip delay for the signals between the FPGA and the memory device is within one or more clock cycles signal `dvo_dly` (Data Valid Out Delay) needs to be set accordingly. The `dvo_dly` signal ensures that the read data valid signal (`dataout_valid`) will be generated after the correct delay by the IP. To ensure maximum flexibility in using the IP core, these signals are designed as inputs to the IP core that can be tied to desired values within the top level RTL file. The different values for signal `dvo_dly` are shown in the table below.

dvo_dly	Direction	Value
Less than or equal to 1 Clock Cycle	Input	2'b00
Greater than 1 Clock & Less than 2 Clock Cycle	Input	2'b01
Greater than 2 Clock & Less than 3 Clock Cycle	Input	2'b10
Greater than 3 Clock & Less than 4 Clock Cycle	Input	2'b11

Figure 15 shows the generic interface timing for the LatticeECP/EC devices. The timing for the `datain_valid` signal (marked with a * below) has been modified as it is used on the LatticeECP/EC implementation. The timing for all other signals remains unchanged compared to the ORCA 4 implementation shown in Figure 2.

In this LatticeECP/EC implementation, the IP will provide the active high `datain_valid` signal based on which the user presents the data "d0 and d1" on the "datain" bus on the NEXT clock cycle.

Figure 15. Generic I/F Timing Diagram for LatticeECP/EC