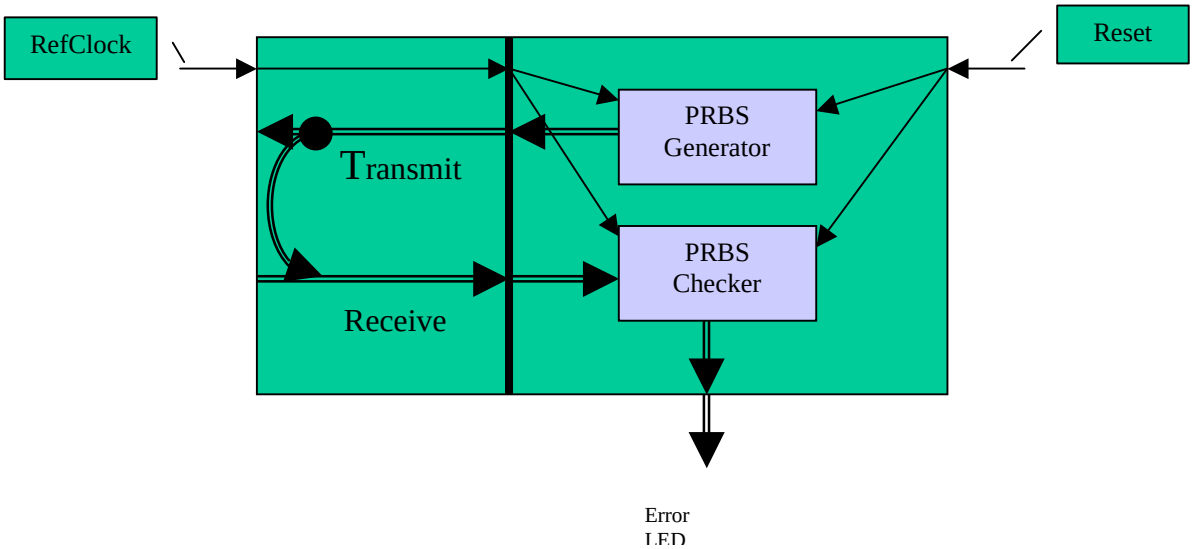
ORLI10G Evaluation Board Tutorial

Overview

This tutorial will assist first-time users of the ORCA ORLI10G how to use the evaluation board to understand the device features as well as the capabilities of the evaluation board. To use the tutorial, the user must have an installed copy of ORCA Foundry 2001 software and an understanding of the ORCA Device Programming Download Cable which is described in the Lattice Semiconductor technical note TN1009. Users should also reference the ORLI10G Evaluation Board Users Manual.

The tutorial and the supporting design files can be downloaded from the design tools section of the Lattice web site at http://www.latticesemi.com. The tutorial design was created for use as a template for future designs. This design includes simple pattern generation for the purpose of demonstrating the high speed interface from the XSBI core.



Getting Started

The following steps will make the proper board interconnections for power supplies, input signals, and output signals. Add push-on jumper shunts for the following.

Jumper	Pin	Pin
J53	3	5
J51	3	5
J59	3	5
J57	3	5
J55	3	5
J128	2	3
J130	2	3
J131	2	3
J71	1	2
J78	1	2
J77	1	2
J114	1	2
J113	1	2

- Connect a 0.025” square-pin receptacle patch cable(Pomona Electronics P/N 4741) between J5.1 and J16.1 http://www.pomonaelectronics.com/
- Connect 20 conductor IDT ribbon cable between J4 and J13
- Connect DB-25 connector of download cable to DB-9 adapter
- Plug DB-9 connector in a serial PC port(COM1or COM2)
- Connect J67 to +5VDC power pack
- Attach 300-pin MSA loopback PCB to CON1 receptacle.

Note: 644 MHz oscillator should be installed in socket Y8
All switches of SW3 should be in the ON position

Programming the Device

- Connect 8-pin dongle of download cable to J3
- Green LED on download cable should light
- From an MS-DOS command window (computer with ORCA Foundry 2001 installed)
  Type”devprog –c serial –p –j COM1(or 2) ORL!10G_eval_1.bit <enter>
  ORLI10G_eval_1.bit can be downloaded from the design tools section of the Lattice web site at http://www.latticesemi.com
- Download cable LED should illuminate yellow while loading
- Downloading bit stream
- D17 LED lights and download cable LED goes green

Functional Design Overview

This design uses a simple PRBS generator design in the FPOA logic that transmits the PRBS data out the XSBI high speed interface through the loop-back PCB and back into the receivers of the XSBI. The data is checked inside the FPGA logic by the PRBS checker logic. When no errors are present, the error flag which is connected to LED-D1 will not be illuminated. When an error is detected the LED will light. An error can be noticed if the loop-back PCB is removed.

- SW3 is used to select functions.
- SW3/2 is the control bit that selects between PRBS patterns or count patterns. SW3/2 should be OFF for PRBS. If SW3/2 is ON and the count pattern is running the checker always senses an error.
- SW3/3 is the checker enable bit and ON selects the checker to analyze the data.
- SW3/5 is the RESETN bit OFF holds logic in reset state.

Note: The push button of SW6 may have to be depressed when desynchronizing the high speed data.