



Lattice Propel 2026.1.1

Release Notes

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This document was created consistent with Lattice Semiconductor's inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice's inclusive language [FAQ 6878](#) for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

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About Lattice Propel™ 2026.1.1

Welcome to the Lattice Propel 2026.1.1 design environment for Lattice FPGA system design. Lattice Propel is a complete set of graphical and command-line tools to create, analyze, compile, and debug both FPGA-based hardware and software processor systems.

Tools and Enhancements

- Provides a Verification IP — AXI Manager BFM Lite Version:
 - AXI manager interface compliant with the AMBA 4 AXI Protocol
 - Single read/write transaction generation
 - Pipelined read/write transaction generation
 - Burst read/write transaction generation
 - Configurable address width (13–64 bits), ID width (2–11 bits), and user signal width (1–128 bits)
- Synchronizes device, IP, and Questa Sim libraries from Lattice Radiant software.
- Miscellaneous bug fixes.

Key Features

Device Family Support

Lattice LAV-AT (Avant™)
Lattice LFMXO5 (MachXO5™-NX)
Lattice LIFCL (CrossLink™-NX)
Lattice LFCPNX (CertusPro™-NX)
Lattice LFMNX (Mach™-NX)
Lattice LFD2NX (Certus™-NX)
Lattice MachXO3D™
Lattice MachXO2™
Lattice MachXO3L™
Lattice MachXO3LF™
Lattice ECP5U™
Lattice ECP5UM™
Lattice ECP5UM5G™
Lattice ECP3™
Lattice ICE40UP™
Lattice LN2-CT (Certus™-N2)
Lattice LFMXO4 (MachXO4™)
Lattice LN2-MH (Mach™-N2)

Processor Support

RISC-V Micro Controller (MC)
RISC-V State Machine (SM)
RISC-V Real Time OS (RX)
RISC-V NANO (NANO)

Operating System Support

Microsoft Windows 10 Enterprise (64-bit)
Microsoft Windows 11 Pro (64-bit)
Red Hat Enterprise Linux 8.10 (64-bit)
Red Hat Enterprise Linux 9.6 (64-bit)
Ubuntu 22.04 LTS (64-bit)
Ubuntu 24.04 LTS (64-bit)

Lattice Propel SDK

Integrated picolibc as the default standard C library to support three levels of printf.

Built-in industry standard components and tools for embedded software development and debugging.

Optimized project management flow for Lattice FPGA platform.

Supports creating both C and C++ software projects based on Lattice SoC platform.

Supports Lattice Diamond®, Lattice Radiant™, and Propel Builder bridges.

Integrated GNU Debugger (GDB) and Open On-Chip-Debugging (OCD) with chained JTAG.

Supports peripherals view with register description during debug session.

Supports syntax highlighting for various development languages.

Supports semihosting for On-Chip-Debugging and QEMU Virtual Platform.

Supports multiple channels for On-Chip-Debugging.

Supports “Attach to running target” for On-Chip-Debugging.

Supports user custom application templates.

Supports QEMU Virtual Platform.

Lattice Propel Builder

- Supports adding some Lattice Radiant foundation IP.
- Supports creating SoC and SoC verification project in project wizard Graphic User Interface (GUI).
- Supports Lattice Diamond, Lattice Radiant, QuestaSim, and Propel SDK bridges.
- Supports generating simulation environment, testbench, and script.
- Integrated QuestaSim Original Equipment Manufacturer (OEM).
- Supports creating more flexible AXI-based SoC.
- Supports reference IP RTL from user-specified library in IP Packager.
- Supports generation and reconfiguration of IP from centralized IP repository.
- Improved customized templates with constraint file included.
- Optimized warnings and disabled modifying Propel IP in Radiant software.
- Supports TCL in IP Packager.
- Supports GUI colour customization options for schematic.
- Supports a new entry to distinguish SoC creation from custom templates or built-in templates.
- Supports generating default value in top RTL file for AMBA4 interface dangling input ports.
- Supports DRC of cacheable address range on SoC including RISC-V RX processor.
- Supports DRC of connection compatibility between RISC-V RX processor and TCM.
- Supports Verilog/VHDL for RTL module of glue logic.
- Improved readability of Interface Type items in IP Packager GUI, such as Lattice External Flash Interface and AMBA AXI-4 Stream.
- Supports license debugger tool.
- Supports TCL mode entry for Builder and IP Packager.

IP Support

For IP support, refer to related IP user guides for detailed information.

SoC Template Design and System Simulation

- Provides Scalable RISC-V RX/MC/SM/Nano SoC template designs on the following devices: LAV-AT, LFCPNX, LFD2NX, LFMXO4, LFMXO5, LIFCL, LN2-CT, LatticeECP3, ECP5U, ECP5UM, ECP5UM5G, iCE40UP, MachXO2, MachXO3D, MachXO3L, and MachXO3LF.
- Provides CertusPro-NX template design, the *RISC-V MC Dual Processor Project*.
- Provides Avant template design, the *RISC-V MC Multi Processor Project*.
- Provides CertusPro-NX template design, the *Low Power Project*.
- Provides CertusPro-NX template design, the *RISC-V RX SHA-3 CXU Project*.
- Provides CertusPro-NX and Avant template design, the *JTAG Bridge Demo Project*.
- Provides MachXO3D template design *Lattice Sentry RoT Project*.
- Provides Mach-NX template design, the *Lattice Sentry RoT Project (484)* and *Lattice Sentry RoT Project (256)*.
- Provides *Empty Project* on all devices to build from scratch.
- Supports functional verification using system-level simulation environment for templates.
- Supports DUT with one-level sub SBX in verification project.
- Updated Simulation Tool.

Application Template Design

- Provides template design *Hello World Project*
- Provides template design *FreeRTOS-LTS PMP-Blinky Project*
- Provides template design *RISC-V RX Demo Project*
- Provides template design *QEMU_helloworld Project*
- Provides template design *Timing Profiling Project*
- Provides template design *Code Coverage Project*
- Provides template design *FreeRTOS-LTS minimal Project*
- Provides template design *I2C Communication Project*
- Provides template design *Mtimer Project*
- Provides template design *Hardware Interrupt Project*
- Provides template design *Real Timer Project*
- Provides template design *Software Interrupt Project*
- Provides template design *SPI Controller Project*
- Provides template design *Watchdog Timer Project*
- Provides template design *I3C Communication Project*
- Provides template design *General Purpose Timer Project*
- Provides template design *Bootloader Launch Firmware from SPI Flash Project*
- Provides template design *Bootloader Launch Firmware in XIP mode Project*

Release Contents

- Propel_2026.1.1.exe (Windows 10/11 64-bit Operating System)
- Propel_2026.1.1_lin.run (Red Hat Enterprise Linux 64-bit & Ubuntu LTS Operating System)
- Propel_2026.1.1_lin.md5 (Red Hat Enterprise Linux 64-bit & Ubuntu LTS Operating System)

Validated Boards in This Release

- AVANT-AT-E Evaluation Board (REV D P/N: LAV-E70-EVN-ES1)
- CertusPro-NX Evaluation Board (REV A P/N: LFCPNX-EVN)
- Certus-NX Versa Evaluation Board (REV B P/N: LFD2NX-VERSA-EVN)
- MachXO4 Development Board (REV A P/N: LFMXO4-110-ENV)

System Requirements

The basic system requirements for Lattice Propel 2026.1.1 on Microsoft Windows and Linux Operating System (OS):

- Windows 10/11 64-bit OS
- Red Hat Enterprise Linux 64-bit OS (RHEL8.10/9.6)
- Ubuntu 22.04/24.04 LTS OS
- Free Disk Space: approximately 12 GB
- Network adapter and network connectivity for IP server access

Known Limitations

This release of Lattice Propel 2026.1.1 has the following limitations:

- DUT with one-level sub SBX is with limited support in verification project.
- During GDB debugging, breakpoints outside the current active project may lead to unexpected breakpoint behavior.
- Opening a non-UART port with the terminal_cli tool can lead to unexpected results.
- Porting an SoC from one device to another may fail without manually adapting the TCL scripts.
- Encrypted VHDL IP is only supported in Lattice Radiant flow, but not in Lattice Diamond flow.
- The MAX_PATH inside Windows file I/O API is restricted to 260 characters, but the usable path is even more constrained. The MAX_PATH must contain the drive letter and the NULL character to terminate the string correctly.
- Current OpenOCD cannot read Float Point Unit (FPU) registers, which makes Propel SDK unable to show FPU related register values.
- Lattice Propel software does not support HW-USB-2A cable.

Known Issues

This release of Lattice Propel 2026.1.1 has the following known issue:

An invalid read error occurs during the QEMU launch, but it does not actually affect functionality.

Notes

- It is recommended to use the same version of Lattice Radiant and Propel software for best compatibility.
- RISC-V RX v2.7.0+ requires TCM v1.5.3+; all other combinations are unsupported.
- Balanced or advanced RISC-V RX core requires TCM with ATOMIC enabled. Lite RISC-V RX core requires TCM with ATOMIC disabled.
- With *Response to Write Error* enabled, the RISC-V RX core stalls on *AXI ID Width* mismatch. Suggest equalizing *AXI ID Width* when upgrading IPs.

Technical Support

- For assistance, submit a technical support case at www.latticesemi.com/techsupport.
- For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/en/Support/AnswerDatabase.
- Previous Lattice Propel software versions are available on Software Archive page on Company Public website: <https://www.latticesemi.com/Support/SoftwareArchive>.

Revision History

Revision 1.0, October 2026

Section	Change Summary
All	Production release.



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