

Lattice Radiant Known Issues

2026.1.1 Known Issues

The following are known issues for Radiant Software 2026.1.1. If no workaround is available, please contact Lattice Technical Support for further assistance.

Installation

Issue	Workaround	Affected Devices
Installer download may be blocked due to 7z security restrictions. Reference number: DNG-34722	Contact your network or security administrator with the download URL, file name, and error screenshot to request download approval. If the issue persists, contact Lattice Support for further assistance.	All devices

Bitstream

Issue	Workaround	Affected Devices
Flash Partition Capacity is Insufficient for Most Major Designs. Reference number: DNG-34032	When configuring the flash, use the CFG_EBRUFM/CFGUFM setting.	Lattice Avant (LAV-AT)

GUI

Issue	Workaround	Affected Devices
RAMW Instances Not Displayed in the Physical Designer Instance Tree. In Physical Designer, RAMW instances fail to appear in the netlist instance tree when expanding the hierarchy and cannot be highlighted in the floorplan view. Reference number: DNG-31731	None	All devices

Issue	Workaround	Affected Devices
Device Constraint Editor Prevents Simultaneous Editing of UserCode and Unique ID for MachXO4/MachXO4D Devices In the Radiant GUI (Device Constraint Editor), when the UserCode Format is set to HEX or Binary for MachXO4/MachXO4D devices, the Unique ID (TraceID) field becomes read-only. As a result, you cannot set both a custom UserCode and a custom Unique ID simultaneously through the GUI. Reference number: DNG-34458	For detailed guidance on the step-by-step documentation, please contact Lattice Technical Support.	MachXO4 (LFMXO4, LFMXO4D)

Place & Route

Issue	Workaround	Affected Devices
PAR Fails to Pack Design when set_false_path Constraints from MIPI CSI/DSI IP (v4.1.0) are Present, even with MAP Utilization Below 60%. On Nexus devices running Radiant 2026.1, PAR may not fit the designs into the device even when MAP reports utilization below 60%. This is caused by set_false_path constraints in the SDC file preventing registers from packing together, inflating the effective SLICE requirement. Reference number: DNG-33897	Remove the set_false_path constraints from the SDC file (timing results may differ after this change).	CrossLink-NX (LIFCL)
PAR Unable to Route High-Density MIPI Designs (≥20 Instances) on Avant Due to RCLK Region Constraint Violations. On Avant devices, PAR may fail in designs with high clock utilization due to Region Clock (RCLK) reachability and routing congestion constraints, resulting in errors such as RCLK '<clock_net>' cannot drive loads in CLKREG_<Region_B> or Design is unrouteable due to invalid placement or locked signals. Reference number: DNG-34109	None	Lattice Avant (LAV-AT)
Large Reset Fanout and Cross-Chip Reset Path Cause High-Frequency PAR Failures Reference number: DNG-33043	Instantiate local reset synchronizers or insert a balanced reset register tree across clock regions to duplicate reset signals and limit reset fanout within each local region.	Lattice Avant (LAV-AT)
Auto-Placer PAR Failure with Unconstrained Clock Pins Place and Route (PAR) can fail during placement if clock I/O pins are left unconstrained, as the implementation tool's auto-placer cannot automatically resolve valid device pin and clocking resource placement. Reference number: DNG-33668	Add a Clock IO location constraint.	CertusPro-NX (LFCPNX)
Place and Route Fails with Unrouted Signal Errors on High-Density Designs Due to Routing Congestion Under Tight I/O Timing Requirements Reference number: DNG-32999	Run Place and Route (PAR) with -hos (hold over setup).	All devices

Programmer

Issue	Workaround	Affected Devices
TraceID (Unique ID) Operations Unavailable for MachXO4 and MachXO4D Devices in Programmer In Programmer, TraceID (Unique ID) operations are unavailable for MachXO4 and MachXO4D devices. MachXO4 devices do not support TraceID programming, while MachXO4D devices do not support TraceID read or programming operations. Reference number: DNG-34342	1. Manually add the Display TraceID (ID 67) and Program TraceID (ID 27) operations to the MachXO4/MachXO4D device XDF file: data\vmdata\database\MachNG\ispVM_031.xdf 2. Restart Programmer after modifying the XDF file.	MachXO4 (LFMXO4, LFMXO4D)
Encrypted Multiboot from External SPI Flash May Fail for Alternate Images on LN2-CT-20 On the LN2-CT-20 device, encrypted multiboot from external SPI flash may fail when booting an alternate image because the default start addresses do not provide enough spacing for AES padding. Non-encrypted multiboot is unaffected. Reference number: DNG-34142	In Deployment Tool, move each alternate-image start address 5 sectors farther into the SPI flash than the default address. Regenerate the multiboot file, then erase, program, and verify the external SPI flash. This workaround applies to both AES encryption and AES with authentication.	Certus-N2 (LN2-CT-20)

Reveal

Issue	Workaround	Affected Devices
Post-PAR Reveal Debugging Is Not Supported When the LSE Synthesis Tool Is Selected in the Radiant Project In Reveal Inserter, setting the Debug Stage to Post-Place & Route for a design synthesized with Lattice Synthesis Engine (LSE) causes the Place & Route Reveal step to fail. The process reports the error "ERROR <35001355> - Cannot find reveal_workspace\tmpreveal\top_la0_trig_gen.v. File does not exist." even though the file is present, and no bitstream is generated. Reference number: DNG-33819	Select Synplify as the synthesis tool in the Radiant project for any Post-PAR Reveal debugging.	Mach-N2 (LN2-MH-20)

Power Calculator

Issue	Workaround	Affected Devices
MPPHY/MPPCIE Power Calculator Warning Messages in Legacy Projects	Regenerate all MPPHY and MPPCIE line items in Power	Lattice Avant (LAV-AT)

Issue	Workaround	Affected Devices
Opening older power projects (.pcf files) in Power Calculator may generate warning messages for MPPHY and MPPCIE because the power models were updated with new fields that are not automatically populated in legacy files. Reference number: DNG-34193	Calculator to populate the updated fields.	
Internal Flash Dynamic Power Estimation Displays Zero for LN2-MH-20 Devices Due to an Unassigned Supply Voltage Domain in the Device Power Model Reference number: DNG-33929	None	Mach-N2 (LN2-MH-20)
Power Calculator Reports Integer or Float Termination Key Warning Messages for Avant Designs Containing DDRPHY Blocks Reference number: DNG-33066	None	Lattice Avant (LAV-AT)
MPPHY Power Estimation May Be Incomplete for Avant FBG644 Devices Due to Incorrect MPP Tab Reporting In the Power Calculator, the MPP tab for Avant devices in the FBG644 package displays only MPQ0 and MPQ2, both showing 0.0% utilization. However, the generated power report indicates that a different quad (MPQ5) is in use. As a result, MPPHY power consumption may not be correctly accounted for in the power estimation. Reference number: DNG-34439	None	Lattice Avant (LAV-AT)

Simulation

Issue	Workaround	Affected Devices
Synopsys VCS Simulation Fails to Compile for Certus-NX Devices Due to Missing Library File When performing design simulation using Synopsys VCS, compilation fails for certain Certus-NX (LFD2NX) devices because the simulation library is missing the lifcl_sp.v source file. Reference number: DNG-33480	None	Certus-NX (LFD2NX)
VCS or Xcelium Simulation of LN2-CT Designs Containing MPPHY or MPPCIE Primitives Fails with an ELAB Error Due to Missing Library Modules. Reference number: DNG-33534	Use the ln2_mh device family instead of ln2_ct when running the cmpl_libs script.	Certus-N2 (LN2-CT)

Synthesis

Issue	Workaround	Affected Devices
LSE drops CDC_Register=1 attribute under the circumstance of EnableMux between CDC_Register and Driving_Register along with the presence of syn_preserve attribute. Reference number: DNG-33901	Apply set_max_constraint directly at the post-synthesis constraint processing stage.	Lattice Avant (LAV-AT)
Elaboration Fails Due to Invalid LUT4 Port Names from Synplify Pro. Invalid LUT4 port names in the Synplify Pro post-synthesis netlist cause elaboration to fail during Map. Reference number: DNG-33371	Modify the RTL assignment to avoid 4-input LUT inference by replacing the ternary assignment with either of the following: - assign stream_active = tx_protocol_datain_valid_i; - assign stream_active = 1'b1;	Lattice Avant (LAV-AT)
Synplify Pro Generates Warning FX310 During MachXO4 Design Synthesis Because the -dcc_insertion Option Is Ignored for Technologies That Do Not Support DCC Reference number: DNG-33496	None	MachXO4 (LFXM4)
Backward Retiming Is Not Performed on Register Paths in Synplify Pro, Resulting in Increased Logic Depth and Setup Timing Violations Reference number: DNG-33051	Apply the syn_retime_to_net attribute with the value BACKWARD to the affected register path: <pre>define_attribute {n:Backplane_TopLevel.Backplane_ X2XPlus.ZpuBlock\ .ZpuCore.un1_pc_r_1[14:0]} {syn_retime_to_net} {BACKWARD}</pre>	CertusPro-NX (LFCPNX)
Synplify Pro Register Retiming Causes False Setup Violations on Byte-to-Pixel (B2P) CDC Paths In Synplify Pro, enabling register retiming on designs containing the B2P IP renames and relocates synchronizer registers outside the IP hierarchy, causing internal clock-domain crossing (CDC) false path timing constraints to not match and resulting in false setup timing violations during timing analysis. Reference number: DNG-33305	Prevent the synthesis tool from retiming the synchronizer registers by using either of the following methods: Add Synthesis Directives to RTL/Constraints: Apply the syn_allow_retiming or syn_preserve attribute to the wc_pix_sync registers in the B2P RTL source or project .fdc constraint file:	Lattice Avant (LAV-AT) All Nexus devices

Issue	Workaround	Affected Devices
	<pre>/* synthesis syn_preserve=1 syn_allow_retiming=0 */</pre> 2. Modify Strategy Settings: In the Radiant Strategy settings under Synplify Pro, set optimization to Pipelining instead of Pipelining and Retiming to disable register retiming across the design.	
Lattice Synthesis Engine (LSE) Fails to Infer Packed-Struct Memory Arrays With Independent Byte-Field Write Enables as Block RAM (EBR), Resulting in Device Overutilization and Map Fitting Errors Reference number: DNG-34016	None	Lattice Avant (LAV-AT)
LSE Does Not Map Initial Register Values of '1' to Preset Registers Because the dolnitEval Device Capability Flag Is Disabled for All Devices Reference number: DNG-33872	None	All devices except iCE40
Synthesis of Long Priority-Encoder RTL With 16 or More Chained If/Else-If Conditions May Produce Incorrect Logic and Functional Failures Reference number: DNG-33871	Disable constant propagation using the -propagate_constants 0 option, or restructure the RTL to avoid a single chain of 16 or more sequential if/else-if conditions (for example, by using a case statement or splitting the logic into smaller blocks), which avoids the issue.	All devices
LSE Verific-Based Elaboration Falsely Rejects Legal Hierarchical RTL with Incorrect VDB-1011 Error Reference number: DNG-34071	Flatten the submodule logic into the top-level module by removing the hierarchy boundary at the affected instance. This allows elaboration to be completed successfully and avoids the false VDB-1011 error.	Lattice Avant (LAV-AT)

Timing Analysis

Issue	Workaround	Affected Devices
JTAG Timing Paths Missing in Timing Analysis	If Reveal insertion causes hardware failures despite timing closure in Radiant, rerun Place and Route (PAR) with a different	All Nexus devices

Issue	Workaround	Affected Devices
In Timing Analysis, paths between TCK and the internal JTAG interface are not analyzed or reported, potentially resulting in hardware functional failures even when no timing violations are reported. Reference number: DNG-33306	placement seed, as changing the seed may produce an implementation that functions correctly on hardware.	
help * Output Does Not Identify Legacy TCL Commands In Timing Analysis, the TCL command help * lists legacy commands (sta_get_clocks, sta_get_info, sta_get_terms, and sta_path_info) alongside their replacements without identifying them as legacy. However, the legacy notice is displayed when help is run on each command individually. Reference number: DNG-34147	None	All devices

IP Foundation

Issue	Workaround	Affected Devices
GDDR Timing Regression Due to Map Changes Designs utilizing the GDDR IP may observe timing regressions (such as hold violations between the synchronization clock and output clock domains) due to Map changes. Reference number: DNG-33930	None	CertusPro-NX (LFCPNX)
PMI/LSC FIFO in First-Word Fall-Through (FWFT) Mode Prematurely Asserts Empty Flag Reference number: DNG-33899	Disable first-word fall-through mode in the FIFO configuration and allow one extra cycle of read latency in the receiving logic.	Lattice Avant (LAV-AT) All Nexus devices
FIFO_DC Reports Incorrect Empty Status with FWFT=1 Across Asynchronous Clock Domains When using the FIFO_DC module with First-Word Fall-Through enabled (FWFT=1) across asynchronous clock domains during concurrent read and write operations, the empty flag can remain asserted even when data is available in the FIFO. Reference number: DNG-25191	- In the FIFO_DC module configuration, enable the almost_empty flag with a deassertion level set to 2 or higher. - In your design logic, use the almost_empty signal as the read-enable condition instead of the empty flag.	Lattice Avant (LAV-AT) All Nexus devices

Known Issues from Earlier Releases

GUI

Issue	Workaround	Affected Devices
Radiant 2026.1 and the 2026.1 Standalone Tools Cannot Be Uninstalled Using the Windows Add or Remove Programs Interface. Reference number: DNG-33155	To uninstall Radiant 2026.1 or 2026.1 standalone tools (such as Reveal Analyzer, Programmer, or Power Calculator), navigate to the installation directory and run uninstaller.exe.	All devices
Intermittent Radiant Crash when Launching Device Constraint Editor. Radiant may intermittently crash when launching the Device Constraint Editor (DCE) or when a design compilation is triggered from the DCE, due to a race condition when loading device data files (GUI). Reference number: DNG-28678	Close the Device Constraint Editor before starting design compilation. If the crash occurs during DCE launch, re-launch Radiant and try again.	All devices

Timing Analysis

Issue	Workaround	Affected Devices
Hold Time Violations May Occur in LAV-AT Designs When Using the MPPHY Module. Radiant software automatically inserts LMMI arbiter logic to enable access to the MPPHY LMMI interface. This implementation introduces a LUT4-based clock multiplexer in the LMMI clock path to enable Reveal Controller access to the MPPHY LMMI interface. The additional LUT4 logic can introduce significant clock skew, which may result in hold time violations in user designs. This issue applies to the following Lattice IPs that incorporate the MPPHY module: • DisplayPort IP • JESD204B IP • PCIe x8 IP • Ethernet IPs (Tri-Speed, 2.5G, 5G, 10G, and 25G) Reference number: DNG-29323	Try running your design using different Lattice Radiant tool settings such as Impose Hold Timing Correction or seeds. For further assistance, contact Lattice support. For the latest update, refer to the Lattice Knowledge Base article.	Lattice Avant (LAV-AT)
Missing Timing Arcs for JTAG Primitive May Cause Functional Failures on Nexus Devices.	If functional failures are seen when using Reveal or other modules that include the JTAG block, and timing	All Nexus devices

Issue	Workaround	Affected Devices
Timing Analysis may not report timing violations for designs using the JTAG interface on Nexus devices because timing arcs for the JTAG primitive are incomplete, which may lead to functional failures on the hardware even when timing analysis reports no violations. Reference number: DNG-32467	analysis does not report violations, re-run Place and Route with a different placement seed, as changing the seed may result in the design passing on hardware.	
Timing Analysis Reports Incorrect Delay Values for Certain DELAYA Paths. The timing model for certain DELAYA paths contains incorrect delay values (~6 ns vs. the expected 0.4–1 ns range), causing Timing Analysis to report false timing violations on designs that use these paths. Reference number: DNG-29460	Set the affected DELAYA timing paths as false paths.	Certus-NX (LFD2NX)
Timing Fails After Relaxing IO Slew Rate Constraint. In Place and Route, changing an output IO's slew rate from FAST to MED increases the clock path delay significantly, causing hold violations that the router attempts to fix by detouring data paths, which in turn degrades setup timing and results in setup failures. Reference number: DNG-29537	None	CrossLink-NX (LIFCL)
Spurious Hold Timing Failure on D-PHY RX Internal Path. When using the CSI-2/DSI D-PHY Receiver IP on Nexus devices, Timing Analysis reports a spurious hold timing violation on an internal path from INLP to LSR, because the IP's embedded false path constraint does not take effect. Reference number: DNG-30147	Add the following false path constraint in the physical design constraints (.pdc) file using the full hierarchical net and pin path: <pre>set_false_path -through [get_nets -hierarchical {mipi_rx_inst/u_dphyrx_ip/ls cc_dphy_rx_inst/ NOCIL_TOP. u_dphy_rx_core/rx_global_c trl_inst/ LP_HS_CLK_CONTROL.lp _hs_ctrl_clk/ lp11_reset_n_i}] \ -to [get_pins - hierarchical {mipi_rx_inst/u_dphyrx_ip/ls cc_dphy_rx_inst/ NOCIL_TOP.u_dphy_rx_cor e/ rx_global_ctrl_inst/ LP_HS_CLK_CONTROL.lp _hs_ctrl_clk/ hs_en_o.ff_inst/LSR}]</pre>	All Nexus devices
DELAYE Used on a Clock Path Can Cause the Delayed Output to be Stuck Low in Hardware. For Avant devices, a design that routes a clock through a DELAYE element to drive a delayed output can result in the delayed output pin being stuck low in hardware, even though post map and post PAR simulation waveforms appear correct. The issue is related to an incorrect DELAYMUX selection for the DELAYE path in the generated bitstream.	None	Lattice Avant (LAV-AT)

Issue	Workaround	Affected Devices
Reference number: DNG-31260		
Maximum Slack Limit Option in Timing Analyzer Has No Effect on Reported Paths. In the Timing Analyzer, the Maximum Slack Limit setting is currently non functional. Paths are reported regardless of the configured slack limit. Reference number: DNG-30518	None	All devices
Changing VCC in DCE and Standalone Timing Analyzer Does Not Affect Hold Analysis. Hold Analysis Always Uses VCC Max for Analysis. Reference number: DNG-29957	None	All devices
Radiant Timing Analysis for Designs Using LMMI_CLK / LMMI_CLKO May Show: - A missing timing arc from OSCA to CONFIG_CLKRST_CORE on the LMMI clock path (this is a bug). - A 0 ns net delay from CONFIG_CLKRST_CORE to CONFIG_LMMI (this is expected behavior per the current timing model). As a result, the report may present a direct path from the OSC IP to CONFIG_LMMI without explicitly reflecting the expected clock path delay from LMMI_CLK to LMMI_CLKO (i.e., OSCA → CONFIG_CLKRST_CORE). Reference number: DNG-27889	None	CertusPro-NX (LFCPNX)
Standalone Timing Analyzer Results May Differ from Runsta Results Even When Using the Same Pdc File. The results from RunSTA are correct. Reference number: DNG-27523	None	Certus-NX (LFD2NX)

Bitstream

Issue	Workaround	Affected Devices
SEDC May Fail to Detect Errors After 1-Bit or 2-Bit SEI Bitstream Injection on Avant Devices. Some 1-bit and 2-bit Soft Error Injection (SEI) bitstreams do not function correctly on Avant devices. After the SEI bitstream is injected, the Soft Error Detection and Correction (SEDC) logic may fail to detect the injected error, report an incorrect error bit location, or return zero for the error bit location. The error frame location is typically reported correctly. The failure pattern depends on the target block (PFU, DSP, routing, or mixed-block injection). Reference number: DNG-26267	None	Lattice Avant (LAV-AT)
SEI Bitstream Error Bit and Region Locations May Differ Between Hardware and Software on Avant Devices.	None	Lattice Avant (LAV-AT)

Issue	Workaround	Affected Devices
When using Soft Error Injection (SEI) bitstreams for Soft Error Detection and Correction (SEDC) testing, the error bit location and error region location reported by the hardware do not match the values specified by the software-generated SEI bitstream profile. The error frame location is reported correctly. Reference number: DNG-26257		
Bitstream Generation Produces Incorrect Configuration for Designs Using IMON with DelayC. Bitstream Generation may produce an incorrect bitstream for designs that use IMON (current monitoring) with DelayC on LIFCL devices. In such cases, the MIBMEM_56/MC1_SEL_FINE_DELAY_CODE_REG_OR_BYPASS_ENABLE_A setting may not be properly enabled, which can lead to device hardware failure. Reference number: DNG-32594	None	Certus-NX (LFD2NX), CertusPro-NX (LFCPNX), CrossLink-NX (LIFCL)
UFM JED File Cannot Be Generated for MachXO5-NX Devices In the Deployment Tool (Bitstream Generation), the UFM-specific JED file cannot be generated for LFMXO5-35/T and LFMXO5-65/T devices, preventing users from programming user data to the internal flash using a UFM JED file. Reference number: DNG-32987	None	MachXO5-NX (LFMXO5)
Using Distributed RAM (DPRAM) for a Shift-register Path That Feeds a Delay Element Can Cause the Delay Element Output to Behave Incorrectly. With syn_keep or syn_preserve applied to the shift array, simulation shows glitches, and Reveal capture shows unintended or corrupted data. The problem is observed in both pre synthesis and post synthesis Reveal. Reference number: DNG-29618	• Avoid DPRAM for the shift chain feeding the Delay Element. Use EBR or PFU registers for the shift register resource. ○ In IP configuration, select EBR or Registers as the resource. ○ For inferred RTL, guide synthesis to map to block RAM or registers (e.g., set ramstyle to block RAM or registers in your synthesis attributes). • If you must use DPRAM: ○ Keep the shift depth ≤ 32 where practical to reduce risk. ○ Remove syn_keep and syn_preserve on the internal shift array when not strictly required or apply them at module boundaries instead of the array element level.	Lattice Avant (LAV-AT-E70)

Issue	Workaround	Affected Devices
	Reverify with simulation and Reveal after changing the resource selection. Designs using EBR or PFU registers do not show the issue.	
Avant Bitstream Generation May Consume Significantly More Host Memory Than Reported. During bitstream generation for Avant devices, the Bitgen process may consume significantly more system memory than the reported peak memory usage. This can result in unexpected host memory pressure and, in some cases, out of memory failures. Reference number: DNG-29447	- Run Bitgen on hosts with additional available RAM. - Do not rely on the reported peak memory usage values. - Prefer machines with larger memory capacity or Linux hosts for improved stability.	Lattice Avant (LAV-AT)

Synthesis

Issue	Workaround	Affected Devices
Synplify Pro May Ignore SDC create_clock Constraints in Designs Using PLLs. In Synplify Pro, create_clock constraints defined in an SDC file may not be recognized for designs that use one or more PLLs, resulting in near-zero timing constraint coverage. The same constraints are recognized correctly when using the Lattice Synthesis Engine (LSE). Reference number: DNG-25214	None	All devices
Synplify Pro Does Not Correctly Apply the add_delay Option for set_output_delay and set_input_delay Constraints. Synplify Pro does not correctly apply the add_delay option for set_output_delay and set_input_delay constraints when multiple clocks are defined, resulting in incorrect timing analysis results. Reference number: DNG-31290	Ensure that constraints are defined in the correct order within the SDC file.	All devices
Synplify Pro May Not Infer IO Registers When syn_useioff Is Applied Directly to Top-Level Ports. When using Synplify Pro for synthesis, applying the syn_useioff attribute directly on top-level ports may not infer IO registers, which is a change in behavior compared to previous Radiant releases. Reference number: DNG-32343	Apply the syn_useioff attribute on intermediate signals instead of directly on top-level ports.	CrossLink-NX (LIFCL), Lattice Avant (LAV-AT)
Synplify Pro Ignores the syn_useioff Attribute in User VHDL Code. In certain VHDL designs, Synplify Pro does not pack registers into I/O pad cells when the syn_useioff attribute is specified. As a result, the Map report	Apply the syn_useioff attribute directly to the I/O signals.	CrossLink-NX (LIFCL)

Issue	Workaround	Affected Devices
indicates zero input/output I/O registers used. In contrast, LSE recognizes and applies the attribute as expected. Reference number: DNG-30879		
Synplify Pro Does Not Report an Error When Memory Initialization File Is Missing. Synplify Pro in Radiant reports missing data files used by readmemh/readmemb as warnings instead of errors. Due to the large number of synthesis warnings, this can be easily overlooked and may lead to incorrect results. Reference number: DNG-31492	Explicitly provide the data file specified in readmemh (or readmemb). Also, monitor warning message WARNING <2012641> - CG371: Cannot find data file ... for task \$readmemh and add the missing data file if it appears.	All devices
SDC set_multicycle_path -setup Constraint Dropped when Using Encrypted IP. When using Synplify Pro, a set_multicycle_path -setup constraint defined in the SDC file is dropped during post-synthesis constraint processing when the target paths reside inside an encrypted IP block, while the corresponding -hold constraint is preserved. Reference number: DNG-31443	Define the multicycle path constraints in the physical design constraints (pdc) file instead of the SDC file, as PDC constraints are applied after mapping when the encrypted paths become visible.	CertusPro-NX (LFCPNX)
You May Encounter a Large RAM DP True Synthesis Error When Port B Byte Enable is Used. The Large RAM DP True (LRAM_DP_TRUE) IP can fail synthesis when Port B byte enable is enabled with 16-bit data width and output registers on both ports. The generated RTL creates an invalid ben_b_w part select, leading to errors such as index out of range and multiple non tristate drivers on ben_b_i[1]. Reference number: DNG-31307	Do not use LRAM_DP_TRUE with byte enable enabled on both ports and output registers enabled on both ports. If the design allows, temporarily disable byte enable or the output register on one or both ports. If you must use this configuration, a temporary RTL edit can be used: locate the generated RTL file for the instance, find the assign statement that defines the overflow padding for ben_b_w, and modify it to remove the extra +1 and match the ben_a_w form, for example: <pre>assign ben_b_w[(BWID_B - 1):(BYTE_WIDTH_B - (BWID_B * i1))] = {(BYTE_WIDTH_B - (BWID_B * i1)){1'b1}};</pre> Then rebuild the project using the edited RTL.	Certus-NX (LFD2NX)
There Are Missing AXI4 Lite Constraints When Using Encrypted IP for Avant Devices. For encrypted AXI4 Lite IP used with Avant devices in Radiant 2025.2, some dpram related false path constraints are not applied, causing hold timing	Update the AXI4 Lite constraints to replace the encrypted portion of the instance path (for example gen_pmi.gen_async.u_fifo)	Lattice Avant (LAV-AT)

Issue	Workaround	Affected Devices
violations. The same constraints are applied correctly, and timing violations do not occur when using the unencrypted IP with the same configuration. Reference number: DNG-29853	with a wildcard (/*) so the constraints match the renamed instances in the encrypted IP. Use this with care to avoid unintentionally setting false paths on other parts of the design.	
LOC Attribute May Be Ignored for Output Ports Declared as Reg When Using Synplify Pro. In Synplify Pro, a LOC attribute attached to an output port declared as a reg and driving a flip flop can be ignored. As a result, PAR may place the output on a different package pin than specified by the LOC. The issue is not seen with LSE or when the output is declared as a wire with the LOC on the IO net. Reference number: DNG-30603	None	MachXO5 (LFMXO5)
When the Width of ROM Data in a Memory Initialization File is Wider Than the Defined ROM Width, Radiant Issues Warnings and Ignores the Extra Bits. The synthesis engine treats these extra bits as don't-care values and ROM module may be optimized away during synthesis. In contrast, Diamond enforces strict consistency between the ROM width and the initialization file width, resulting in an error instead of continuing. Reference number: DNG-29440	- Ensure that the memory initialization file width matches the ROM width defined in your design. - Treat Radiant warnings (e.g., CG1194, CG532, MO156) as critical and correct the file before synthesis. - If strict error handling is required, add a manual check in your design flow to validate memory file widths.	MachXO4 (LFMXO4)
LSE Synthesis May Fail When Crc_register Attribute is Used with an Error: "Cdc_register Chain Cannot Be Fully Determined for Register...". Reference number: DNG-29431	None	All devices
Designs Using Nested VMs Fail During Post-Synthesis. Reference number: DNG-27317	None	Lattice Avant (LAV-AT)
When Using Synplify Pro, User-Defined Create_Generated_Clock Constraints in the SDC File for PLL Clock Outputs May Be Overwritten by Auto-generated PLL Clock Constraints if a Reveal Core is Added to the Design. Without Reveal, user-defined constraints propagate correctly through synthesis and implementation. With Reveal present, the constraints are accepted during Constraint Propagation Engine (CPE) but fail to persist after synthesis. Reference number: DNG-26270	- Define PLL clock constraints in the PDC file instead of SDC. PDC constraints are preserved even when Reveal is added. - If SDC-based constraints are required, use post-synthesis Reveal debug flow.	CrossLink-NX (LIFCL)

Issue	Workaround	Affected Devices
Synplify Pro Synthesis May Fail If The .Sdc File Contains a User-defined Constraint Referencing a Hierarchical Object That Includes a Dot (.). Example: Top.Inst/Out. Reference number: DNG-20134	- Create the constraint in the .pdc file instead of .sdc file. - Use LSE for synthesis.	CrossLink-NX (LIFCL)
Synthesis Fails When Migrating pmi_ram_dp_true from MachXO3L to MachXO4 A design originally targeting MachXO3L in Diamond (using SynplifyPro) synthesizes successfully, but after migration to Radiant for MachXO4 (using the official migration tool), synthesis fails with an error about multiple write clocks in the RAM instance. The same synthesis tool (SynplifyPro) is used in both flows, but only Radiant reports an error. Reference number: DNG-31065	None	MachXO4 (LFMXO4)
LSE Resource Sharing Can Cause Mismatches Between RTL Simulation and Synthesized Behavior on Certus-NX Devices. When using LSE synthesis with resource sharing enabled on Certus NX devices, RTL simulation may pass, but post synthesis simulation and hardware behavior may not match the RTL. This mismatch is not observed when LSE resource sharing is disabled or when using Synplify Pro for synthesis. Reference number: DNG-30896	Disable LSE resource sharing (set Resource Sharing to FALSE in the LSE strategy) or use Synplify Pro for synthesis.	Certus-NX (LFD2NX)

Power Calculator

Issue	Workaround	Affected Devices
Power Calculator Reports 100 Percent Utilization for MPPHY with Partial Lane Usage. The Power Calculator displays 100 percent resource utilization for an MPPHY when fewer than all four lanes are in use. The displayed value does not reflect the actual percentage based on the number of lanes used. For example, using three of four lanes shows 100 percent instead of the expected 75 percent. Reference number: DNG-23785	None	Lattice Avant (LAV-AT)
Power Calculator Reports Incorrect Available MPPHY Quad Count for LAV-AT-X70 FBG644 Package. The Power Calculator MPPHY tab reports an incorrect number of available MPPHY Quads for the LAV-AT-X70 FBG644 package. For example, MAP reports that 2 MPPHY Quads are available for this package, but the Power Calculator displays 7, which is incorrect. Reference number: DNG-32825	None	Lattice Avant (LAV-AT-X70)

Issue	Workaround	Affected Devices
Power Calculator Does Not Constrain RAMX16/RAMX32 Count by Existing LUT Usage. In the Power Calculator estimation mode, the maximum allowable count for RAMX16 and RAMX32 entries is not adjusted based on existing LUT usage for Avant and Khronos devices, allowing users to enter RAM values that exceed the device's actual available resources and producing misleading power estimates. Reference number: DNG-31896	None	Lattice Avant (LAV-AT)
Power Calculator Selects Incorrect Default Device for Unsupported Avant PLC L-Variant. When loading a Power Calculator project file (.pcf) that targets an Avant PLC L-variant device into a Radiant version released before the device is enabled, the Power Calculator silently selects a different default Avant device without issuing a warning, resulting in incorrect power estimates. Reference number: DNG-32443	None	Lattice Avant (LAV-AT)
Power Calculator DDRPHY Tab Activity Inputs Use AF And EF Instead of RX/TX/IDLE. In the Power Calculator DDRPHY tab, the AF and EF fields are still displayed instead of the RX percent, TX percent, IDLE percent, and data_H/data_L percentages. The RX, TX, and IDLE percentages must sum to 100%. Reference number: DNG-31469	None	Lattice Avant (LAV-AT)

Simulation

Issue	Workaround	Affected Devices
ECO Does Not Update RAM_DP Memory Content Correctly When Using Byte Enable with Byte Size 8. ECO flow may incorrectly update RAM_DP memory content when byte enable is used with a byte size of 8, resulting in incorrect memory initialization after the ECO operation. Reference number: DNG-32505	Use one of the following alternatives: 1. Do not use the ECO flow — regenerate the design if a memory content change is required. 2. Use a byte size of 9 instead of 8. 3. Use RAM_DP_TRUE instead of RAM_DP (the problem is specific to PDPW8KC primitive).	MachXO4 (LFMXO4)
Simulation Model Returns Incorrect Read Data for PDP8KC Primitive in 2-Bit Read Mode. Simulation Model for the PDP8KC memory primitive returns corrupted read data when configured in mixed-width mode with a 2-bit read width	None	MachXO4 (LFMXO4)

Issue	Workaround	Affected Devices
(DATA_WIDTH_R = 2), where bit-1 of every 5th read data value in an 8-address segment does not reflect the data that was written. Reference number: DNG-30663		
DDRDLA Primitive Takes Extended Time to Lock in Simulation. The DDRDLA primitive simulation model may require more than 300 microseconds of simulation time (approximately 10 minutes of real time) to assert the ready_o signal when using the default DIV="1" setting. This behavior can significantly increase overall simulation runtime. Reference number: DNG-31228	None	Lattice Avant (LAV-AT), Certus-N2 (LN2-CT)
CONFIG_LMMID Simulation Model Does Not Fully Align with LMMI Specification. The CONFIG_LMMID primitive simulation model (HW SIM Model) may not fully reflect silicon behavior when processing configuration commands, which can cause simulation results to differ from actual device operation. Reference number: DNG-30574	None	Lattice Avant (LAV-AT), Certus-N2 (LN2-CT), Mach-N2 (LN2-MH)
RTL Simulation of CONFIG_LMMIE And CONFIG_LMMIB Primitives May Fail or Produce Incorrect Results. When using CONFIG_LMMIE or CONFIG_LMMIB primitives in RTL simulation, the simulation may produce incorrect results or fail entirely. This is a simulation model issue and does not affect hardware behavior. Reference number: DNG-22187	None	MachXO5-NX (LFMXO5)
FIFO32K Simulation Model Output Data Latency Is Longer Than Expected with OUTREG Parameter. Simulation Model for the FIFO32K primitive produces output data (DO) with an additional read clock cycle of latency than expected, both when the output register is bypassed (OUTREG = "BYPASSED") and when it is enabled (OUTREG = "USED"), causing simulation results to not be cycle-accurate. Reference number: DNG-32149	None	Lattice Avant (LAV-AT), Certus-N2 (LN2-CT)

Physical Designer

Issue	Workaround	Affected Devices
Physical Designer Displays Incorrect SLICE Configuration Values and Missing Connection Highlights. In Physical Designer, SLICE LUT INIT values may not accurately reflect their corresponding logic equations, and some internal SLICE connections may not be highlighted in Routing Mode. Reference number: DNG-31474	None	Lattice Avant (LAV-AT)
Net Display is Incorrect in Logic Block View in Physical Designer.	None	Lattice Avant (LAV-AT)

Issue	Workaround	Affected Devices
In the Radiant Physical Designer GUI, certain nets may display incorrectly in the Logic Block View, showing inaccurate signal connections. This is a visual display issue only and does not affect design functionality. Reference number: DNG-23192		
Physical Designer IO Mode Pin Labels Overlap and Are Unreadable on LFMXO4-050 and LFMXO4-080 Devices. In the Radiant Physical Designer GUI, when viewing IO mode for LFMXO4-050 and LFMXO4-080 devices, pin name labels overlap each other, rendering them unreadable. Users cannot clearly identify specific pins or their locations in IO mode. This issue is observed specifically on LFMXO4-050HC and LFMXO4-080HC does not appear on other devices. Reference number: DNG-32777	None	MachXO4 (LFMXO4)
Physical Designer Displays Incorrect Rendering for IFD1P3BX Primitive. In Radiant Physical Designer, the IFD1P3BX primitive may be displayed incorrectly in the GUI during routing mode, with some ports shown inverted or not filled as expected. This is a display-only issue and does not affect design functionality or results. Similar display inconsistencies may also appear for other logic block primitives. Reference number: DNG-14531	None	Lattice Avant (LAV-AT)
The Location for a Secured Component (Hard DPHY) Cannot Be Changed. Reference number: DNG-24746	None	CrossLink-NX (LIFCL)

IP Generation

Issue	Workaround	Affected Devices
DDR Memory Controller IP Generation Failure on Linux. The import construct is not supported in the IP Generation Engine on some Linux OS versions. This may cause the DDR Memory Controller IP to fail to generate. Reference number: DNG-31278	Avoid using the import construct and reference everything explicitly.	Lattice Avant (LAV-AT)
FIFO Empty Signal May Be Incorrect If the Clear Signal is Asserted During the First Clock Cycle on Avant Devices. On Avant devices, if the FIFO clear signal is asserted during the first clock cycle after reset, the FIFO empty signal may not match the synthesized or Place and Route (PAR) netlist behavior. This can result in incorrect FIFO status reporting immediately after reset. Reference number: DNG-24704	- Do not assert the clear signal during the first clock cycle. - Apply the clear signal after at least one valid clock cycle has elapsed to ensure proper alignment of the FIFO empty signal. - Verify FIFO behavior in simulation and	Lattice Avant (LAV-AT)

Issue	Workaround	Affected Devices
	hardware after applying this change.	

Place and Route

Issue	Workaround	Affected Devices
Place and Route Places Clock Buffer Instances Outside the Placement Group Boundary For designs using regional clocks, the clock sources are restricted to specific device locations due to architectural limitations. If such a source is assigned to a PGROUP that does not include any valid placement locations, placement issues may occur. Reference number: DNG-30821	This is not a functional issue but may appear as a quality issue. If you see WARNING <61293316> - par: discard locked instance messages in the log file and observe poor WNS after placement, it is recommended to avoid using PGROUPs.	Lattice Avant (LAV-AT)
PAR Fails When Implementation Directory Path Contains './' in the Radiant Project File. In Radiant project (.rdf) files, inclusion of './' in the implementation directory value, whether manually specified or assigned via Tcl, results in incorrect path resolution. An extra './' is introduced, leading to PAR failure. Reference number: DNG-33083	Manually update the .rdf file and remove './' from the implementation directory path.	All devices

Programmer

Issue	Workaround	Affected Devices
Programmer GUI Theme Displays Incorrectly when Windows and Radiant Use Different Themes In the Programmer tool, the GUI theme colors display inconsistently when Windows is set to Dark mode while Radiant is configured to Light mode. This results in mixed styling and reduces readability of GUI elements. Reference number: DNG-32395	Set the Radiant theme to match the Windows theme. If the Windows theme is Dark, select the Dark theme for Radiant as well.	All devices
Programming May Fail When Using Compressed Bitstreams. Reference number: DNG-26097	Use plain or uncompressed bitstream formats.	Lattice Avant (LAV-AT), Certus-N2 (LN2-CT-20)

Device Constraint Editor

Issue	Workaround	Affected Devices
Bounding Box Selected Instance Resource Count Does Not Report Register Usage Correctly. In the Bounding Box user interface, Selected Instance Resource Count can show zero usage for selected registers or flops because the count is taken from the MAP resource usage report, which does not include these instances for the affected designs. Reference number: DNG-26318	None	MachXO5-NX (LFMXO5)

Reveal

Issue	Workaround	Affected Devices
Inserting Reveal During Pre-Synthesis Causes Change in the Hierarchy Names When OSC IP Is Used. It Results in Timing Constraints That Use Hierarchical Objects to be Dropped. Reference number: DNG-29637	Use Post-Synthesis Reveal debug flow.	All devices

ECO Editor

Issue	Workaround	Affected Devices
ECO Editor Updates to EBR based ROM Initialization May Result in INITVAL Contents That Differ from Ip generated ROM Initialization for the Same Data Pattern. When using the ECO flow to modify the initialization contents of EBR based ROMs, the resulting gate level memory initialization (INITVAL_xx) may not match the initialization produced by the IP Foundation (FIP) flow for the same intended data pattern. This can cause simulation and hardware behavior of ECO updated ROM contents to differ from the original FIP generated design, leading to potential functional mismatches. Reference number: DNG-30489	Avoid using the ECO editor to modify EBR ROM contents. Instead, update the ROM hex file and regenerate the ROM using the IP Foundation (FIP) flow, then rerun the full implementation flow (synthesis followed by place and route) so that the final gate level netlist uses consistent INITVAL_xx contents based on the updated hex file.	All devices

Hardware Data File

Issue	Workaround	Affected Devices
Missing Timing Arcs in CONFIG_CLKRST_CORE. In Timing Analysis, timing arcs are missing for the CONFIG_CLKRST_CORE block when using the OSC_CRE CFG_CLK with manually defined constraints, and the auto-generated constraints for CFG_CLK and LMMI_CLK are also absent, resulting in incomplete timing coverage. Reference number: DNG-28315	None	MachXO5-NX (LFMXO5)
CONFIG_LMMI Writes to Enable Multiboot May Fail in Hardware on Crosslink-NX When Using Higher LMMICLK Frequencies. In Multiboot Reference Designs targeting CrossLink NX, LMMI writes to CONFIG_LMMI can fail at LMMICLK frequencies above ~40 MHz, even though timing reports are clean. This may prevent the SPIM bit from being set in Control Register 0 and cause the multiboot sequence to fail. Reference number: DNG-30992	Constrain and operate LMMICLK at or below ~10–12 MHz when performing LMMI writes (e.g., when enabling multiboot).	CrossLink-NX (LIFCL)
Gate-level Timing Simulation May Show an Unexpected Jitter for PLL. This only affects the gate level timing simulation, and HW behavior is unaffected. Reference number: DNG-29299	None	Lattice Avant (LAV-AT-E70)
Clocks Using Pclk Routing and Driving Only Fabric Registers May Have Reduced Minimum Pulse Width at Higher Speed Grades. Reference number: DNG-21315	None	CertusPro-NX (LFCPNX)
In Certus NX LRAM IP Simulation, When DPS is Asserted High, LRAM_Ready May Remain High Instead of Going Low. This does not affect HW functionality and only affects simulation. Expected behavior: Driving DPS high powers down LRAM, so lram_ready should be low. Reference number: DNG-27555	None	Certus-NX (LFD2NX)