

Lattice Radiant 2026.1.1 Software Release Notes

Welcome to Lattice Radiant® software, the complete design environment for Lattice Semiconductor Field Programmable Gate Arrays (FPGAs).

What's New in Radiant 2026.1.1 Software

▶ Device Support

- MachXO4™ (LFMXO4D)
 - 040HC (-5/-6) 2.5V/3.3V (COM/IND) – BBG256, BFG256
 - 040HC (-5) 2.5V/3.3V (AUTO) – BBG256
 - 040ZC (-2/-3) 2.5V/3.3V (COM/IND) – BBG256, BFG256
 - 050HC (-5/-6) 2.5V/3.3V (COM/IND) – BBG256, BFG256
 - 050HC (-5) 2.5V/3.3V (AUTO) – BBG256
 - 050ZC (-2/-3) 2.5V/3.3V (COM/IND) – BBG256, BFG256
 - 080HC (-5/-6) 2.5V/3.3V (COM/IND) – BBG256, BBG400
 - 080HE (-5) 2.5V/3.3V (COM/IND) – UTG69
 - 080HE (-5/-6) 2.5V/3.3V (COM/IND) – BBG256, BBG400
 - 080HE (-5) 2.5V/3.3V (AUTO) – BBG256
 - 080ZC (-2/-3) 2.5V/3.3V (COM/IND) – BBG256, BBG400
 - 080ZC (-2) 2.5V/3.3V (AUTO) – BBG256
 - 110HC (-5/-6) 2.5V/3.3V (COM/IND) – BBG256, BBG400, BBG484
 - 110HE (-5) 2.5V/3.3V (COM/IND) – UTG69
 - 110HE (-5/-6) 2.5V/3.3V (COM/IND) – BBG256, BBG400, BBG484
 - 110HE (-2) 2.5V/3.3V (AUTO) – BBG256, BBG484
 - 110ZC (-5/-6) 2.5V/3.3V (COM/IND) – BBG256, BBG400, BBG484
 - 110ZC (-2) 2.5V/3.3V (AUTO) – BBG256, BBG484
- Lattice Avant™ (LAV-AT)
 - E30 (-1/-2/-3) 1.0V (COM/IND) – ASGA410, FBG644, LFG676
 - G30 (-1/-2/-3) 1.0V (COM/IND) – ASGA410, FBG644, LFG676
 - X30 (-1/-2/-3) 1.0V (COM/IND) – ASGA410, FBG644, LFG676

- Certus-N2™ (LN2-CT)
 - 16 (-1/-2/-3) 0.82V (COM/IND) – ASGA410, LFG676, CBG484
 - 16 (-1) 0.82V (AUTO) – CBG484, ASGA410, LFG676
 - 16E (-1/-2/-3) 0.82V (COM/IND) – ASGA410
 - 20 (-1/-2/-3) 0.82V (COM/IND) – ASGA410, LFG676, CBG484
 - 20 (-1) 0.82V (AUTO) – CBG484, ASGA410, LFG676
 - 20E (-1/-2/-3) 0.82V (COM/IND) – ASGA410
- Mach-N2™ (LN2-MH)
 - 20 (-1/-2/-3) 0.82V (COM/IND) – CBG484
- Certus-NX™ (LFD2NX)
 - 35 (-7/-8/-9) 1.0V (COM/IND) – CABGA400
 - 65 (-7/-8/-9) 1.0V (COM/IND) – CABGA400
- MachXO5-NX™ (LFMXO5)
 - 35T (-7/-8/-9) 1.0V (COM/IND) – BBG400
 - 65T (-7/-8/-9) 1.0V (COM/IND) – BBG400

Note: On LFMXO5/LFD2NX devices, enabling both Authentication and Early IO results in a DRC error during bitstream generation.

► Tool and Other Enhancements

- **Bitstream** – Bitstream generation is now supported for Certus-NX (LFD2NX-25P, LFD2NX-15P) and MachXO5-NX (LFMXO5-15P) devices.
- **Device Constraint Editor**
 - The pin layout file export now includes trace length and package delay information.
 - Radiant now displays a warning message when any WRIO bank on an LFMXO5D device is assigned to a VCCIO voltage below 2.5 V. This applies to all LFMXO5D devices and packages, including LFMXO5-15D, LFMXO5-55TD, LFMXO5-55TDQ, LFMXO5-65TDQ, LFMXO5-20/30TD/TDQ/D/DQ, and enhanced (E) variants.
- **Package Data Updates** – Package data was updated for LAV-AT-E30, LAV-AT-G30, LAV-AT-X30, LN2-CT, and LN2-MH devices.
- **Power Calculator** – Worst-case leakage power data for CrossLink-NX and CrossLinkU-NX was updated based on new silicon correlation data.
- **Radiant GUI** – Added Reports menu for centralized location of generating and viewing design analysis reports — Report Utilization, Report Control Sets, Report

High Fanout Nets, and Analyze Complexity. All reporting commands are accessible through Tcl command (radiantc).

- **Strategies** – The **No Header**, **Reset Config RAM in re-configuration**, and **Run DRC** bitstream strategies have been added for the LFMXO4D device.
- **FPGA Libraries** – Added support for Mach-N2 (LN2-MH) internal Flash access via the CONFIG_LMMI MSPI bridge or direct UFM primitive instantiation.

Updating Projects from an Earlier Version

If you want to work on a design project created with an earlier version of Radiant software, it may be necessary to re-create some IP, per the procedures described in the following table.

These procedures adapt the project for the changes in Radiant software.

Versions	IP Regeneration Procedures				Description
	Avant (LAV-AT)	MachXO4 (LFMXO4)	CrossLink-NX (LIFCL), Certus-N2 (LN2-CT-ES), Mach-N2 (LN2-MH), Certus-NX (LFD2NX), Certus-NX-RT (UT24C), CertusPro-NX (LFCPNX), and CertusPro-NX-RT (UT24CP), MachXO5-NX (LFMXO5)	ICE40UP	
2026.1.1	1D_Filter	FIFO_DC	Complex_Mult	Complex_Mult	These IP used in designs created in Radiant 2026.1 or earlier must be re-generated in Radiant 2026.1.1
	Adder_Tree	RAM_DP	FFT_Butterfly	FFT_Butterfly	
	Voltage Temperature Monitor	RAM_DP_True	FIFO	FIFO	
	CREA	RAM_DQ	FIFO_DC	FIFO_DC	
	DDRPHY	ROM	Mult_Accumulate	Mult_Accumulate	
	MIPI_DPHY	Complex_Mult	Mult_Add_Sub	Mult_Add_Sub	
	MPPHY	FFT_Butterfly	Mult_Add_Sub_Sum	Mult_Add_Sub_Sum	
	SEDC Controller	Mult_Accumulate	Multiplier	Multiplier	
	Complex_Mult	Mult_Add_Sub			
	FFT_Butterfly	Mult_Add_Sub_Sum			
	FIFO	Multiplier			
	FIFO_DC				
	Mult_Accumulate				
	Mult_Add_Sub				
	Mult_Add_Sub_Sum				
	Multiplier				
	PLL				

Global Set/Reset (GSR) Support

Lattice **Global Set/Reset (GSR)** support for **Avant and Nexus 2** is disabled by default in Radiant 2026.1.1. Customers requiring GSR functionality must obtain a license and follow the associated usage requirements provided by Lattice Technical Support. Projects from earlier Radiant releases that are

updated to use licensed GSR functionality must be re-implemented starting from the **Map** stage through the remaining implementation stages.

Supported Devices

Lattice Radiant software can be used with either a free license or a subscription license. The two licenses provide access to different device families.

Device Family	Free License	Subscription License
iCE40 UltraPlus (iCE40UP)	◀	◀
Lattice Avant (LAV-AT) ¹		◀
CertusPro™-NX (LFCPNX)	Evaluation Mode ²	◀
Certus-NX (LFD2NX)	◀	◀
Certus-N2 (LN2-CT-ES)		◀
Mach-N2 (LN2-MH) ³		◀
MachXO4 (LFMXO4)	◀	◀
MachXO4D (LFMXO4D)	◀	◀
MachXO5-NX (LFMXO5-15D) ¹		◀
MachXO5-NX (LFMXO5-20TD) ¹		◀
MachXO5-NX (LFMXO5-20TDQ) ¹		◀
MachXO5-NX (LFMXO5-25)	◀	◀
MachXO5-NX (LFMXO5-100T)	Evaluation Mode ²	◀
MachXO5-NX (LFMXO5-30TD) ¹		◀

Device Family	Free License	Subscription License
MachXO5-NX (LFMXO5-30TDQ) ¹		◀
MachXO5-NX (LFMXO5-35)	◀	◀
MachXO5-NX (LFMXO5-35T)	Evaluation Mode ²	◀
MachXO5-NX (LFMXO5-55T)	Evaluation Mode ²	◀
MachXO5-NX (LFMXO5-55TD) ¹		◀
MachXO5-NX (LFMXO5-55TDQ) ¹		◀
MachXO5-NX (LFMXO5-65)	◀	◀
MachXO5-NX (LFMXO5-65T)	Evaluation Mode ²	◀
CrossLink-NX (LIFCL)	◀	◀
CrossLink-NX (LIFCL-33U)	Evaluation Mode ²	◀
Certus-NX-RT (UT24C)	Evaluation Mode ²	◀
CertusPro-NX-RT (UT24CP)	Evaluation Mode ²	◀

1. To enable this device, please [submit a support ticket](#).
2. Evaluation mode includes time-limited bitstream capability.
3. Publicly launched but license-controlled devices.

Support for Third-Party Synthesis and Simulator Tools

The Synopsys Synplify Pro® for Lattice synthesis and the Siemens QuestaSim® Lattice Edition simulator tools are included in the Radiant software.

▶ Synopsys Synplify Pro FPGA synthesis software version X-2025.09LR-SP1

- ▶ Release Notes for Synplify Pro are located in
`..\<install_directory>\radiant\2026.1.1\synpbase\doc\pdf.`
 The file name is `fpga_rn.pdf`.
- ▶ A full set of documents for Synplify Pro are also located in
`\<install_directory>\radiant\2026.1.1\synpbase\doc\pdf.`

▶ Siemens QuestaSim Lattice Edition 2025.2

- ▶ Release Notes for QuestaSim Lattice Edition are located in
`<install_directory>\radiant\2026.1.1\questasim\.`
 The file names are `RELEASE_NOTES.html` or `RELEASE_NOTES.txt`.
- ▶ A full set of documents for QuestaSim Lattice Edition are located in
`<install_directory>\radiant\2026.1.1\questasim\docs\pdfdocs.`

▶ Siemens Questa® 2022.3

▶ Cadence Xcelium® 24.03.003

▶ Synopsys VCS® U-2023.03-SP2

Help Resources

- ▶ Online Help updated with CertusPro-NX (LFCPNX), Certus-NX (LFD2NX), MachXO4 (LFMXO4), MachXO4D (LFMXO4D), MachXO5-NX (LFMXO5), Certus-N2 (LN2-CT), Mach-N2 (LN2-MH), CrossLink-NX (LIFCL), Certus-NX-RT (UT24C), CertusPro-NX-RT (UT24CP), and Lattice Avant (LAV-AT) content.
- ▶ To view the Online Help, start the Lattice Radiant software and select the  “Getting Started” icon under Information Center.

Note: The Firefox Snap install is not supported if you are using Ubuntu 20.04 or 18.04 to access the Radiant Help. This is a result of the snap install's inability to open local HTML pages. You may reinstall the latest version of Firefox using Apt install. For installation instructions, please refer to this [guide](#).

System Requirements

The following shows the basic system requirements for Radiant software:

- ▶ Intel x86 64-bit or 64-bit-compatible PC
- ▶ OS Support:

64-bit OS	Radiant	Synplify Pro	QuestaSim
Windows 11	✓	✓*	✓
Red Hat Enterprise Linux 8.10	✓	✓	✓
Red Hat Enterprise Linux 9.6	✓	✓	✓
Ubuntu version 24.04 LTS	✓	✓*	✓*
Ubuntu version 22.04 LTS	✓	✓*	✓*

***Note:** The third-party tools have been tested by Lattice on the listed platforms, but the vendors do not officially support them.

- ▶ Approximately 50GB free disk space
- ▶ Computer Memory Requirement:
 - ▶ Nexus – 16GB
 - ▶ LAV-AT– 32GB Recommended for running a single project. If running multiple projects, the memory requirement will be higher.
- ▶ 1024 X 768 graphics display
- ▶ Network adapter for license and network connectivity
- ▶ A Web browser with JavaScript capability
- ▶ Acrobat Reader

Issues Fixed in this Release

The following known issues are fixed in this release. Their workarounds are no longer needed.

During Bitstream Generation, the Process Terminates Unexpectedly During License Checkout Without Displaying an Error Message.

Devices affected: MachXO5 (LFMXO5-15D)

Reference number: DNG-31187

In Simulation, Third-Party Simulators (Such as VCS and Xcelium) Report an ELAB Error Due to a Missing MPPHY Module Definition When Simulating Designs That Use MPPHY or MPPCIE Primitives.

Devices affected: Lattice Avant (LAV-AT)

Reference number: DNG-33534

Designs Utilizing MPPHY May Encounter Hold Time Violations on LMMI Clock Paths Due to Clock Skew on Gated Clock Networks.

Devices affected: Lattice Avant (LAV-AT)

Reference number: DNG-29323

The DCC and DCM Resource Utility in PAR Report are Missing.

You can still view the usage in the clock report area of the PAR report.

Devices affected: MachXO4 (LFMXO4)

Reference number: DNG-29345

Designs Utilizing the DQSBUF Primitive May Report Shifted Clock Delays (DQSR90, DQSW, and DQSW270) That Do Not Match Post Place and Route Simulation Values.

Devices affected: CertusPro-NX (LFPCNX)

Reference number: DNG-30385

Designs Using the IDDRX2 Primitive May Exhibit Incorrect Output Data During Gate-Level Timing Simulation Due to a DQS Buffer Timing Model Delay Discrepancy.

Devices affected: CertusPro-NX (LFCPNX)

Reference number: DNG-31855

PCIe and MPPHY Link-Up and Enumeration Failures on Lane 2 May Occur for Avant Devices Configured in xSPI Mode.

Devices affected: Lattice Avant (LAV-AT)

Reference number: DNG-31227

DRC Does Not Validate the Reset Connection Between Oscillator and Soft Error Detection Primitives, Allowing Invalid Configurations to Proceed Through the Design Flow.

Devices affected: MachXO5 (LFMXO5)

Reference number: DNG-33379

Bitstream Generation Does Not Perform a Size Check for MachXO5-15D Designs, Which May Result in Oversized Bitstreams Causing Boot Lock-Up During Field Updates.

Devices affected: MachXO5 (LFMXO5-15D)

Reference number: DNG-33141

Bitstreams Generated for Secure Devices Could Cause the Device to Lock Up During Boot and Fail to Recover.

Devices affected: MachXO5 (LFMXO5)

Reference number: DNG-33136

Place and Route Takes Longer Than Expected to Complete.

Devices affected: Lattice Avant (LAV-AT)

Reference number: DNG-33523

Internal Pin Functions Displayed in Device Constraint Editor Spreadsheet View.

In the Device Constraint Editor (DCE), internal test and manufacturing pin function names (such as MFGOUT, ATB, and scan data signals) are visible in the Dual Function column of the DCE pin spreadsheet view, exposing internal-only information that is not relevant to design use.

Devices affected: All devices

Reference number: DNG-28674

Place and Route Crashes During Placer Phase when DDRDLL Placement Conflicts Exist.

In Place and Route, the placer crashes without a meaningful error message during placement when IO location constraints cause multiple DDRDLL instances to be assigned to the same HPIO bank site, instead of reporting a clear constraint conflict error.

Devices affected: Lattice Avant (LAV-AT)

Reference number: DNG-33026

Radiant Programmer Batch Mode May Generate an Incorrect XCF File for AS2 Boards.

When running Radiant Programmer in batch mode for AS2 boards, the generated .xcf file may be incorrect. The same project, when programmed using the GUI mode, produces the correct XCF file. This issue is specific to AS2 board configurations. Batch mode functions correctly for ES1 boards.

Devices affected: Lattice Avant (LAV-AT)

Reference number: DNG-29314

Physical Designer GUI Does Not Display or Highlight All Instances Within a Hierarchy.

In the Physical Designer GUI, not all instances are displayed in the netlist instance tree when expanding a hierarchy node. In addition, instances that are not shown in the tree are also not highlighted when using the highlight selection feature.

Devices affected: All devices

Reference number: DNG-31731

PCIe Configuration Issue (x4 and x8 Lane Configurations).

An issue has been identified in PCIe configurations involving x4 and x8 lane modes. When the `Iscc_misc_lock` bit is asserted in the 03B device, access to the user INIT register space is blocked. This restriction prevents proper programming of lane 2.

Devices affected: Lattice Avant (LAV-AT) -- All LAV-AT devices utilizing MPPHYx4 or MPPCIEx4 in their design are impacted.

Reference number: DNG-31227

Inserting a Reveal Core May Cause Undesired Toggling of the FIFO Empty Flag in Pmi_fifo Designs Synthesized with Synplify Pro.

Devices affected: CertusPro-NX (LFCPNX)

Reference number: DNG-24358

In PLL Simulation, the Phase Stops Moving When It Goes Over 360 Degrees.

In a Phase-Locked Loop (PLL) simulation, the phase should not stop moving but only reset to stay within a specific range (such as 0°–360°).

Devices affected: CrossLink-NX (LIFCL)

Reference number: DNG-23458

LSE Synthesis May Fail with an Error If the Project Path Length is Too Long. This Occurs Because the Synthesis Engine Has a Limit on the Maximum Path Length It Can Handle for Project Files and Directories.

Devices affected: All devices

Reference number: DNG-28606

LSE Synthesis May Fail Without Providing a Clear Error Message If the Design Includes Module Instantiations That Do Not Have Instance Names.

The same design may be compiled successfully with Synplify Pro but later fail during PAR.

Devices affected: Certus-NX (LFD2NX)

Reference number: DNG-29029

Unique ID Field is Not Editable in Device Constraint Editor.

For MachXO4 devices, the Unique ID (formerly TraceID) field in the sysCONFIG settings of the Device Constraint Editor is not editable and is locked to the default value of "0000". You cannot configure a custom Unique ID value through the DCE GUI. This is a software limitation in the current release.

Devices affected: MachXO4 (LFMXO4)

Reference number: DNG-29265

Reveal Debug Insertion Can Cause Invalid EN_CIL And HSEL Parameter Values in DPHY CORE.

When Reveal is inserted into a design that instantiates DPHY CORE, Synplify can generate incorrect EN_CIL and HSEL parameter values for a secured DPHY instance.

Devices affected: CrossLink-NX (LIFCL)

Reference number: DNG-30353

Synplify Optimization Can Cause Undesired Shift Register Output in Post Synthesis Simulation.

In some Ethernet based designs targeting Avant devices, Synplify can over optimize shift register logic that implements a delay element. When the array in the shift register is optimized, the post synthesis simulation shows undesired output on the shift register logic output, even though timing analysis passes and LSE does not exhibit the issue.

Devices affected: Lattice Avant (LAV-AT)

Reference number: DNG-25076

In Radiant 2025.2, PAR Ignores User Location Constraints for Instantiated DCC and Performs Automatic Placements of the Instantiated DCCs.

The `Idc_set_location` constraint is not supported for DCC instances in PAR because of hardware limitations.

Devices affected: Lattice Avant (LAV-AT)

Reference number: DNG-30001

There is an IBIS Model Mismatch for Pull Mode and Series Resistance When Using the LFMXO4 Device.

In the LFMXO4 device family, pull mode and series resistance are not loaded correctly during IBIS report generation, which prevents the system from finding a matching IBIS model. When this issue occurs, you will see warning 1191010, and the affected input pins will not have IBIS information listed in the IBIS report.

Devices affected: MachXO4 (LFMXO4)

Reference number: DNG-31303

DQSBUF Delay Values in Timing Analyzer Does Not Match with Post PAR Simulation.

For LFCPNX designs, DQSBUF shifted clock delays (`DQSI2DQSR_DEL`, `S2DQSW_DEL`) reported in Static Timing Analysis can differ significantly from post PAR simulation values. The STA reports about 0.5 ns larger delay than post PAR for arcs such as `DQSI` to `DQSR90` and `ECLKIN` to `DQSW270`, which can cause confusion when correlating STA and simulation results.

Devices affected: CertusPro-NX (LFCPNX)

Reference number: DNG-30385

PCIe Primitive Parameter Overrides Do Not Take Effect.

PCIe primitive parameters set in the `PCIE.v` module are not correctly applied to the PCIe core registers in hardware or simulation. As a result, the PCIe link may fail to train or link up.

Devices affected: CrossLink-NX (LIFCL)

Reference number: DNG-28201

GDDR Aligned Mode Capture Clock Phase Not Configured for Avant Device.

When GDDR RX in Avant devices is configured to Aligned mode, the capture clock lacks the expected phase shift or delay, which can cause timing analysis failures.

Devices affected: Lattice Avant (LAV-AT)

Reference number: DNG-31269

Timing Report Shows Infinite Slack on Output Paths When Set_Max_Delay Uses Datapath_Only.

In some designs that use a generated clock on an output port, applying a set_max_delay constraint with the datapath_only option on output paths can cause the timing report to show INF (infinite) slack for those paths. The affected paths are not reported as violating even when they should, because the tool initializes timing at the generated clock output with a default clock phase that does not match the generated clock definition.

Devices affected: CertusPro-NX (LFCPNX)

Reference number: DNG-29538

DSP PREADD9 Asynchronous Reset Causes Functional Failure on Hardware.

DSP block's PREADD9 multiplier output is stuck at all-zero on hardware when the RESET property is set to ASYNC.

Devices affected: CertusPro-NX (LFCPNX), CrossLink-NX (LIFCL-40, LIFCL-33), Certus-NX (LFD2NX-35, LFD2NX-65), MachXO5 (LFMXO5-35T, LFMXO5-65T)

Reference number: DNG-32692, DNG-32693, DNG-32694, DNG-32695

iCE40 PLL Timing Is Not Modeled Correctly in Radiant.

Timing Analysis reports significantly different PLL timing values for iCE40UP devices compared to iCEcube2, which may result in inaccurate timing closure.

Devices affected: iCE40UP (iCE40 UltraPlus)

Reference number: DNG-32321

Incorrect PLL Timing Model for iCE40UP Devices in Radiant.

In Timing Analysis, the PLL timing model for iCE40UP devices in Radiant is incomplete, with missing PLL intrinsic delay, missing derating on PLL tap delay, incorrect delay from PLL to global clock mux, and incorrect clock B adjustment, resulting in inaccurate timing analysis results.

Devices affected: iCE40 UltraPlus (iCE40UP)

Reference number: DNG-33029

Place and Route Assigns CDR SGMIIIN Input to an Unbonded I/O Site.

The Place and Route tool incorrectly assigns the SGMIIIN CDR input to an unbonded I/O site (PB10A) on LFD2NX-15P and LFD2NX-25P devices. This results in a placement error that prevents successful design completion.

Devices affected: Certus-NX (LFD2NX-15P, LFD2NX-25P)

Reference number: DNG-33068

Incorrect Auto-Generated Clock Constraint for PCIe x8 IP on Avant.

In Timing Analysis, the auto-generated clock constraint for the PCIe x8 IP link0_clk_usr_o output on Avant devices is set to an incorrect frequency (e.g., 50 MHz instead of the expected 250 MHz for Gen4x8), due to missing timing arcs from REFCLK to TXOUTCLK in the device timing model.

Devices affected: Lattice Avant (LAV-AT)

Reference number: DNG-28241

IDDRX2 Produces Incorrect Output in Gate-Level Simulation.

Timing simulation encounters clock domain crossing issue due to intrinsic delay mismatch on DQSBUF output signals – write pointer and clock DQSR90 that are used to drive subsequent IO Logic. If not fixed, the clock domain crossing issue will cause the RXDATA/output to be incorrect for IDDRX2 design.

Devices affected: CrossLink-NX (LIFCL)

Reference number: DNG-31855

Place and Route Errors Out on Designs with Unbalanced Wide LUT.

Place and Route encounters an error when processing designs that contain unbalanced wide LUTs, preventing the design from completing successfully.

Devices affected: MachXO4 (LFMXO4)

Reference number: DNG-33063

Place and Route Crashes During Placer Phase when DDRDLL Placement Conflicts Exist.

In Place and Route, the placer crashes without a meaningful error message during placement when IO location constraints cause multiple DDRDLL instances to be assigned to the same HPIO bank site, instead of reporting a clear constraint conflict error.

Devices affected: Lattice Avant (LAV-AT)

Reference number: DNG-33026

Simulation Model Incorrectly Maps RX/TX Polarity Inversion Parameters in PCS Core and EOM Control Parameters in PCIe Core.

The simulation model for the PCS_CORE incorrectly maps the RX_POLINV and TX_POLINV polarity inversion parameters to the wrong register bit indices, causing simulation results to not reflect the configured polarity inversion behavior. In addition, the simulation model for the PCIe Core incorrectly maps the EOMMODE, EOMRDSEL, EOMDIVDIS, and EOMCTRL0_LOW parameters to the wrong register bit indices, causing simulation results to not reflect the configured EOM control behavior defined in the specification.

Devices affected: CertusPro-NX (LFPCPX)

Reference number: DNG-32515

Exported Pin Layout File Shows Package Delay and Trace Length as -1 for LAV-AT-X30 and LN2-CT-20 LFG676 Packages.

Package delay and trace length values are displayed as -1 in the exported pin layout file for LAV-AT-X30 and LN2-CT-20 LFG676 packages.

Devices affected: Lattice Avant (LAV-AT-X30), Certus-N2 (LN2-CT-20)

Reference number: DNG-32472

When the Signals Column is Empty, clicking MSB/LSB Removes Virtual SW/LED Entries.

In Reveal Inserter, an empty signals column for multiple virtual switches/LEDs causes incorrect GUI behavior. When the LSB and MSB buttons are clicked, other virtual switches or LEDs are removed from the display.

Devices affected: All devices

Reference number: DNG-32369

Certus-N2 Devices Missing IBIS HW Data Status in .ibs Report.

Certus-N2 (LN2-CT) devices are missing IBIS hardware data status entries in the generated .ibs report. This issue is caused by the IBIS generator referencing incorrect master IBIS files for these devices, leading to absent status information.

Devices affected: Certus-N2 (LN2-CT)

Reference number: DNG-32156

DELAYB Delay Reports as Zero in Hold Timing Analysis.

In Timing Analysis, the DELAYB primitive delay is incorrectly reported as zero during hold time analysis when using the "m" speed grade, regardless of the DEL_VALUE and COARSE_DELAY settings, leading to inaccurate hold timing results.

Devices affected: CertusPro-NX (LFCPNX)

Reference number: DNG-32000

Physical Designer GUI Does Not Display or Highlight All Instances Within a Hierarchy.

In the Physical Designer GUI, not all instances are displayed in the netlist instance tree when expanding a hierarchy node. In addition, instances that are not shown in the tree are also not highlighted when using the highlight selection feature.

Devices affected: All devices

Reference number: DNG-31731

Post-Place and Route Simulation Shows Incorrect Memory Initialization for EBR Primitives with Non-Zero INITVAL.

The Post-Place and Route Simulation Model returns incorrect data at the initial addresses of EBR memory primitives (SP8KC, DP8KC, PDP8KC) when non-zero INITVAL attributes are configured.

Devices affected: MachXO4 (LFMXO4)

Reference number: DNG-31327

Timing Report Shows Infinite Slack on Output Paths When Set_Max_Delay Uses Datapath_Only.

In some designs that use a generated clock on an output port, applying a set_max_delay constraint with the datapath_only option on output paths can cause the timing report to show INF (infinite) slack for those paths. The affected paths are not reported as violating even when they should, because the tool initializes timing at the generated clock output with a default clock phase that does not match the generated clock definition.

Devices affected: CertusPro-NX (LFPCPX)

Reference number: DNG-29538

Internal Pin Functions Displayed in Device Constraint Editor Spreadsheet View.

In the Device Constraint Editor (DCE), internal test and manufacturing pin function names (such as MFGOUT, ATB, and scan data signals) are visible in the Dual Function column of the DCE pin spreadsheet view, exposing internal-only information that is not relevant to design use.

Devices affected: All devices

Reference number: DNG-28674

LSE Synthesis May Fail with an Error If the Project Path Length is Too Long. This Occurs Because the Synthesis Engine Has a Limit on the Maximum Path Length It Can Handle for Project Files and Directories.

Devices affected: All devices

Reference number: DNG-28606

PCIe Primitive Parameter Overrides Do Not Take Effect.

PCIe primitive parameters set in the PCIE.v module are not correctly applied to the PCIe core registers in hardware or simulation. As a result, the PCIe link may fail to train or link up.

Devices affected: CrossLink-NX (LIFCL)

Reference number: DNG-28201

Device Provisioning of the MachXO5-55TD Using UFM with STAPL is Not Functioning.

When using the Programmer to generate a STAPL file for device provisioning (Erase, Program, Verify, Refresh) with UFM on MachXO5-55TD devices, the file generation fails.

Devices affected: MachXO5-NX (LFMXO5)

Reference number: DNG-33024

Place and Route Failure when Using Four MIPI RX DPHY Interfaces in the Same I/O Bank on Avant Devices.

Place and Route may fail with a routing error when four MIPI DPHY RX IP instances are placed in the same I/O bank on Avant devices, due to limited clock routing resources for edge clocks within a single bank (Place and Route).

Devices affected: Lattice Avant (LAV-AT)

Reference number: DNG-32974

Run All Button Does Not Execute the Design Flow for EAPR Devices

In the Radiant GUI, clicking the Run All button on EAPR (Early Access Program) devices does not run any process (Synthesis, Map, and Place & Route). This is because the tool incorrectly requires the Export/Bitstream stage which is not available on these devices.

Devices affected:

- Certus-N2 (LN2-CT-20ES)
- Lattice Avant (LAV-AT-E70ES1/E70/E50)
- MachXO5-NX (LFMXO5-25/35T/55T/65T/100T)
- Certus-NX (LFD2NX-9/15/17/25/28/35/40/65)
- MachXO4 (LFMXO4-010HE/HC, 015HE/HC, 025HE/HC, 050HE/HC; 080HE/HC, 110HE/HC)

Reference number: DNG-32987, DNG-31168

Lattice Synthesis (LSE) Intermittently Crashes During Synthesis.

LSE intermittently crashes with a segmentation violation or unknown signal error during synthesis, causing the design to fail with "error code 1" approximately 50% of the time.

Devices affected: Certus-NX (LFD2NX)

Reference number: DNG-31070

Multiple issues in GPLL IP software model such as incorrect VCO phase shift equation, premature PLL lock assertion, long clock pulse during phase shift, inaccurate VCO frequency and sticky lock behavior.

Devices affected: CrossLink-NX (LIFCL), CertusPro-NX (LFCPNX), Certus-NX (LFD2NX), MachXO5-NX (LFMXO5)

Reference number: DNG-31972

Known Issues for Radiant 2026.1.1

To view the complete list of known issues, refer to the [Lattice Radiant Software Known Issues](#) document. For further assistance, please contact Lattice Technical Support.