



Lattice Avant-E70 Development Board

Preliminary

Evaluation Board User Guide

FPGA-EB-02070-0.80

March 2026

Disclaimers

Lattice makes no warranty, representation, or guarantee regarding the accuracy of information contained in this document or the suitability of its products for any particular purpose. All information herein is provided AS IS, with all faults, and all associated risk is the responsibility entirely of the Buyer. The information provided herein is for informational purposes only and may contain technical inaccuracies or omissions, and may be otherwise rendered inaccurate for many reasons, and Lattice assumes no obligation to update or otherwise correct or revise this information. Products sold by Lattice have been subject to limited testing and it is the Buyer's responsibility to independently determine the suitability of any products and to test and verify the same. LATTICE PRODUCTS AND SERVICES ARE NOT DESIGNED, MANUFACTURED, OR TESTED FOR USE IN LIFE OR SAFETY CRITICAL SYSTEMS, HAZARDOUS ENVIRONMENTS, OR ANY OTHER ENVIRONMENTS REQUIRING FAIL-SAFE PERFORMANCE, INCLUDING ANY APPLICATION IN WHICH THE FAILURE OF THE PRODUCT OR SERVICE COULD LEAD TO DEATH, PERSONAL INJURY, SEVERE PROPERTY DAMAGE OR ENVIRONMENTAL HARM (COLLECTIVELY, "HIGH-RISK USES"). FURTHER, BUYER MUST TAKE PRUDENT STEPS TO PROTECT AGAINST PRODUCT AND SERVICE FAILURES, INCLUDING PROVIDING APPROPRIATE REDUNDANCIES, FAIL-SAFE FEATURES, AND/OR SHUT-DOWN MECHANISMS. LATTICE EXPRESSLY DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY OF FITNESS OF THE PRODUCTS OR SERVICES FOR HIGH-RISK USES. The information provided in this document is proprietary to Lattice Semiconductor, and Lattice reserves the right to make any changes to the information in this document or to any products at any time without notice.

Inclusive Language

This document was created consistent with Lattice Semiconductor's inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice's inclusive language [FAQ 6878](#) for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

Contents

Contents	3
Abbreviations in This Document.....	6
1. Introduction.....	7
1.1. Avant-E70 Development Board.....	7
1.2. Features	7
1.3. Avant-E Device	10
1.4. Applying Power to the Board	10
2. Jumper Definition	11
3. Power Scheme.....	16
4. Programming Platform Manager 2.....	18
4.1. JTAG Download Interface.....	18
4.2. Programming for Platform Manager 2.....	18
5. Programming Avant-E.....	20
5.1. JTAG Download Interface.....	20
5.2. Alternate JTAG Download Interface.....	20
5.3. Global Setting in Lattice Radiant software.....	21
5.4. Other Configuration Pins.....	24
5.5. Programming of Avant SRAM.....	24
5.6. Programming of Flash	25
5.7. Boot of Flash	28
6. Avant Clock Sources.....	29
7. Control Buses – I2C, UART, and SPI	30
7.1. I2C Topology.....	30
7.2. UART Topology.....	30
7.3. SPI Topology	30
7.4. LPDDR4 Topology.....	31
8. LEDs, Switches and Segment Displays	34
8.1. DIP Switch	34
8.2. General Purpose Push Buttons	34
8.3. General Purpose LEDs	35
8.4. Segment Displays	35
9. Headers/Connectors and Avant Device Ball Mapping.....	36
9.1. FMC1 Connector	36
9.2. FMC2 Connector	39
9.3. Parallel FMC1 Configuration Header.....	42
9.4. Parallel FMC2 Configuration Header.....	42
9.5. Raspberry PI Board GPIO Header.....	43
9.6. External Flash Configuration Header	44
9.7. PMOD Header	44
9.8. Through Hole Extended Area	45
10. Software Requirements	47
11. Storage and Handling	47
12. Ordering Information.....	47
Appendix A. Avant-E70 Development Schematics	48
Appendix B. Avant-E70 Development Board Bill of Materials.....	69
References.....	81
Technical Support Assistance	82
Revision History	83

Figures

Figure 1.1. Top View of Avant-E70 Development Board	8
Figure 1.2. Bottom View of Avant-E70 Development Board	9
Figure 1.3. 12 V DC Power Supply.....	10
Figure 2.1. Top View of Avant-E70 Development Board – Jumper Locations	11
Figure 3.1. Board Power Scheme (1)	16
Figure 3.2. Board Power Scheme (2)	16
Figure 4.1. Lattice Radiant Programmer.....	19
Figure 5.1. Configuration, UART and I2C Architecture	20
Figure 5.2. Global Settings (1).....	21
Figure 5.3. Global Settings (2).....	22
Figure 5.4. Global Settings (3).....	23
Figure 5.5. Radiant Programmer	24
Figure 5.6. Radiant Programmer – Device Properties	25
Figure 5.7. Radiant Programmer Interface	26
Figure 5.8. Radiant Programmer – Device Properties	27
Figure A.1. Title Page	48
Figure A.2. Block Diagram.....	49
Figure A.3. USB Interface	50
Figure A.4. Bank-0, 1 External Flash	51
Figure A.5. Bank-2 JTAG, UART.....	52
Figure A.6. Bank-3, 4, 5 FMC1.....	53
Figure A.7. FMC1 LA&HA	54
Figure A.8. Bank-6 LED, SWITCH.....	55
Figure A.9. Bank-7, 8 FMC2	56
Figure A.10. FMC2 LA.....	57
Figure A.11. Bank-9, 10, 11 LPDDR4	58
Figure A.12. Bank-12, 13 PMODs.....	59
Figure A.13. Bank-14 Segment & RPI.....	60
Figure A.14. Bank Power.....	61
Figure A.15. Power Decoupling	62
Figure A.16. Power Supplies 1	63
Figure A.17. Power Supplies 2	64
Figure A.18. Ground.....	65
Figure A.19. Platform Manager 2	66
Figure A.20. USB Power Sink	67
Figure A.21. Power Block Diagram	68

Tables

Table 1.1. Board Power Supply	10
Table 2.1. Jumper Setting	12
Table 3.1. V _{CCIO} Supply Options	17
Table 3.2. Power Status LED Definition	17
Table 4.1. JTAG Header Connections	18
Table 4.2. Cable Fly Wire JTAG Connections	18
Table 5.1. Programming Cable JTAG Connections	20
Table 5.2. Other Configuration Signals	24
Table 6.1. Clock Sources	29
Table 7.1. I2C Bus Connections	30
Table 7.2. UART Bus Connections	30
Table 7.3. SPI Bus Connections	30
Table 7.4. LPDDR4 Interface Connections	31
Table 8.1. DIP Switch Signals	34
Table 8.2. Push Button Switch Signals	34
Table 8.3. General Purpose LED Signals	35
Table 8.4. Segment Display	35
Table 9.1. FMC1 Pin Connections	36
Table 9.2. FMC2 Pin Connections	39
Table 9.3. Parallel FMC1 Configuration Header Pin Connections	42
Table 9.4. Parallel FMC2 Configuration Header Pin Connections	42
Table 9.5. Raspberry PI header Pin Connections	43
Table 9.6. SPI Flash Configuration Header Pin Connections	44
Table 9.7. PMOD Header Pin Connections	44
Table 9.8. Through Hole Extended Area Pin Connections	45
Table 12.1. Ordering Information	47

Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviation	Definition
AC/DC	Alternating Current and Direct Current
ADC	Analog-to-digital Converter
DIP	Dual Inline Package
ESD	Electro-Static Discharge
FMC	FPGA Mezzanine Card
FPGA	Field Programmable Gate Array
FTDI	Future Technology Devices International
GPIO	General Purpose Input/Output
HPC	High Pin Connector
I2C	Inter-Integrated Circuit
I/O	Input/Output
JTAG	Joint Test Action Group
LED	Light Emitting Diode
LPDDR4	Low Power Double Data Rate 4
LVDS	Low-Voltage Differential Signaling
OSC	Oscillator
PC	Personal Computer
PMOD	Peripheral Module
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus

1. Introduction

The Lattice Semiconductor Avant™-E70 Development Board allows you to investigate and experiment with the features of the Avant-E Field Programmable Gate Array (FPGA). The features of the Avant-E70 Development Board can assist you with the rapid prototyping and testing of your specific design. The Avant-E70 Development Board is part of the Avant-E70 Development Board Kit. This guide is intended to be referenced to demonstrate the Avant-E FPGA and introduce board resources.

The Avant-E70 Development Board Kit includes the following:

- Avant-E70 Development Board is pre-loaded with blinking lights demo design.
- USB-A to USB-B (Mini) cable for programming FPGA SRAM through a PC.
- 12 V AC/DC power adapter and international plug adapters.
- The Lattice Radiant™ software download information.

The contents of this user guide include top-level functional descriptions of the various portions of the development board, descriptions of the on-board headers, status indicators, push buttons and switches and a complete set of schematics.

1.1. Avant-E70 Development Board

The Avant-E70 Development Board features the Avant-E FPGA in the LFG1156 package. The board has the ability to expand the usability of the Avant-E FPGA with FMC HPC, PMOD, and Raspberry PI connectors. Easy-to-use board resources such as jumpers, LED indicators, push buttons and switches are available for user-defined applications.

[Figure 1.1](#) shows the top view of the Avant-E70 Development Board. [Figure 1.2](#) shows the bottom view of the Avant-E70 Development Board.

1.2. Features

The Avant-E70 Development Board includes the following features:

- Avant-E FPGA (LAV-AT-E70-3LFG1156C).
- General purpose Input/Output (GPIO) breakout with 2 FMC, PMOD, and Raspberry PI connectors.
- A plentiful wide-range I/O and high-speed differential I/O were extended onboard.
- On board memory – LPDDR4 x64 bit.
- USB-B (Mini) connection for device programming.
- Optional USB type-C power supply.
- On-board Boot Flash – 512 MB of Serial Peripheral Interface (SPI) Flash, with Single/Dual/Quad support.
- Eight input DIP switches, four push buttons, sixteen yellow green LEDs and three seven-segment LEDs are available for designer configuration.
- Lattice Radiant software programming support.
- Reference clock sources.
- Lattice Platform Manager 2 for board power management functions.

Caution: The Avant-E70 Development Board has ESD-sensitive components. The ESD safe practices should be followed while handling and using the Avant-E70 Development Board.

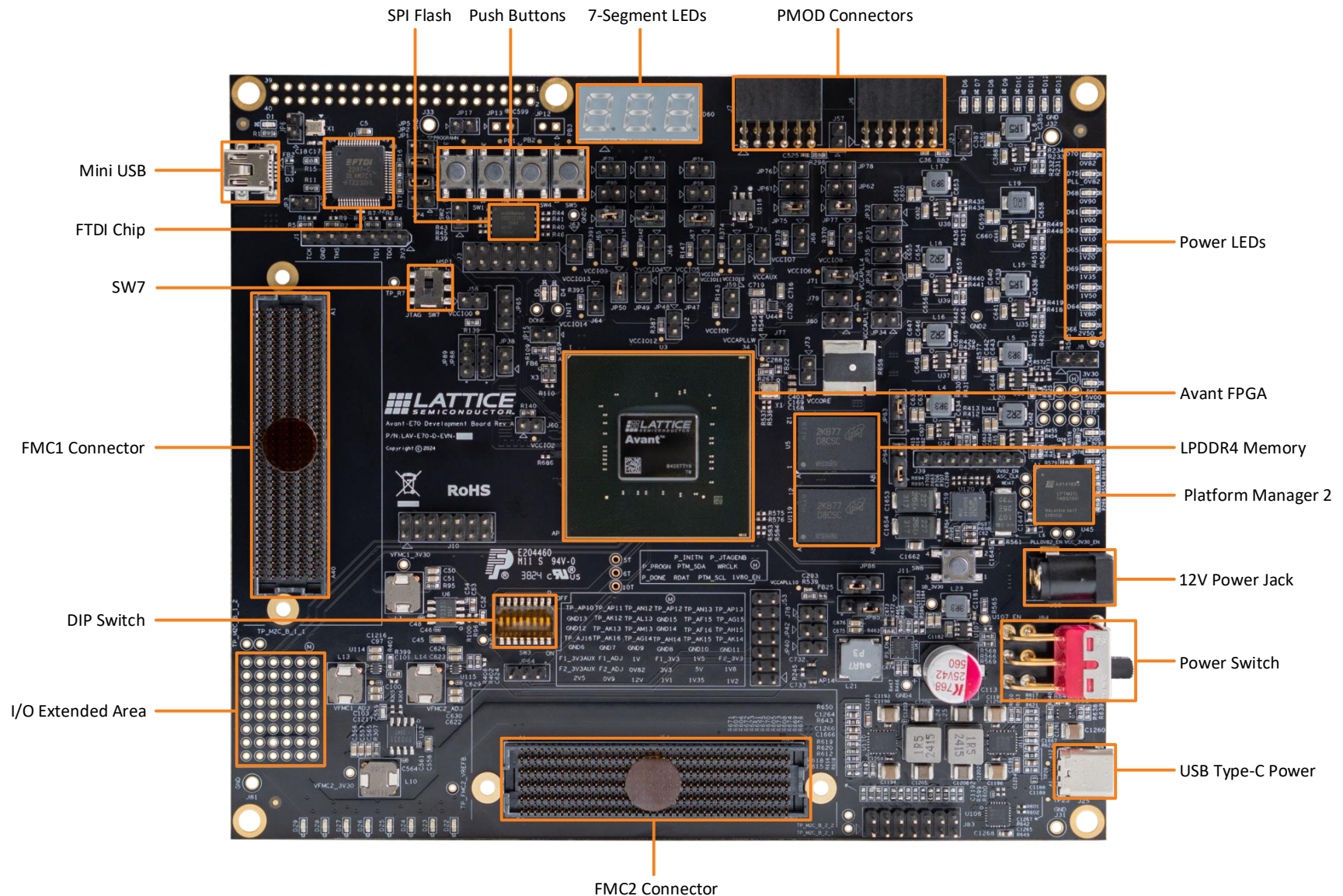


Figure 1.1. Top View of Avant-E70 Development Board

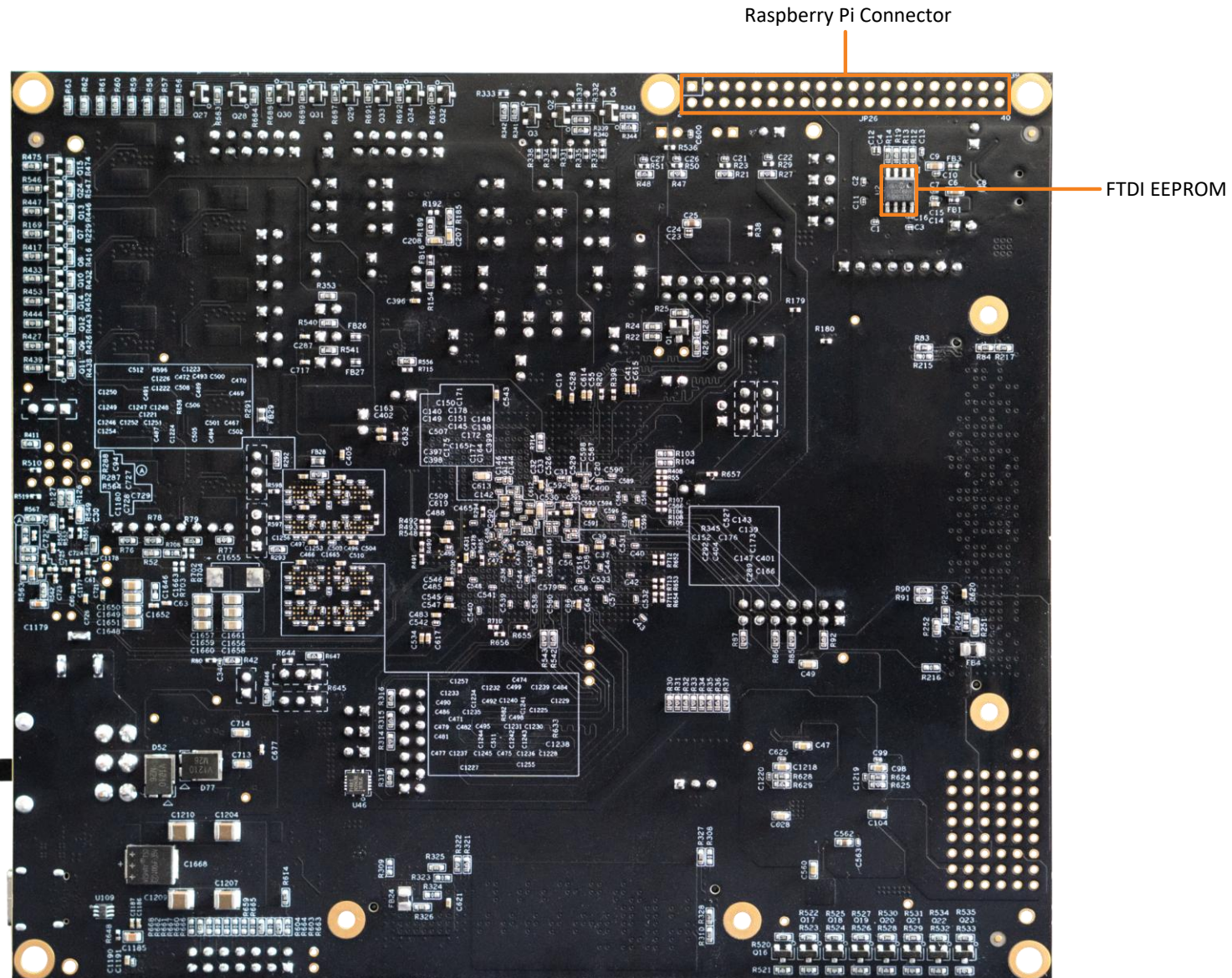


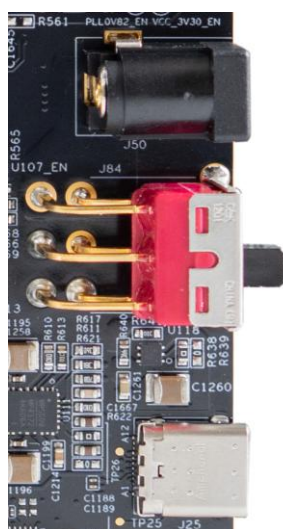
Figure 1.2. Bottom View of Avant-E70 Development Board

1.3. Avant-E Device

The Avant-E70 Development Board features the Avant-E device in an LFG1156 package, also referred to as LAV-AT-E70-3LFG1156C. The low-power general purpose FPGA can be used in a wide range of applications across multiple markets and is optimized for bridging and processing needs in edge applications. For more information on the capabilities of Avant-E devices, see the [Lattice Avant Platform – Overview Data Sheet \(FPGA-DS-02107\)](#) and the [Lattice Avant Platform – Specifications Data Sheet \(FPGA-DS-02112\)](#).

1.4. Applying Power to the Board

The Avant-E70 Development Board can be powered up using the 12 V AC/DC power adapter included with the kit. The power adapter should be connected to the power input jack J50. The Avant-E70 Development Board also can be powered up using USB type-C charger which can support 20 V/5 A output capability. USB type-C cable should connect to type-C power connector J25 as shown in [Figure 1.3](#) and [Table 1.1](#). Power switch J84 can choose between these two power supplies. Flip up to select power adapter and flip down to select USB type-C power.



2. Jumper Definition

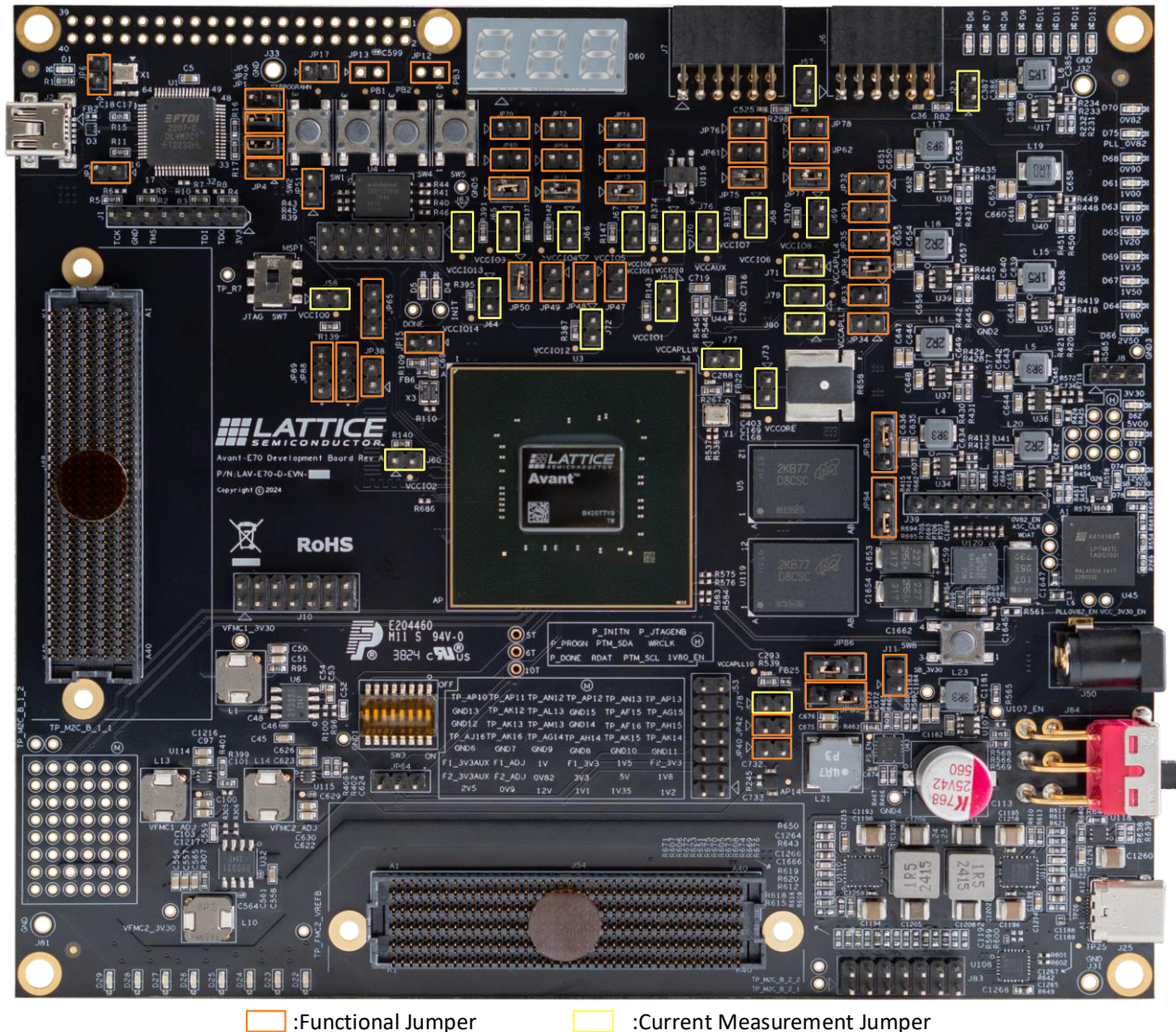


Figure 2.1. Top View of Avant-E70 Development Board – Jumper Locations

Table 2.1. Jumper Setting

Part Designator	Description	Setting	Default
J11	Platform Manager 2 (U45) Power	Open – No Power to Platform Manager 2 Close – Power to Platform Manager 2	Open
J23	Power Measurement Header for PMOD Header J6		
J57	Power Measurement Header for PMOD Header J7		
J58	Power Measurement Header for VCCIO0		
J59	Power Measurement Header for VCCIO1		
J60	Power Measurement Header for VCCIO2		
J63	Power Measurement Header for VCCIO13		
J64	Power Measurement Header for VCCIO14		
J65	Power Measurement Header for VCCIO3		
J66	Power Measurement Header for VCCIO4		
J67	Power Measurement Header for VCCIO5		
J68	Power Measurement Header for VCCIO7		
J69	Power Measurement Header for VCCIO8		
J70	Power Measurement Header for VCCIO9, VCCIO10, VCCIO11		
J71	Power Measurement Header for VCCIO6		
J72	Power Measurement Header for VCCIO12		
J73	Power Measurement Header for Avant VCC		
J76	Power Measurement Header for Avant VCCAUX		
J77	Power Measurement Header for Avant VCCAPLLW		
J78	Power Measurement Header for Avant VCCAPLL10		
J79	Power Measurement Header for Avant VCCAPLL4		
J80	Power Measurement Header for Avant VCCAPLL7		
JP1, JP2	FTDI UART Debug	Open – UART bus unconnected Close – UART bus connected	Open
JP3	FTDI Reset	Open – FTDI active Close – Holds FTDI in reset	Open
JP4, JP5	FTDI I2C	Open – I2C bus unconnected Close – I2C bus connected	Open
JP6	FTDI 12 MHz Oscillator Jumper	Open – 12 MHz oscillator goes only to FTDI chip Close – 12 MHz oscillator goes to FTDI chip and ball U3 of FPGA through JP65	Open
JP12	Raspberry PI Connector (JP26) Power	Open – Raspberry PI self-power Close – 3.3 V supplied to Raspberry PI connector	Open
JP13	Raspberry PI Connector (JP26) Power	Open – Raspberry PI self-power Close – 5.0 V supplied to Raspberry PI connector	Open
JP15	125 MHz OSC (X3) Standby	Open – OSC enabled Close – OSC in standby	Open
JP17	PROGRAMN Pull-down Jumper	Open – MSPI boot mode Close – Secondary configuration mode	Open
JP31	Avant Bank 6 Power Select (VCCIO6)	JP31, JP32, JP33, JP34, JP35, and JP36 select voltage to VCCIO6. Only one of these jumpers should be inserted. Open – VCCIO6 voltage based on JP32, JP33, JP34, JP35, and JP36 settings. Close – VCCIO6 = 0.9 V	Open

Part Designator	Description	Setting	Default
JP32	Avant Bank 6 Power Select (VCCIO6)	JP31, JP32, JP33, JP34, JP35, and JP36 select voltage to VCCIO6. Only one of these jumpers should be inserted. Open – VCCIO6 voltage based on JP31, JP33, JP34, JP35, and JP36 settings. Close – VCCIO6 = 1.0 V	Open
JP33	Avant Bank 6 Power Select (VCCIO6)	JP31, JP32, JP33, JP34, JP35, and JP36 select voltage to VCCIO6. Only one of these jumpers should be inserted. Open – VCCIO6 voltage based on JP31, JP32, JP34, JP35, and JP36 settings. Close – VCCIO6 = 1.1 V	Open
JP34	Avant Bank 6 Power Select (VCCIO6)	JP31, JP32, JP33, JP34, JP35, and JP36 select voltage to VCCIO6. Only one of these jumpers should be inserted. Open – VCCIO6 voltage based on JP31, JP32, JP33, JP35, and JP36 settings. Close – VCCIO6 = 1.35 V	Open
JP35	Avant Bank 6 Power Select (VCCIO6)	JP31, JP32, JP33, JP34, JP35, and JP36 select voltage to VCCIO6. Only one of these jumpers should be inserted. Open – VCCIO6 voltage based on JP31, JP32, JP33, JP34, and JP36 settings. Close – VCCIO6 = 1.5 V	Open
JP36	Avant Bank 6 Power Select (VCCIO6)	JP31, JP32, JP33, JP34, JP35, and JP36 select voltage to VCCIO6. Only one of these jumpers should be inserted. Open – VCCIO6 voltage based on JP31, JP32, JP33, JP34, and JP35 settings. Close – VCCIO6 = 1.8 V	Close
JP38	FMC1 Reference Voltage	Open – Leaves FMC1 VREF_A_M2C (J48D.H1) pin open Close – Connects Avant ball AF13 to FMC1 VREF_A_M2C (J48D.H1)	Open
JP40	FMC2 Reference Voltage	Open – Leaves FMC2 VREF_A_M2C (J54D.H1) pin open Close – Connects Avant ball AF18 to FMC2 VREF_A_M2C (J54D.H1)	Open
JP42	FMC2 Reference Voltage	Open – Leaves FMC2 VREF_A_M2C (J54D.H1) pin open Close – Connects Avant ball AF24 to FMC2 VREF_A_M2C (J54D.H1)	Open
JP47	Avant Bank 12 Power Select (VCCIO12)	JP47, JP48, JP49, and JP50 select voltage to VCCIO12. Only one of these jumpers should be inserted. Open – VCCIO12 voltage based on JP48, JP49, and JP50 settings. Close – VCCIO12 = 1.2 V	Open
JP48	Avant Bank 12 Power Select (VCCIO12)	JP47, JP48, JP49, and JP50 select voltage to VCCIO12. Only one of these jumpers should be inserted. Open – VCCIO12 voltage based on JP47, JP49, and JP50 settings. Close – VCCIO12 = 1.8 V	Open

Part Designator	Description	Setting	Default
JP49	Avant Bank 12 Power Select (VCCIO12)	JP47, JP48, JP49, and JP50 select voltage to VCCIO12. Only one of these jumpers should be inserted. Open – VCCIO12 voltage based on JP47, JP48, and JP50 settings. Close – VCCIO12 = 2.5 V	Open
JP50	Avant Bank 12 Power Select (VCCIO12)	JP47, JP48, JP49, and JP50 select voltage to VCCIO12. Only one of these jumpers should be inserted. Open – VCCIO12 voltage based on JP48, and JP49 settings. Close – VCCIO12 = 3.3 V	Close
JP51	SPI Chip Select	Open – Flash (U4) CS# is only connected to pin 2 of J3 Header Close – Connects Avant MCSN ball (P7) to Flash (U4) CS# pin	Close
JP58	Avant Bank 5 Power Select (VCCIO5)	JP58, JP73, and JP74 select voltage to VCCIO5. Only one of these jumpers should be inserted. Open – VCCIO5 based on JP73 and JP74 settings. Close – VCCIO5 = 1.2 V	Open
JP59	Avant Bank 4 Power Select (VCCIO4)	JP59, JP71 and JP72 select voltage to VCCIO4. Only one of these jumpers should be inserted. Open – VCCIO4 based on JP71 and JP72 settings. Close – VCCIO4 = 1.2 V.	Open
JP60	Avant Bank 3 Power Select (VCCIO3)	JP60, JP69, and JP70 select voltage to VCCIO3. Only one of these jumpers should be inserted. Open – VCCIO3 based on JP69 and JP70 settings. Close – VCCIO3 = 1.2 V	Open
JP61	Avant Bank 7 Power Select (VCCIO7)	JP61, JP75, and JP76 select voltage to VCCIO7. Only one of these jumpers should be inserted. Open – VCCIO7 based on JP75 and JP76 settings. Close – VCCIO7 = 1.2 V	Open
JP62	Avant Bank 8 Power Select (VCCIO8)	JP62, JP77, and JP78 select voltage to VCCIO8. Only one of these jumpers should be inserted. Open – VCCIO8 based on JP77 and JP78 settings. Close – VCCIO8 = 1.2 V	Open
JP65	Avant Ball U3	1–2 – Avant ball U3 connected to Raspberry Pi Header (JP26) pin 26 2–3 – Avant ball U3 connected to 12 MHz oscillator (X1) through JP6 jumper	Open
JP69	Avant Bank 3 Power Select (VCCIO3)	JP60, JP69, and JP70 select voltage to VCCIO3. Only one of these jumpers should be inserted. Open – VCCIO3 based on JP60 and JP70 settings. Close – VCCIO3 = 1.8 V	Close
JP70	Avant Bank 3 Power Select (VCCIO3)	JP60, JP69, and JP70 select voltage to VCCIO3. Only one of these jumpers should be inserted. Open – VCCIO3 based on JP60, and JP69 settings. Close – VCCIO3 = VFMC1_ADJ	Open
JP71	Avant Bank 4 Power Select (VCCIO4)	JP59, JP71, and JP72 select voltage to VCCIO4. Only one of these jumpers should be inserted. Open – VCCIO4 based on JP59, and JP72 settings. Close – VCCIO4 = 1.8 V	Close

Part Designator	Description	Setting	Default
JP72	Avant Bank 4 Power Select (VCCIO4)	JP59, JP71, and JP72 select voltage to VCCIO4. Only one of these jumpers should be inserted. Open – VCCIO4 based on JP59, and JP71 settings. Close – VCCIO4 = VFMC1_ADJ	Open
JP73	Avant Bank 5 Power Select (VCCIO5)	JP58, JP73, and JP74 select voltage to VCCIO5. Only one of these jumpers should be inserted. Open – VCCIO5 based on JP58 and JP74 settings. Close – VCCIO5 = 1.8 V	Close
P74	Avant Bank 5 Power Select (VCCIO5)	JP58, JP73, and JP74 select voltage to VCCIO5. Only one of these jumpers should be inserted. Open – VCCIO5 based on JP58, and JP73 settings. Close – VCCIO5 = VFMC1_ADJ	Open
JP75	Avant Bank 7 Power Select (VCCIO7)	JP61, JP75, and JP76 select voltage to VCCIO7. Only one of these jumpers should be inserted. Open – VCCIO7 based on JP61, and JP76 settings. Close – VCCIO7 = 1.8 V	Close
JP76	Avant Bank 7 Power Select (VCCIO7)	JP61, JP75, and JP76 select voltage to VCCIO7. Only one of these jumpers should be inserted. Open – VCCIO7 based on JP61, and JP75 settings. Close – VCCIO7 = VFMC2_ADJ	Open
JP77	Avant Bank 8 Power Select (VCCIO8)	JP62, JP77, and JP78 select voltage to VCCIO8. Only one of these jumpers should be inserted. Open – VCCIO8 based on JP62, and JP78 settings. Close – VCCIO8 = 1.8 V	Close
JP78	Avant Bank 8 Power Select (VCCIO8)	JP62, JP77, and JP78 select voltage to VCCIO8. Only one of these jumpers should be inserted. Open – VCCIO8 based on JP62 and JP77 settings. Close – VCCIO8 = VFMC2_ADJ	Open
JP83	LPDDR4 ODT_CA_A Enable	1-2 – Turn off the on-die termination for CA pins 2-3 – Turn on the on-die termination for CA pins	Open
JP84	LPDDR4 ODT_CA_B Enable	1-2 – Turn on the on-die termination for CA pins 2-3 – Turn off the on-die termination for CA pins	Open
JP85	LPDDR4 ODT_CA_C Enable	1-2 – Turn off the on-die termination for CA pins 2-3 – Turn on the on-die termination for CA pins	Open
JP86	LPDDR4 ODT_CA_D Enable	1-2 – Turn on the on-die termination for CA pins 2-3 – Turn off the on-die termination for CA pins	Open
JP88	FMC1 Reference Voltage	1-2 – Connects Avant ball AA11 to FMC1 VREF_B_M2C (J48E.K1) 2-3 – Connects Avant ball AA11 to FMC1 VREF_A_M2C (J48D.H1)	Open
JP89	FMC1 Reference Voltage	1-2 – Connects Avant ball AG6 to FMC1 VREF_B_M2C (J48E.K1) 2-3 – Connects Avant ball AG6 to FMC1 VREF_A_M2C (J48D.H1)	Open

Table 3.1. V_{CCIO} Supply Options

V _{CCIO} Bank	3.30 V	2.50 V	1.80 V	1.50 V	1.35 V	1.20 V	1.10 V	1.00 V	0.90 V	FMC_ADJ
V _{CCIO0}	Fixed	—	—	—	—	—	—	—	—	—
V _{CCIO1}	Fixed	—	—	—	—	—	—	—	—	—
V _{CCIO2}	Fixed	—	—	—	—	—	—	—	—	—
V _{CCIO3}	—	—	Default	—	—	Selectable	—	—	—	Selectable
V _{CCIO4}										
V _{CCIO5}										
V _{CCIO6}	—	—	Default	Selectable	Selectable	—	Selectable	Selectable	Selectable	—
V _{CCIO7}	—	—	Default	—	—	Selectable	—	—	—	Selectable
V _{CCIO8}										
V _{CCIO9}	—	—	—	—	—	—	Fixed	—	—	—
V _{CCIO10}										
V _{CCIO11}										
V _{CCIO12}	Default	Selectable	Selectable	—	—	Selectable	—	—	—	—
V _{CCIO13}	Fixed	—	—	—	—	—	—	—	—	—
V _{CCIO14}	Fixed	—	—	—	—	—	—	—	—	—

The Avant-E70 Development Boards provide status LEDs to provide a visual indication of power status (Table 3.2).

Table 3.2. Power Status LED Definition

LED Designator	Color	Description
D1	Yellow green	J2 USB connector
D61	Yellow green	1.00 V power on
D62	Yellow green	3.30 V power on
D63	Yellow green	1.10 V power on
D64	Yellow green	1.80 V power on
D65	Yellow green	1.20 V power on
D66	Yellow green	2.50 V power on
D67	Yellow green	1.50 V power on
D68	Yellow green	0.90 V power on
D69	Yellow green	1.35 V power on
D70	Yellow green	0.82 V to Avant V _{CC} power rails
D73	Yellow green	5.00 V power on
D74	Yellow green	12.00 V from external power source
D75	Yellow green	0.82 V to Avant VCCA_PLLx power rails
D78	Yellow green	3.30 V to Platform Manager 2

4. Programming Platform Manager 2

4.1. JTAG Download Interface

J39 is a stand-alone, eight-pin JTAG header that can be used with an external Lattice Programming Cable (available separately) to interface with the Platform Manager 2 device. For details on the connection between the USB Programming Cable and J39, refer to the [Programming Cables User Guide \(FPGA-UG-02042\)](#). The JTAG connections for Platform Manager 2 are listed in [Table 4.1](#).

Table 4.1. JTAG Header Connections

J39 Pin Number	JTAG Signal Name	Platform Manager 2 Bank	Platform Manager 2 Ball Location for JTAG
1	SB_3V30	—	—
2	PTM_TDO	0	A3
3	PTM_TDI	0	B3
4	—	—	—
5	—	—	—
6	PTM_TMS	0	B4
7	GND	—	—
8	PTM_TCK	0	A4

4.2. Programming for Platform Manager 2

The Lattice Diamond Programmer can be used to program the .jed file in Platform Manager 2. The Lattice Diamond Programmer is integrated into the Lattice Diamond software and is also available as a stand-alone version.

To program Platform Manager 2's configuration flash memory:

Connect the Lattice programming cable fly wires to the Platform Manager 2 JTAG header (J39) as shown in [Table 4.2](#).

Table 4.2. Cable Fly Wire JTAG Connections

J39 Pin Number	JTAG Signal Name	Lattice Programming Cable	
		Cable Wire	Cable Wire Color
1	SB_3V30	VCC	Red
2	PTM_TDO	TDO/SO	Brown
3	PTM_TDI	TDI/SI	Orange
4	—	—	—
5	—	—	—
6	PTM_TMS	TMS	Purple
7	GND	GND	Black
8	PTM_TCK	TCK	White

1. Connect the PC and the Lattice programming cable using the USB cable.
2. In the Lattice Diamond software, click **Tools > Programmer** or in Windows, go to **Start > Lattice Diamond 3.13 > Diamond Programmer**.
3. The Lattice Diamond programmer interface opens as shown in [Figure 4.1](#).

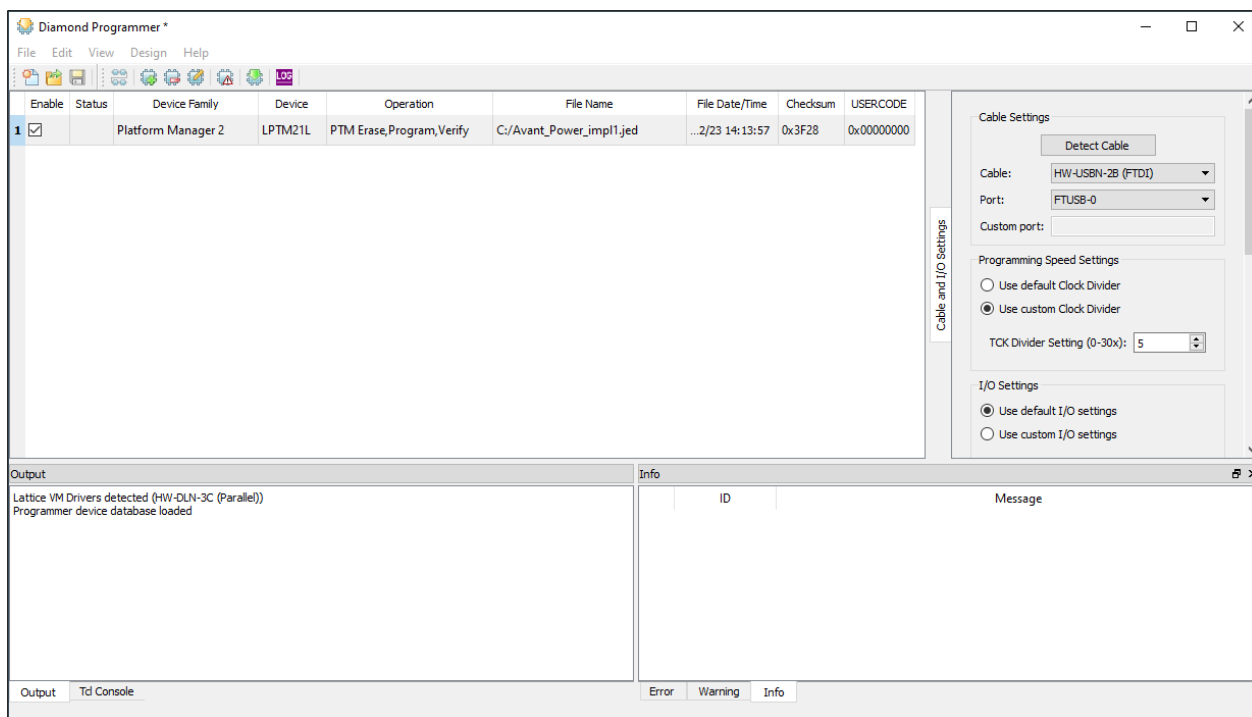


Figure 4.1. Lattice Radiant Programmer

4. Select the .jed file in the **File Name** column.

To program the .jed file, click the **Program** button in the Lattice Diamond Programmer or select **Run > Program Device**. If successful, the **Status** column shows **PASS**. The **Output** pane also shows **INFO—Operation: successful**.

5. Programming Avant-E

The JTAG/SPI programming architecture of the Avant-E70 Development Board is shown in [Figure 5.1](#).

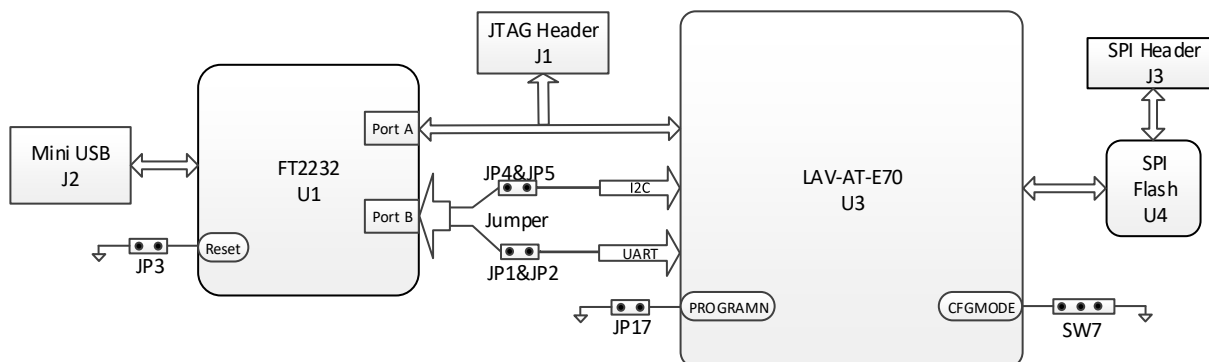


Figure 5.1. Configuration, UART and I2C Architecture

5.1. JTAG Download Interface

The Avant-E70 Development Board has a built-in download controller for programming the Avant device. It uses the FT2232H part of Future Technology Devices International Ltd. (FTDI) to convert USB to JTAG. To use the built-in download cable, connect the USB cable from a PC with Radiant Programmer installed to the mini-USB connector (J2) on the board. A USB-A to USB-B (Mini) cable is included in the Avant-E70 Development Board Kit. The USB hub on the PC detects the cable of the USB function on Port A, making the built-in cable available for use with the Radiant programming software.

5.2. Alternate JTAG Download Interface

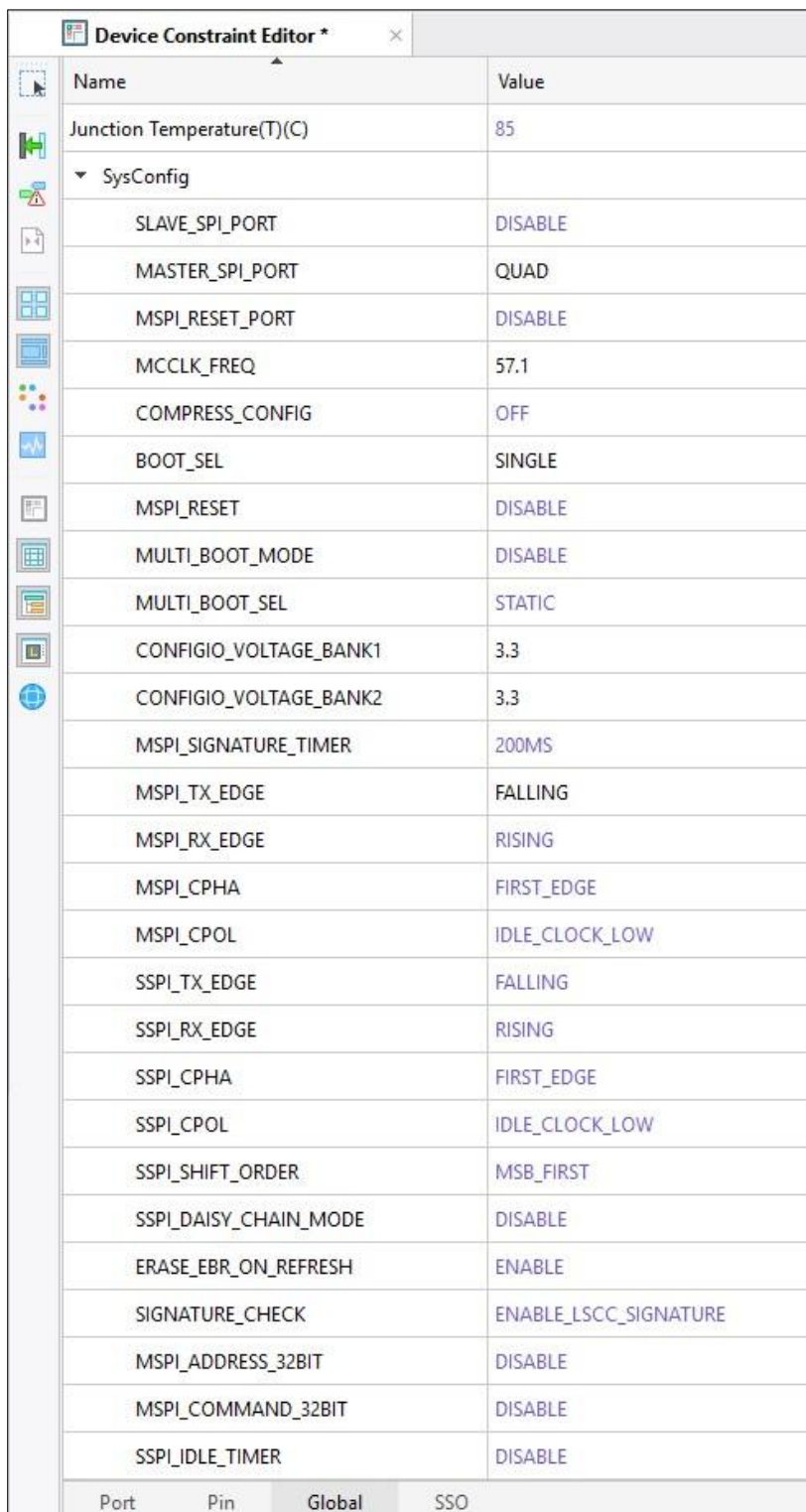
J1 is a stand-alone, eight-pin JTAG header that can be used with an external Lattice Programming Cable that is available separately. When the FTDI part is disabled from the JTAG chain by installing the JP3 jumper, the USB Programming Cable can be connected to J1 to interface with the Avant device. For details on the connection between the USB Programming Cable and J1, refer to the [Programming Cables User Guide \(FPGA-UG-02042\)](#). J1 can also be used as a test point when the configuration from USB to JTAG is working. The JTAG connections are listed in [Table 5.1](#).

Table 5.1. Programming Cable JTAG Connections

J1 Pin Number	JTAG Signal Name	Avant Bank	Avant Ball Location for JTAG
1	VCC_3V30	—	—
2	TDO	2	U2
3	TDI	2	U1
4	—	—	—
5	—	—	—
6	TMS	2	R1
7	GND	—	—
8	TCK	2	T1

5.3. Global Setting in Lattice Radiant software

The Avant-E70 Development Board has been downloaded with the LED blinking project beforehand. Some **Global** settings in the **Device Constraint Editor** are configured. These settings are shown in Figure 5.2, Figure 5.3, and Figure 5.4.



Name	Value
Junction Temperature(T)(C)	85
▼ SysConfig	
SLAVE_SPI_PORT	DISABLE
MASTER_SPI_PORT	QUAD
MSPI_RESET_PORT	DISABLE
MCCLK_FREQ	57.1
COMPRESS_CONFIG	OFF
BOOT_SEL	SINGLE
MSPI_RESET	DISABLE
MULTI_BOOT_MODE	DISABLE
MULTI_BOOT_SEL	STATIC
CONFIGIO_VOLTAGE_BANK1	3.3
CONFIGIO_VOLTAGE_BANK2	3.3
MSPI_SIGNATURE_TIMER	200MS
MSPI_TX_EDGE	FALLING
MSPI_RX_EDGE	RISING
MSPI_CPHA	FIRST_EDGE
MSPI_CPOL	IDLE_CLOCK_LOW
SSPI_TX_EDGE	FALLING
SSPI_RX_EDGE	RISING
SSPI_CPHA	FIRST_EDGE
SSPI_CPOL	IDLE_CLOCK_LOW
SSPI_SHIFT_ORDER	MSB_FIRST
SSPI_DAISSY_CHAIN_MODE	DISABLE
ERASE_EBR_ON_REFRESH	ENABLE
SIGNATURE_CHECK	ENABLE_LSCC_SIGNATURE
MSPI_ADDRESS_32BIT	DISABLE
MSPI_COMMAND_32BIT	DISABLE
SSPI_IDLE_TIMER	DISABLE

Port	Pin	Global	SSO
------	-----	--------	-----

Figure 5.2. Global Settings (1)

Device Constraint Editor *	
Name	Value
MSPI_PREAMBLE_DETECTION_TIMER	200MS
BACKGROUND_RECONFIG	OFF
DAISY_CHAIN	DISABLE
DAISY_CHAIN_WAIT_DONE	DISABLE
TRANSFER	OFF
▼ User Code	
UserCode Format	Binary
UserCode	00000000000000000000000000000000
MultiBoot Offset	000000000000000000000000000000...
▼ Bitstream Revision	
BitstreamRevision Format	Binary
BitstreamRevision	00000000000000000000000000000000
▼ Derating	
Core	NOMINAL
▼ VCCIO	
bank 0	NOMINAL
bank 1	NOMINAL
bank 2	NOMINAL
bank 3	NOMINAL
bank 4	NOMINAL
bank 5	NOMINAL
bank 6	NOMINAL
bank 7	NOMINAL
bank 8	NOMINAL
bank 9	NOMINAL
bank 10	NOMINAL
bank 11	NOMINAL
bank 12	NOMINAL
bank 13	NOMINAL
Port	Pin
Global	SSO

Figure 5.3. Global Settings (2)

Device Constraint Editor *			
Name		Value	
bank 14		NOMINAL	
▼ Bank VCCIO			
Bank0(V)		3.3	
Bank1(V)		3.3	
Bank2(V)		3.3	
Bank3(V)		1.8	
Bank4(V)		1.8	
Bank5(V)		1.8	
Bank6(V)		1.8	
Bank7(V)		1.8	
Bank8(V)		1.8	
Bank9(V)		1.1	
Bank10(V)		1.1	
Bank11(V)		1.1	
Bank12(V)		3.3	
Bank13(V)		3.3	
Bank14(V)		3.3	
Global Set/Reset Net			
Use Primary Net			
Vref Locate			
Port	Pin	Global	SSO

Figure 5.4. Global Settings (3)

5.4. Other Configuration Pins

The Avant-E70 Development Board provides test points for other configuration pins, as shown in [Table 5.2](#).

Table 5.2. Other Configuration Signals

Signal Name	Avant Bank	Avant Ball Location	Test Point	Button/Jumper
PROGRAMN	2	P2	PROGRAMN	SW2/JP17
INITN	2	T5	INIT	—
DONE	2	U4	DONE	—
CFGMODE	2	P1	—	SW7

- **INITN:** Open drain pin. This signal is driven to LOW when the configuration sequence is started, indicating the device is in an initialization state. At this moment, the LED (D4) is lit with a yellow green color. This signal is released after initialization is completed and the configuration download starts.
- **DONE:** Open drain pin. This signal is driven to LOW during configuration time. This signal releasing indicates the device has completed configuration. At this moment, the LED (D5) is lit with a yellow green color.

For more information on Avant JTAG and SPI programming, refer to the [Lattice Avant sysCONFIG User Guide \(FPGA-TN-02299\)](#).

5.5. Programming of Avant SRAM

Radiant Programmer can be used to program the .bit file to the Avant SRAM. Radiant Programmer is integrated into the Radiant Software and is also available as a stand-alone version.

To program the Avant SRAM:

1. Connect the PC and Avant-E70 Development Board (J2) using the USB cable.
2. Set SW7 to the JTAG position.
3. Closed the jumper JP36.
4. In the Lattice Radiant software, click **Tools>Programmer** or in Windows, go to **Start > Lattice Radiant Software 2025.1 > Radiant Programmer**.
5. The Radiant Programmer interface opens as shown in [Figure 5.5](#). Double-click the **Operation** field.

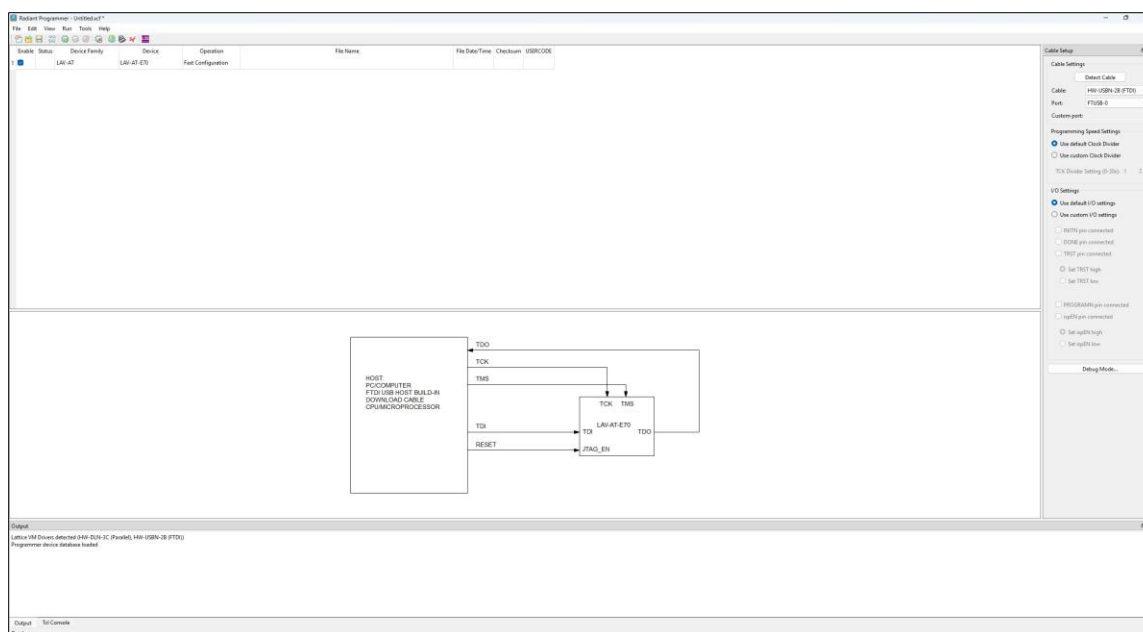


Figure 5.5. Radiant Programmer

6. The Device Properties dialog box opens as shown in [Figure 5.6](#). Select the following options:
- **Target Memory – Configuration Random Access Memory (CRAM)**
 - **Port Interface – JTAG**
 - **Access Mode – Direct Programming**
 - **Operation – Fast Configuration**
 - **Programming file –** Select the .bit file to be programmed.

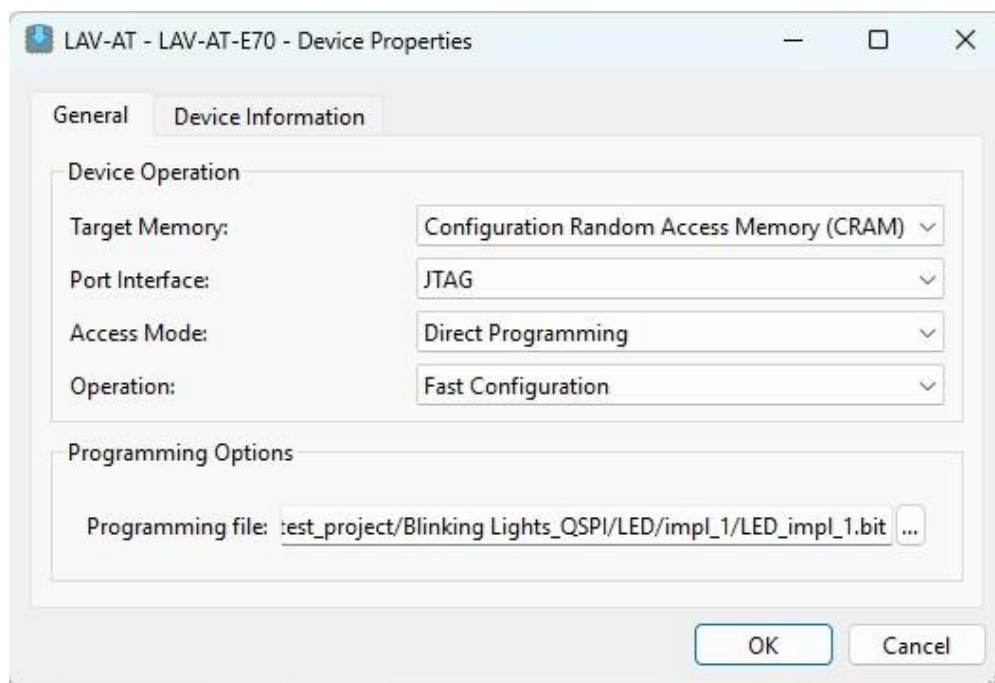


Figure 5.6. Radiant Programmer – Device Properties

7. Click **OK**.

To program the .bit file, click the **Program Device** button in the Lattice Radiant Programmer or select **Run > Program Device**. If successful, the **Status** column shows **PASS**. The **Output** pane also shows **INFO – Operation: successful**.

5.6. Programming of Flash

The on-board Flash (U4) device is a Macronix MX25L51273GZ4I-08G that powers up through the 3.3 V supply. The Flash device can be programmed with Radiant Programmer through the J2 header. Radiant Programmer is integrated into the Lattice Radiant software and is also available as a stand-alone version.

To program the on-board flash:

1. Connect the PC and the Avant-E70 Development board (J2) using the USB cable.
2. Insert the jumper to close JP51.
3. In the Lattice Radiant software, click **Tools>Programmer**, or in Windows, go to **Start > Lattice Radiant Software 2025.1 > Radiant Programmer**.
4. The Lattice Radiant Programmer interface opens ([Figure 5.7](#)). Double-click the **Operation** field.

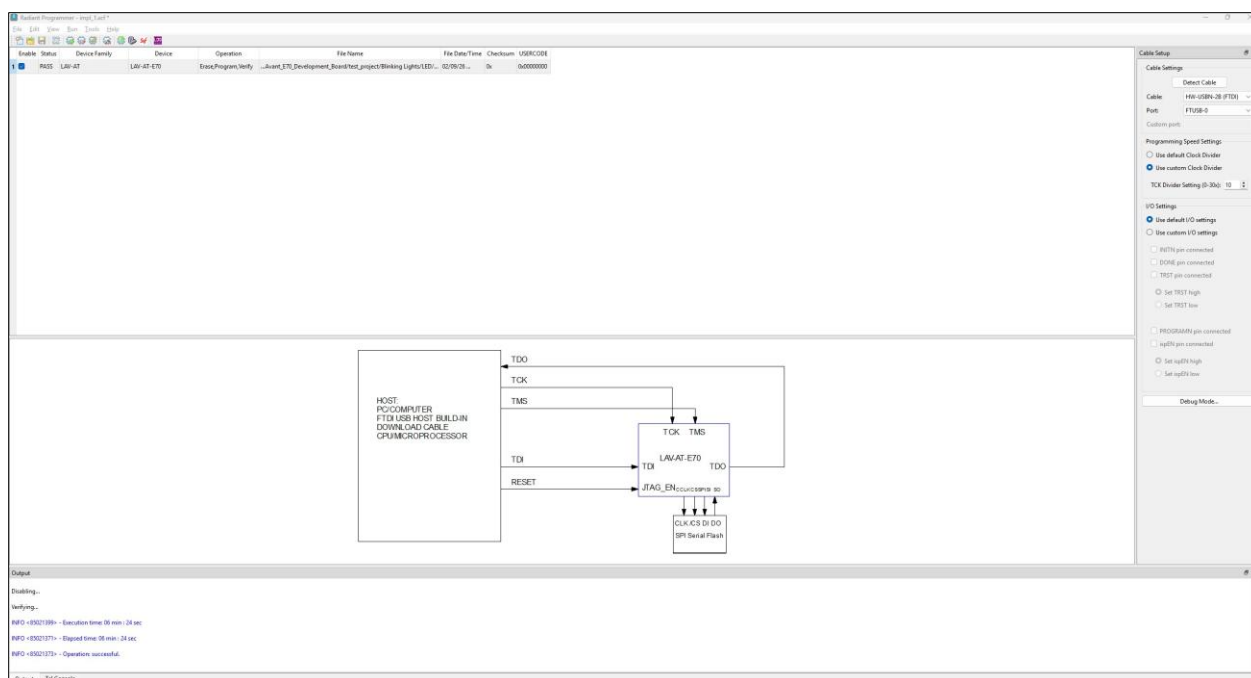


Figure 5.7. Radiant Programmer Interface

5. The Device Properties dialog box opens (Figure 5.8). Select the following options:
 - **Target Memory – External SPI Flash Memory (SPI Flash)**
 - **Port Interface – JTAG2SPI**
 - **Access Mode – Direct Programming**
 - **Operation – Erase, Program, Verify**
 - **Programming file – Select the .bit file to be programmed.**
 - **Family – SPI Serial Flash**
 - **Vendor – Macronix**
 - **Device – MX25L51245G**
 - **Package – 8-land WSON**

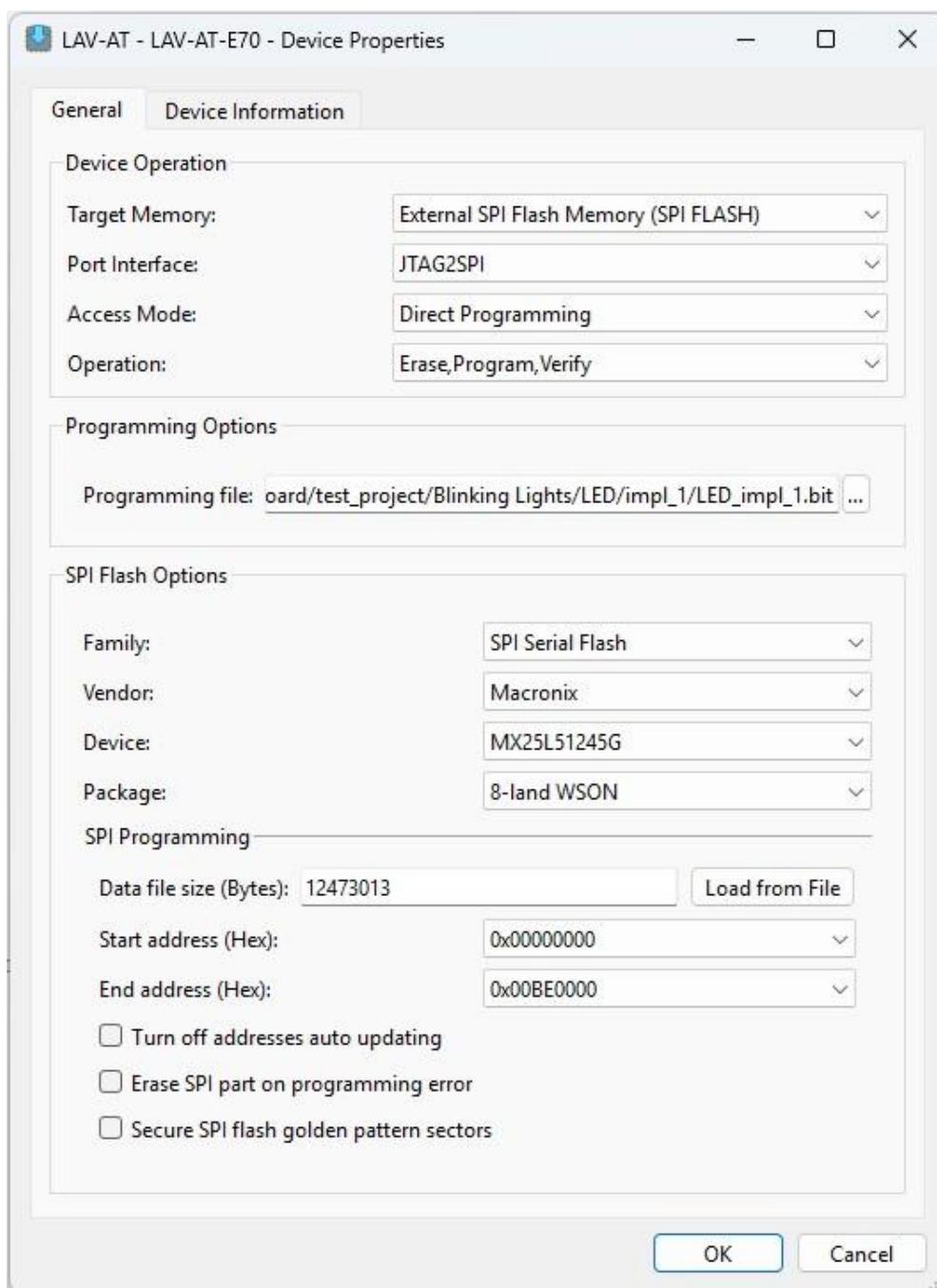


Figure 5.8. Radiant Programmer – Device Properties

6. Click **OK**.
7. Set **TCK Divider Setting (0–30x)**: = 10.

To program the **.bit** file, click the **Program** button in the Lattice Radiant programmer or select **Run>Program Device**. If successful, the **Status** column shows **PASS**. The **Output** pane also shows **INFO – Operation: successful**.

5.7. Boot of Flash

1. Power off the board through J84.
2. Set SW7 to the MSPI position.
3. Insert jumper to close JP51, JP36.
4. Power on the board through J84.
5. If successful, the following LEDs D6,D7,D8,D9,D10,D11,D12,D13,D22,D23,D24,D25,D26,D27,D28, and D29, should blink.

6. Avant Clock Sources

The Avant-E70 Development Board has three options for the Avant clock sources, as shown in [Table 6.1](#).

Table 6.1. Clock Sources

Clock Frequency (MHz)	Signal Name	Avant Bank	Avant Ball Location	Clock Source	Comments
12	12_MHz	2	U3	X1	JP6 is installed and JP65 set to 2-3
100	F_DDR_100MHz_P/N	10	AD32/ AD31	Y1	HCSL differential output
125	125_MHz	1	N7	X3	Jumper JP15 open

7. Control Buses – I2C, UART, and SPI

This section describes the topology of the various configuration and communication buses.

7.1. I2C Topology

The Avant-E70 Development Board has four sets of I2C buses. One I2C bus is through the output port B of the FTDI chip. The second I2C bus is out of Bank 6 at a header. There is an I2C bus for each of the FMC connectors. The I2C connections are summarized in [Table 7.1](#).

Table 7.1. I2C Bus Connections

Signal Name	Avant Bank	Avant Ball Location	Other Connection	Comments
SCL	14	R12	U1.38	R103 and JP4 need to be installed.
SDA	14	T11	U1.39 and U1.40	R104 and JP5 need to be installed.
B6_SCL	6	AH16	JP64.3	Debug Header
B6_SDA	6	AG16	JP64.1	Debug Header
FMC1_SCL	0	T8	J48.C30 and J10.10	FMC Header and Debug Header
FMC1_SDA	0	U8	J48.C31 and J10.14	FMC Header and Debug Header
FMC2_SCL	13	R15	J54.C30 and J53.10	FMC Header and Debug Header
FMC2_SDA	13	R14	J54.C31 and J53.14	FMC Header and Debug Header

7.2. UART Topology

The board provides one UART communication interface by providing a flexible connection between the Avant device and the FTDI chip. Close the two jumpers, JP1 and JP2, to connect to two general-purpose I/O in Bank 2, as shown in [Table 7.2](#). This UART connection is shared with the I2C bus connection on the FTDI device.

Table 7.2. UART Bus Connections

Signal Name	Avant Bank	Avant Ball Location	FTDI Chip Ball Location	Jumper
TXD_UART	2	T3	38	JP1
RXD_UART	2	R3	39	JP2

7.3. SPI Topology

7.3.1. SPI Configuration

One of the major functions of SPI connections on the board is to support Avant configuration from the SPI Flash or the Parallel Configuration Header (J3), as shown in [Table 7.3](#). The Avant-E70 Development Board can support both Controller SPI (MSPI) and Target SPI (SSPI) modes for Avant configuration. Jumper JP51 selects chip select connection to flash (U4), either from Avant or Header J3.

Table 7.3. SPI Bus Connections

Signal Name	Avant Bank	Avant Ball	Parallel Configuration Header Pin
SPI_MCLK	1	P9	12
DQ0_MOSI	1	L12	5
DQ1_MISO	1	L11	7
CSSPIN	1	P7	8
DQ2	1	L10	11
DQ3	1	L9	9
FLASH_CS	—	—	2

7.4. LPDDR4 Topology

The board provides one 64-bit LPDDR4 communication interface between the Avant device and the LPDDR4 chip. This LPDDR4 interface provides a high bandwidth data cache channel. To implement this function, you need to use three general-purpose I/O in Bank 9, 10 and 11, as shown in [Table 7.4](#).

Table 7.4. LPDDR4 Interface Connections

Signal Name	Avant Bank	Avant Ball	LPDDR4 Chip Ball Location
LPDDR4_DQ11_C	9	AF28	U119.F11
LPDDR4_DQ10_C	9	AF29	U119.E11
LPDDR4_DQ3_D	9	AJ31	U119.U2
LPDDR4_DQ2_D	9	AJ32	U119.V2
LPDDR4_DQ15_C	9	AF30	U119.B9
LPDDR4_DQ14_C	9	AG30	U119.C9
LPDDR4_DQ7_D	9	AJ34	U119.AA4
LPDDR4_DQ6_D	9	AJ33	U119.Y4
LPDDR4_UDQS_C_P	9	AF31	U119.D10
LPDDR4_UDQS_C_N	9	AG31	U119.E10
LPDDR4_LDQS_D_P	9	AK29	U119.W3
LPDDR4_LDQS_D_N	9	AK30	U119.V3
LPDDR4_DQ9_C	9	AG32	U119.C11
LPDDR4_DQ8_C	9	AF32	U119.B11
LPDDR4_DQ1_D	9	AK31	U119.Y2
LPDDR4_DQ0_D	9	AK32	U119.AA2
LPDDR4_DQ13_C	9	AH34	U119.E9
LPDDR4_DQ12_C	9	AG34	U119.F9
LPDDR4_DQ5_D	9	AK33	U119.V4
LPDDR4_DQ4_D	9	AK34	U119.U4
LPDDR4_UDM_C	9	AG33	U119.C10
LPDDR4_LDM_D	9	AM30	U119.Y3
LPDDR4_DQ11_D	9	AG27	U119.U11
LPDDR4_DQ10_D	9	AG28	U119.V11
LPDDR4_DQ15_D	9	AH29	U119.AA9
LPDDR4_DQ14_D	9	AG29	U119.Y9
LPDDR4_UDQS_D_P	9	AH30	U119.W10
LPDDR4_UDQS_D_N	9	AJ30	U119.V10
LPDDR4_DQ9_D	9	AJ28	U119.Y11
LPDDR4_DQ8_D	9	AJ29	U119.AA11
LPDDR4_DQ13_D	9	AH26	U119.V9
LPDDR4_DQ12_D	9	AG26	U119.U9
LPDDR4_UDM_D	9	AJ27	U119.Y10
LPDDR4_CLK_A_P	10	AB25	U5.J8 & U5.P8 & U119.J8 & U119.P8
LPDDR4_CLK_A_N	10	AC25	U5.J9 & U5.P9 & U119.J9 & U119.P9
LPDDR4_CKE_A	10	AB26	U5.J4 & U5.P4 & U119.J4 & U119.P4
LPDDR4_A0_A	10	AC26	U5.H2 & U5.R2 & U119.H2 & U119.R2
LPDDR4_A1_A	10	AB27	U5.J2 & U5.P2 & U119.J2 & U119.P2
LPDDR4_A2_A	10	AB28	U5.H9 & U5.R9 & U119.H9 & U119.R9
LPDDR4_A3_A	10	AC29	U5.H10 & U5.R10 & U119.H10 & U119.R10
LPDDR4_A4_A	10	AB29	U5.H11 & U5.R11 & U119.H11 & U119.R11
LPDDR4_CS_A	10	AA31	U5.H4 & U5.R4 & U119.H4 & U119.R4

Signal Name	Avant Bank	Avant Ball	LPDDR4 Chip Ball Location
LPDDR4_A5_A	10	AD27	U5.J11 & U5.P11 & U119.J11 & U119.P11
F_DDR_100MHz_P	10	AD32	—
F_DDR_100MHz_N	10	AD31	—
LPDDR4_DQ3_A	10	AE24	U5.F2
LPDDR4_DQ2_A	10	AE25	U5.E2
LPDDR4_DQ11_A	10	AE31	U5.F11
LPDDR4_DQ10_A	10	AE32	U5.E11
LPDDR4_DQ7_A	10	AC24	U5.B4
LPDDR4_DQ6_A	10	AB24	U5.C4
LPDDR4_DQ15_A	10	AB33	U5.B9
LPDDR4_DQ14_A	10	AB34	U5.C9
LPDDR4_LDQS_A_P	10	AC23	U5.D3
LPDDR4_LDQS_A_N	10	AD23	U5.E3
LPDDR4_UDQS_A_P	10	AC34	U5.D10
LPDDR4_UDQS_A_N	10	AC33	U5.E10
LPDDR4_DQ1_A	10	AD21	U5.C2
LPDDR4_DQ0_A	10	AD22	U5.B2
LPDDR4_DQ9_A	10	AD33	U5.C11
LPDDR4_DQ8_A	10	AD34	U5.B11
LPDDR4_DQ5_A	10	Y21	U5.E4
LPDDR4_DQ4_A	10	AA21	U5.F4
LPDDR4_DQ13_A	10	AE34	U5.E9
LPDDR4_DQ12_A	10	AE33	U5.F9
LPDDR4_LDM_A	10	AC21	U5.C3
LPDDR4_UDM_A	10	AF33	U5.C10
LPDDR4_RESET	10	AF34	U5.T11 & U119.T11
LPDDR4_DQ4_C	11	AA27	U119.F4
LPDDR4_DQ5_C	11	Y27	U119.E4
LPDDR4_DQ4_B	11	Y28	U5.U4
LPDDR4_DQ5_B	11	AA28	U5.V4
LPDDR4_DQ0_C	11	V28	U119.B2
LPDDR4_DQ1_C	11	U28	U119.C2
LPDDR4_DQ0_B	11	U29	U5.AA2
LPDDR4_DQ1_B	11	V29	U5.Y2
LPDDR4_LDQS_C_P	11	U27	U119.D3
LPDDR4_LDQS_C_N	11	V27	U119.E3
LPDDR4_LDQS_B_P	11	Y29	U5.W3
LPDDR4_LDQS_B_N	11	W29	U5.V3
LPDDR4_DQ6_C	11	AA26	U119.C4
LPDDR4_DQ7_C	11	Y26	U119.B4
LPDDR4_DQ6_B	11	V30	U5.Y4
LPDDR4_DQ7_B	11	W30	U5.AA4
LPDDR4_DQ2_C	11	W26	U119.E2
LPDDR4_DQ3_C	11	V26	U119.F2
LPDDR4_DQ2_B	11	U30	U5.V2
LPDDR4_DQ3_B	11	U31	U5.U2
LPDDR4_LDM_C	11	V25	U119.C3
LPDDR4_LDM_B	11	V32	U5.Y3

Signal Name	Avant Bank	Avant Ball	LPDDR4 Chip Ball Location
LPDDR4_DQ12_B	11	U25	U5.U9
LPDDR4_DQ13_B	11	T25	U5.V9
LPDDR4_DQ8_B	11	AA24	U5.AA11
LPDDR4_DQ9_B	11	Y24	U5.Y11
LPDDR4_UDQS_B_P	11	W23	U5.W10
LPDDR4_UDQS_B_N	11	W24	U5.V10
LPDDR4_DQ14_B	11	U24	U5.Y9
LPDDR4_DQ15_B	11	T24	U5.AA9
LPDDR4_DQ10_B	11	U23	U5.V11
LPDDR4_DQ11_B	11	U22	U5.U11
LPDDR4_UDM_B	11	V22	U5.Y10

8. LEDs, Switches and Segment Displays

This section describes the Avant-E70 Development Board LEDs, switches, and segment displays that can be used in demo and customer designs.

8.1. DIP Switch

Eight Avant pins are connected to the DIP switch (SW3) to allow manual actuating input to the FPGA. The OFF side of each switch is connected to GPIOs within Bank 6 and is pulled up through 4.7 kΩ resistors. The ON side of each switch is grounded. The designated pins are connected as shown in [Table 8.1](#).

Table 8.1. DIP Switch Signals

Signal Name	Avant Ball Location	Avant Bank
DIP_SW1	AA16	6
DIP_SW2	AA17	6
DIP_SW3	AL16	6
DIP_SW4	AM16	6
DIP_SW5	AB16	6
DIP_SW6	AB17	6
DIP_SW7	AP16	6
DIP_SW8	AN16	6

8.2. General Purpose Push Buttons

The Avant-E70 Development Board provides four push-button switches, SW1, SW2, SW4, and SW5, for demo and user applications. One of the buttons is a pre-defined functional pin, and the other three are generic pins. Pressing these buttons drives a logic level “0” to the corresponding I/O pins. The designated pins are connected, as shown in [Table 8.2](#).

Table 8.2. Push Button Switch Signals

Signal Name	Avant Bank	Avant Ball Location	Push Button Reference	Logic Level at Button Pressed
PROGRAMN	2	P2	SW2	0
PUSHBUTTON1	6	AC17	SW1	0
PUSHBUTTON2	6	AC16	SW4	0
PUSHBUTTON3	6	AP15	SW5	0

For more information on PROGRAMN, refer to the [Lattice Avant sysCONFIG User Guide \(FPGA-TN-02299\)](#). SW1, SW4, and SW5 can be used as generic input.

8.3. General Purpose LEDs

The Avant-E70 Development Board provides 16 LEDs that are connected to I/O within Banks 1 and 6. The LEDs are all yellow green, as shown in [Table 8.3](#).

Table 8.3. General Purpose LED Signals

Signal Name	Avant Ball Location	Avant Bank	LED	Avant Color
LED_0	L8	1	D6	Yellow green
LED_1	P8	1	D7	Yellow green
LED_2	M8	1	D8	Yellow green
LED_3	M9	1	D9	Yellow green
LED_4	P10	1	D10	Yellow green
LED_5	N10	1	D11	Yellow green
LED_6	AL10	6	D12	Yellow green
LED_7	AL11	6	D13	Yellow green
LED_8	AN15	6	D22	Yellow green
LED_9	AH17	6	D23	Yellow green
LED_10	AG17	6	D24	Yellow green
LED_11	AM14	6	D25	Yellow green
LED_12	AL14	6	D26	Yellow green
LED_13	AK17	6	D27	Yellow green
LED_14	AJ17	6	D28	Yellow green
LED_15	AN14	6	D29	Yellow green

8.4. Segment Displays

The Avant-E70 Development Board provides a 3-Character, 7-Segment LED display (D60) that is connected to I/O within Bank 14. The designated pins are connected, as shown in [Table 8.4](#).

Table 8.4. Segment Display

Signal Name	Avant Ball Location	Avant Bank	Segment Display
SEG_A	V10	14	A
SEG_B	T10	14	B
SEG_C	V12	14	C
SEG_D	V13	14	D
SEG_E	W10	14	E
SEG_F	V11	14	F
SEG_G	W12	14	G
SEG_DP	W11	14	DP
K_DIG1	W9	14	K_DIG1
K_DIG2	V9	14	K_DIG2
K_DIG3	R10	14	K_DIG3

9. Headers/Connectors and Avant Device Ball Mapping

This section describes the Avant-E70 Development Board headers, connectors, and ball mapping. FMC1 occupies Bank 3, Bank 4, and Bank 5. FMC1 supports the connection of LA[0:33], HA[0:23], and HB[0:12] signals. FMC2 occupies Bank 7 and Bank 8. FMC2 supports the connection of LA[0:33] and HA[0:11] signals.

9.1. FMC1 Connector

Table 9.1. FMC1 Pin Connections

J48 Pin Name	Signal Name	Avant Bank	Avant Ball Location
B1	FMC1_RES1	0	V5
B40	FMC1_RES0	0	W5
C10	FMC1_LA06_P	3	Y8
C11	FMC1_LA06_N	3	Y9
C14	FMC1_LA10_P	3	Y5
C15	FMC1_LA10_N	3	AA5
C18	FMC1_LA14_P	3	AC3
C19	FMC1_LA14_N	3	AC2
C22	FMC1_LA18_CLK_P	4	AH1
C23	FMC1_LA18_CLK_N	4	AJ1
C26	FMC1_LA27_P	4	AF10
C27	FMC1_LA27_N	4	AE10
C30	FMC1_SCL	0	T8
C31	FMC1_SDA	0	U8
C34	FMC1_GA0	—	—
D1	FMC1_PG_C2M	0	V4
D8	FMC1_LA01_CLK_P	3	AC8
D9	FMC1_LA01_CLK_N	3	AC9
D11	FMC1_LA05_P	3	AA8
D12	FMC1_LA05_N	3	AA9
D14	FMC1_LA09_P	3	AA2
D15	FMC1_LA09_N	3	Y2
D17	FMC1_LA13_P	3	AA4
D18	FMC1_LA13_N	3	Y4
D20	FMC1_LA17_CLK_P	4	AP2
D21	FMC1_LA17_CLK_N	4	AP3
D23	FMC1_LA23_P	4	AF3
D24	FMC1_LA23_N	4	AE3
D26	FMC1_LA26_P	4	AE11
D27	FMC1_LA26_N	4	AF11
D29	FMC1_TCK	0	T7
D30	FMC1_TDI	0	W1
D31	FMC1_TDO	0	V1
D33	FMC1_TMS	0	W7
D34	FMC1_TRST_L	—	—
D35	FMC1_GA1	—	—
E2	FMC1_HA01_CLK_P	5	AF12
E3	FMC1_HA01_CLK_N	5	AE12
E6	FMC1_HA05_P	5	AB14

J48 Pin Name	Signal Name	Avant Bank	Avant Ball Location
E7	FMC1_HA05_N	5	AB15
E9	FMC1_HA09_P	5	AG12
E10	FMC1_HA09_N	5	AG13
E12	FMC1_HA13_P	5	AH9
E13	FMC1_HA13_N	5	AG9
E15	FMC1_HA16_P	5	AK10
E16	FMC1_HA16_N	5	AK11
E18	FMC1_HA20_P	5	AM6
E19	FMC1_HA20_N	5	AM5
F1	FMC1_PG_M2C	0	W4
F4	FMC1_HA00_CLK_P	5	AJ12
F5	FMC1_HA00_CLK_N	5	AJ11
F7	FMC1_HA04_P	5	AA15
F8	FMC1_HA04_N	5	AA14
F10	FMC1_HA08_P	5	AG10
F11	FMC1_HA08_N	5	AG11
F13	FMC1_HA12_P	5	AH7
F14	FMC1_HA12_N	5	AH8
F16	FMC1_HA15_P	5	AK5
F17	FMC1_HA15_N	5	AK6
F19	FMC1_HA19_P	5	AK9
F20	FMC1_HA19_N	5	AK8
G2	FMC1_CLK1_M2C_P	4	AF6
G3	FMC1_CLK1_M2C_N	4	AE6
G6	FMC1_LA00_CLK_P	3	AB7
G7	FMC1_LA00_CLK_N	3	AA7
G9	FMC1_LA03_P	3	Y11
G10	FMC1_LA03_N	3	Y10
G12	FMC1_LA08_P	3	AB4
G13	FMC1_LA08_N	3	AB5
G15	FMC1_LA12_P	3	AA3
G16	FMC1_LA12_N	3	Y3
G18	FMC1_LA16_P	3	AD2
G19	FMC1_LA16_N	3	AD1
G21	FMC1_LA20_P	4	AE2
G22	FMC1_LA20_N	4	AF2
G24	FMC1_LA22_P	4	AG1
G25	FMC1_LA22_N	4	AG2
G27	FMC1_LA25_P	4	AL1
G28	FMC1_LA25_N	4	AK1
G30	FMC1_LA29_P	4	AG7
G31	FMC1_LA29_N	4	AG8
G33	FMC1_LA31_P	4	AF9
G34	FMC1_LA31_N	4	AE9
G36	FMC1_LA33_P	4	AM4
G37	FMC1_LA33_N	4	AL4
H1	FMC1_VREFA	3/4/5	AA11/AG6/AF13
H2	FMC1_PRSNT_M2C_L	0	U7

J48 Pin Name	Signal Name	Avant Bank	Avant Ball Location
H4	FMC1_CLK0_M2C_P	3	Y7
H5	FMC1_CLK0_M2C_N	3	Y6
H7	FMC1_LA02_P	3	AB13
H8	FMC1_LA02_N	3	AB12
H10	FMC1_LA04_P	3	AC13
H11	FMC1_LA04_N	3	AC12
H13	FMC1_LA07_P	3	Y1
H14	FMC1_LA07_N	3	AA1
H16	FMC1_LA11_P	3	AD3
H17	FMC1_LA11_N	3	AD4
H19	FMC1_LA15_P	3	AC7
H20	FMC1_LA15_N	3	AC6
H22	FMC1_LA19_P	4	AE4
H23	FMC1_LA19_N	4	AF4
H25	FMC1_LA21_P	4	AJ2
H26	FMC1_LA21_N	4	AK2
H28	FMC1_LA24_P	4	AH2
H29	FMC1_LA24_N	4	AJ3
H31	FMC1_LA28_P	4	AH6
H32	FMC1_LA28_N	4	AH5
H34	FMC1_LA30_P	4	AN1
H35	FMC1_LA30_N	4	AM1
H37	FMC1_LA32_P	4	AN4
H38	FMC1_LA32_N	4	AP4
J2	FMC1_CLK3_M2C_P	4	AF1
J3	FMC1_CLK3_M2C_N	4	AE1
J6	FMC1_HA03_P	5	AC15
J7	FMC1_HA03_N	5	AC14
J9	FMC1_HA07_P	5	AH10
J10	FMC1_HA07_N	5	AJ10
J12	FMC1_HA11_P	5	AL5
J13	FMC1_HA11_N	5	AL6
J15	FMC1_HA14_P	5	AP9
J16	FMC1_HA14_N	5	AP8
J18	FMC1_HA18_P	5	AM8
J19	FMC1_HA18_N	5	AM9
J21	FMC1_HA22_P	5	AP5
J22	FMC1_HA22_N	5	AP6
K4	FMC1_CLK2_M2C_P	5	AJ5
K5	FMC1_CLK2_M2C_N	5	AJ6
K7	FMC1_HA02_P	5	AE14
K8	FMC1_HA02_N	5	AF14
K10	FMC1_HA06_P	5	AK7
K11	FMC1_HA06_N	5	AJ7
K13	FMC1_HA10_P	5	AL8
K14	FMC1_HA10_N	5	AL9
K16	FMC1_HA17_CLK_P	5	AN7
K17	FMC1_HA17_CLK_N	5	AP7

J48 Pin Name	Signal Name	Avant Bank	Avant Ball Location
K19	FMC1_HA21_P	5	AN6
K20	FMC1_HA21_N	5	AN5
K22	FMC1_HA23_P	5	AN9
K23	FMC1_HA23_N	5	AN8
K25	FMC1_HB00_P_CC	3	AB1
K26	FMC1_HB00_N_CC	3	AC1
J24	FMC1_HB01_P	3	AD9
J25	FMC1_HB01_N	3	AD10
F22	FMC1_HB02_P	3	AD6
F23	FMC1_HB02_N	3	AD5
E21	FMC1_HB03_P	3	AC4
E22	FMC1_HB03_N	3	AC5
F25	FMC1_HB04_P	3	AB10
F26	FMC1_HB04_N	3	AC10
E24	FMC1_HB05_P	3	AD7
E25	FMC1_HB05_N	3	AD8
K28	FMC1_HB06_P_CC	4	AL2
K29	FMC1_HB06_N_CC	4	AM2
J27	FMC1_HB07_P	3	AD12
J28	FMC1_HB07_N	3	AD11
F28	FMC1_HB08_P	4	AE7
F29	FMC1_HB08_N	4	AF7
E27	FMC1_HB09_P	4	AE5
E28	FMC1_HB09_N	4	AF5
K31	FMC1_HB10_P	4	AM3
K32	FMC1_HB10_N	4	AN3
J30	FMC1_HB11_P	4	AJ4
J31	FMC1_HB11_N	4	AK4
F31	FMC1_HB12_P	4	AH4
F32	FMC1_HB12_N	4	AH3

9.2. FMC2 Connector

Table 9.2. FMC2 Pin Connections

J54 Pin Name	Signal Name	Avant Bank	Avant Ball Location
B1	FMC2_RES1	13	R18
B40	FMC2_RES0	13	R19
C10	FMC2_LA06_P	7	AB18
C11	FMC2_LA06_N	7	AA18
C14	FMC2_LA10_P	7	AN20
C15	FMC2_LA10_N	7	AP20
C18	FMC2_LA14_P	7	AM23
C19	FMC2_LA14_N	7	AL23
C22	FMC2_LA18_CLK_P	8	AK24
C23	FMC2_LA18_CLK_N	8	AK23
C26	FMC2_LA27_P	8	AP28
C27	FMC2_LA27_N	8	AP27

J54 Pin Name	Signal Name	Avant Bank	Avant Ball Location
C30	FMC2_SCL	13	R15
C31	FMC2_SDA	13	R14
C34	FMC2_GA0	—	—
D1	FMC2_PG_C2M	13	T18
D8	FMC2_LA01_CLK_P	7	AP22
D9	FMC2_LA01_CLK_N	7	AN22
D11	FMC2_LA05_P	7	AE18
D12	FMC2_LA05_N	7	AE19
D14	FMC2_LA09_P	7	AF19
D15	FMC2_LA09_N	7	AF20
D17	FMC2_LA13_P	7	AK21
D18	FMC2_LA13_N	7	AK22
D20	FMC2_LA17_CLK_P	8	AN28
D21	FMC2_LA17_CLK_N	8	AM28
D23	FMC2_LA23_P	8	AB19
D24	FMC2_LA23_N	8	AA19
D26	FMC2_LA26_P	8	Y20
D27	FMC2_LA26_N	8	AA20
D29	FMC2_TCK	13	U15
D30	FMC2_TDI	13	U16
D31	FMC2_TDO	13	U17
D33	FMC2_TMS	13	W14
D34	FMC2_TRST_L	—	—
D35	FMC2_GA1	—	—
E2	FMC2_HA01_CLK_P	7	AP17
E3	FMC2_HA01_CLK_N	7	AN17
E6	FMC2_HA05_P	8	AM26
E7	FMC2_HA05_N	8	AM25
E9	FMC2_HA09_P	7	AD17
E10	FMC2_HA09_N	7	AE17
F1	FMC2_PG_M2C	13	T19
F4	FMC2_HA00_CLK_P	8	AM24
F5	FMC2_HA00_CLK_N	8	AL24
F7	FMC2_HA04_P	8	AN25
F8	FMC2_HA04_N	8	AP25
F10	FMC2_HA08_P	7	AH18
F11	FMC2_HA08_N	7	AG18
G2	FMC2_CLK1_M2C_P	8	AE22
G3	FMC2_CLK1_M2C_N	8	AE23
G6	FMC2_LA00_CLK_P	7	AJ18
G7	FMC2_LA00_CLK_N	7	AK18
G9	FMC2_LA03_P	7	Y17
G10	FMC2_LA03_N	7	Y18
G12	FMC2_LA08_P	7	AM18
G13	FMC2_LA08_N	7	AL18
G15	FMC2_LA12_P	7	AM21
G16	FMC2_LA12_N	7	AL21
G18	FMC2_LA16_P	7	AJ22

J54 Pin Name	Signal Name	Avant Bank	Avant Ball Location
G19	FMC2_LA16_N	7	AJ21
G21	FMC2_LA20_P	8	AE20
G22	FMC2_LA20_N	8	AE21
G24	FMC2_LA22_P	8	AC20
G25	FMC2_LA22_N	8	AB20
G27	FMC2_LA25_P	8	AJ23
G28	FMC2_LA25_N	8	AH23
G30	FMC2_LA29_P	8	AH24
G31	FMC2_LA29_N	8	AH25
G33	FMC2_LA31_P	8	AG25
G34	FMC2_LA31_N	8	AF25
G36	FMC2_LA33_P	8	AK28
G37	FMC2_LA33_N	8	AK27
H1	FMC2_VREFA	7/8	AF18/AF24
H2	FMC2_PRSNT_M2C_L	13	T15
H4	FMC2_CLK0_M2C_P	7	AG20
H5	FMC2_CLK0_M2C_N	7	AH20
H7	FMC2_LA02_P	7	AK19
H8	FMC2_LA02_N	7	AJ19
H10	FMC2_LA04_P	7	AM17
H11	FMC2_LA04_N	7	AL17
H13	FMC2_LA07_P	7	AK20
H14	FMC2_LA07_N	7	AJ20
H16	FMC2_LA11_P	7	AN19
H17	FMC2_LA11_N	7	AP19
H19	FMC2_LA15_P	7	AH21
H20	FMC2_LA15_N	7	AH22
H22	FMC2_LA19_P	8	AD19
H23	FMC2_LA19_N	8	AD20
H25	FMC2_LA21_P	8	AF21
H26	FMC2_LA21_N	8	AG21
H28	FMC2_LA24_P	8	AG23
H29	FMC2_LA24_N	8	AG24
H31	FMC2_LA28_P	8	AK25
H32	FMC2_LA28_N	8	AL25
H34	FMC2_LA30_P	8	AL27
H35	FMC2_LA30_N	8	AL28
H37	FMC2_LA32_P	8	AL29
H38	FMC2_LA32_N	8	AM29
J2	FMC2_CLK3_M2C_P	8	AP29
J3	FMC2_CLK3_M2C_N	8	AN29
J6	FMC2_HA03_P	8	AN24
J7	FMC2_HA03_N	8	AP24
J9	FMC2_HA07_P	7	AL20
J10	FMC2_HA07_N	7	AM20
J12	FMC2_HA11_P	7	AN18
J13	FMC2_HA11_N	7	AP18
K1	FMC2_VREFB	—	—

J54 Pin Name	Signal Name	Avant Bank	Avant Ball Location
K4	FMC2_CLK2_M2C_P	7	AP21
K5	FMC2_CLK2_M2C_N	7	AN21
K7	FMC2_HA02_P	8	AP26
K8	FMC2_HA02_N	8	AN26
K10	FMC2_HA06_P	8	AL26
K11	FMC2_HA06_N	8	AK26
K13	FMC2_HA10_P	7	AN23
K14	FMC2_HA10_N	7	AP23

9.3. Parallel FMC1 Configuration Header

Table 9.3. Parallel FMC1 Configuration Header Pin Connections

J10 Pin Name	Signal Name	Avant Bank	Avant Ball Location
1	VCC_3V30	—	—
2	VCC_3V30	—	—
3	FMC1_TCK	0	T7
4	FMC1_PG_C2M	0	V4
5	FMC1_PG_M2C	0	W4
6	FMC1_TRST_L	—	—
7	FMC1_TDI	0	W1
8	FMC1_PRST_M2C_L	0	U7
9	FMC1_TDO	0	V1
10	FMC1_SCL	0	T8
11	GND	—	—
12	GND	—	—
13	FMC1_TMS	0	W7
14	FMC1_SDA	0	U8

9.4. Parallel FMC2 Configuration Header

Table 9.4. Parallel FMC2 Configuration Header Pin Connections

J53 Pin Name	Signal Name	Avant Bank	Avant Ball Location
1	VCC_3V30	—	—
2	VCC_3V30	—	—
3	FMC2_TCK	13	U15
4	FMC2_PG_C2M	13	T18
5	FMC2_PG_M2C	13	T19
6	FMC2_TRST_L	—	—
7	FMC2_TDI	13	U16
8	FMC2_PRST_M2C_L	13	T15
9	FMC2_TDO	13	U17
10	FMC2_SCL	13	R15
11	GND	—	—
12	GND	—	—
13	FMC2_TMS	13	W14
14	FMC2_SDA	13	R14

9.5. Raspberry PI Board GPIO Header

The Avant-E70 Development Board provides a 40-pin receptacle that is compatible with the GPIO header of Raspberry Pi 2/3 serial models or can be used for general-purpose I/O.

Table 9.5. Raspberry PI header Pin Connections

JP26 Pin Name	Signal Name	Avant Bank	Avant Ball Location
1	VCC_3V30 ¹	—	—
2	VCC_5V00 ¹	—	—
3	RASP_IO02	13	V15
4	VCC_5V00 ¹	—	—
5	RASP_IO03	13	T13
6	GND	—	—
7	RASP_IO04	2	P6
8	RASP_IO14	13	V14
9	GND	—	—
10	RASP_IO15	13	R13
11	RASP_IO17	13	V16
12	RASP_IO18	14	T12
13	RASP_IO27	2	P3
14	GND	—	—
15	RASP_IO22	0	W6
16	RASP_IO23	2	P4
17	VCC_3V30 ¹	—	—
18	RASP_IO24	2	N5
19	RASP_IO10	2	R6
20	GND	—	—
21	RASP_IO09	2	R5
22	RASP_IO25	0	V2
23	RASP_IO11	14	U12
24	RASP_IO08	2	P5
25	GND	—	—
26	RASP_IO07 ²	2	U3
27	RASP_ID_SD	14	T11
28	RASP_ID_SC	14	R12
29	RASP_IO05	14	V8
30	GND	—	—
31	RASP_IO06	14	W8
32	RASP_IO12	2	U5
33	RASP_IO13	14	R9
34	GND	—	—
35	RASP_IO19	14	R11
36	RASP_IO16	2	N6
37	RASP_IO26	14	T9
38	RASP_IO20	0	T6
39	GND	—	—
40	RASP_IO21	0	U6

Notes:

1. 3.3 V and 5 V provide power to the Raspberry PI board when JP12 and JP13 are installed. When JP12 and JP13 are not installed, the Raspberry PI needs its own 3.3 V and 5 V power.
2. When JP65 = 1–2, RASP_IO07 is routed to Avant Ball U3.

When connecting directly to a Raspberry PI board, depending on the individual setup, an adapter may be needed to avoid mechanical interference between the two boards. A generic 40-pin (2×20), 100-mil spacing header extender serves this function. Alternately, the two boards can be connected by a length of ribbon cable with 2×20 connectors on either end.

9.6. External Flash Configuration Header

Table 9.6. SPI Flash Configuration Header Pin Connections

J3 Pin Name	Signal Name	Avant Bank	Avant Ball Location
1	PROGRAMN	2	P2
2	FLASH_CS ¹	—	—
3	—	—	—
4	DONE	2	U4
5	DQ0_MOSI	1	L12
6	INITN	2	T5
7	DQ1_MISO	1	L11
8	CSSPIN	1	P7
9	DQ3	1	L9
10	VCCIO1_IN	—	—
11	DQ2	1	L10
12	SPI_MCLK	1	P9
13	GND	—	—
14	GND	—	—

Note:

1. Connected to Pin 1 of the Flash (U4) device. It can be connected to the Avant FPGA through JP51.

9.7. PMOD Header

J6 and J7 headers can be used as GPIOs or as connectors for PMOD interfaces.

Table 9.7. PMOD Header Pin Connections

	Pin Name	Signal Name	Avant Bank	Avant Ball Location
J6	1	PMOD2_1	12	P18
	2	PMOD2_2	12	N19
	3	PMOD2_3	12	N20
	4	PMOD2_4	12	P20
	7	PMOD2_5	12	R17
	8	PMOD2_6	12	M19
	9	PMOD2_7	12	M20
	10	PMOD2_8	12	P19

	Pin Name	Signal Name	Avant Bank	Avant Ball Location
J7	1	PMOD3_1	12	P14
	2	PMOD3_2	12	N15
	3	PMOD3_3	12	N16
	4	PMOD3_4	12	R16
	7	PMOD3_5	12	P13
	8	PMOD3_6	12	N14
	9	PMOD3_7	12	P15
	10	PMOD3_8	12	N17

9.8. Through Hole Extended Area

Table 9.8. Through Hole Extended Area Pin Connections

	Pin Name	Signal Name	Avant Bank	Avant Ball Location
	TP_AN13	EPS1_AN13_P	6	AN13
	TP_AP13	EPS1_AP13_N	6	AP13
	TP_AJ16	EPS2_AJ16	6	AJ16
	TP_AK16	EPS2_AK16	6	AK16
	TP_AL13	EPS3_AL13_P	6	AL13
	TP_AM13	EPS3_AM13_N	6	AM13
	TP_AG15	EPS4_AG15_P	6	AG15
	TP_AH15	EPS4_AH15_N	6	AH15
	TP_AK13	EPS5_AK13_P	6	AK13
	TP_AK12	EPS5_AK12_N	6	AK12
	TP_AF15	EPS6_AF15_P	6	AF15
	TP_AF16	EPS6_AF16_N	6	AF16
	TP_AP12	EPS7_AP12_P	6	AP12
	TP_AN12	EPS7_AN12_N	6	AN12
	TP_AH14	EPS8_AH14_P	6	AH14
	TP_AG14	EPS8_AG14_N	6	AG14
	TP_AP10	EPS9_AP10_P	6	AP10
	TP_AP11	EPS9_AP11_N	6	AP11
	TP_AK14	EPS10_AK14_P	6	AK14
	TP_AK15	EPS10_AK15_N	6	AK15
	0V82	VCC_0V82	—	—
	0V9	VCC_0V90	—	—
	1V	VCC_1V00	—	—
	1V1	VCC_1V10	—	—
	1V2	VCC_1V20	—	—
	1V35	VCC_1V35	—	—
	1V5	VCC_1V50	—	—
	1V8	VCC_1V80	—	—
	2V5	VCC_2V50	—	—
	3V3	VCC_3V30	—	—
	F1_3V3	VFMC1_3V30	—	—
	F2_3V3	VFMC2_3V30	—	—
	F1_3V3AUX	VFMC1_3V30AUX	—	—
	F2_3V3AUX	VFMC2_3V30AUX	—	—

Pin Name	Signal Name	Avant Bank	Avant Ball Location
F1_ADJ	VFMC1_ADJ	—	—
F2_ADJ	VFMC2_ADJ	—	—
5V	VCC_5V00	—	—
12V	VCC_12V00	—	—
GND6	GND	—	—
GND7	GND	—	—
GND8	GND	—	—
GND9	GND	—	—
GND10	GND	—	—
GND11	GND	—	—
GND12	GND	—	—
GND13	GND	—	—
GND14	GND	—	—
GND15	GND	—	—

10. Software Requirements

The following software versions are required to develop designs for the Avant-E70 Development Board:

- Lattice Radiant Software 2023.2 or later
- Lattice Radiant Programmer 2023.2 or later
- Lattice Diamond Software 3.13 or later
- Lattice Diamond Programmer 3.13 or later

11. Storage and Handling

Static electricity can shorten the life span of electronic components. Observe these tips to prevent damage that can occur from electrostatic discharge:

- Use antistatic precautions, such as operating on an antistatic mat and wearing an antistatic wristband.
- Store the development board in the packaging provided.
- Touch a metal USB housing to equalize the voltage potential between you and the board.

12. Ordering Information

Table 12.1. Ordering Information

Description	Ordering Part Number	China RoHS Environment-Friendly Use Period (EFUP)
Avant-E70 Development Board	LAV-E70-D-EVN LAV-E70-D-EVN-AS LAV-E70-D-EVN-ES LAV-E70-D-EVN-ES1	

Appendix A. Avant-E70 Development Schematics

Avant-E70 Development Board REVA	
01 - Title Page	
02 - Block Diagram	
03 - USB Interface	
04 - Bank-0,1 External Flash	
05 - Bank-2 JTAG, UART	
06 - Bank-3,4,5 FMC1	
07 - FMC1 LA&HA	
08 - Bank-6 LED, SWITCH	
09 - Bank-7,8 FMC2	
10 - FMC2 LA	
11 - Bank-9,10,11 LPDDR4	
12 - Bank-12,13 PMODs	
13 - Bank-14 Segment & RPi	
14 - Bank Power	
15 - Power Decoupling	
16 - Power Supplies 1	
17 - Power Supplies 2	
18 - Ground	
19 - Platform Manager 2	
20 - USB Power Sink	
21 - Power Block Diagram	

		Lattice Semiconductor Applications Email: techsupport@latticesemi.com	
Title Page			
Size B	Project Avant-E70 Development Board	Schematic Rev 1.0	Board Rev A
Date: Tuesday, February 10, 2026	Sheet 1	of 21	

Figure A.1. Title Page

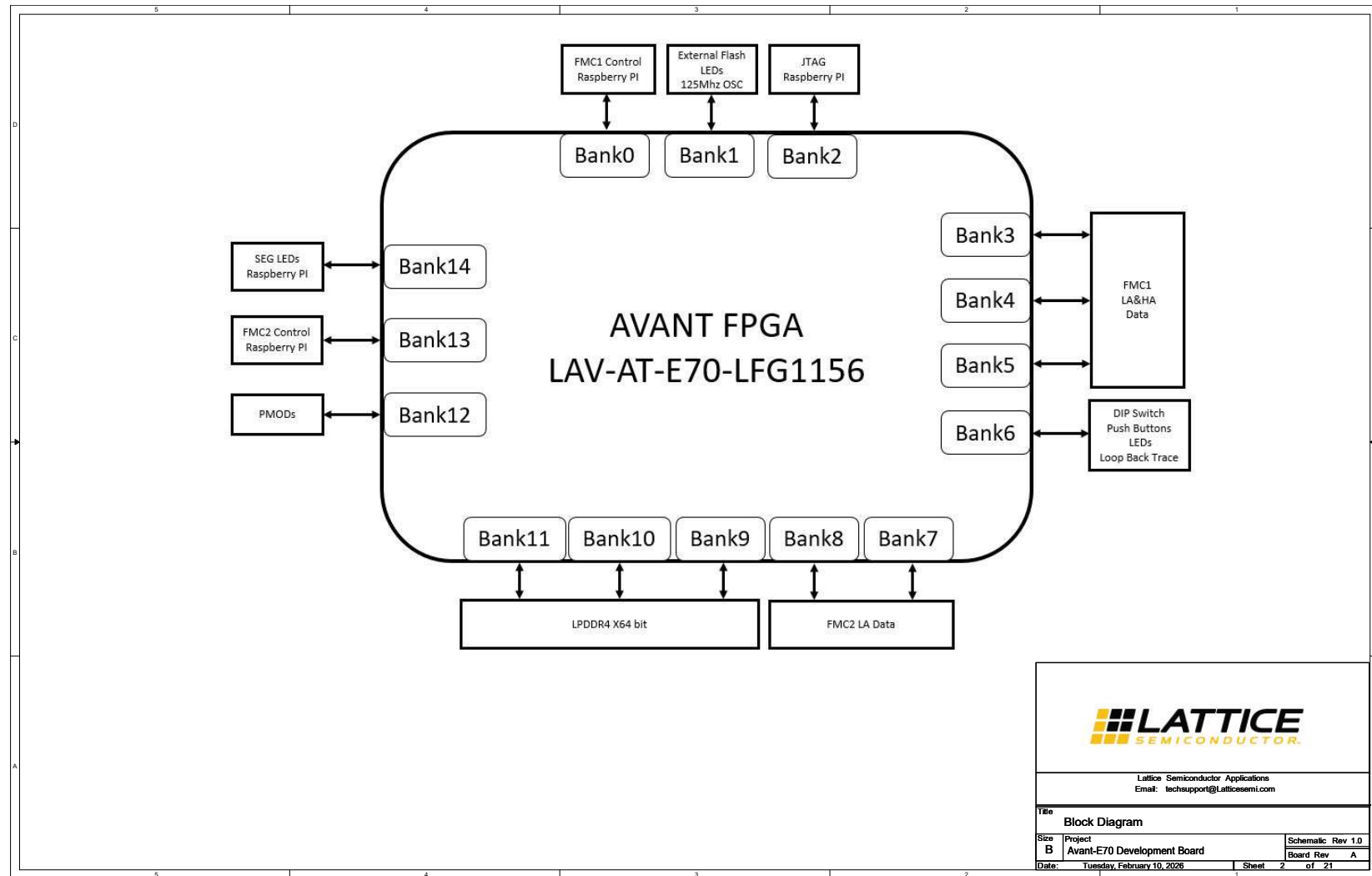


Figure A.2. Block Diagram



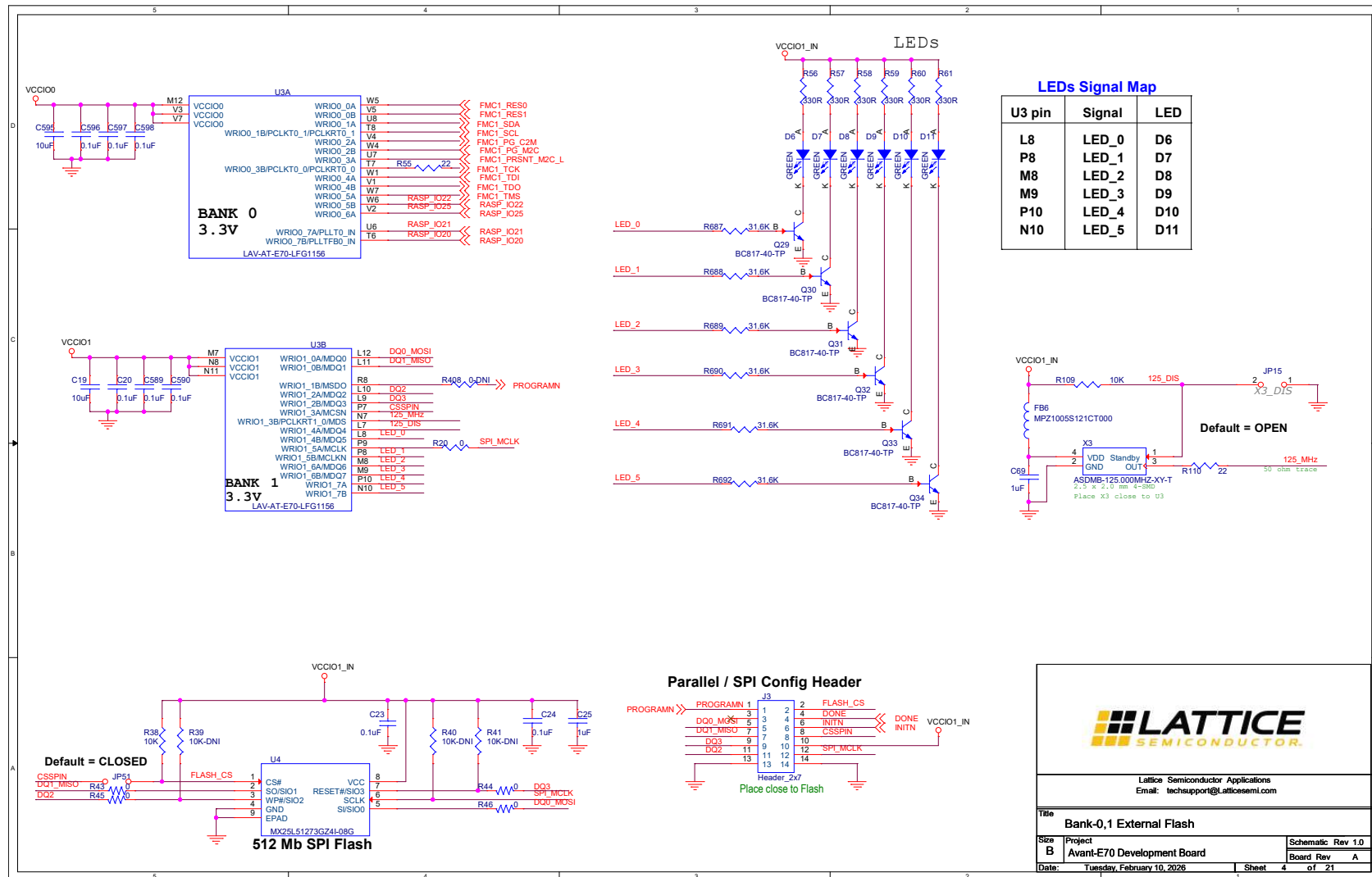


Figure A.4. Bank-0, 1 External Flash

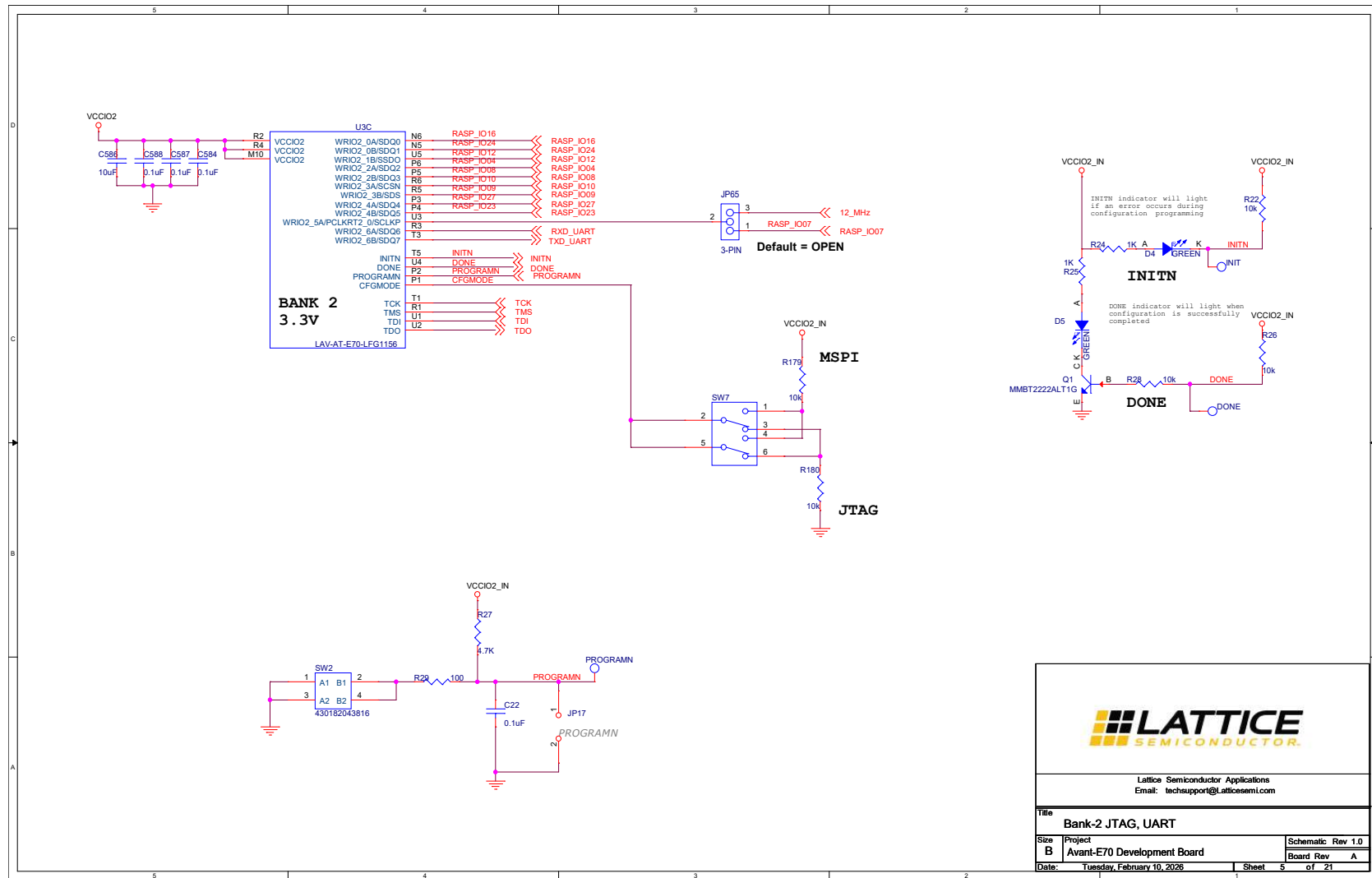


Figure A.5. Bank-2 JTAG, UART

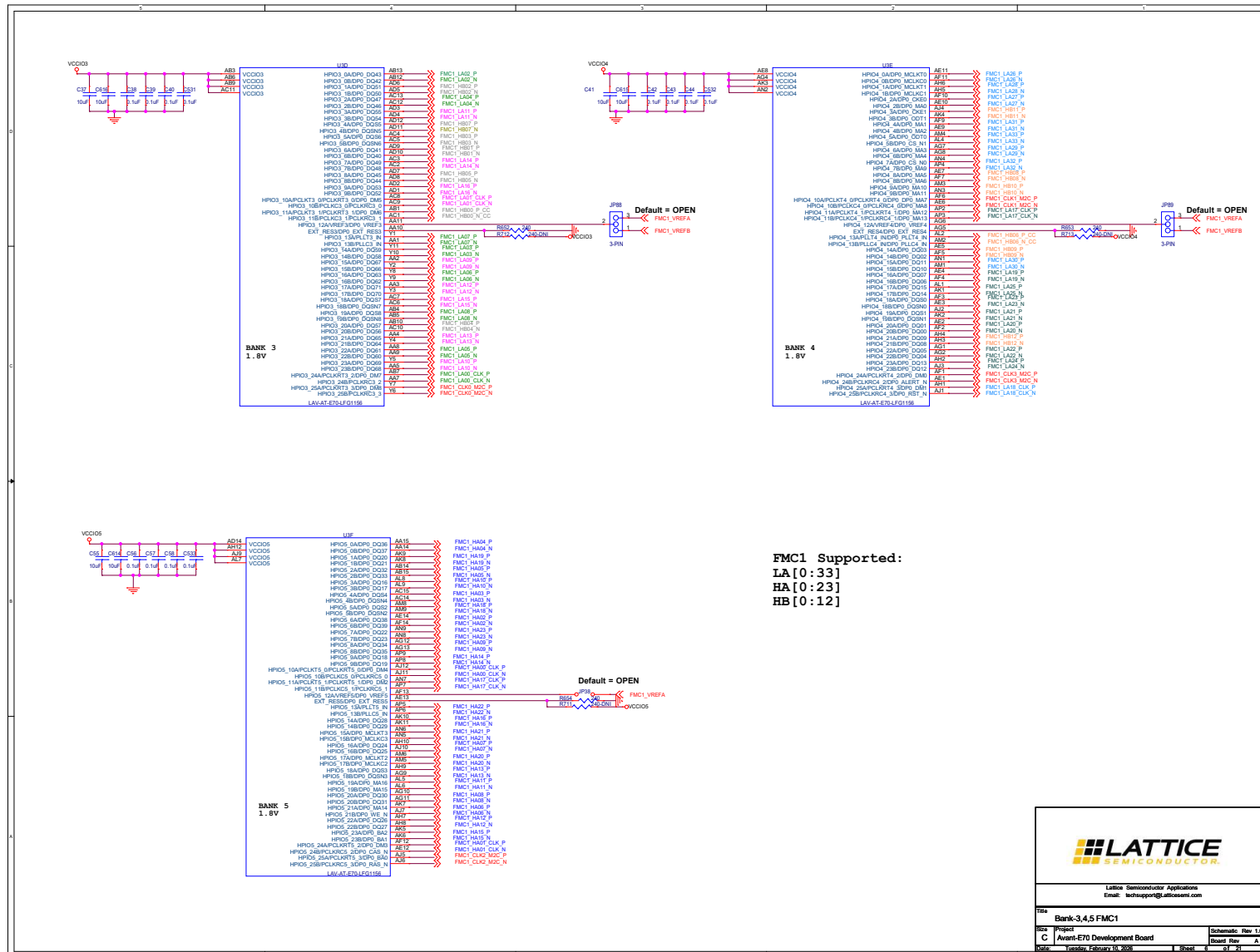


Figure A.6. Bank-3, 4, 5 FMC1



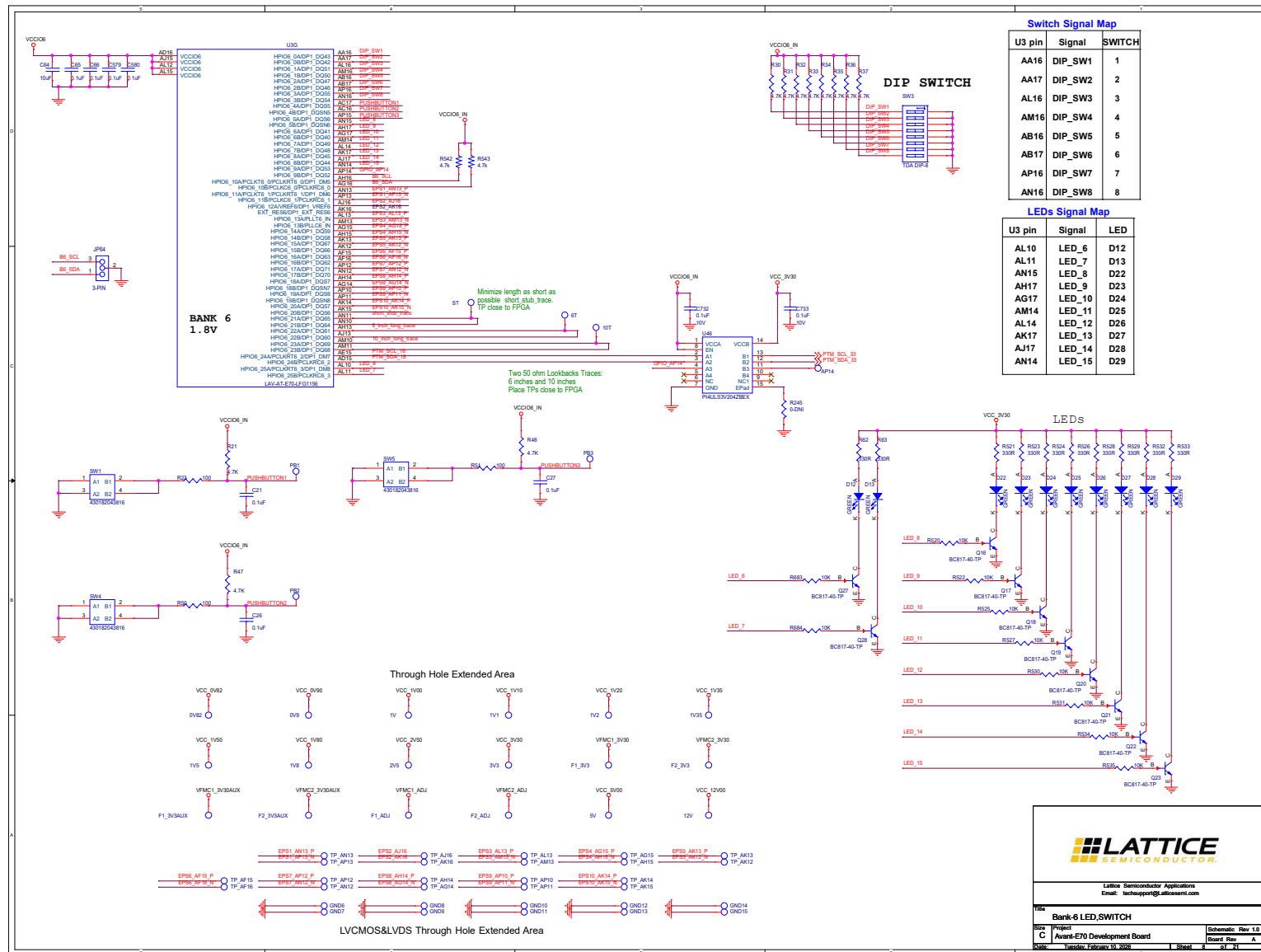


Figure A.8. Bank-6 LED, SWITCH

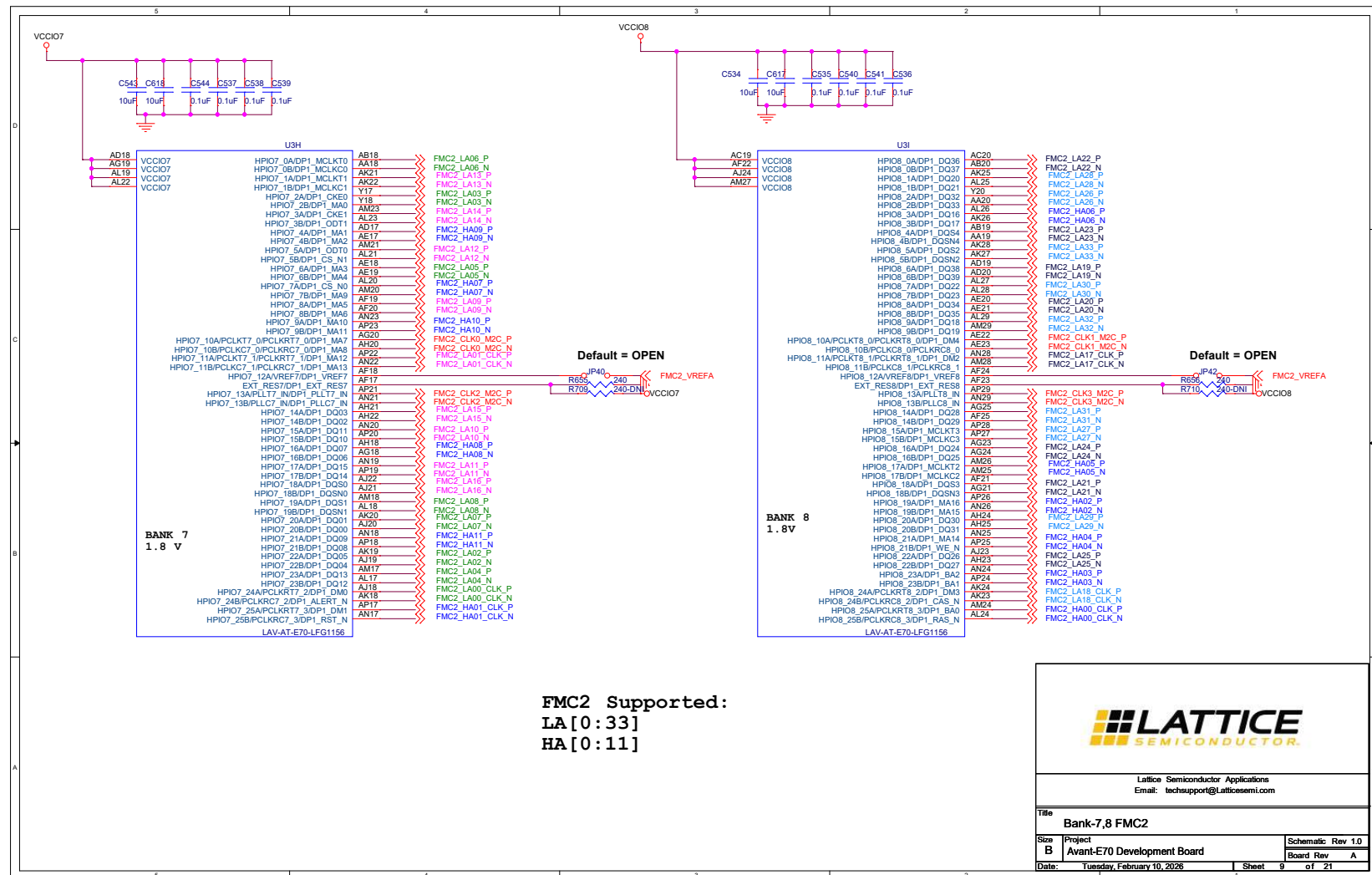
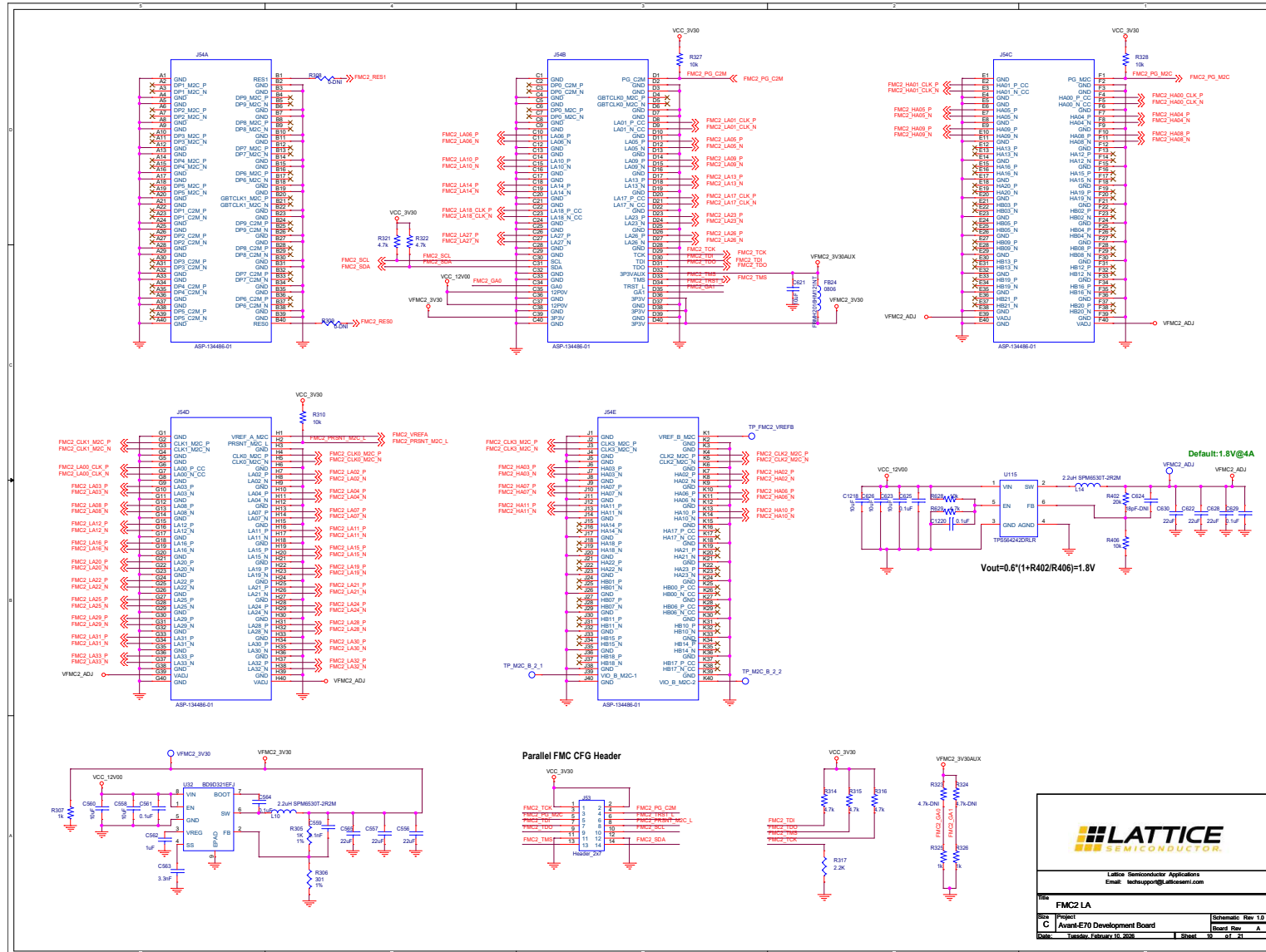


Figure A.9. Bank-7, 8 FMC2



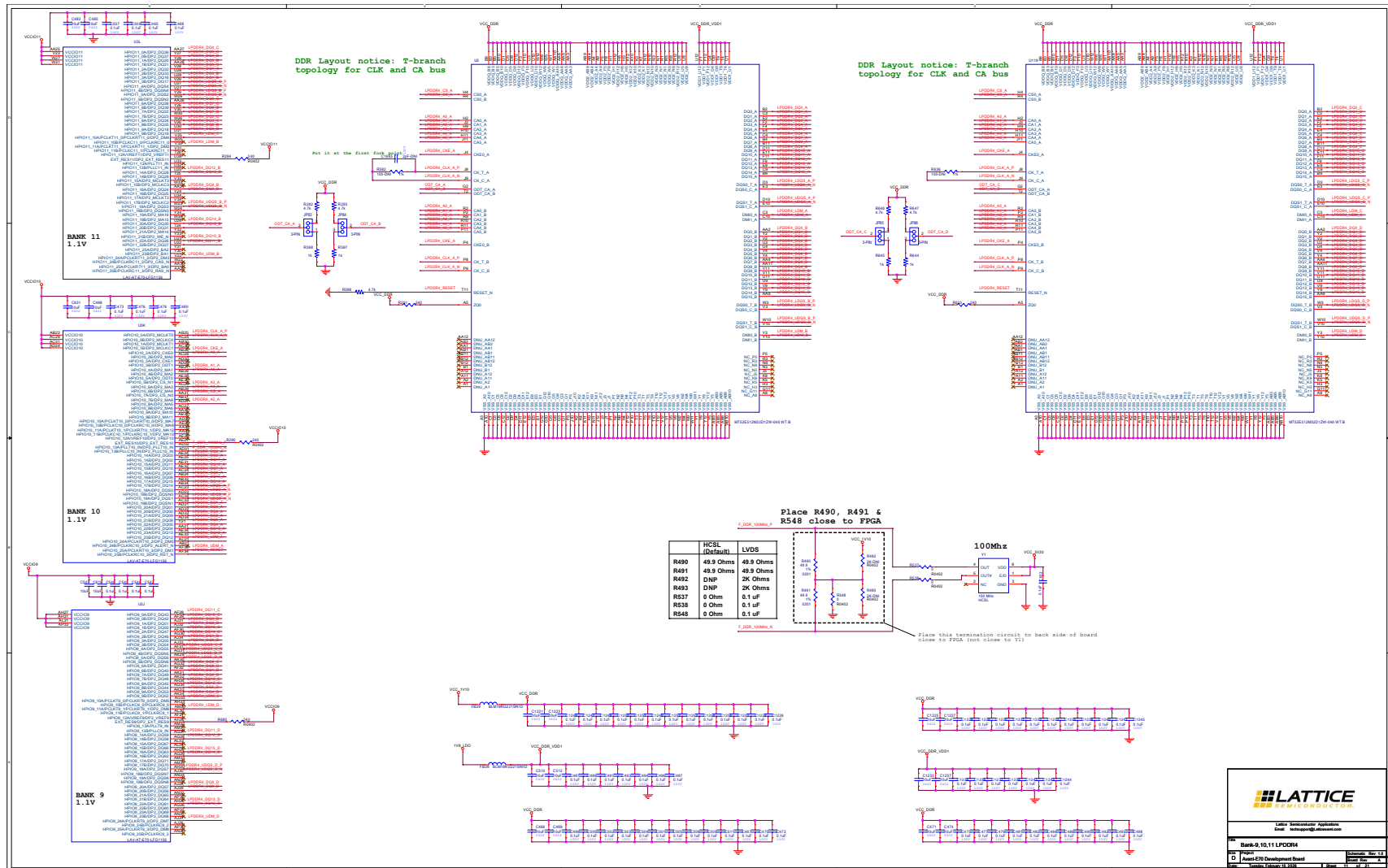


Figure A.11. Bank-9, 10, 11 LPDDR4

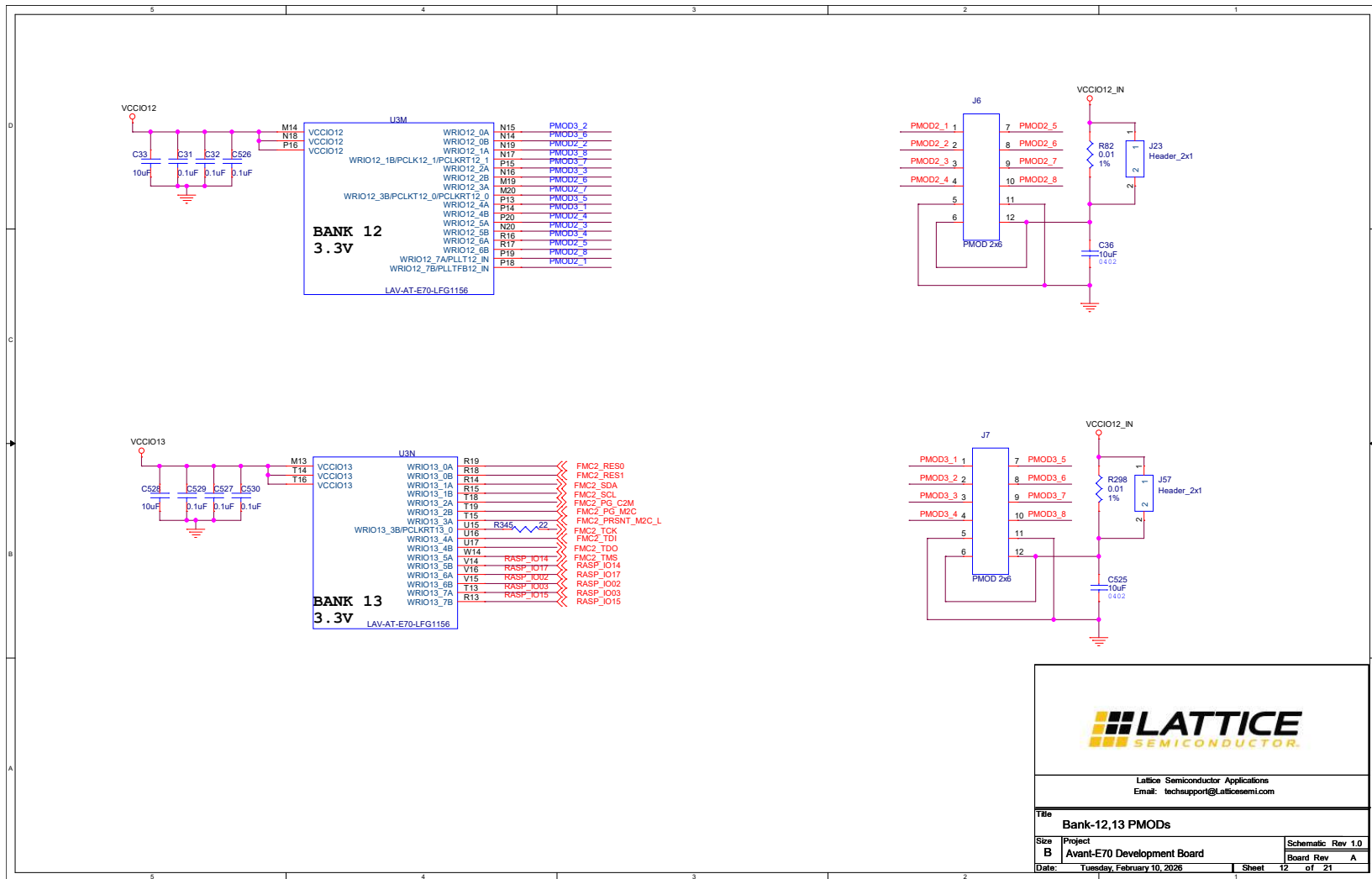


Figure A.12. Bank-12, 13 PMODs

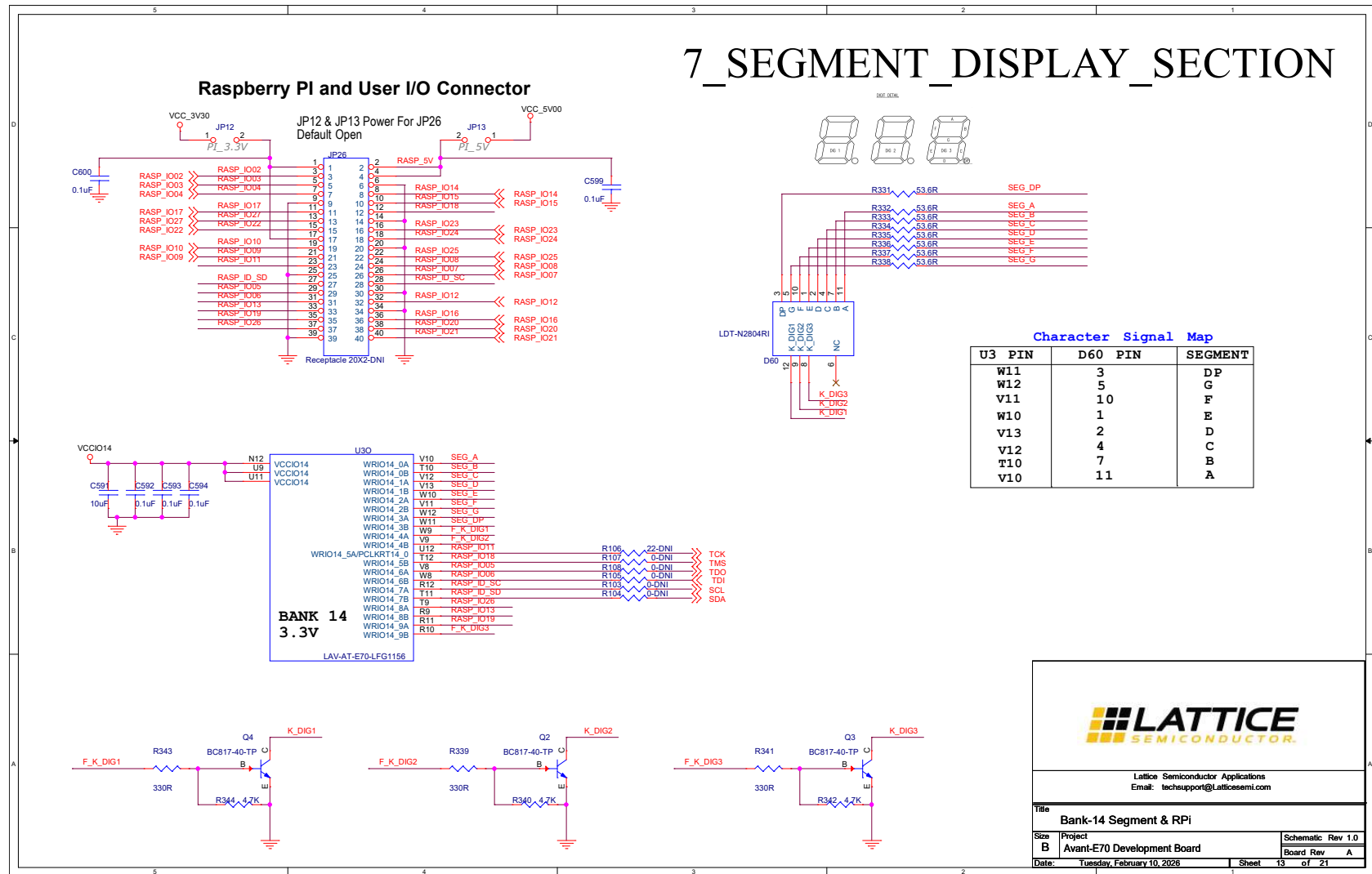
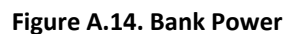


Figure A.13. Bank-14 Segment & RPI







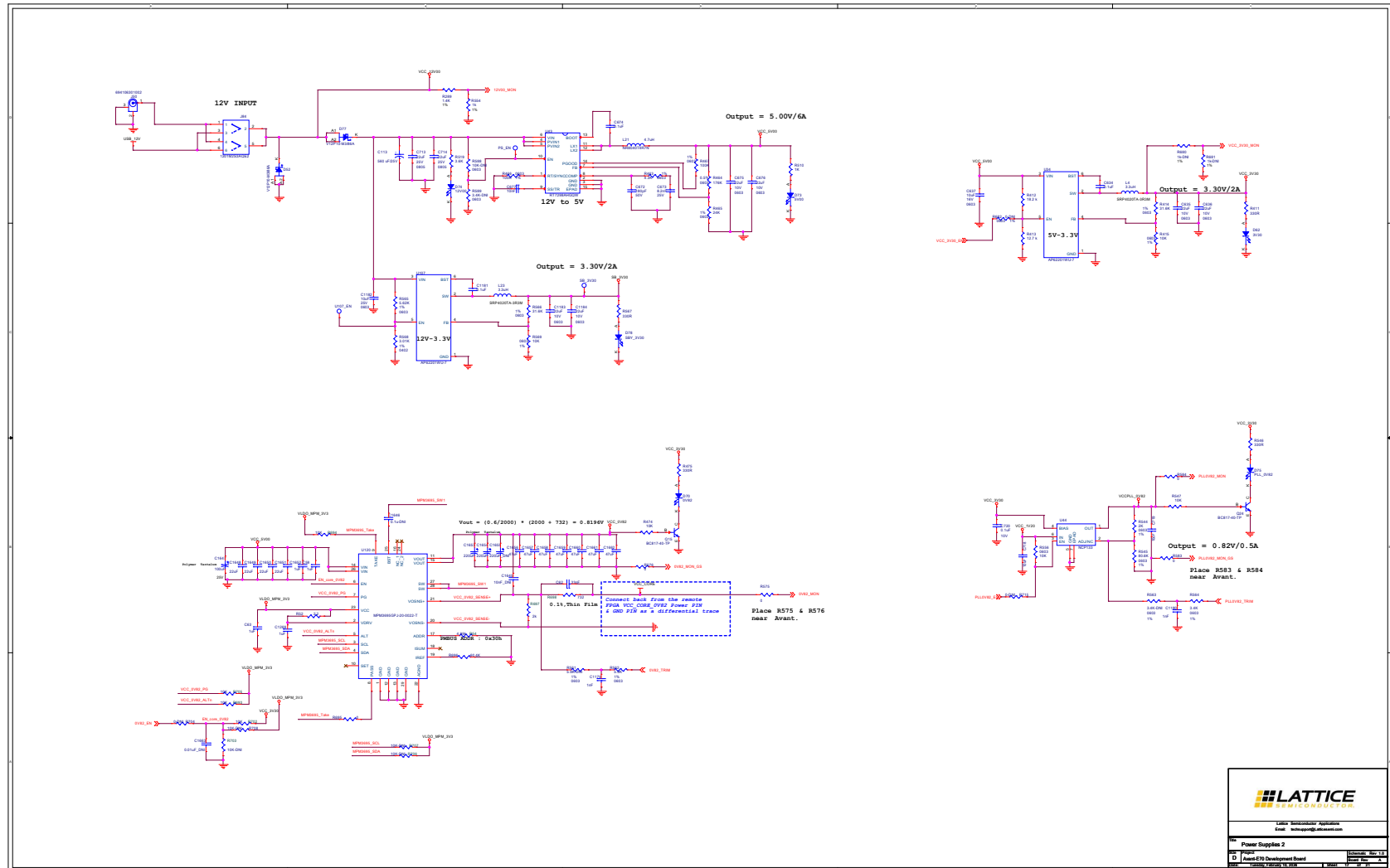
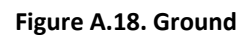


Figure A.17. Power Supplies 2







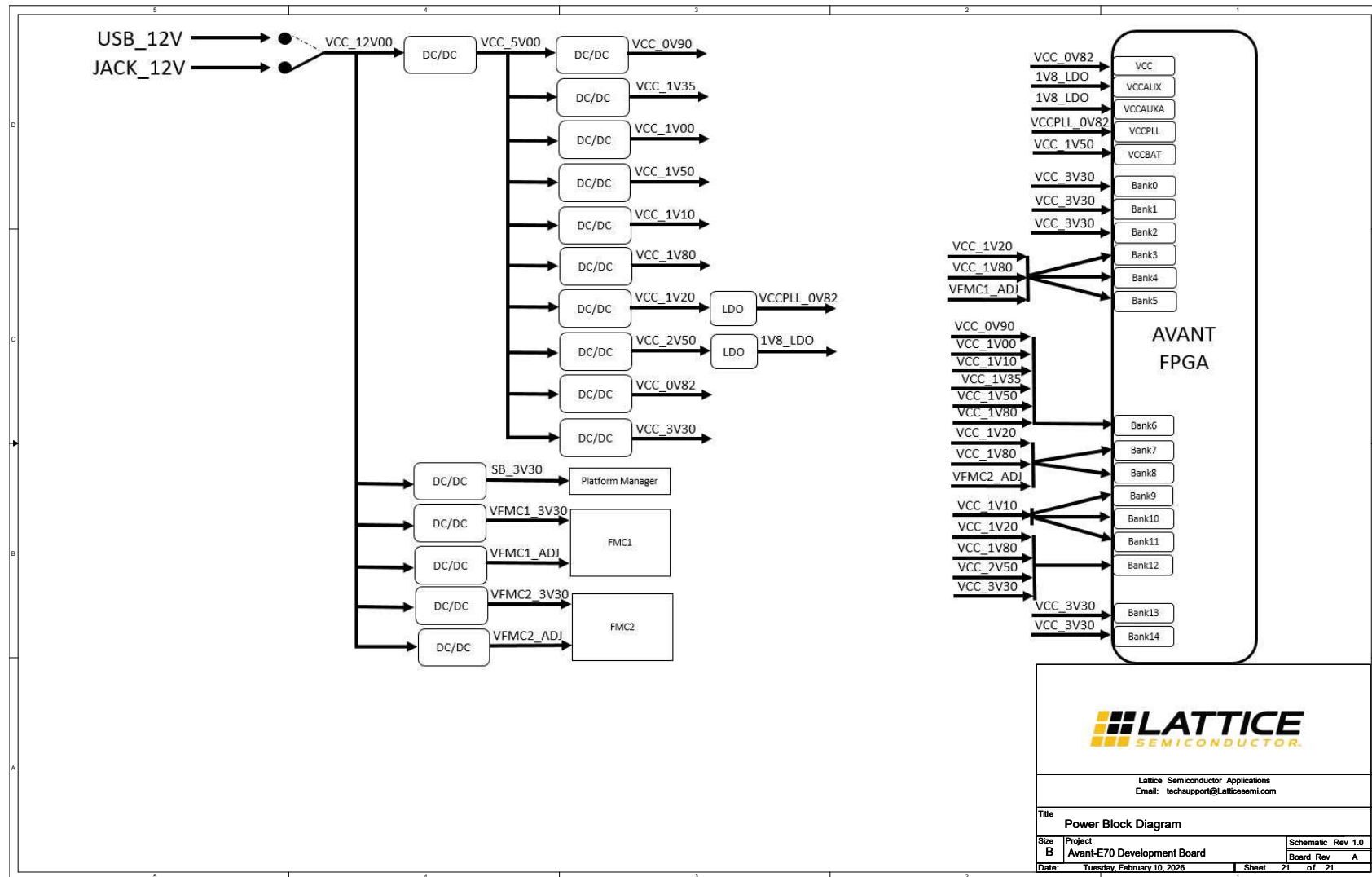


Figure A.21. Power Block Diagram

Appendix B. Avant-E70 Development Board Bill of Materials

Item	Reference	Qty	Value	PCB Footprint	Comments	Part Number	Manufacturer	Description
1	VFMC1_ADJ,VCCIO1,PB1,VFMC2_ADJ, VCCIO2,PB2,VCCIO3,PB3,VCCIO4, VCCAPLL4,VCCIO5,VCCIO6,VCCIO7,VCCAP LL7,VCCIO8,VCCIO9,VCCIO10,VCCAPLL10, VCCIO11,VCCIO12,VCCIO13,VCCIO14, AP14,TP25,TP26,VCCORE,VCCIO0, VCCAUX,VCCAPLLW,PS_EN,PROGRAMN	31	TestPoint_SMT	TPC32	DNI	—	—	—
2	6T,10T,VFMC1_3V30,VFMC2_3V30, WRCLK,WDAT,ST,RDAT,P_PROGN, P_JTAGENB,P_INITN,P_DONE,PTM_SDA, PTM_SCL,ASC_CLK	15	VTTVREF	TP_50	DNI	—	—	—
3	C1,C2,C3,C4,C7,C8,C10,C11,C12,C13,C15, C16,C20,C21,C22,C23,C24,C26,C27,C31, C32,C34,C38,C39,C40,C42,C43,C44,C46, C48,C56,C57,C58,C65,C66,C99,C100,C142, C143,C144,C145,C146,C147,C148,C149, C150,C151,C152,C164,C165,C166,C167, C171,C172,C173,C174,C175,C176,C177, C178,C289,C290,C291,C292,C398,C399, C400,C401,C404,C465,C467,C468,C470, C472,C473,C475,C476,C477,C478,C479, C480,C481,C482,C484,C486,C487,C489, C490,C491,C492,C493,C494,C495,C496, C497,C498,C499,C500,C501,C502,C503, C504,C505,C506,C507,C508,C509,C511, C526,C527,C529,C530,C531,C532,C533, C535,C536,C537,C538,C539,C540,C541, C542,C544,C545,C546,C548,C561,C564, C579,C580,C584,C587,C588,C589,C590, C592,C593,C594,C596,C597,C598,C599, C600,C625,C629,C1191,C1192,C1202, C1203,C1219,C1220,C1222,C1224,C1226, C1228,C1229,C1230,C1231,C1232,C1233, C1234,C1235,C1236,C1237,C1238,C1239, C1240,C1241,C1242,C1243,C1244,C1245, C1246,C1247,C1248,C1249,C1250,C1251, C1252,C1253,C1254,C1256	183	0.1uF	C0201	—	GRM033R61E104KE14J	Murata	CAP CER 0.1UF 25V 10% X5R 0201
4	C5,C6,C9	3	4.7uF	C0603	—	CL10A475KA8NQNC	Samsung	CAP CER 4.7UF 25V X5R 0603

Item	Reference	Qty	Value	PCB Footprint	Comments	Part Number	Manufacturer	Description
5	C14,C19,C33,C36,C37,C41,C55,C64,C138,C139,C140,C163,C168,C169,C396,C397,C402,C403,C405,C466,C469,C471,C474,C483,C485,C488,C510,C512,C525,C528,C534,C543,C547,C586,C591,C595,C614,C615,C616,C617,C618,C619,C620,C621,C631,C721,C726,C1190,C1221,C1223,C1225,C1227,C1255,C1257	54	10uF	C0402	—	CL05A106MP8NUB8	Samsung	CAP CER 10UF 10V X5R 0402
6	C17,C18	2	18pF	C0402	—	CL05C180JB5NNNC	Samsung	CAP CER 18PF 50V COG/NPO 0402
7	C25,C53,C69,C562,C1264,C1265,C1266,C1267,C1268	9	1uF	C0603	—	TMK107B7105KA-T	Taiyo Yuden	CAP CER 1UF 25V 10% X7R 0603
8	C29,C30,C1666,C1667	4	50pF	C0603	—	06035A500JAT2A	KYOCERA AVX	CAP CER 50PF 50V NPO 0603
9	C45,C47,C97,C98,C207,C208,C388,C558,C560,C623,C626,C637,C641,C644,C648,C652,C656,C661,C665,C718,C719,C1182,C1216,C1218,C1261	25	10uF	C0603	—	C1608X5R1E106M080AC	TDK	CAP CER 10UF 25V X5R 0603
10	C49,C50,C51,C103,C104,C386,C387,C556,C557,C565,C612,C613,C622,C628,C630,C635,C636,C639,C640,C642,C643,C646,C647,C650,C651,C654,C655,C659,C660,C663,C664,C675,C676,C713,C714,C1183,C1184,C1217	38	22uF	C0603	—	GRM188C61E226ME01J	Murata	MLCC - SMD/SMT 0603 25VDC X5S 22UF 20%
11	C52,C559	2	0.1nF	C0603	—	CC0603JRNPO9BN101	Yageo	CAP CER 100PF 50V COG/NPO 0603
12	C54,C563	2	3.3nF	C0201	—	GRM033R71E332KA12D	Murata	CAP CER 3300PF 25V X7R 0201
13	C59,C63,C1269,C1652	4	1uF	C0402	—	GRM155R61E105KA12D	Murata	MLCC - SMD/SMT 1UF 25 VDC 10% 0402 X5R
14	C60,C61,C385,C632,C634,C638,C645,C649,C653,C657,C658,C662,C674,C720,C722,C723,C724,C725,C727,C728,C729,C732,C733,C1177,C1178,C1181	26	0.1uF	C0402	—	CL05B104KA5NNNC	Samsung	CAP CER 0.1UF 25V 10% X7R 0402
15	C62	1	33nF	C0603	—	C0603C333K5RACTU	KEMET	MLCC - SMD/SMT 50V 0.033UF X7R 0603 10%
16	C94,C287,C288,C293,C677,C717,C1186,C1187	8	10nF	C0402	—	CC0402KRX7R7BB103	Yageo	CAP CER 10000PF 16V X7R 0402

Item	Reference	Qty	Value	PCB Footprint	Comments	Part Number	Manufacturer	Description
17	C101,C624	2	18pF	C0402	DNI	CL05C180JB5NNNC	Samsung	CAP CER 18PF 50V COG/NP0 0402
18	C113	1	560uF/25V	RAD_CAN_ A768MS	—	A768MS567M1ELAS017	KEMET	CAP ALUM POLY 560UF 20% 25V SMD
19	C672	1	180pF	C0402	—	04025C181KAT2A	KYOCERA AVX	CAP CER 180PF 50V X7R 0402
20	C673	1	8.2nF	C0402	—	GRM155R71E822KA01D	Murata	CAP CER 8200PF 25V X7R 0402
21	C734	1	0.1uF	C0402	DNI	CL05B104KA5NNNC	Samsung	CAP CER 0.1UF 25V 10% X7R 0402
22	C1179,C1180,C1214,C1215	4	1nF	C0603	—	C0603C102K4RECAUTO	KEMET	CAP CER 1NF 16V X7R 10% 0603
23	C1185	1	0.1uF/50V	C0805	—	VJ0805Y104KXAMR	Vishay	MLCC - SMD/SMT 0805 0.1UF 50V X7R 10%
24	C1188,C1189	2	390pF	C0201	—	0201YC391KAT2A	KYOCERA AVX	MLCC - SMD/SMT 16V 390PF X7R 0201 10%
25	C1193,C1194,C1195,C1196,C1260	5	10uF/50V	C1210	—	KAM32LR71H106KU	KYOCERA AVX	MLCC - SMD/SMT 50V 10UF X7R 1210 10% AEC-Q200
26	C1198,C1199,C1258,C1259	4	0.1uF/50V	C0402	—	CGA2B3X5R1H104K050BB	TDK	MLCC - SMD/SMT CGA 0402 50V 0.1UF X5R 10% AEC-Q200
27	C1204,C1205,C1206,C1207,C1208,C1209, C1210,C1211	8	47uF	C1210	—	12103D476MAT2A	KYOCERA AVX	MLCC - SMD/SMT 25V 47UF 581- KGM32LR51E476MU
28	C1645	1	10nF	C0402	DNI	CC0402KRX7R7BB103	Yageo	CAP CER 10000PF 16V X7R 0402
29	C1646	1	0.1u	C0603	DNI	CC0603ZRY5V9BB104	Yageo	CAP CER 0.1UF 50V Y5V 0603
30	C1647	1	100uF	TC7343	—	T521X107M025ATE060	KEMET	T521, Polymer Tantalum, 100UF, 20%, 25V DC, SMD, Polymer,ESR=60mΩ
31	C1648,C1649,C1650,C1651	4	22uF	C0805	—	GRM21BR61E226ME44L	Murata	MLCC - SMD/SMT 22UF 25V DC 20% 0805 X5R

Item	Reference	Qty	Value	PCB Footprint	Comments	Part Number	Manufacturer	Description
32	C1653,C1654	2	220uF	TC7343	—	T598D227M2R5ATE009	KEMET	Polymer Tantalum, 2.5V 220UF 7343 20% ESR=0.009Ω
33	C1655	1	220uF	TC7343	DNI	T598D227M2R5ATE009	KEMET	Polymer Tantalum, 2.5V 220UF 7343 20% ESR=0.009Ω
34	C1656,C1657,C1658,C1659,C1660,C1661, C1662	7	47uF	C0805	—	GRM219R60J476ME44D	Murata	MLCC - SMD/SMT 47UF 6.3V DC 20% 0805 X5R
35	C1663	1	0.01uF	C0402	DNI	KAM05AR71H103KH	KYOCERA AVX	0402, 50V, X7R, 0.01UF, 10%, AE
36	C1665	1	2pF	C0201	DNI	CBR02C209B9GAC	KEMET	MLCC - SMD/SMT 6.3V 2PF C0G 0201 0.1pF
37	C1668	1	100uF/35V	7360-20	—	T52M1107M035C0055	Vishay	100UF 35volts 20% 55mΩ max ESR
38	TP_FMC2_VREFB,TP_M2C_B_1_1, TP_M2C_B_1_2,TP_M2C_B_2_1, TP_M2C_B_2_2,INIT,DONE	7	TestPoint	TP50	DNI	—	—	—
39	D1,D4,D5,D6,D7,D8,D9,D10,D11,D12,D13, D22,D23,D24,D25,D26,D27,D28,D29,D61, D62,D63,D64,D65,D66,D67,D68,D69,D70, D73,D74,D75,D78	33	GREEN	APT1608	—	LTST-C191KGKT	Lite on Group	Yellow green
40	D3	1	ESDR0502N- UDFN6	UDFN6_040	—	ESDR0502NMUTBG	Onsemi	TVS DIODE 5.5VWM 6UDFN
41	D52,D77	2	V12P10- M3/86A	TO-277A	—	V12P10-M3/86A	Vishay	DIODE SCHOTTKY 100V 12A TO277A
42	D60	1	LDT-N2804RI	display_ 12P-PTH	—	LDT-N2804RI	Lumex Opto/Compo nents Inc.	DISPLAY 7SEG 0.28" TRP RED 12DIP
43	FB1,FB2,FB3,FB6,FB16	5	MPZ1005S121 CT000	FB0402	—	MPZ1005S121CT000	TDK Corporation	FERRITE BEAD 120Ω 0402 1LN
44	FB4,FB24	2	FBMH2016HM 121NT	806	—	FBMH2016HM121NT	Taiyo Yuden	FERRITE BEAD 120Ω 0806 1LN
45	FB22,FB25,FB26,FB27	4	BLM15AX601S N1D	402	—	BLM15AX601SN1D	Murata	FERRITE BEAD 600Ω 0402 1LN
46	FB28,FB29	2	BLM18KG221S N1D	FB0603	—	BLM18KG221SN1D	Murata	0603 220Ω, 2.2A, EMIFIL BLM18K, 0.05Ω, 25%

Item	Reference	Qty	Value	PCB Footprint	Comments	Part Number	Manufacturer	Description
47	F1_ADJ,1V,F2_ADJ,5V,GND6,TP_R7,GND7,GND8,GND9,0V9,TP_AP10,GND10,TP_AP11,GND11,1V1,TP_AP12,TP_AN12,TP_AK12,GND12,1V2,12V,TP_AP13,TP_AN13,TP_AM13,TP_AL13,TP_AK13,GND13,TP_AK14,TP_AH14,TP_AG14,GND14,TP_AK15,TP_AH15,TP_AG15,TP_AF15,GND15,1V5,TP_AK16,TP_AJ16,TP_AF16,1V8,2V5,3V3,PLLOV82_EN,OV82_EN,OV82,U107_EN,F1_3V3AUX,F1_3V3,1V35,1V80_EN,F2_3V3AUX,F2_3V3,VCC_3V30_EN,SB_3V30	55	T POINT R	TP	DNI	—	—	—
48	GND1,GND2,GND3,GND4,GND5	5	TestPoint_Hole	TP	DNI	—	—	—
49	JP1,JP2,JP3,JP4,JP5,JP6,JP15,JP17	8	JUMPER	Header_1x2		Regular 100mil Header		
50	JP12,JP13	2	JUMPER	Header_1x2	DNI	Regular 100mil Header	—	—
51	JP26	1	Receptacle 20X2	HDR254-2X20_socket	DNI	Regular 100mil Header	—	—
52	JP31,JP32,JP33,JP34,JP35,JP36,JP38,JP40,JP42,JP47,JP48,JP49,JP50,JP51,JP58,JP59,JP60,JP61,JP62,JP69,JP70,JP71,JP72,JP73,JP74,JP75,JP76,JP77,JP78	29	J-2 Pin Jumper	Op1_2-Pin_TH	—	0022284020	Molex	CONN HEADER VERT 2POS 2.54MM
53	JP64,JP65,JP83,JP84,JP85,JP86,JP88,JP89	8	3-PIN	HDR254M-1X3	—	PEC03SAAN	Sullins	CONN HEADER VERT 3POS 2.54MM
54	J1	1	Header 1x8	hdr_amp_87 220_8_1x8_100	—	0022284081	Molex	CONN HEADER VERT 8POS 2.54MM
55	J2	1	USB_MINI_B	USB_MINI_B -1734035-2	—	1734035-2	TE	CONN RCPT USB2.0 MINI B SMD R/A
56	J3,J10,J53,J83	4	Header_2x7	Header_2x7	—	Regular 100mil Header	—	—
57	J6,J7	2	PMOD 2x6	PPPC062LJB N-RC	—	PPPC062LJB N-RC	Sullins	CONN HDR 12POS 0.1 GOLD PCB R/A
58	J8	1	CON3	HDR1X3	—	PEC03SAAN	Sullins	CONN HEADER VERT 3POS 2.54MM
59	J11	1	HEADER 2	22284024	—	22284024	Molex	CONN HEADER VERT 2POS 2.54MM
60	J23,J57	2	Header_2x1	Header_2x1	—	Regular 100mil Header	—	—
61	J25	1	12401610E4#2A	USB_TYPEC_RA_SMT	—	12401610E4#2A	Amphenol	USB TYPE C RCPT R/A SMT TOP MOUNT
62	J31,J32,J33,J81	4	GND	TUR_TH	DNI	—	—	—

Item	Reference	Qty	Value	PCB Footprint	Comments	Part Number	Manufacturer	Description
63	J39	1	PTM_JTAG	hdr_amp_87 220_8_1x8_ 100	—	22284081	Molex	CONN HEADER 8POS .100 VERT TIN
64	J48,J54	2	ASP-134486-01	ASP-134486- 01	—	ASP-134486-01	Samtec Inc.	CONN ARRAY RCPT 400POS SMD GOLD
65	J50	1	694106301002	6941063010 02	—	694106301002	Würth Elektronik	CONN PWR JACK 2.1X5.5MM SOLDER
66	J58,J59,J60,J63,J64,J65,J66,J67,J68,J69, J70,J71,J72,J73,J76,J77,J78,J79,J80	19	J-Header_2x1	Header_2X1 _100MIL	—	Regular 100mil Header	—	—
67	J84	1	1201M2S3AQE2	1201M2S3A QE2	—	1201M2S3AQE2	C&K Components	DPDT Side Slide 6@120VAC28V DC4.72 PC
68	L1,L10,L13,L14	4	2.2uH SPM6530T- 2R2M	SPM6530T- 2R2M	—	SPM6530T-2R2M	TDK Corporation	FIXED IND 2.2UH 8.2A 19mΩ SMD
69	L3,L6	2	600ohm 500mA	fb0603	—	BLM18AG601SN1D	Murata	FERRITE BEAD 600Ω 0603 1LN
70	L4,L5,L17,L23	4	3.3uH	SRP4020TA- 3R3M	—	SRP4020TA-3R3M	Bourns Inc.	FIXED IND 3.3UH 3.5A 76mΩ SMD
71	L8,L15	2	1.5uH	SRP4020TA- 1R5M	—	SRP4020TA-1R5M	Bourns Inc.	FIXED IND 1.5UH 4.5A 42mΩ SMD
72	L16,L18,L20	3	2.2uH	SRP4020TA- 2R2M	—	SRP4020TA-2R2M	Bourns Inc.	FIXED IND 2.2UH 4A 61mΩSMD
73	L19	1	1uH	SMD	—	SRP4020TA-1R0M	Bourns Inc.	FIXED IND 1UH 5A 27mΩ SMD
74	L21	1	4.7uH	8mmx8mm	—	NR8040T4R7N	Taiyo Yuden	FIXED IND 4.7UH 4.1A 23.4mΩ SMD
75	L24,L25	2	1.5uH	L6R6X6R4- 4R8	—	SRP6050CA-1R5M	Bourns Inc.	1.5UH 20% 17A
76	Q1	1	MMBT2222ALT 1G	MMBT2222 ALT-1	—	MMBT2222ALT1G	Onsemi	TRANS NPN 40V 0.6A SOT23-3
77	Q2,Q3,Q4,Q7,Q8,Q9,Q10,Q11,Q12,Q13,Q 14,Q15,Q16,Q17,Q18,Q19,Q20,Q21,Q22, Q23,Q24,Q27,Q28,Q29,Q30,Q31,Q32, Q33,Q34	29	BC817-40-TP	SOT23-3	—	BC817-40-TP	Micro Commercial Co	TRANS NPN 45V 0.8A SOT-23
78	Q26	1	MGSF1N02LT1G	SOT23_MGS F1N02L	—	MGSF1N02LT1G	Onsemi	MOSFET N-CH 20V 750MA SOT23-3
79	R1,R5,R11,R19,R77,R92,R126,R127,R317	9	2.2K	R0603	—	RC0603FR-072K2L	Yageo	RES SMD 2.2KΩ 1% 1/10W 0603

Item	Reference	Qty	Value	PCB Footprint	Comments	Part Number	Manufacturer	Description
80	R2,R3,R4,R21,R27,R30,R31,R32,R33,R34,R35,R36,R37,R42,R47,R48,R76,R78,R79,R85,R86,R87,R90,R91,R185,R292,R293,R314,R315,R316,R321,R322,R340,R342,R344,R542,R543,R596,R603,R604,R606,R607,R623,R625,R629,R646,R647,R662	48	4.7K	R0603	—	CRCW06034K70FKEA	Vishay	RES 4.70KΩ 1/10W 1% 0603 SMD
81	R6,R55,R110,R345,R549,R550,R551,R552	8	22	R0402	—	ERJ-2RKF22R0X	Panasonic	RES SMD 22Ω 1% 1/10W 0402
82	R7,R8,R9,R20,R43,R44,R45,R46,R536,R537,R538,R548,R575,R576,R577,R583,R584,R601,R602,R657,R695	21	0	R0402	—	RC0402FR-070RL	Yageo	RES 0 Ω JUMPER 1/16W 0402
83	R10,R105,R107,R108,R245,R408,R704,R715,R716	9	0	R0402	DNI	RC0402FR-070RL	Yageo	RES 0Ω JUMPER 1/16W 0402
84	R12,R13,R14,R16,R17,R22,R26,R28,R81,R83,R84,R109,R217,R229,R232,R310,R327,R328,R401,R406,R416,R421,R424,R426,R430,R432,R436,R438,R442,R443,R446,R451,R452,R457,R474,R520,R522,R525,R527,R530,R531,R534,R535,R547,R556,R569,R613,R614,R624,R628,R641,R683,R684	53	10K	R0603	—	RC0603FR-0710KL	Yageo	RES SMD 10KΩ 1% 1/10W 0603
85	R15	1	12K	R0603	—	RC0603FR-0712KL	Yageo	RES 12KΩ 1/10W 1% 0603 SMD
86	R23,R29,R50,R51,R80	5	100	R0402	—	ERJ-2RKF1000X	Panasonic	RES SMD 100Ω 1% 1/10W 0402
87	R24,R25,R95,R251,R252,R307,R325,R326,R554	9	1k	R0603	—	RC0603FR-071KL	Yageo	RES 1KΩ 1/10W 1% 0603 SMD
88	R38,R179,R180,R398,R572,R693,R694,R702,R705	9	10K	R0402	—	RC0402FR-0710KL	Yageo	RES SMD 10KΩ 1% 1/16W 0402
89	R39,R40,R41,R192,R703,R706,R707	7	10K	R0402	DNI	RC0402FR-0710KL	Yageo	RES SMD 10KΩ 1% 1/16W 0402
90	R52	1	2.2	R0603	—	RC0603FR-072R2L	Yageo	SMD 2.2Ω 100mW 0603 1%
91	R54	1	4.99k	R0402	—	RC0402FR-074K99L	Yageo	SMD 4.99KΩ 62.5mW 0402 1%
92	R56,R57,R58,R59,R60,R61,R62,R63,R169,R339,R341,R343,R411,R417,R427,R433,R439,R444,R447,R453,R475,R521,R523,R524,R526,R528,R529,R532,R533,R546,R567,R579	32	330R	R0603	—	ERJ-3EKF3300V	Panasonic	RES SMD 330Ω 1% 1/10W 0603

Item	Reference	Qty	Value	PCB Footprint	Comments	Part Number	Manufacturer	Description
93	R82,R137,R139,R140,R142,R143,R147, R298,R353,R370,R374,R378,R387,R391, R395	15	0.01	R0603	—	PF0603FRE7T0R01Z	Yageo	RES 0.01Ω 1% 0.3W 0603
94	R96,R305,R510,R585,R597,R598,R644, R645,R686	9	1k	R0402	—	RC0402FR-071KL	Yageo	RES 1KΩ 1% 1/16W 0402
95	R100,R306	2	301	R0402	—	RC0402FR-07301RL	Yageo	RES 301Ω 1% 1/16W 0402
96	R103,R104,R215,R216,R308,R309,R615, R649,R650,R651,R663,R664,R665,R666, R667,R668,R669,R670,R671,R672,R682	21	0	R0603	DNI	RC0603JR-070RL	Yageo	RES 0Ω JUMPER 1/10W 0603
97	R106	1	22	R0402	DNI	ERJ-2RKF22R0X	Panasonic	RES SMD 22Ω 1% 1/10W 0402
98	R154	1	0.1	603	—	RCWE0603R100FNEA	Vishay	RES 0.1Ω 1% 1/5W 0603
99	R189,R616,R638,R642,R643,R673,R674	7	0	R0603	—	RC0603JR-070RL	Yageo	RES 0Ω JUMPER 1/10W 0603
100	R231	1	2.61K	603	—	RC0603FR-072K61L	Yageo	RES 2.61KΩ 1% 1/10W 0603
101	R233,R412,R418,R428,R434,R441,R448, R454	8	18.2K	res0402	—	RT0402BRD0718K2L	Yageo	RES SMD 18.2KΩ 0.1% 1/16W 0402
102	R234,R413,R419,R425,R429,R435,R440, R449,R455	9	12.7K	res0402	—	ERJ-2RKF1272X	Panasonic	RES SMD 12.7KΩ 1% 1/10W 0402
103	R249,R250,R323,R324,R605,R608,R659, R660,R661,R675,R676	11	4.7K	R0603	DNI	CRCW06034K70FKEA	Vishay	RES 4.7KΩ 1/10W 1% 0603 SMD
104	R267,R539,R540,R541	4	1R	603	—	ERJ-3BQF1R0V	Panasonic	RES SMD 1Ω 1% 1/4W 0603
105	R287	1	19.1K	R0603	—	RC0603FR-0719K1L	Yageo	RES 19.1KΩ 1% 1/10W 0603
106	R288	1	19.1K	R0603	DNI	RC0603FR-0719K1L	Yageo	RES 19.1KΩ 1% 1/10W 0603
107	R289	1	1.4K	R0603	—	RC0603FR-071K4L	Yageo	RES 1.4KΩ 1% 1/10W 0603
108	R290,R291,R294,R633,R652,R653,R654, R655,R656,R685	10	240	R0402	—	RC0402FR-07240RL	Yageo	RES 240Ω 1% 1/16W 0402
109	R331,R332,R333,R334,R335,R336,R337, R338	8	53.6R	res0402	—	RC0402FR-0753R6L	Yageo	RES SMD 53.6Ω 1% 1/16W 0402

Item	Reference	Qty	Value	PCB Footprint	Comments	Part Number	Manufacturer	Description
110	R399,R402	2	20k	R0603	—	RT0603FRE1320KL	Yageo	Thin film chip resistor SMD 1/10W 20KΩ 1% 50ppm
111	R414,R566,R640,R687,R688,R689,R690, R691,R692	9	31.6K	R0603	—	RC0603FR-0731K6L	Yageo	RES 31.6KΩ 1% 1/10W 0603
112	R415	1	10K	603	—	RC0603FR-0710KL	Yageo	RES SMD 10KΩ 1% 1/10W 0603
113	R420	1	3.83K	603	—	RC0603FR-073K83L	Yageo	RES 3.83KΩ 1% 1/10W 0603
114	R431	1	5.11K	603	—	RC0603FR-135K11L	Yageo	RES 5.11KΩ 1% 1/10W 0603
115	R437	1	21.5K	603	—	RC0603FR-0721K5L	Yageo	RES 21.5KΩ 1% 1/10W 0603
116	R445	1	8.87K	603	—	RC0603FR-078K87L	Yageo	RES 8.87KΩ 1% 1/10W 0603
117	R450	1	1.33K	603	—	RC0603FR-071K33L	Yageo	RES 1.33KΩ 1% 1/10W 0603
118	R456	1	6.98K	603	—	RC0603FR-076K98L	Yageo	RES 6.98KΩ 1% 1/10W 0603
119	R463	1	4.3K	603	—	RC0603FR-074K3L	Yageo	RES 4.3KΩ 1% 1/10W 0603
120	R464	1	176K	603	—	RT0603DRE07176KL	Yageo	RES SMD 176KΩ 0.5% 1/10W 0603
121	R465	1	24K	603	—	RC0603FR-0724KL	Yageo	RES 24KΩ 1% 1/10W 0603
122	R466,R467,R609,R610,R618,R619,R622	7	100K	R0603	—	RC0603FR-07100KL	Yageo	RES 100KΩ 1% 1/10W 0603
123	R490,R491	2	49.9	R0402	—	RC0402FR-0749R9L	Yageo	SMD 49.9Ω 62.5mW 0402 1%
124	R492,R493	2	2K	R0402	DNI	RC0402FR-072KL	Yageo	RES 2KΩ 1% 1/16W 0402
125	R519	1	3.6K	R0402	—	RC0402JR-073K6L	Yageo	RES 3.6KΩ 5% 1/16W 0402
126	R544,R697	2	2k	R0603	—	RC0603FR-072KL	Yageo	RES 2KΩ 1% 1/10W 0603
127	R545	1	80.6K	603	—	RC0603FR-0780K6L	Yageo	RES 80.6KΩ 1% 1/10W 0603

Item	Reference	Qty	Value	PCB Footprint	Comments	Part Number	Manufacturer	Description
128	R561	1	5.9K	603	DNI	RC0603FR-075K9L	Yageo	RES 5.9KΩ 1% 1/10W 0603
129	R562	1	5.9K	603	—	RC0603FR-075K9L	Yageo	RES 5.9KΩ 1% 1/10W 0603
130	R563,R589	2	3.4K	603	DNI	RC0603FR-073K4L	Yageo	RES 3.4KΩ 1% 1/10W 0603
131	R564	1	3.4K	603	—	RC0603FR-073K4L	Yageo	RES 3.4KΩ 1% 1/10W 0603
132	R565	1	5.62K	603	—	RC0603FR-075K62L	Yageo	RES 5.62KΩ 1% 1/10W 0603
133	R568	1	3.01K	402	—	RC0402FR-073K01L	Yageo	RES 3.01KΩ 1% 1/16W 0402
134	R578	1	33R	603	—	RC0603JR-0733RL	Yageo	RES 33Ω 5% 1/10W 0603
135	R582,R636	2	100	R0201	DNI	RC0201FR-07100RL	Yageo	RES 100Ω 1% 1/20W 0201
136	R588,R639,R708	3	10K	R0603	DNI	RC0603FR-0710KL	Yageo	RES SMD 10KΩ 1% 1/10W 0603
137	R599,R600,R648	3	10	R0402	—	RC0402FR-0710RL	Yageo	RES 10Ω 1% 1/16W 0402
138	R611,R612	2	15K	R0603	—	RC0603FR-0715KL	Yageo	RES 15KΩ 1% 1/10W 0603
139	R617	1	12.1K	R0603	—	RC0603FR-0712K1L	Yageo	RES 12.1KΩ 1% 1/10W 0603
140	R620,R621	2	5.23K	R0603	—	RC0603FR-075K23L	Yageo	RES 5.23KΩ 1% 1/10W 0603
141	R658	1	0.002ohm	R3637	—	Y14880R00200B9R	Vishay	SMD 0.002Ω 0.1% 3W
142	R680,R681	2	1k	R0603	DNI	RC0603FR-071KL	Yageo	RES 1KΩ 1/10W 1% 0603 SMD
143	R696	1	60.4K	R0603	—	RT0402BRD0760K4L	Yageo	SMD 1/16W 60.4KΩ 0.1% 25ppm
144	R698	1	732	R0603	—	CPF0603B732RE1	TE Connectivity	Thin film chip resistor SMD CPF 0603 732R 0.1% 25ppm
145	R709,R710,R711,R712,R713	5	240	R0402	DNI	RC0402JR-07240RL	Yageo	RES 240Ω 5% 1/16W 0402

Item	Reference	Qty	Value	PCB Footprint	Comments	Part Number	Manufacturer	Description
146	R714	1	0.01	R0603	DNI	PF0603FRE7T0R01Z	Yageo	RES 0.01Ω 1% 0.3W 0603
147	SW1,SW2,SW4,SW5,SW8	5	430182043816	430182043816	—	430182043816	Würth Elektronik	SWITCH TACTILE SPST-NO 0.05A 12V
148	SW3	1	TDA DIP-8	TDA08H0SB1	—	TDA08H0SB1	C&K	SWITCH SLIDE DIP SPST 25MA 24V
149	SW7	1	SW- Würth_452403012014	452403012014	—	452403012014	Würth Elektronik	SWITCH SLIDE DPDT 300MA 6V
150	U1	1	FT2232HL	tqfp64_0p5_12p2x12p2_h1p6	—	FT2232HL	FTDI	IC USB HS DUAL UART/FIFO 64-LQFP
151	U2	1	93LC56C-I/SN	so8_50_244	—	93LC56C-I/SN	Microchip	IC EEPROM 2KBIT 3MHZ 8SOIC
152	U3	1	LAV-AT-E70-LFG1156	LAV-AT-500-L_1156	—	LAV-AT-E70B-3LFG1156C	Lattice	Lattice Avant FPGA 1156LFG package
153	U4	1	MX25L51273GZ4I-08G	8-WSON	—	MX25L51273GZ4I-08G	Macronix	IC FLASH 512MBIT SPI/QUAD 8WSON
154	U5,U119	2	MT53E512M32D1ZW-046 WT:B	BGA_SDRAM_200	—	MT53E512M32D1ZW-046 WT:B	Micron Technology Inc.	IC MEMORY DRAM 16G 512MX32 FBGA
155	U6,U32	2	BD9D321EFJ	HTSOP_8_B D9D321	—	BD9D321EFJ-E2	Rohm Semiconductor	IC REG BUCK ADJ 3A 8HTSOP-J
156	U17,U34,U35,U36,U37,U38,U39,U40,U41,U107	10	AP62201WU-7	TSOT26_AP62201WU-7	—	AP62201WU-7	Diodes Incorporated	DCDC CONV HV BUCK TSOT26 T&R 3K
157	U43	1	RT7298AHGQW	14-WQFN	—	RT7298AHGQW	Richtek USA Inc.	IC REG BUCK ADJUSTABLE 6A 14WQFN
158	U44	1	NCP133	XDFN6	—	NCP133AMXADJTCG	Onsemi	IC REG LIN POS ADJ 500MA 6XDFN
159	U45	1	LPTM21L-CAG100	LPTM21L-CAG100	—	LPTM21L-1A BG100 I	Lattice	Lattice Platform Manager
160	U46	1	PI4ULS3V204ZBEX	TQFN-14	—	PI4ULS3V204ZBEX	Diodes Incorporated	IC TRANSLTR BIDIRECTIONAL 14TQFN
161	U108	1	MPF52002GRE-0012-Z	QFN24N4X4 P0_5	—	MPF52002GRE-0012-Z	MPS	MPS USB PD controller QFN-24
162	U109	1	ESD1L001W1T2G	SC-88	—	ESD1L001W1T2G	Onsemi	TVS 4 CH LOW CAP ESD PROTECT

Item	Reference	Qty	Value	PCB Footprint	Comments	Part Number	Manufacturer	Description
163	U110,U111	2	MPQ4372GVTE-1001-AEC1-Z	QFN-23	—	MPQ4372GVTE-1001-AEC1-Z	MPS	36V, 6A-11A Low EMI Synchronous Step-Down Converters
164	U114,U115	2	TPS564242DRLR	SOT-563-6	—	TPS564242DRLR	TI	IC REG BUCK ADJ 6A SOT563
165	U116	1	RP115H181D-T1-FE	SOT89-5	—	RP115H181D-T1-FE	Nisshinbo	Low noise LDO Regulator 1.8V,1A
166	U118	1	MP2013AGG-Z	QFN6-MP2013	—	MP2013AGG-Z	MPS	40V, 150mA, Low-Quiescent Current Linear Regulator
167	U120	1	MPM3695GPJ-20-0022-T	ECLGA-29-5x6x4r4	—	MPM3695GPJ-20-0022-T	MPS	2.95V to 16V Input Power Module Continuous 20A,Peak 25A
168	X1	1	7M-12.000MAAJ-T	xtal_4p_7m	—	7M-12.000MAAJ-T	TXC	CRYSTAL 12MHZ 18PF SMD
169	X3	1	ASDMB-125.000MHZ-XY-T	x4-2520	—	ASDMB-125.000MHZ-XY-T	Abracon	OSC MEMS 125.000MHZ CMOS SMD 10ppm
170	Y1	1	100 MHz	SMD6_AX3H AF1	—	AX3HAF1-100.0000	Abracon	Oscillators 153fs 100.00 MHZ HCSSL XO
171	Avant-E70 Development Board RevA PCB	1	—	—	—	—	—	—

References

- [Avant-E](#) web page
- [Avant-G](#) web page
- [Avant-X](#) web page
- [Platform Manager 2 and L-ASC10](#) web page

A variety of technical notes for the Lattice Avant platform are available.

- [Programming Cables User Guide \(FPGA-UG-02042\)](#)
- [Lattice Avant sysCONFIG User Guide \(FPGA-TN-02299\)](#)
- [Lattice Avant Platform Data Sheet – Overview \(FPGA-DS-02107\)](#)
- [Lattice Avant Platform Data Sheet – Specifications \(FPGA-DS-02112\)](#)

For more information on Lattice Avant-related IP, reference designs, and board documents, refer to the following pages:

- [Solutions > Kits & Boards for Avant-E/Avant-G/Avant-X](#)
- [Solutions > IP Cores and Reference Designs for Avant-E/Avant-G/Avant-X](#)

Other references:

- [Lattice Diamond](#) FPGA design software
- [Lattice Radiant](#) FPGA design software
- [Lattice Insights](#) for Lattice Semiconductor training courses and learning plans.

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 0.80, March 2026

Section	Change Summary
All	Initial Preliminary release.



www.latticesemi.com