



MachXO4 Family Root-of-Trust Devices

Data Sheet

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Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviation	Definition
AES	Advanced Encryption Standard
BGA	Ball Grid Array
BLVDS	Bidirectional Low Voltage Differential Signaling
CMOS	Complementary Metal Oxide Semiconductor
CRE	Cryptographic Engine
EBR	Embedded Block RAM
ECDSA	Elliptic Curve Digital Signature Algorithm
ECDH	Elliptic Curve Diffie-Hellman
ECIES	Elliptic Curve Integrated Encryption Scheme
ECLK	Edge Clock
FIPS	Federal Information Processing Standard
HMAC	Hash Message Authentication Code
HSP	High Speed Port
I2C	Inter-Integrated Circuit
I3C	Improved Inter-Integrated Circuit
IP	Intellectual Property
JTAG	Joint Test Action Group
LED	Light-Emitting Diode
LUT	Look Up Table
LVC MOS	Low Voltage CMOS
LVDS	Low Voltage Differential Signaling
LVPECL	Low Voltage Positive Emitter Coupled Logic
LVTTL	Low Voltage Transistor-Transistor Logic
MIPI	Mobile Industry Processor Interface
MLVDS	Multipoint Low-Voltage Differential Signaling
MES	Manufacture Electronic Signature
OTP	One Time Programmable
PCLK	Primary Clock
PFU	Programmable Functional Unit
PLL	Phase Locked Loop
POR	Power On Reset
RAM	Random Access Memory
RoT	Root of Trust
SHA	Secure Hash Algorithm
SPI	Serial Peripheral Interface
TransFR	Transparent Field Reconfiguration
TRNG	True Random Number Generator
TTL	Transistor-Transistor Logic
UFM	User Flash Memory

1. Introduction

The MachXO4™ family of ultra-low-density and low-power FPGAs supports advanced programmable bridging and I/O expansion, making it ideal for a variety of applications in consumer electronics, computing and storage, wireless communications, industrial control, and automotive systems. It offers exceptional I/O density and a wide range of programmability options with integrated support for the latest industry-standard I/O interfaces.

To meet the demands of advanced system security, the MachXO4 family is expanded with secure control devices that are capable of running several cryptographic algorithms including Advanced Encryption Standard (AES-128/256), Secure Hash Algorithm (SHA-256), Elliptic Curve Digital Signature Algorithm (ECDSA), Elliptic Curve Integrated Encryption Scheme (ECIES), and Hash Message Authentication Code (HMAC-SHA256). These devices also support public key cryptography and feature a Unique Secure ID for robust identity protection. As a Root-of-Trust hardware solution, the MachXO4 family offers scalable protection across entire systems, leveraging enhanced bitstream security and secure user mode functionality. This datasheet provides detailed information about the MachXO4 Root-of-Trust (RoT) devices. For specifications and features of other MachXO4 family devices, refer to [MachXO4 Family Data Sheet \(FPGA-DS-02125\)](#).

The MachXO4 RoT devices consist of low-power, instant-on, non-volatile, and Flash-based FPGAs with four devices, featuring densities ranging from 3000 to 9400 Look-Up Tables (LUTs). These devices include LUT-based programmable logic, Embedded Block RAM (EBR), Distributed RAM, User Flash Memory (UFM), Phase Locked Loops (PLLs), pre-engineered source synchronous I/O support, advanced configuration support including dual-boot capability, and hardened versions of commonly used functions such as SPI controller, I2C controller, and timer/counter.

Built on a 65-nm non-volatile low-power process, MachXO4 devices offer several architectural features to manage static and dynamic power consumption, including programmable low-swing differential I/O, the ability to turn off I/O banks, and dynamically controlled on-chip PLLs and oscillators.

The MachXO4 devices come in two versions: ultra-low power, ZC, and high-performance, HC, and HE. The ultra-low power devices are available in two speed grades: –2 (slow) and –3 (fast), while the high-performance devices are also available in two speed grades, –5 (slow) and –6 (fast). HC and ZC devices have an internal linear voltage regulator supporting external VCC supply voltages of 3.3 V or 2.5 V, while HE devices accept only 1.2 V as the external VCC supply voltage. All three types, ZC, HC, and HE, are functionally- and pin-compatible.

These RoT FPGAs are available in a range of advanced halogen-free packages, from the compact 5.2 x 6.2 mm WLCSP to the 19 x 19 mm BGA, supporting density migration within the same package. [Table 1.1](#) shows the logic densities, package, and I/O options, along with other key parameters.

The MachXO4 devices also provide enhanced I/O features such as drive strength control, slew rate control, PCI compatibility, bus-keeper latches, pull-up resistors, pull-down resistors, open drain outputs, and hot socketing. Pull-up, pull-down, and bus-keeper features are controllable on a per-pin basis.

Additionally, a user-programmable internal oscillator is included in MachXO4 devices. The clock output from this oscillator may be divisible by the timer/counter and can be used as a clock input in functions such as LED control, keyboard scanning, and similar state machines.

These devices also offer flexible, reliable, and secure configuration from on-chip Flash with encryption and authentication options. They can configure themselves from external SPI Flash or be configured by an external master through the JTAG test access port or the SPI/I2C port. Moreover, MachXO4 devices support dual-boot capability using external Flash memory and remote field upgrade TransFR capability.

Meanwhile, the Lattice Radiant™ design software allows large complex user designs to be efficiently implemented on the MachXO4 FPGA family. Synthesis library support for these devices is available for popular logic synthesis tools. The Lattice Radiant software uses the synthesis tool output along with constraints from its floor planning tools, to place and route the user design in a MachXO4 device. The tools extract timing from the routing and back-annotate it into the design for timing verification. Lattice Semiconductor provides many pre-engineered Intellectual Property (IP) modules for the MachXO4 family. By using these configurable soft IP cores as standardized blocks, designers can concentrate on the unique aspects of their design, increasing productivity.

Table 1.1. Specification Status for MachXO4 RoT Devices

Device		Package	Grade	Status
LFMXO4D-040	LFMXO4D-040HC/ZC	BFG256	Commercial/Industrial	Production
	LFMXO4D-040HC	BBG256	Commercial/Industrial/Automotive	Production
	LFMXO4D-040ZC	BBG256	Commercial/Industrial	Production
	LFMXO4D-040HC	BSG132	Commercial/Industrial/Automotive	Advance
	LFMXO4D-040HC/ZC	BTG256	Commercial/Industrial/Automotive	Advance
	LFMXO4D-040HC/ZC	TSG144	Commercial/Industrial	Advance
	LFMXO4D-040ZC	BSG132	Commercial/Industrial	Advance
LFMXO4D-050	LFMXO4D-050HC/ZC	BFG256	Commercial/Industrial	Production
	LFMXO4D-050HC	BBG256	Commercial/Industrial/Automotive	Production
	LFMXO4D-050ZC	BBG256	Commercial/Industrial	Production
	LFMXO4D-050HC	BSG132	Commercial/Industrial/Automotive	Advance
	LFMXO4D-050HC/ZC	BTG256	Commercial/Industrial/Automotive	Advance
	LFMXO4D-050HC/ZC	TSG144	Commercial/Industrial	Advance
	LFMXO4D-050ZC	BSG132	Commercial/Industrial	Advance
LFMXO4D-080	LFMXO4D-080HC	BBG256	Commercial/Industrial	Production
	LFMXO4D-080HE/ZC	BBG256	Commercial/Industrial/Automotive	Production
	LFMXO4D-080HC/HE/ZC	BBG400	Commercial/Industrial	Production
	LFMXO4D-080HE	UTG69	Commercial/Industrial	Advance
	LFMXO4D-080HC	BTG256	Commercial/Industrial	Advance
	LFMXO4D-080HC	BTG400	Commercial/Industrial	Advance
	LFMXO4D-080HE/ZC	BTG256	Commercial/Industrial/Automotive	Advance
	LFMXO4D-080HE/ZC	BTG400	Commercial/Industrial/Automotive	Advance
LFMXO4D-110	LFMXO4D-110HC	BBG256	Commercial/Industrial	Production
	LFMXO4D-110HE/ZC	BBG256	Commercial/Industrial/Automotive	Production
	LFMXO4D-110HC/HE/ZC	BBG400	Commercial/Industrial	Production
	LFMXO4D-110HC	BBG484	Commercial/Industrial	Production
	LFMXO4D-110HE/ZC	BBG484	Commercial/Industrial/Automotive	Production
	LFMXO4D-110HE	UTG69	Commercial/Industrial	Advance
	LFMXO4D-110HC	BTG256	Commercial/Industrial	Advance
	LFMXO4D-110HC	BTG400	Commercial/Industrial	Advance
	LFMXO4D-110HE/ZC	BTG256	Commercial/Industrial/Automotive	Advance
	LFMXO4D-110HE/ZC	BTG400	Commercial/Industrial/Automotive	Advance

1.1. Features

1.1.1. Low Power and Programmable Architecture

- Logic Density ranging from 3k to 9.4k LUT4
- 80 to 432 kb of embedded memory (EBR)
- Up to 73 kbit Distributed RAM
- Dedicated FIFO control logic
- Advanced 65-nm low-power process
- Programmable low-swing differential I/O

1.1.2. High Performance, Flexible I/O Buffer

- Programmable sysI/O™ buffer supports wide range of interfaces:
 - LVCMOS 3.3/2.5/1.8/1.5/1.2/1.0
 - LVTTTL
 - LVDS, Bus-LVDS, MLVDS, LVPECL
 - MIPI D-PHY Emulated
 - Schmitt trigger inputs, up to 0.5 V hysteresis
- I/O support hot socketing
- On-chip differential termination
- Programmable pull-up or pull-down mode

1.1.3. Pre-Engineered Source Synchronous I/O

- DDR registers in I/O cells
- Dedicated gearing logic
- 7:1 Gearing for Display I/O
- Generic DDR, DDRx2, DDRx4

1.1.4. Dedicated Cryptographic Engine

- AES-128/256 and ECIES Encryption/Decryption
- ECDSA-based and HMAC-SHA256 Authentication
- Secure Hash Algorithm (SHA): SHA-256
- True Random Number Generator (TRNG)
- Key Management using Elliptic Curve Diffie-Hellman (ECDH) Public Key Cryptography
- Unique Secure ID
- Interface for user logic through WISHBONE and High Speed Port (HSP)
- Federal Information Processing Standard (FIPS) supported Security Protocols

1.1.5. Non-volatile, Multi-time Programmable

- Instant-on; Powers up in microseconds
- Optional dual-boot with external SPI memory
- Single-chip, secure solution
- Programmable through JTAG, SPI or I2C

- Reconfigurable Flash up to 100,000 write/erase cycles for commercial/industrial devices and 10,000 for automotive devices
- Supports background programming of non-volatile memory
- In-field logic update while I/O holds the system state through TransFR Reconfiguration

1.1.6. Flexible On-Chip Clocking

- On-chip oscillator with 5.5% accuracy for commercial/industrial devices
- Eight primary clocks
- Up to two edge clocks for high-speed I/O interfaces (top and bottom sides only)
- Up to two analog PLLs per device with fractional-n frequency synthesis
- Wide input frequency range (7 MHz to 400 MHz)

1.1.7. Enhanced System-Level Support

- On-chip hardened functions: SPI, I2C, timer/counter
- Unique TraceID for system tracking
- Single power supply with extended operating range
- IEEE Standard 1149.1 boundary scan
- IEEE 1532 compliant in-system programming

1.1.8. Broad Range of Advanced Packaging

- Compact packages with high I/O-to-LUT ratio up to 381 I/O
- 0.5 mm pitch: 3000 to 4320 LUTs in 8 x 8 mm BGA to 20 x 20 mm TQFP packages with up to 112 I/O
- 0.65 mm pitch: 3000 to 9400 LUTs in 5.2 x 6.2 mm WLCSP to 15 x 15 mm BGA packages with up to 333 I/O
- 0.8 mm pitch: 3000 to 9400 LUTs in 14 x 14 mm to 19 x 19 mm BGA packages with up to 381 I/O
- 1.0 mm pitch: 3000 to 4320 LUTs in 17 x 17 mm BGA package with 204 I/O

1.1.9. State-of-the-Art Design Software

- MachXO4 devices are supported in the Lattice Radiant software
- Industry-leading RTL language support for VHDL, VHDL-2008, Verilog, and SystemVerilog
- Advanced scripting capability on command-line and TCL design flow
- One-click compilation flow and cross-probing between analysis tools
- Embedded timing and logic analyzer

Table 1.2. MachXO4 Family RoT Devices Selection Guide

Feature		LFMXO4D-040	LFMXO4D-050	LFMXO4D-080	LFMXO4D-110
LUTs		3000	4320	6864	9400
Logic Cells		3600	5200	8300	11300
Distributed RAM (kbits)		34	34	73	73
Embedded RAM (kbits)		80	92	240	432
Embedded RAM (M9k Blocks)		8	10	26	48
UFM (kbits)		367/1122 ¹	367/1122 ¹	1088/2693 ¹	1088/2693 ¹
Device Option	ZC (VCC = 2.5 – 3.3 V)	Yes	Yes	Yes	Yes
	HC (VCC = 2.5 – 3.3 V)	Yes	Yes	Yes	Yes
	HE (VCC = 1.2 V)	—	—	Yes	Yes
Number of PLLs		2	2	2	2
Hardened Functions	Security	1	1	1	1
	I2C	2	2	2	2
	SPI	1	1	1	1
	Timer/Counter	1	1	1	1
	Oscillator	1	1	1	1
On-chip Dual-Boot		Yes	Yes	Yes	Yes
I3C Compatible I/O		Yes ²	Yes ²	Yes ²	Yes ²
MIPI D-PHY Support ³		Yes	Yes	Yes	Yes
Temperature	Commercial	Yes	Yes	Yes	Yes
	Industrial	Yes	Yes	Yes	Yes
	Automotive	Yes ⁴	Yes ⁴	Yes ⁵	Yes ⁵
Packages		Total I/O Count			
69-ball WLCSP ⁶ (5.2 × 6.2 mm, 0.65 mm)		—	—	57	57
132-ball csBGA (8 mm × 8 mm, 0.5 mm)		102	102	—	—
144-pin TQFP (20 mm × 20 mm, 0.5 mm)		112	112	—	—
256-ball caBGA (14 × 14 mm, 0.8 mm)		204 ⁷	204 ⁷	204 ⁷	204 ⁷
400-ball caBGA (17 × 17 mm, 0.8 mm)		—	—	333	333
484-ball caBGA (19 × 19 mm, 0.8 mm)		—	—	—	381 ⁷
256-ball ftBGA (17 × 17 mm, 1.0 mm)		204	204	—	—
256-ball caBGA (12 × 12 mm, 0.65 mm)		204	204	204	204
400-ball caBGA (15 × 15 mm, 0.65 mm)		—	—	333	333

Notes:

1. When dual-boot is disabled, image space can be repurposed as extra UFM. Refer to [Table 2.18](#) for more details.
2. Four pairs of I/O in Bank 3 with I3C dynamic pull up capability.
3. HC device only.
4. HC lowest speed grade device only.
5. ZC and HE lowest speed grade device only.
6. Package is only available for HE (VCC = 1.2 V) devices.
7. Package is available for automotive devices.

2. Architecture

2.1. Architecture Overview

The MachXO4 family RoT device architecture contains an array of logic blocks surrounded by Programmable I/O (PIO). All logic density devices in this family have sysCLOCK™ PLLs and blocks of sysMEM Embedded Block RAM (EBRs).

Figure 2.1 shows representative block diagrams of the various family members.

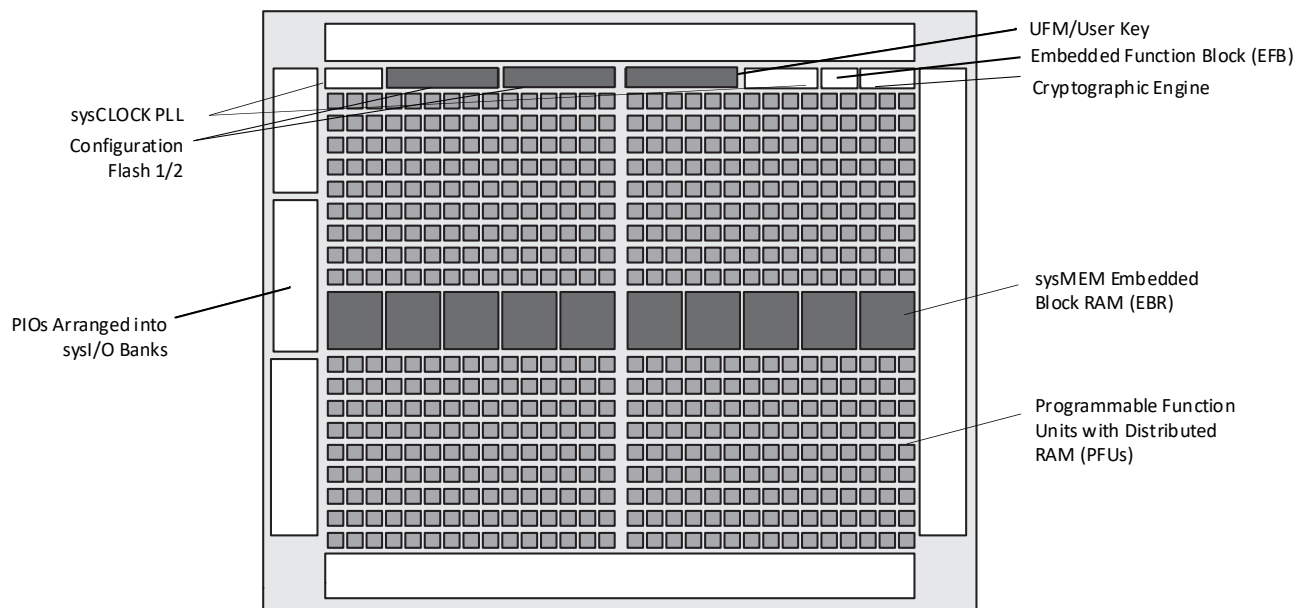


Figure 2.1. Top View of the MachXO4 RoT Device

The logic blocks, Programmable Functional Unit (PFU) and sysMEM EBR blocks, are arranged in a two-dimensional grid with rows and columns. Each row has either the logic blocks or the EBR blocks. The PIO cells are located at the periphery of the device, arranged in banks. The PFU contains the building blocks for logic, arithmetic, RAM, ROM, and register functions. The PIOs use a flexible I/O buffer referred to as a sysI/O buffer that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

In MachXO4 RoT device, the number of sysI/O banks varies by device. There are different types of I/O buffers on the different banks. Refer to the details in later sections of this document. The sysMEM EBRs are large, dedicated fast memory blocks. These blocks can be configured as RAM, ROM, or FIFO. FIFO support includes dedicated FIFO pointer and flag *hard* control logic to minimize LUT usage.

The MachXO4 RoT registers in PFU and sysI/O can be configured to be SET or RESET. After power up and device is configured, the device enters into user mode with these registers SET/RESET according to the configuration setting, allowing the device to enter a known state for predictable system function.

The MachXO4 RoT architecture also provides up to two sysCLOCK Phase Locked Loop (PLL) blocks. These blocks are located at the ends of the on-chip Flash block. The PLLs have multiply, divide, and phase shifting capabilities that are used to manage the frequency and phase relationships of the clocks.

The Cryptographic Engine (CRE) integrates multiple security blocks used for authenticated boot function of the MachXO4 RoT device. User IP located in the fabric can also use these hardened blocks for implementing system level security functions.

MachXO4 RoT devices provide commonly used hardened functions such as SPI controller, I2C controller, and timer/counter.

MachXO4 RoT devices also provide multiple blocks of User Flash Memory (UFM). These hardened functions and the UFM interface to the core logic and routing through a WISHBONE interface. The UFM space also provides the User Key storage for customer security functions. The UFM can also be accessed through the SPI, I2C, and JTAG ports.

Every device in the family has a JTAG port that supports programming and configuration of the device as well as access to the user logic. The MachXO4 RoT devices are available for operation from 3.3 V and 2.5 V power supplies, providing easy integration into the overall system.

2.2. PFU Blocks

The core of the MachXO4 RoT device consists of PFU blocks, which can be programmed to perform logic, arithmetic, distributed RAM and distributed ROM functions. Each PFU block consists of four interconnected slices numbered 0 to 3 as shown in Figure 2.2. Each slice contains two LUTs and two registers. There are 53 inputs and 25 outputs associated with each PFU block.

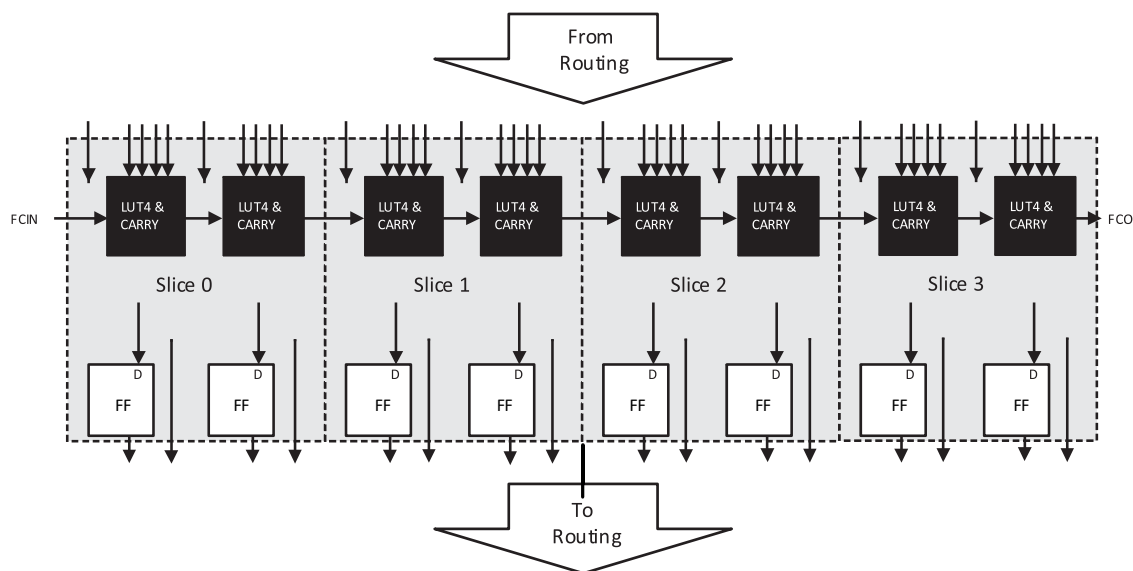


Figure 2.2. PFU Block Diagram

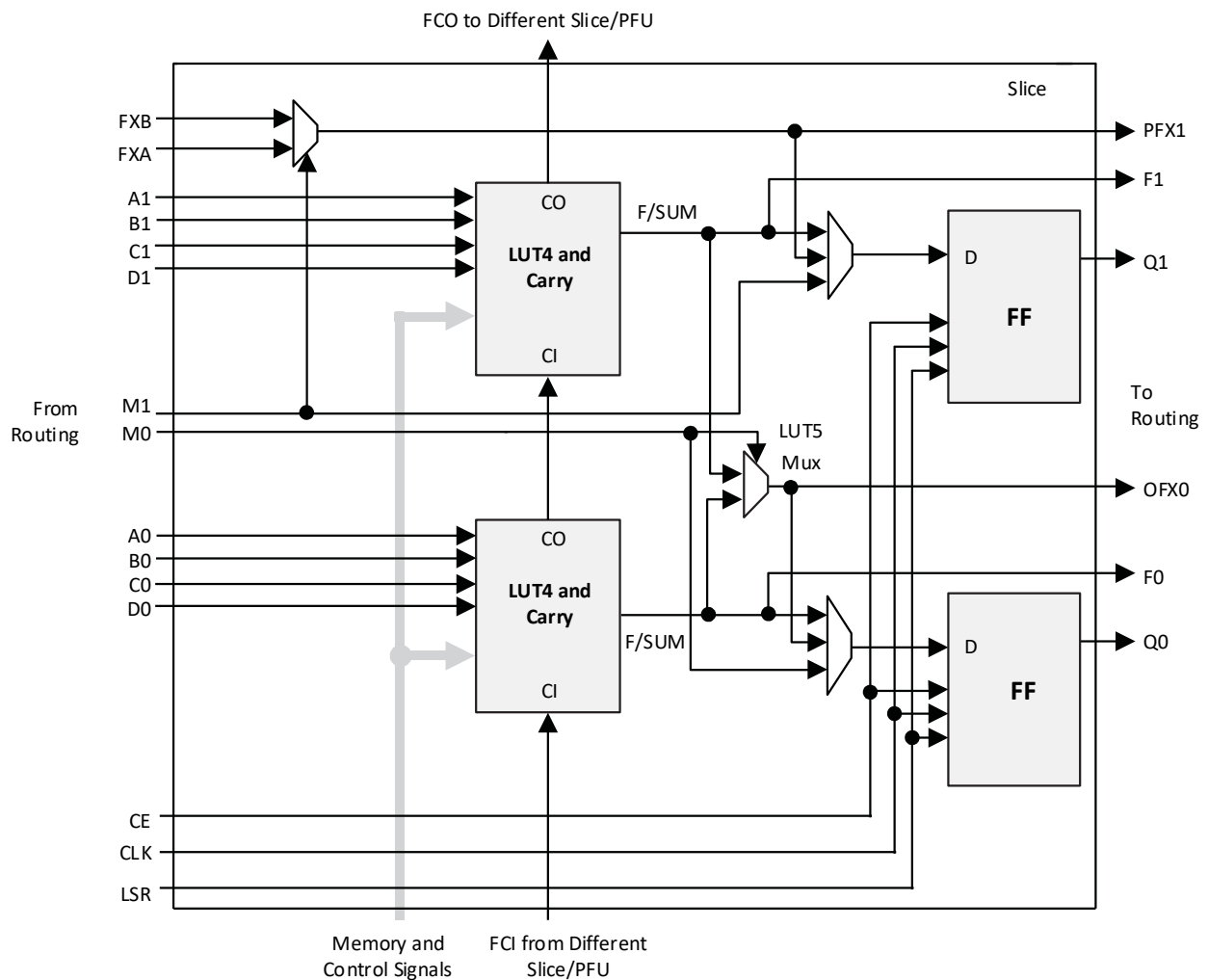
2.2.1. Slices

Slices 0-3 contain two LUT4s feeding two registers. Slices 0-2 can be configured as distributed memory. Table 2.1 shows the capability of the slices in PFU blocks along with the operation modes they enable. In addition, each PFU contains logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7, and LUT8. The control logic performs set/reset functions (programmable as synchronous/asynchronous), clock select, chip-select and wider RAM/ROM functions.

Table 2.1. Resources and Modes Available per Slice

Slice	PFU Block	
	Resource	Mode
Slice 0	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM
Slice 1	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM
Slice 2	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM
Slice 3	2 LUT4s and 2 Registers	Logic, Ripple, ROM

Figure 2.3 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge triggered or level sensitive clocks. All slices have 15 inputs from routing and one from the carry-chain (from the adjacent slice or PFU). There are seven outputs: six for routing and one to carry-chain (to the adjacent PFU). Table 2.2 lists the signals associated with Slices 0-3.



For Slice 0 and 1, memory control signals are generated from Slice 2 as follows:

- WCK is CLK
- WRE is from LSR
- DI[3:2] for Slice 1 and DI[1:0] for Slice 0 data from Slice 2
- WAD[A:D] is a 4-bit address from Slice 2 LUT input

Figure 2.3. Slice Diagram

Table 2.2. Slice Signal Descriptions

Function	Type	Signal Name	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0/M1	Multi-purpose input
Input	Control signal	CE	Clock enable
Input	Control signal	LSR	Local set/reset
Input	Control signal	CLK	System clock
Input	Inter-PFU signal	FCIN	Fast carry in ¹
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8 ² MUX depending on the slice
Output	Inter-PFU signal	FCO	Fast carry out ¹

Notes:

1. See [Figure 2.2](#) for connection details.
2. Requires two PFUs.

2.2.2. Modes of Operation

Each slice has up to four potential modes of operation: Logic, Ripple, RAM, and ROM.

2.2.2.1. Logic Mode

In this mode, the LUTs in each slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any four input logic functions can be generated by programming this lookup table. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger look-up tables such as LUT6, LUT7, and LUT8 can be constructed by concatenating other slices. Note that LUT8 requires more than four slices.

2.2.2.2. Ripple Mode

Ripple mode supports the efficient implementation of small arithmetic functions. In Ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/down counter with asynchronous clear
- Up/down counter with preload (sync)
- Ripple mode multiplier building block Multiplier support
- Comparator functions of A and B inputs
 - A greater-than-or-equal-to B
 - A not-equal-to B
 - A less-than-or-equal-to B

Ripple mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2 mode), two additional signals, Carry Generate and Carry Propagate, are generated on a per-slice basis to allow fast arithmetic functions to be constructed by concatenating slices.

2.2.3. RAM Mode

In this mode, a 16×4-bit distributed single-port RAM (SPR) can be constructed by using each LUT block in Slice 0 and Slice 1 as a 16×1-bit memory. Slice 2 is used to provide memory address and control signals.

MachXO4 RoT devices support distributed memory initialization.

The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software constructs these using distributed memory primitives that represent the capabilities of the PFU. [Table 2.3](#) shows the number of slices required to implement different distributed RAM primitives.

Table 2.3. Number of Slices Required for Implementing Distributed RAM¹

	SPR 16 x 4	PDPR 16 x 4
Number of slices	3	3

Note:

1. SPR = Single-Port RAM, PDPR = Pseudo Dual-Port RAM

2.2.4. ROM Mode

ROM mode uses the LUT logic; hence, Slices 0-3 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

2.3. Routing

There are many resources provided in the MachXO4 RoT devices to route signals individually or as buses with related control signals. The routing resources consist of switching circuitry, buffers, and metal interconnect (routing) segments.

The inter-PFU connections are made with three different types of routing resources: x1 (spans two PFUs), x2 (spans three PFUs) and x6 (spans seven PFUs). The x1, x2, and x6 connections provide fast and efficient connections in the horizontal and vertical directions.

The design tools take the output of the synthesis tool and place and route the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

2.4. Clock/Control Distribution Network

Each MachXO4 RoT device has eight clock inputs (PCLK [T, C] [Banknum]_[2..0]) – three pins on the left side, two pins each on the bottom and top sides and one pin on the right side. These clock inputs drive the clock nets. These eight inputs can be differential or single-ended and may be used as general purpose I/O if they are not used to drive the clock nets. When using a single-ended clock input, only the PCLKT input can drive the clock tree directly.

The MachXO4 RoT architecture has three types of clocking resources: edge clocks, primary clocks, and secondary high fanout nets. MachXO4 RoT devices have two edge clocks each on the top and bottom edges. Edge clocks are used to clock I/O registers and have low injection time and skew. Edge clock inputs are from PLL outputs, primary clock pads, edge clock bridge outputs and CIB sources.

The eight primary clock lines in the primary clock network drive throughout the entire device and can provide clocks for all resources within the device including PFUs, EBRs and PICs. In addition to the primary clock signals, MachXO4 RoT devices also have eight secondary high fanout signals, which can be used for global control signals, such as clock enables, synchronous or asynchronous clears, presets, output enables, and so on. Internal logic can drive the global clock network for internally generated global clocks and control signals.

The maximum frequency for the primary clock network is shown in the MachXO4 RoT External Switching Characteristics table, [Table 3.22](#) and [Table 3.23](#).

Primary clock signals for the MachXO4 RoT devices are generated from eight 27:1 muxes. The available clock sources include eight I/O sources, 11 routing inputs, eight clock divider inputs and up to eight sysCLOCK PLL outputs.

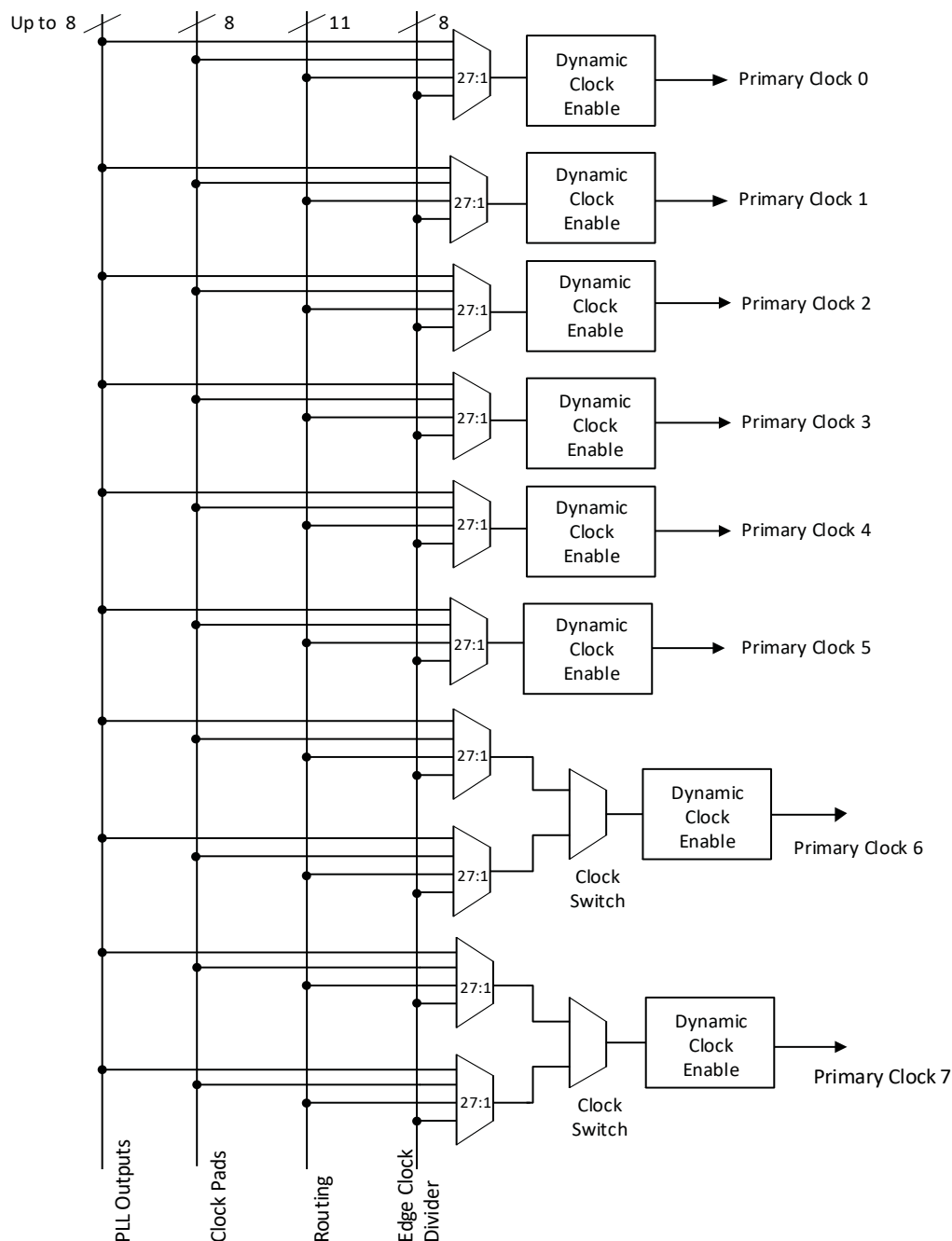


Figure 2.4. Primary Clocks for MachXO4 RoT devices

Eight secondary high fanout nets are generated from eight 8:1 muxes as shown in [Figure 2.5](#). One of the eight inputs to the secondary high fanout net input mux comes from dual-function clock pins and the remaining seven come from internal routing. The maximum frequency for the secondary clock network is shown in the MachXO4 RoT External Switching Characteristics table, [Table 3.22](#) and [Table 3.23](#).

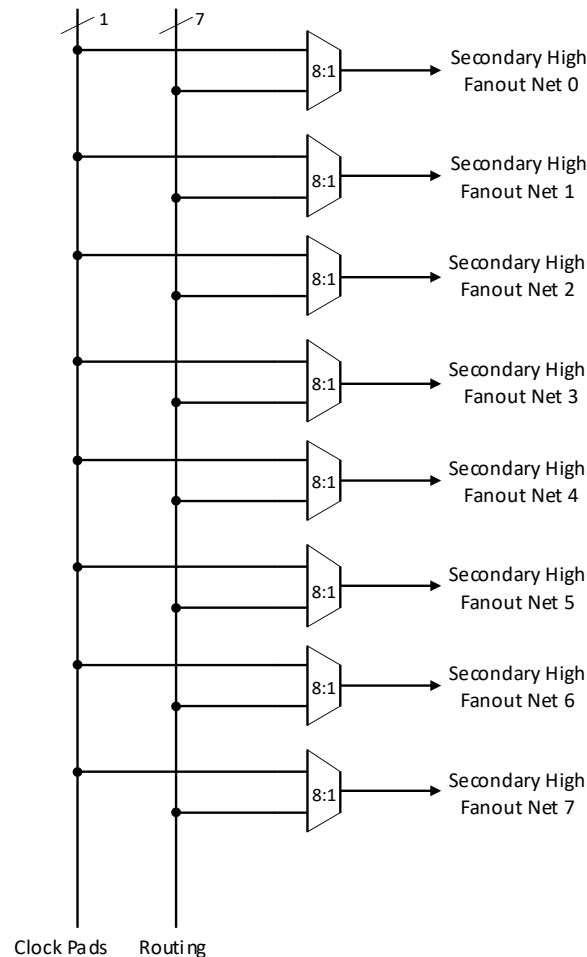


Figure 2.5. Secondary High Fanout Nets for MachXO4 RoT devices

2.4.1. sysCLOCK Phase Locked Loops (PLLs)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. All MachXO4 RoT devices have one or more sysCLOCK PLL. CLKI is the reference frequency input to the PLL and its source can come from an external I/O pin or from internal routing. CLKFB is the feedback signal to the PLL, which can come from internal routing or an external I/O pin. The feedback divider is used to multiply the reference frequency and thus synthesize a higher frequency clock output.

The MachXO4 RoT sysCLOCK PLLs support high resolution (16-bit) fractional-N synthesis. Fractional-N frequency synthesis allows you to generate an output clock, which is a non-integer multiple of the input frequency.

Each output has its own output divider, thus allowing the PLL to generate different frequencies for each output. The output dividers can have a value from 1 to 128. The output dividers may also be cascaded together to generate low frequency clocks. The CLKOP, CLKOS, CLKOS2, and CLKOS3 outputs can all be used to drive the MachXO4 RoT clock distribution network directly or general purpose routing resources can be used.

The LOCK signal is asserted when the PLL determines it has achieved lock and deasserted if a loss of lock is detected. A block diagram of the PLL is shown in [Figure 2.6](#).

The setup and hold times of the device can be improved by programming a phase shift into the CLKOS, CLKOS2, and CLKOS3 output clock, which advance or delay the output clock with reference to the CLKOP output clock.

This phase shift can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after a phase adjustment on the output used as the feedback source and not relock until the t_{LOCK} parameter has been satisfied.

The MachXO4 RoT also has a feature that allows you to select between two different reference clock sources dynamically. This feature is implemented using the PLLREFCS primitive. The timing parameters for the PLL are shown in the [sysCLOCK PLL Timing](#) table.

The MachXO4 RoT PLL contains a WISHBONE port feature that allows the PLL settings, including divider values, to be dynamically changed from the user logic. When using this feature the EFB block must also be instantiated in the design to allow access to the WISHBONE ports. Similar to the dynamic phase adjustment, when PLL settings are updated through the WISHBONE port, the PLL may lose lock and not relock until the t_{LOCK} parameter has been satisfied. The timing parameters for the PLL are shown in the [sysCLOCK PLL Timing](#) table.

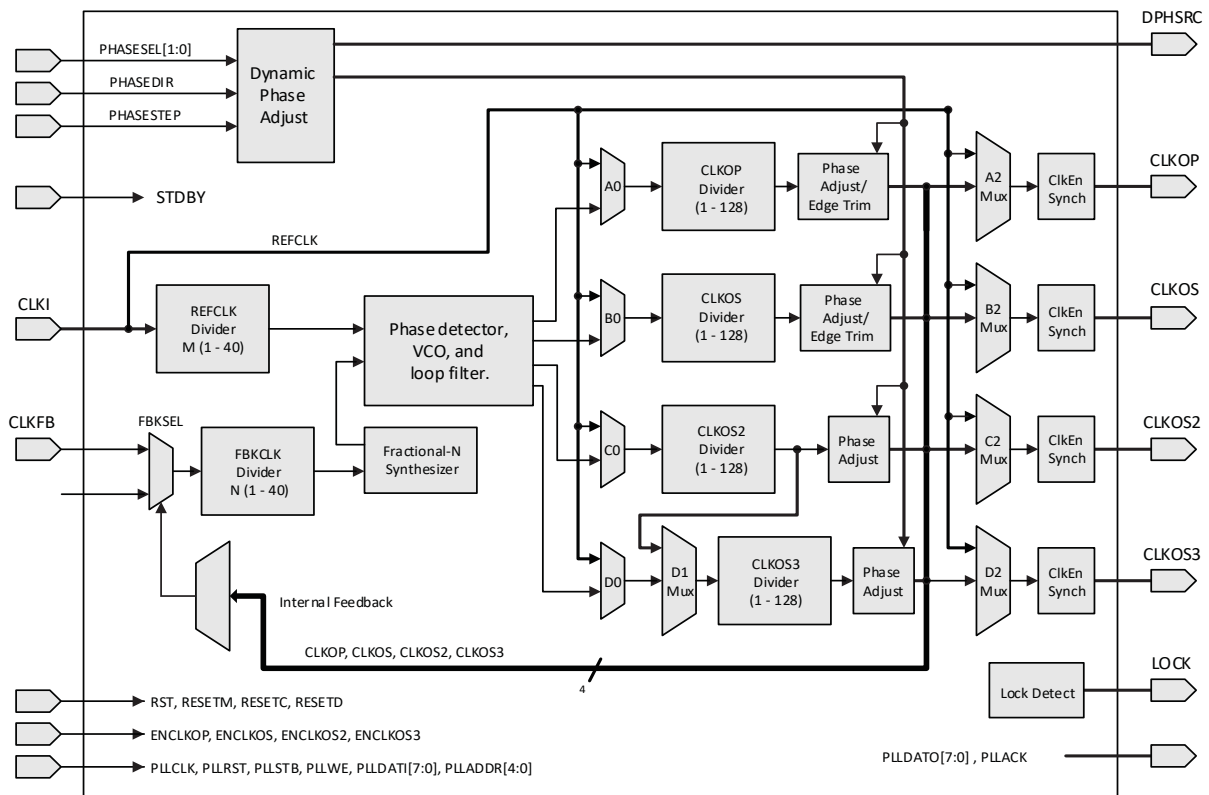


Figure 2.6. PLL Diagram

Table 2.4 provides signal descriptions of the PLL block.

Table 2.4. PLL Signal Descriptions

Port Name	I/O	Description
CLKI	I	Input clock to PLL
CLKFB	I	Feedback clock
PHASESEL[1:0]	I	Select which output is affected by Dynamic Phase adjustment ports
PHASEDIR	I	Dynamic Phase adjustment direction
PHASESTEP	I	Dynamic Phase step – toggle shifts VCO phase adjust by one step.
CLKOP	O	Primary PLL output clock (with phase shift adjustment)
CLKOS	O	Secondary PLL output clock (with phase shift adjust)
CLKOS2	O	Secondary PLL output clock2 (with phase shift adjust)
CLKOS3	O	Secondary PLL output clock3 (with phase shift adjust)
LOCK	O	PLL LOCK, asynchronous signal. Active high indicates PLL is locked to input and feed- back signals.
DPHSRC	O	Dynamic Phase source – ports or WISHBONE is active
STDBY	I	Standby signal to power down the PLL
RST	I	PLL reset without resetting the M-divider. Active high reset.
RESETM	I	PLL reset – includes resetting the M-divider. Active high reset.
RESETC	I	Reset for CLKOS2 output divider only. Active high reset.
RESETD	I	Reset for CLKOS3 output divider only. Active high reset.
ENCLKOP	I	Enable PLL output CLKOP
ENCLKOS	I	Enable PLL output CLKOS when port is active
ENCLKOS2	I	Enable PLL output CLKOS2 when port is active
ENCLKOS3	I	Enable PLL output CLKOS3 when port is active
PLLCLK	I	PLL data bus clock input signal
PLL_RST	I	PLL data bus reset. This resets only the data bus not any register values.
PLLSTB	I	PLL data bus strobe signal
PLLWE	I	PLL data bus write enable signal
PLLADDR [4:0]	I	PLL data bus address
PLLDATI [7:0]	I	PLL data bus data input
PLLDATO [7:0]	O	PLL data bus data output
PLLACK	O	PLL data bus acknowledge signal

2.5. sysMEM Embedded Block RAM Memory

The MachXO4 RoT devices contain sysMEM Embedded Block RAMs (EBRs). The EBR consists of a 9 kb RAM, with dedicated input and output registers. This memory can be used for a wide variety of purposes including data buffering, PROM for the soft processor and FIFO.

2.5.1. sysMEM Memory Block

The sysMEM block can implement single-port, dual-port, pseudo dual-port, or FIFO memories. Each block can be used in a variety of depths and widths as shown in [Table 2.5](#).

Table 2.5. sysMEM Block Configurations

Memory Mode	Configuration
Single-Port	8,192 x 1
	4,096 x 2
	2,048 x 4
	1,024 x 9
True Dual-Port	8,192 x 1
	4,096 x 2
	2,048 x 4
	1,024 x 9
Pseudo Dual-Port	8,192 x 1
	4,096 x 2
	2,048 x 4
	1,024 x 9
FIFO	512 x 18
	8,192 x 1
	4,096 x 2
	2,048 x 4
	1,024 x 9
	512 x 18

2.5.2. Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1, and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

2.5.3. RAM Initialization and ROM Operation

If desired, the contents of the RAM can be preloaded during device configuration. EBR initialization data can be loaded from the Configuration Flash.

MachXO4 RoT EBR initialization data can also be loaded from the UFM. To maximize the number of UFM bits, initialize the EBRs used in your design to an all-zero pattern. Initializing to an all-zero pattern does not use up UFM bits.

MachXO4 RoT devices have been designed such that multiple EBRs share the same initialization memory space if they are initialized to the same pattern.

By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be used as a ROM.

2.5.4. Memory Cascading

Larger and deeper blocks of RAM can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

2.5.5. Single, Dual, Pseudo-Dual Port and FIFO Modes

Figure 2.7 shows the five basic memory configurations and their input/output names. In all the sysMEM RAM modes, the input data and addresses for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the memory array output.

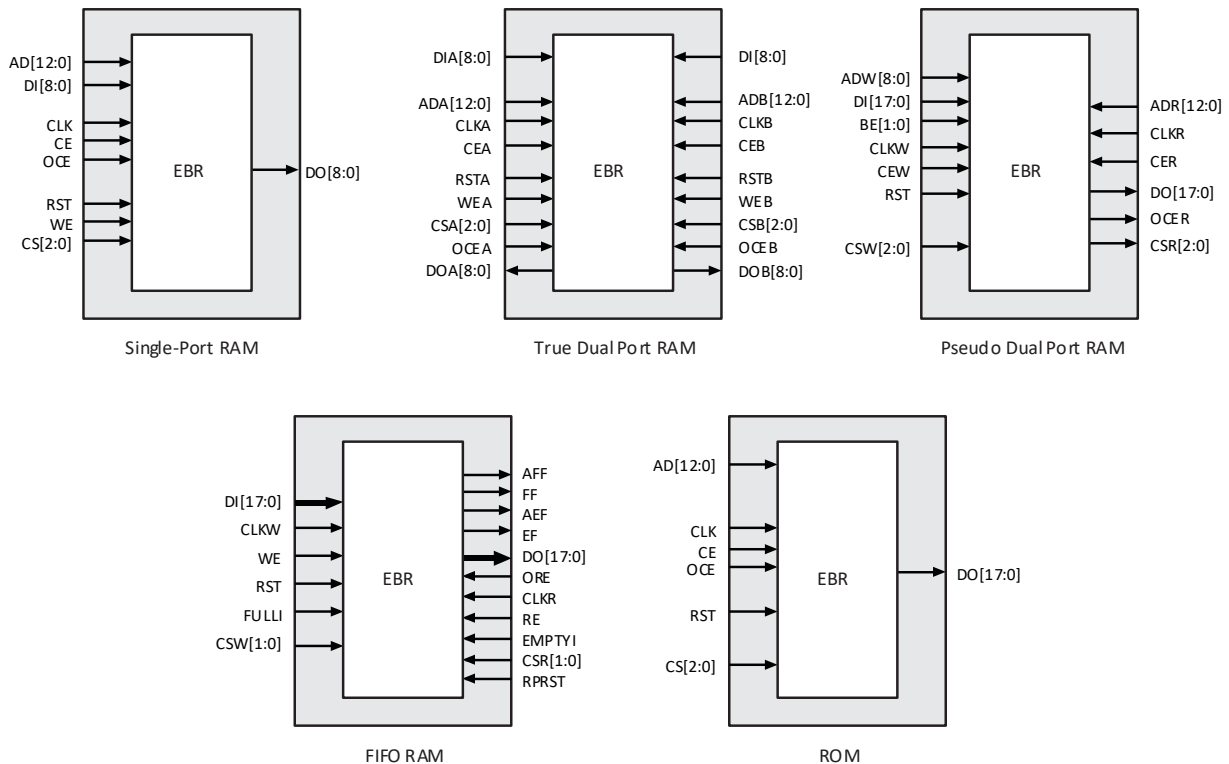


Figure 2.7. sysMEM Memory Primitives

Table 2.6. EBR Signal Descriptions

Port Name	Description	Active State
CLK	Clock	Rising Clock Edge
CE	Clock Enable	Active High
OCE ¹	Output Clock Enable	Active High
RST	Reset	Active High
BE ¹	Byte Enable	Active High
WE	Write Enable	Active High
AD	Address Bus	—
DI	Data In	—
DO	Data Out	—
CS	Chip Select	Active High
AFF	FIFO RAM Almost Full Flag	—
FF	FIFO RAM Full Flag	—

Port Name	Description	Active State
AEF	FIFO RAM Almost Empty Flag	—
EF	FIFO RAM Empty Flag	—
RPRST	FIFO RAM Read Pointer Reset	—

Notes:

- Optional signals.
- For dual-port EBR primitives a trailing 'A' or 'B' in the signal name specifies the EBR port A or port B respectively.
- For FIFO RAM mode primitive, a trailing 'R' or 'W' in the signal name specifies the FIFO read port or write port respectively.
- For FIFO RAM mode primitive, FULLI has the same function as CSW(2) and EMPTYI has the same function as CSR(2).
- In FIFO mode, CLKW is the write port clock, CSW is the write port chip select, CLKR is the read port clock, CSR is the chip select, ORE is the output read enable.

The EBR memory supports three forms of write behavior for single or dual-port operation:

- Normal – Data on the output appears only during the read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.
- Write Through – A copy of the input data appears at the output of the same port. This mode is supported for all data widths.
- Read-Before-Write – When new data is being written, the old contents of the address appears at the output.

2.5.6. FIFO Configuration

The FIFO has a write port with data-in, CEW, WE and CLKW signals. There is a separate read port with data-out, RCE, RE and CLKR signals. The FIFO internally generates Almost Full, Full, Almost Empty and Empty Flags. The Full and Almost Full flags are registered with CLKW. The Empty and Almost Empty flags are registered with CLKR. [Table 2.7](#) shows the range of programming values for these flags.

Table 2.7. Programmable FIFO Flag Ranges

Flag Name	Programming Range
Full (FF)	1 to max (up to 2^N-1)
Almost Full (AF)	1 to Full-1
Almost Empty (AE)	1 to Full-1
Empty (EF)	0

N = Address bit width.

The FIFO state machine supports two types of reset signals: RST and RPRST. The RST signal is a global reset that clears the contents of the FIFO by resetting the read/write pointer and puts the FIFO flags in their initial reset state. The RPRST signal is used to reset the read pointer. The purpose of this reset is to retransmit the data that is in the FIFO. In these applications, it is important to keep careful track of when a packet is written into or read from the FIFO.

2.5.7. Memory Core Reset

The memory core contains data output latches for ports A and B. These are simple latches that can be reset synchronously or asynchronously. RSTA and RSTB are local signals, which reset the output latches associated with port A and port B respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2.8.

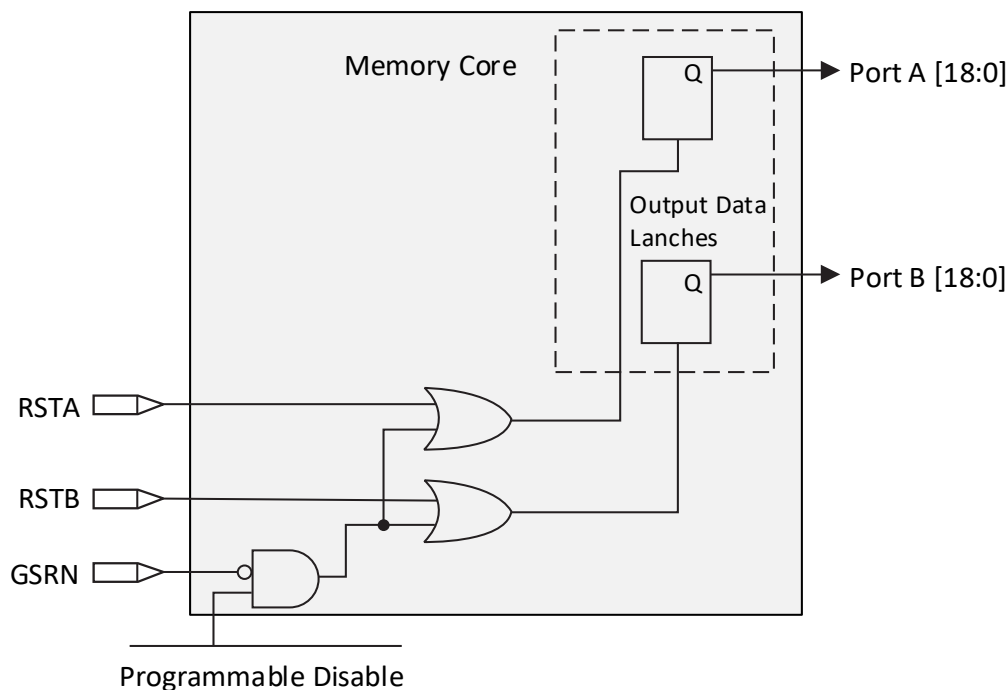


Figure 2.8. Memory Core Reset

2.5.8. EBR Asynchronous Reset

EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the reset is released, as shown in Figure 2.9. The GSR input to the EBR is always asynchronous.

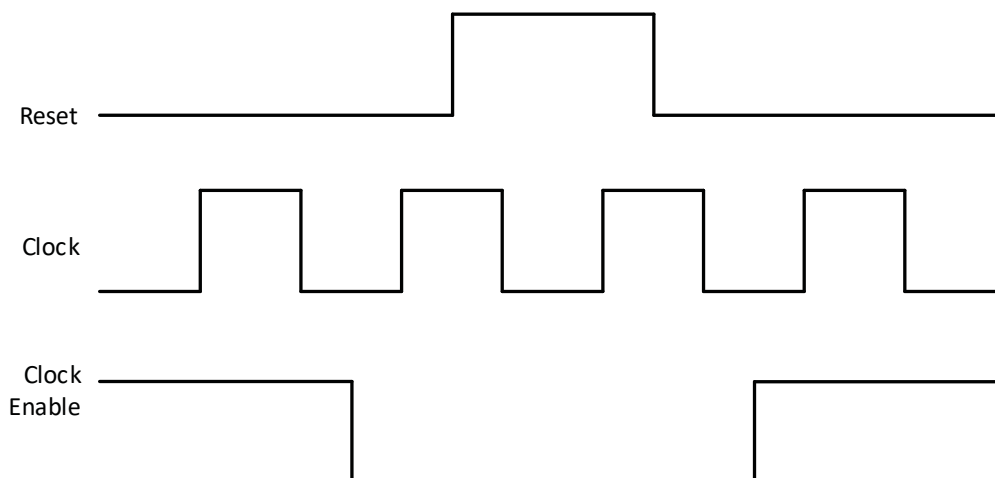


Figure 2.9. EBR Asynchronous Reset (Including GSR) Timing Diagram

If all clock enables remain enabled, the EBR asynchronous reset or GSR may only be applied and released after the EBR read and write clock inputs are in a steady state condition for a minimum of $1/f_{MAX}$ (EBR clock). The reset release must adhere to the EBR synchronous reset setup time before the next active read or write clock edge.

If an EBR is preloaded during configuration, the GSR input must be disabled or the release of the GSR during device wake up must occur before the release of the device I/O becoming active.

These instructions apply to all EBR RAM, ROM and FIFO implementations. For the EBR FIFO mode, the GSR signal is always enabled and the WE and RE signals act like the clock enable signals in [Figure 2.9](#). The reset timing rules apply to the RPRreset input versus the RE input and the RST input versus the WE and RE inputs. Both RST and RPRreset are always asynchronous EBR inputs.

Note that there are no reset restrictions if the EBR synchronous reset is used and the EBR GSR input is disabled.

2.6. Programmable I/O Cells (PIC)

The programmable logic associated with an I/O is called a PIO. The individual PIO are connected to their respective sysI/O buffers and pads. On the MachXO4 RoT devices, the PIO cells are assembled into groups of four PIO cells called a Programmable I/O Cell or PIC. The PICs are placed on all four sides of the device.

On all the MachXO4 RoT devices, two adjacent PIO can be combined to provide a complementary output driver pair.

All PIO pairs can implement differential receivers. Half of the PIO pairs on the top edge of these devices can be configured as true LVDS transmit pairs. The PIO pairs on the bottom edge of these devices have on-chip differential termination.

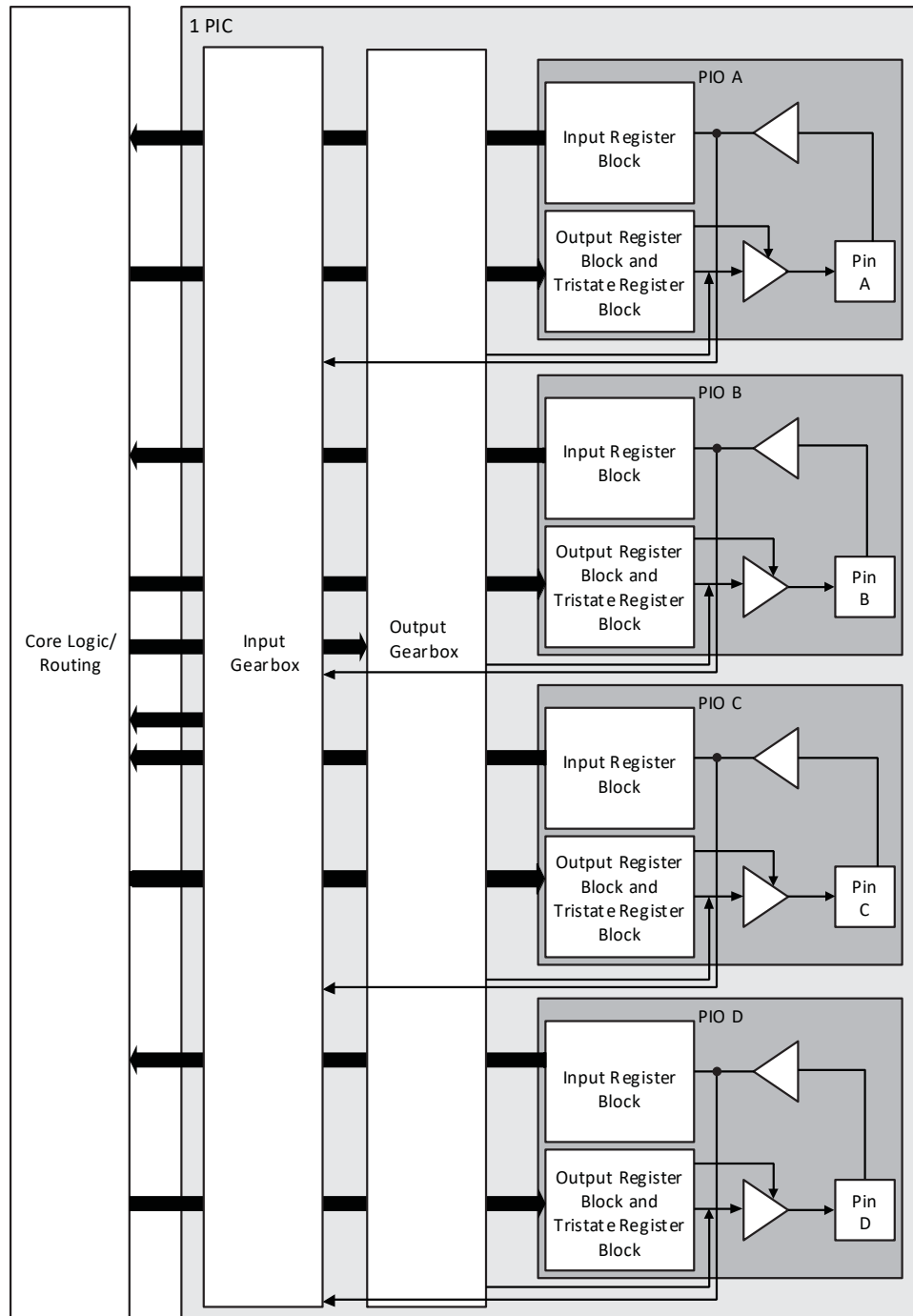


Figure 2.10. Group of Four Programmable I/O Cells

2.7. PIO

The PIO contains three blocks: an input register block, output register block, and tri-state register block. These blocks contain registers for operating in a variety of modes along with the necessary clock and selection logic.

Table 2.8. PIO Signal List

Pin Name	I/O Type	Description
CE	Input	Clock Enable
D	Input	Pin input from sysI/O buffer
INDD	Output	Register bypassed input
INCK	Output	Clock input
Q0	Output	DDR positive edge input
Q1	Output	Registered input/DDR negative edge input
D0	Input	Output signal from the core (SDR and DDR)
D1	Input	Output signal from the core (DDR)
TD	Input	Tri-state signal from the core
Q	Output	Data output signals to sysI/O Buffer
TQ	Output	Tri-state output signals to sysI/O Buffer
SCLK	Input	System clock for input and output/tri-state blocks.
RST	Input	Local set reset signal

2.7.1. Input Register Block

The input register blocks for the PIO on all edges contain delay elements and registers that can be used to condition high-speed interface signals before they are passed to the device core.

2.7.1.1. Left, Top, Bottom Edges

Input signals are fed from the sysI/O buffer to the input register block (as signal D). If desired, the input signal can bypass the register and delay elements and be used directly as a combinatorial signal (INDD), and a clock (INCK). If an input delay is desired, users can select a fixed delay. I/O on the bottom edge also have a dynamic delay, DEL[4:0]. The delay, if selected, reduces input register hold time requirements when using a global clock. The input block allows two modes of operation. In single data rate (SDR) the data is registered with the system clock (SCLK) by one of the registers in the single data rate sync register block. In Generic DDR mode, two registers are used to sample the data on the positive and negative edges of the system clock (SCLK) signal, creating two data streams.

2.7.2. Output Register Block

The output register block registers signals from the core of the device before they are passed to the sysI/O buffers.

2.7.2.1. Left, Top, Bottom Edges

In SDR mode, D0 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as a D-type register or latch.

In DDR generic mode, D0 and D1 inputs are fed into registers on the positive edge of the clock. At the next falling edge, the registered D1 input is registered into the register Q1. A multiplexer running off the same clock is used to switch the mux between the outputs of registers Q0 and Q1 that feeds the output.

Figure 2.11 shows the output register block on the left, top and bottom edges.

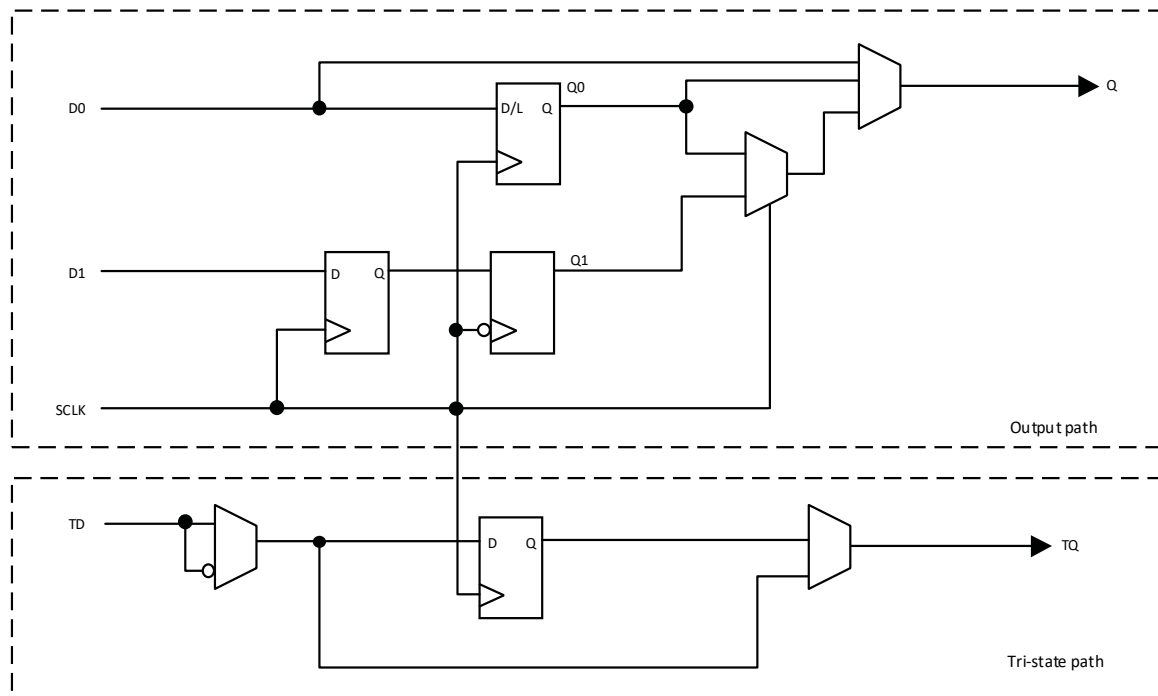


Figure 2.11. MachXO4 RoT Output Register Block Diagram (PIO on the Left, Top and Bottom Edges)

2.7.3. Tri-state Register Block

The tri-state register block registers tri-state control signals from the core of the device before they are passed to the sysI/O buffers. The block contains a register for SDR operation. In SDR, TD input feeds one of the flip-flops that then feeds the output.

2.8. Input Gearbox

Each PIC on the bottom edge has a built-in 1:8 input gearbox. Each of these input gearboxes may be programmed as a 1:7 de-serializer or as one IDDRX4 (1:8) gearbox or as two IDDRX2 (1:4) gearboxes. Table 2.9 shows the gearbox signals.

Table 2.9. Input Gearbox Signal List

Name	I/O Type	Description
D	Input	High-speed data input after programmable delay in PIO A input register block
ALIGNWD	Input	Data alignment signal from device core
SCLK	Input	Slow-speed system clock
ECLK[1:0]	Input	High-speed edge clock
RST	Input	Reset
Q[7:0]	Output	Low-speed data to device core: Video RX(1:7): Q[6:0] GDDR4(1:8): Q[7:0] GDDR2(1:4)(IOL-A): Q4, Q5, Q6, Q7 GDDR2(1:4)(IOL-C): Q0, Q1, Q2, Q3

These gearboxes have three-stage pipeline registers. The first stage registers sample the high-speed input data by the high-speed edge clock on its rising and falling edges. The second stage registers perform data alignment based on the control signals UPDATE and SEL0 from the control block. The third stage pipeline registers pass the data to the device core synchronized to the low-speed system clock. Figure 2.12 shows a block diagram of the input gearbox.

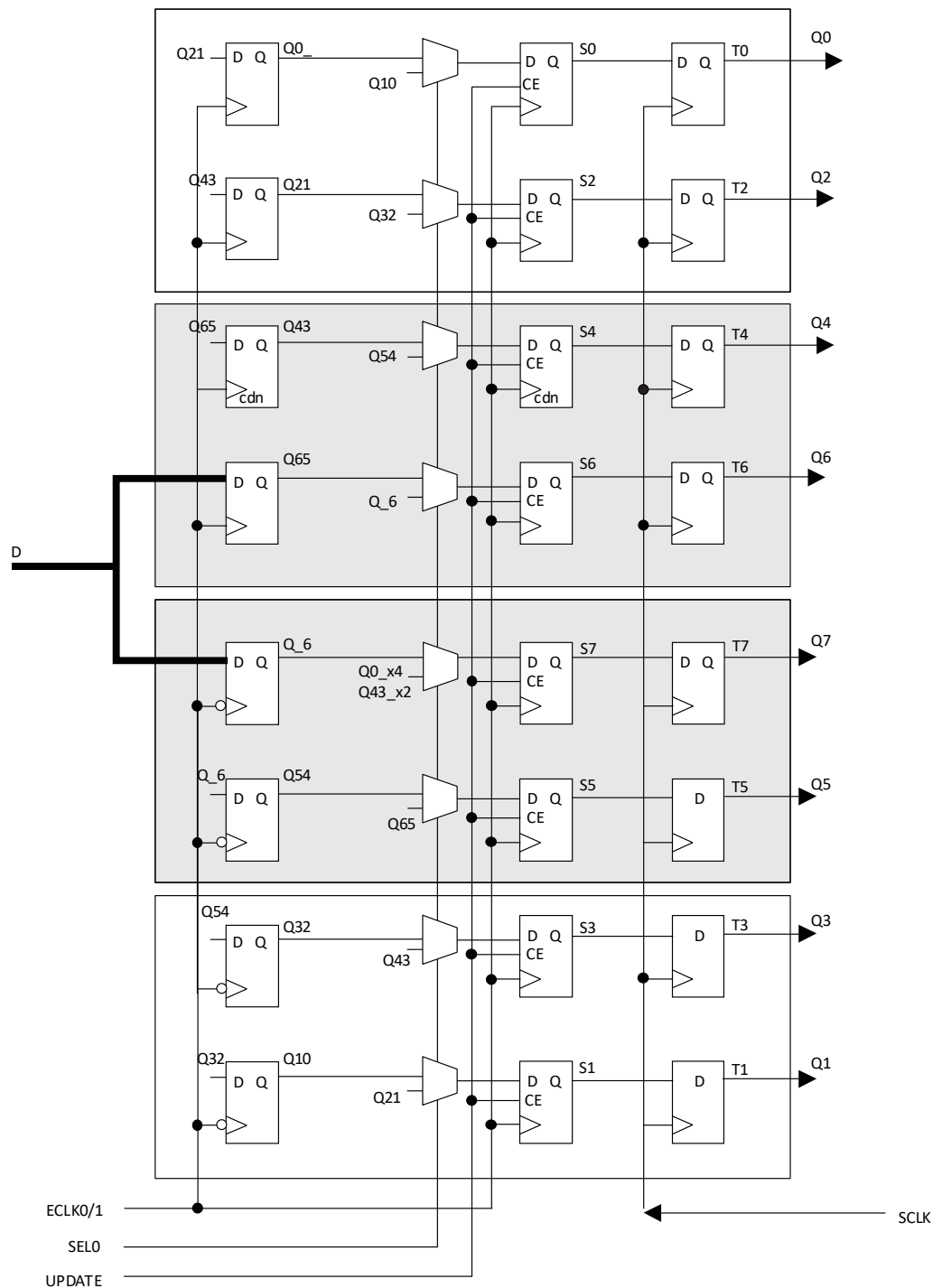


Figure 2.12. Input Gearbox

2.9. Output Gearbox

Each PIC on the top edge has a built-in 8:1 output gearbox. Each of these output gearboxes may be programmed as a 7:1 serializer or as one ODDR4 (8:1) gearbox or as two ODDR2 (4:1) gearboxes. [Table 2.10](#) shows the gearbox signals.

Table 2.10. Output Gearbox Signal List

Name	I/O Type	Description
Q	Output	High-speed data output
D[7:0]	Input	Low-speed data from device core
Video TX(7:1): D[6:0]	—	—
GDDR4(8:1): D[7:0]	—	—
GDDR2(4:1)(IOL-A): D[3:0]	—	—
GDDR2(4:1)(IOL-C): D[7:4]	—	—
SCLK	Input	Slow-speed system clock
ECLK [1:0]	Input	High-speed edge clock
RST	Input	Reset

The gearboxes have three-stage pipeline registers. The first stage registers sample the low-speed input data on the low-speed system clock. The second stage registers transfer data from the low-speed clock registers to the high-speed clock registers. The third stage pipeline registers controlled by high-speed edge clock shift and mux the high-speed data out to the sys/O buffer. [Figure 2.13](#) shows the output gearbox block diagram.

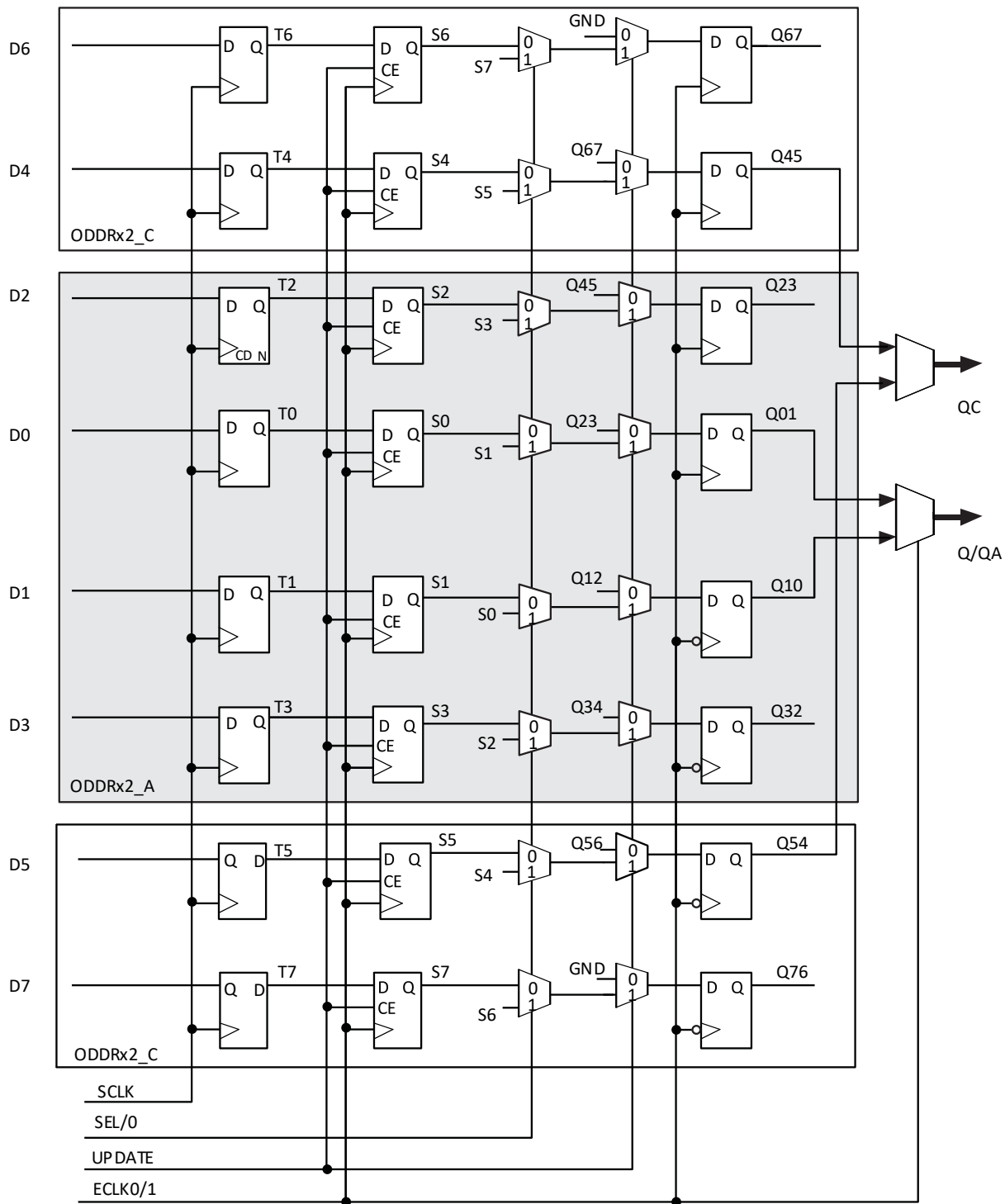


Figure 2.13. Output Gearbox

2.10. sysI/O Buffer

Each I/O is associated with a flexible buffer referred to as a sysI/O buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysI/O buffers allow users to implement a wide variety of standards that are found in today's systems including LVCMOS, TTL, LVDS, BLVDS, MLVDS, LVPECL, and I3C.

Each bank is capable of supporting multiple I/O standards. In the MachXO4 RoT devices, single-ended output buffers, ratioed input buffers (LVTTL, LVCMOS), and differential (LVDS) input buffers are powered using I/O supply voltage (V_{CCIO}). Each sysI/O bank has its own V_{CCIO} .

MachXO4 RoT devices contain three types of sysI/O buffer pairs.

- Left and Right sysI/O Buffer Pairs

The sysI/O buffer pairs in the left and right banks of the device consist of two single-ended output drivers and two single-ended input buffers (for ratioed inputs such as LVCMOS and LVTTL). The I/O pairs on the left and right of the devices also have differential input buffers. The selective I/O pairs of Bank 3 support I3C dynamic pull up capability.

- Bottom sysI/O Buffer Pairs

The sysI/O buffer pairs in the bottom bank of the device consist of two single-ended output drivers and two single-ended input buffers (for ratioed inputs such as LVCMOS and LVTTL). The I/O pairs on the bottom also have differential input buffers. Only the I/O on the bottom banks have differential input termination.

- Top sysI/O Buffer Pairs

The sysI/O buffer pairs in the top bank of the device consist of two single-ended output drivers and two single-ended input buffers (for ratioed inputs such as LVCMOS and LVTTL). The I/O pairs on the top also have differential I/O buffers. Half of the sysI/O buffer pairs on the top edge have true differential outputs. The sysI/O buffer pair comprising of the A and B PIOs in every PIC on the top edge have a differential output driver.

2.10.1. Typical I/O Behavior during Power-up

The internal power-on-reset (POR) signal is deactivated when V_{CC} and V_{CCIO0} have reached VPORUP level defined in the [Power-On-Reset Voltage](#) table in the [DC and Switching Characteristics](#) section of this data sheet. After the POR signal is deactivated, the FPGA core logic becomes active. You need to ensure that all V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. The default configuration of the I/O pins in a blank device is tri-state with a weak pull-down to GND (some pins such as PROGRAMN and the JTAG pins have weak pull-up to V_{CCIO} as the default functionality). The I/O pins maintain the blank configuration until V_{CC} and V_{CCIO} (for I/O banks containing configuration I/O) reach VPORUP levels at which time the I/O takes on the user-configured settings only after a proper download/configuration.

There are various ways for you to ensure that there are no spurious signals on critical outputs as the device powers up.

2.10.2. Supported Standards

The MachXO4 RoT sysI/O buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL and I3C. The buffer supports the LVTTL, I3C, LVCMOS 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V standards. In the LVCMOS and LVTTL modes, the buffer has individually configurable options for drive strength, bus maintenance (weak pull-up, weak pull-down, bus-keeper latch or none) and open drain. BLVDS, MLVDS and LVPECL output emulation is supported on all devices. The MachXO4 RoT devices support on-chip LVDS output buffers on approximately 50% of the I/O on the top bank. Differential receivers for LVDS, BLVDS, MLVDS, and LVPECL are supported on all banks of MachXO4 RoT devices. I3C support is provided with selective I/O in the left bank of the MachXO4 RoT devices.

Table 2.11 summarizes the I/O characteristics of the MachXO4 RoT FPGAs and shows the I/O standards, together with their supply and reference voltages, supported by the MachXO4 RoT devices.

Table 2.11. Supported Input Standards

Input Standard	V _{CCIO} (Typ.)				
	3.3 V	2.5 V	1.8 V	1.5 V	1.2 V
Single-Ended Interfaces					
LVTTL	Yes	Yes ²	Yes ²	Yes ²	—
LVC MOS33	Yes	Yes ²	Yes ²	Yes ²	—
LVC MOS25	Yes ²	Yes	Yes ²	Yes ²	—
LVC MOS18	Yes ²	Yes ²	Yes	Yes ²	—
LVC MOS15	Yes ²	Yes ²	Yes ²	Yes	Yes ²
LVC MOS12	Yes ²	Yes ²	Yes ²	Yes ²	Yes
LVC MOS10R25	—	Yes ³	—	—	—
LVC MOS10R33	Yes ³	—	—	—	—
I3C33	Yes	—	—	—	—
I3C18	—	—	Yes	—	—
I3C12	—	—	—	—	Yes
Differential Interfaces					
LVDS	Yes	Yes	—	—	—
BLVDS, MLVDS, LVPECL, RSDS	Yes	Yes	—	—	—
MIPI ¹	Yes	Yes	—	—	—
LVTTL D	Yes	Yes ²	—	—	—
LVC MOS33D	Yes	—	—	—	—
LVC MOS25D	Yes	Yes	—	—	—
LVC MOS18D	Yes	Yes	Yes	—	—

Notes:

1. These interfaces can be emulated with external resistors in all devices.
2. For reduced functionality, refer to [MachXO4 sysI/O User Guide \(FPGA-TN-02398\)](#) for more details.
3. This input standard can be supported with the referenced input buffer.

Table 2.12. Supported Output Standards

Output Standard	V _{CCIO} (Typ.)
Single-Ended Interfaces	
LVTTL	3.3
LVC MOS33	3.3
LVC MOS25	2.5
LVC MOS18	1.8
LVC MOS15	1.5
LVC MOS12	1.2
LVC MOS10R25, Open Drain	—
LVC MOS10R33, Open Drain	—
LVC MOS33, Open Drain	—
LVC MOS25, Open Drain	—
LVC MOS18, Open Drain	—
LVC MOS15, Open Drain	—
LVC MOS12, Open Drain	—
I3C33	3.3
I3C25	2.5
I3C12	1.2
Differential Interfaces	
LVDS ¹	2.5, 3.3
BLVDS, MLVDS, RS DS ¹	2.5
LVPECL ¹	3.3
MIPI ¹	2.5
LVTTL D	3.3
LVC MOS33D	3.3
LVC MOS25D	2.5
LVC MOS18D	1.8

Note:

1. These interfaces can be emulated with external resistors in all devices.

2.10.3. sysI/O Buffer Banks

MachXO4 RoT device has six I/O banks, one bank on the top, right and bottom side and three banks on the left side. [Figure 2.14](#) shows the sysI/O banks and their associated supplies for all devices.

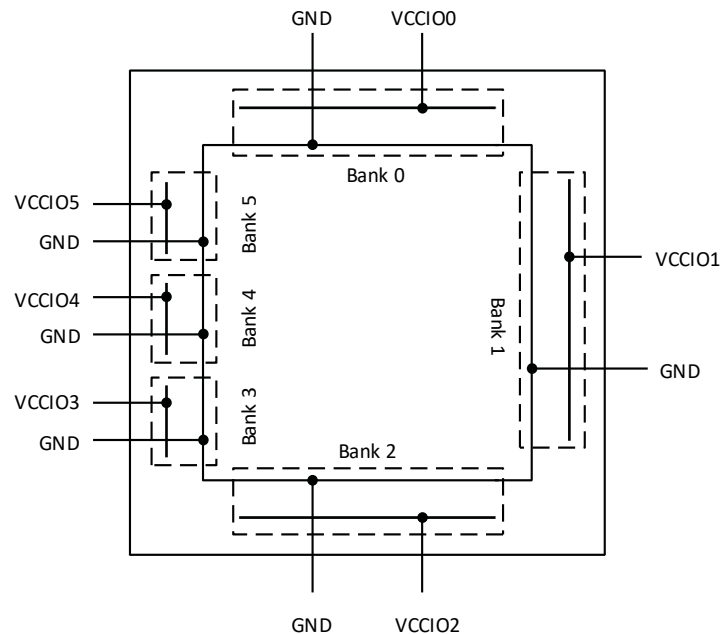


Figure 2.14. MachXO4 RoT I/O Banks

2.11. Hot Socketing

The MachXO4 RoT devices have been carefully designed to ensure predictable behavior during power-up and power-down. Leakage into I/O pins is controlled to within specified limits. This allows for easy integration with the rest of the system. These capabilities make the MachXO4 RoT device ideal for many multiple power supply and hot-swap applications.

2.12. On-chip Oscillator

Every MachXO4 RoT device has an internal CMOS oscillator. The oscillator output can be routed as a clock to the clock tree or as a reference clock to the sysCLOCK PLL using general routing resources. The oscillator frequency can be divided by internal logic. There is a dedicated programming bit and a user input to enable/disable the oscillator. The oscillator frequency ranges from 2.08 MHz to 133 MHz. The software default value of the Master Clock (MCLK) is nominally 2.08 MHz. When a different MCLK is selected during the design process, the following sequence takes place:

1. Device powers up with a nominal MCLK frequency of 2.08 MHz.
2. During configuration, users select a different master clock frequency.
3. The MCLK frequency changes to the selected frequency once the clock configuration bits are received.
4. If you do not select a master clock frequency, then the configuration bitstream defaults to the MCLK frequency of 2.08 MHz.

Table 2.13 lists all the available MCLK frequencies.

Table 2.13. Available MCLK Frequencies

MCLK (MHz, Nominal)	MCLK (MHz, Nominal)	MCLK (MHz, Nominal)
2.08 (default)	9.17	33.25
2.46	10.23	38
3.17	13.3	44.33
4.29	14.78	53.2
5.54	20.46	66.5
7	26.6	88.67
8.31	29.56	133

Table 2.14. Oscillator Output Frequency¹

Symbol	Parameter		Commercial/Industrial Grade Devices			Automotive Grade Devices			Unit
			(-40 °C to 100 °C)			(-40 °C to 125 °C)			
			Min.	Typ.	Max	Min.	Typ.	Max	
f _{MAX}	Oscillator Output Frequency		124.355	133	141.645	122.36	133	143.64	MHz
t _{DT}	Output Clock Duty Cycle		43	50	57	42	50	58	%
t _{OPJIT}	Output Clock Period Jitter	LFMXO4D-080, LFMXO4D-110	—	—	0.031	—	—	0.034	UIPP
		LFMXO4D-040, LFMXO4D-050	—	—	0.38	—	—	0.04	UIPP
t _{STABLEOSC}	STDBY Low to Oscillator Stable		—	—	0.1	—	—	0.1	μs

Note:

1. Recommended single spec for Oscillator Output Frequency is at 133 MHz +/-6.5% for Commercial/Industrial Grade and 133 MHz +/-8% for Automotive Grade. As opposed to MachXO2 where you have 133 MHz +/-5.5% for Commercial and 133 MHz +/-6.5% for Industrial Grade, since data was not collected specific to Commercial Range (0C to 100C) on the MachXO4 RoT device.

2.13. Embedded Hardened IP Functions

All MachXO4 RoT devices provide embedded hardened functions such as Security, SPI, I2C, Timer/Counter, and User Flash Memory (UFM). These embedded blocks interface through the WISHBONE interface with routing as shown in Figure 2.15. For the security block, it also has the high-speed interface with routing.

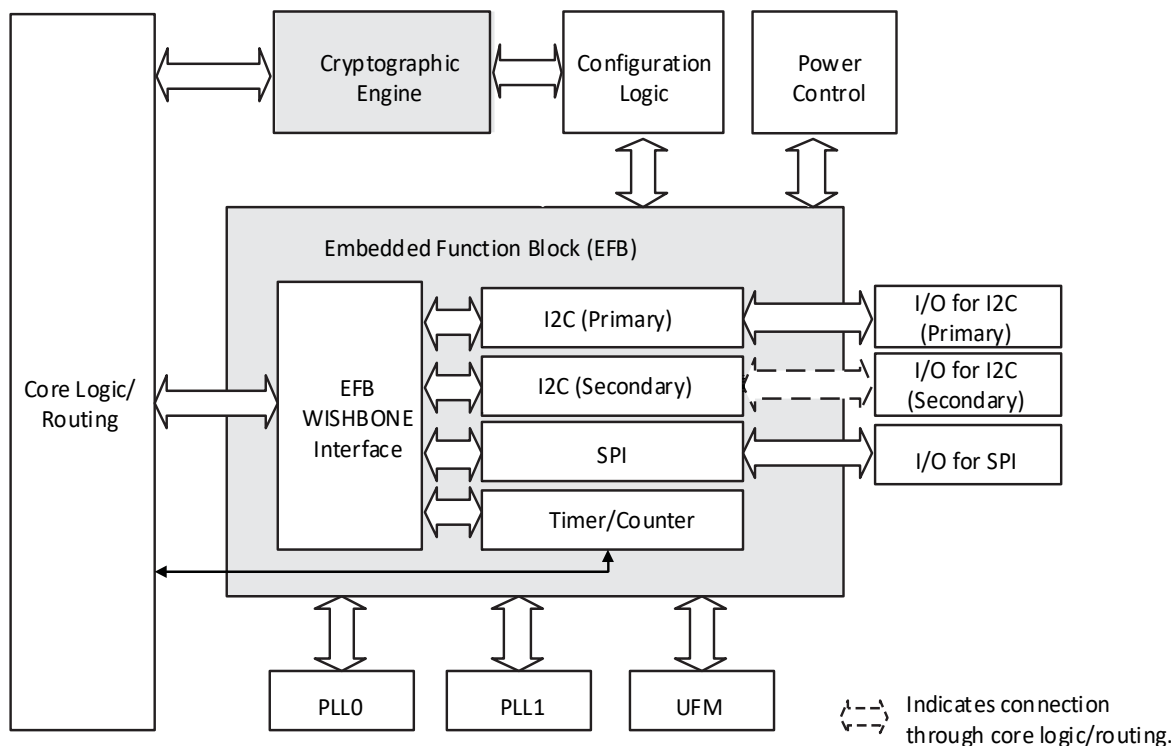


Figure 2.15. Embedded Function Block Interface

2.13.1. CRE IP Core

Every MachXO4 RoT device contains one CRE IP core. The core is responsible for all the security related functions, including encryption, authentication, and key generation in both configuration and user modes.

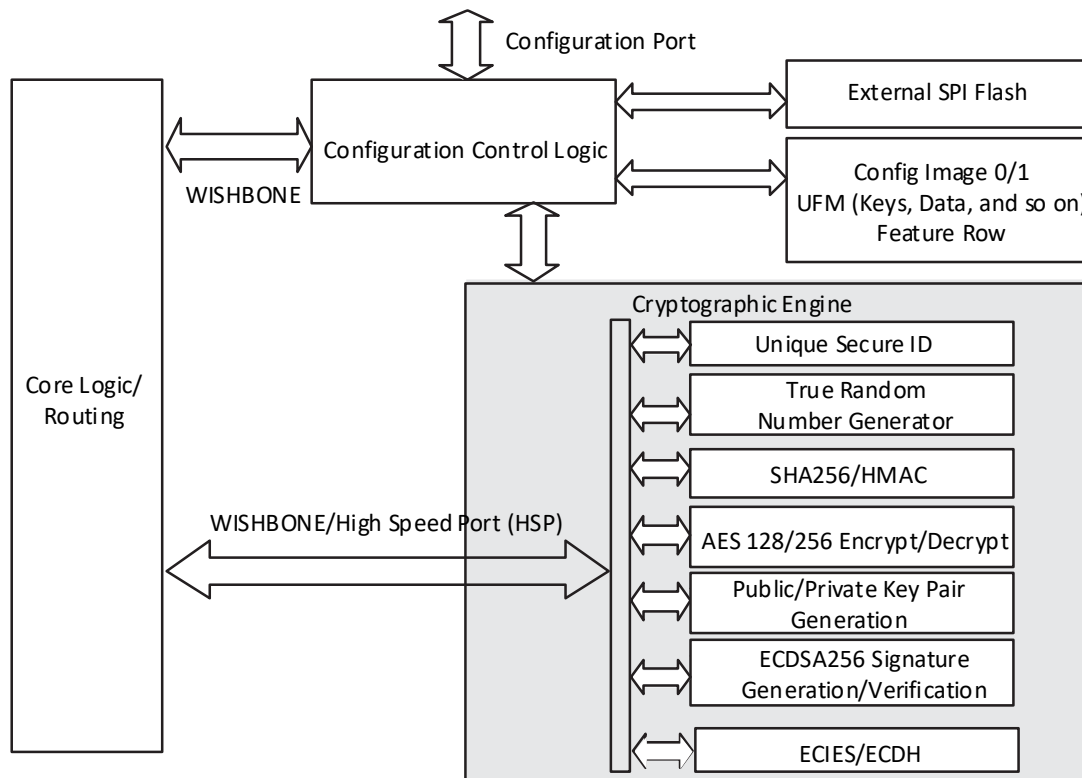


Figure 2.16. CRE Core Block Diagram

The CRE provides the following major functions:

- Secure Hash Algorithm (SHA) — 256 bits
- Elliptic Curve Digital Signature Algorithm (ECDSA) — Generation and verification
- Message Authentication Codes (MACs) — Hash-based MAC (HMAC)
- Elliptic Curve Diffie-Hellman (ECDH) Scheme
- Elliptic Curve Cryptography (ECC) Key Pair Generation — Public key/Private key
- Elliptic Curve Integrated Encryption Standard (ECIES) Encryption/Decryption
- True Random Number Generator (TRNG)
- Advanced Encryption Standard (AES) — 128/256 bits
- Authentication controller for configuration engine
- WISHBONE interface to user logic
- High Speed Port (HSP) for FIFO-based streaming data transfer
- Unique Secure ID

To ensure the security and authenticity of the configuration bitstream, MachXO4 RoT devices offer the following features:

- Bitstream Encryption
- Bitstream Authentication
- Bitstream Encryption and Authentication

When encryption is enabled, the Lattice Radiant software encrypts the bitstream using AES key. When authentication is enabled, the Lattice Radiant software attaches a certificate, which is based on the bitstream digest to the bitstream using customer's private key from the public/private ECDSA key pair. When both features are enabled, the Lattice Radiant software generates the bitstream digest and attaches the ECDSA certificate/signature to this bitstream first. In the second step, this bitstream with the signature is encrypted using the AES Key.

When programming the bitstream to the configuration image space, AES decryption and authentication are executed based on the associated AES/ECDSA public key. Once the authentication is successful, the programming is complete

and the "Done" bit is set. If the authentication is unsuccessful, the MachXO4 RoT device stays in an unprogrammed state.

After programming successfully, the MachXO4 RoT SRAM is configured from flash to enter normal mode after power-cycling, refresh, or ProgramN toggling. It is optional to run the authentication again for each configuration with the selection of fast boot.

There are multiple hard/soft lock controls to enable the reading and writing of specific Flash location, configuration or UFM, for the high security application with the OTP option to prevent any further change to the device.

MachXO4 RoT device provides a unique, immutable key known as the Unique Secure ID. Unique Secure ID is used by CRE to generate paired public key, to perform AES encryption and decryption, and to provide other security related functions. This Unique Secure ID is unique for every device, never leaves the device and is inaccessible. No peripheral can reach the Unique Secure ID including the device's own fabric.

User logic in the fabric can also access security functions in the CRE through the WISHBONE interface for the control and status register access. Payload data transfer in and out of the CRE is enabled through a FIFO-based pipelined High Speed Port. For example, the MachXO4 RoT device can be used to authenticate the microcontroller firmware image stored in the SPI memory chip attached to the MachXO4 RoT device before booting the microcontroller. Here the High Speed Port with the CRE can be used to transfer the contents stored in the SPI memory into the CRE for digesting of the firmware image, a step associated with the overall ECDSA authentication of the microcontroller firmware.

2.13.2. Hardened I2C IP Core

Every MachXO4 RoT device contains two I2C IP cores. These are the primary and secondary I2C IP cores. Either of the two cores can be configured either as an I2C master or as an I2C slave. The only difference between the two IP cores is that the primary core has pre-assigned I/O pins whereas users can assign I/O pins for the secondary core.

When the IP core is configured as a master, it is able to control other devices on the I2C bus through the interface. When the core is configured as the slave, the device is able to provide I/O expansion to an I2C Master. The I2C cores support the following functionality:

- Master and Slave operation
- 7-bit and 10-bit addressing
- Multi-master arbitration support
- Up to 400 kHz data transfer speed general call support
- On-chip spike/glitch rejection to preserve data integrity
- Interface to custom logic through 8-bit WISHBONE interface

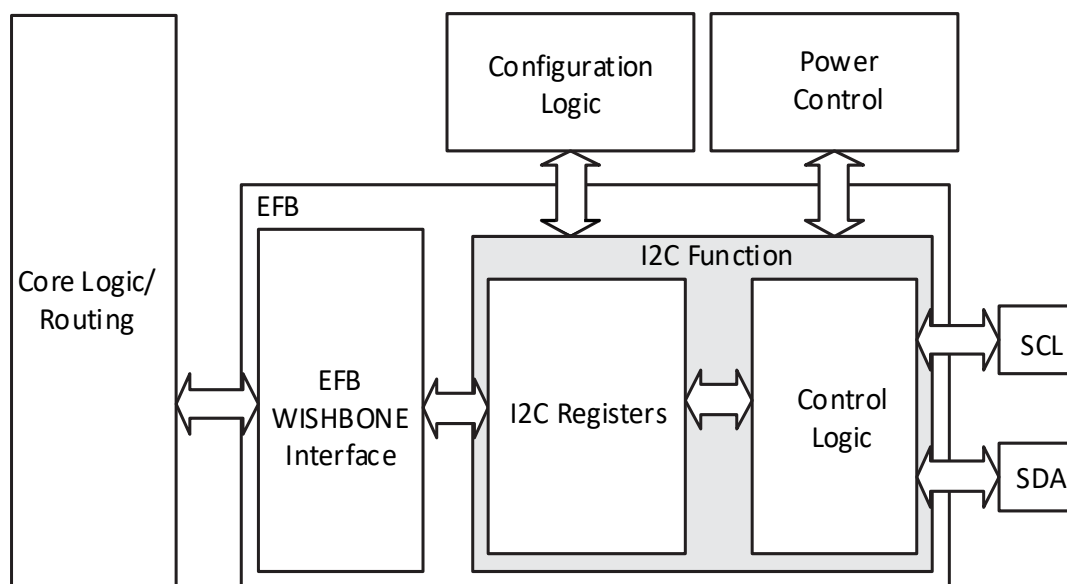


Figure 2.17. I2C Core Block Diagram

Table 2.15 describes the signals interfacing with the I2C cores.

Table 2.15. I2C Core Signal Description

Signal Name	I/O	Description
i2c_scl	Bi-directional	Bidirectional clock line of the I2C core. The signal is an output if the I2C core is in master mode. The signal is an input if the I2C core is in slave mode. MUST be routed directly to the pre-assigned I/O of the chip. Refer to the Pin Information Summary section of this document for detailed pad and pin locations of I2C ports in each MachXO4 RoT device.
i2c_sda	Bi-directional	Bidirectional data line of the I2C core. The signal is an output when data is transmitted from the I2C core. The signal is an input when data is received into the I2C core. MUST be routed directly to the pre-assigned I/O of the chip. Refer to the Pin Information Summary section of this document for detailed pad and pin locations of I2C ports in each MachXO4 RoT device.
i2c_irqo	Output	Interrupt request output signal of the I2C core. The intended usage of this signal is for it to be connected to the WISHBONE master controller (i.e. a microcontroller or state machine) and request an interrupt when a specific condition is met. These conditions are described with the I2C register definitions.
cfg_wake	Output	Wake-up signal – To be connected only to the power module of the MachXO4 RoT device. The signal is enabled only if the “Wakeup Enable” feature has been set within the EFB GUI, I2C Tab.
cfg_stdbby	Output	Stand-by signal – To be connected only to the power module of the MachXO4 RoT device. The signal is enabled only if the “Wakeup Enable” feature has been set within the EFB GUI, I2C Tab.

2.13.3. Hardened SPI IP Core

Every MachXO4 RoT device has a hard SPI IP core that can be configured as an SPI master or slave. When the IP core is configured as a master, it is able to control other SPI enabled chips connected to the SPI bus. When the core is configured as the slave, the device is able to interface to an external SPI master. The SPI IP core on MachXO4 RoT devices supports the following functions:

- Configurable Master and Slave modes
- Full-duplex data transfer
- Mode fault error flag with CPU interrupt capability double-buffered data register
- Serial clock with programmable polarity and phase
- LSB first or MSB first data transfer
- Interface to custom logic through 8-bit WISHBONE interface

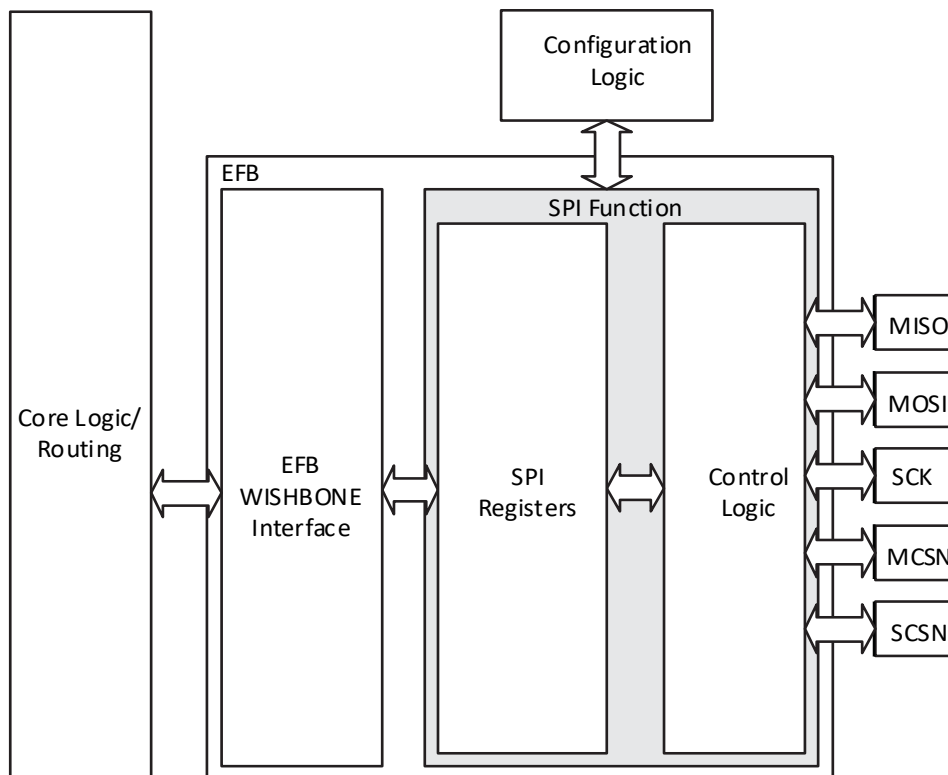


Figure 2.18. SPI Core Block Diagram

Table 2.16 describes the signals interfacing with the SPI cores.

Table 2.16. SPI Core Signal Description

Signal Name	I/O	Master/Slave	Description
spi_csn[0]	O	Master	SPI master chip-select output
spi_csn[1..7]	O	Master	Additional SPI chip-select outputs (total up to eight slaves)
spi_scsn	I	Slave	SPI slave chip-select input
spi_irq	O	Master/Slave	Interrupt request
spi_clk	I/O	Master/Slave	SPI clock. Output in master mode. Input in slave mode.
spi_miso	I/O	Master/Slave	SPI data. Input in master mode. Output in slave mode.
spi_mosi	I/O	Master/Slave	SPI data. Output in master mode. Input in slave mode.
sn	I	Slave	Configuration Slave Chip Select (active low), dedicated for selecting the Configuration Logic.
cfg_stdbby	O	Master/Slave	Stand-by signal – To be connected only to the power module of the MachXO4 RoT device. The signal is enabled only if the “Wakeup Enable” feature has been set within the EFB GUI, SPI Tab.
cfg_wake	O	Master/Slave	Wake-up signal – To be connected only to the power module of the MachXO4 RoT device. The signal is enabled only if the “Wakeup Enable” feature has been set within the EFB GUI, SPI Tab.

2.13.4. Hardened Timer/Counter

MachXO4 RoT devices provide a hard Timer/Counter IP core. This Timer/Counter is a general-purpose, bidirectional, 16-bit timer/counter module with independent output compare units and PWM support. The Timer/Counter supports the following functions:

- Supports the following modes of operation:
 - Watchdog timer
 - Clear timer on compare match
 - Fast PWM
 - Phase and Frequency Correct PWM
- Programmable clock input source
- Programmable input clock prescaler
- One static interrupt output to routing
- One wake-up interrupt to on-chip standby mode controller
- Three independent interrupt sources: overflow, output compare match, and input capture
- Automatically reloading
- Time-stamping support on the input capture unit
- Waveform generation on the output
- Glitch-free PWM waveform generation with variable PWM period
- Internal WISHBONE bus access to the control and status registers
- Stand-alone mode with preloaded control registers and direct reset input

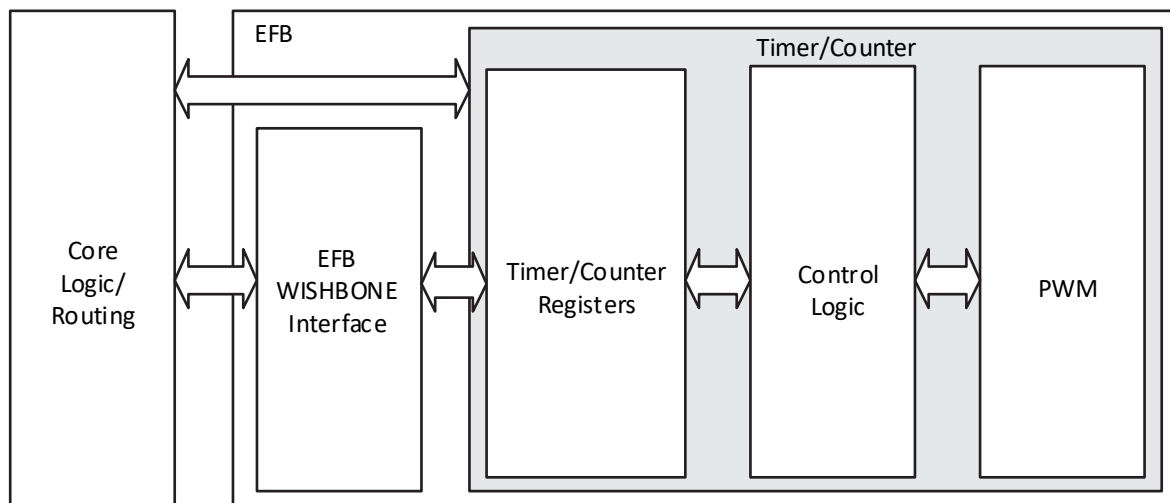


Figure 2.19. Timer/Counter Block Diagram

Table 2.17. Timer/Counter Signal Description

Port	I/O	Description
tc_clk	I	Timer/Counter input clock signal
tc_rstn	I	Register tc_rstn_ena is preloaded by configuration to always keep this pin enabled
tc_ic	I	Input capture trigger event, applicable for non-pwm modes with WISHBONE interface. If enabled, a rising edge of this signal is detected and synchronized to capture tc_cnt value into tc_icr for time-stamping.
tc_int	O	Without WISHBONE – Can be used as overflow flag With WISHBONE – Controlled by three IRQ registers
tc_oc	O	Timer counter output signal

2.14. User Flash Memory (UFM)

MachXO4 RoT devices provide a UFM block that can be used for a variety of applications including storing a portion of the configuration image, initializing EBRs to store PROM data or as a general purpose user Flash memory. It also has a dedicated block for the user key storage and lock control. The UFM block connects to the device core through the embedded function block WISHBONE interface. You can also access the UFM block through the JTAG, I2C, and SPI interfaces of the device. The UFM block offers the following features:

- Non-volatile storage up to 1088 kb
- Dedicated 172 kb non-volatile storage (UFM2/3) for user key
- Write access is performed page-wise; each page has 128 bits (16 bytes)
- Auto-increment addressing
- WISHBONE interface

Table 2.18. MachXO4 RoT UFM Size

Device	UFM0 (kbit)	UFM1 (kbit)	UFM2 (kbit)	UFM3 (kbit)	CFG1 (kbit) ¹
LFMXO4D-040, LFMXO4D-050	98	98	147	24	755
LFMXO4D-080, LFMXO4D-110	458	458	147	24	1,605

Note:

1. When the dual-boot feature is disabled, the CFG1 space can be repurposed as the additional UFM usage.

2.15. Standby Mode and Power Saving Options

MachXO4 RoT devices are available in two options for maximum flexibility: ZC and HC devices. The ZC devices have ultra-low static and dynamic power consumption. The HC devices are designed to provide high performance. The HC devices have a built-in voltage regulator to allow for 2.5 V V_{CC} and 3.3 V V_{CC} .

MachXO4 RoT devices have been designed with features that allow users to meet the static and dynamic power requirements of their applications by controlling various device subsystems such as the bandgap, power-on-reset circuitry, I/O bank controllers, power guard, on-chip oscillator, PLLs, and so on. To maximize power savings, MachXO4 RoT devices support a low power standby mode.

In the standby mode, the MachXO4 RoT devices are powered on and configured. Internal logic, I/O and memories are switched on and remain operational, as the user logic waits for an external input. The device enters this mode when the standby input of the standby controller is toggled or when an appropriate I2C or JTAG instruction is issued by an external master. Various subsystems in the device such as the band gap, power-on-reset circuitry can be configured such that they are automatically turned “off” or go into a low power consumption state to save power when the device enters this state. Note that the MachXO4 RoT devices are powered on when in standby mode and all power supplies should remain in the Recommended Operating Conditions.

Table 2.19. MachXO4 RoT Power Saving Features Description

Device Subsystem	Feature Description
Bandgap	The bandgap can be turned off in standby mode. When the Bandgap is turned off, analog circuitry such as the POR, PLLs, on-chip oscillator, and differential I/O buffers are also turned off.
Power-On-Reset (POR)	The POR can be turned off in standby mode. This monitors V_{CC} levels. In the event of unsafe V_{CC} drops, this circuit reconfigures the device. When the POR circuitry is turned off, limited power detector circuitry is still active. This option is only recommended for applications in which the power supply rails are reliable.
On-Chip Oscillator	The on-chip oscillator has two power saving features. It may be switched off if it is not needed in your design. It can also be turned off in Standby mode.
PLL	Similar to the on-chip oscillator, the PLL also has two power saving features. It can be statically switched off if it is not needed in a design. It can also be turned off in Standby mode. The PLL waits until all output clocks from the PLL are driven low before powering off.
I/O Bank Controller	Differential I/O buffers (used to implement standards such as LVDS) consume more than ratioed single-ended I/O such as LVC MOS and LV TTL. The I/O bank controller allows you to turn these I/O off dynamically on a per bank selection.
Dynamic Clock Enable for Primary Clock Nets	Each primary clock net can be dynamically disabled to save power.
Power Guard	Power Guard is a feature implemented in input buffers. This feature allows users to switch off the input buffer when it is not needed. This feature can be used in both clock and data paths. Its biggest impact is that in the standby mode it can be used to switch off clock inputs that are distributed using general routing resources.

2.16. Power-On-Reset

MachXO4 RoT devices have power-on reset circuitry to monitor V_{CCINT} and V_{CCIO} voltage levels during power-up and operation. At power-up, the POR circuitry monitors V_{CCINT} and V_{CCIO0} (controls configuration) voltage levels. It then triggers download from the on-chip configuration Flash memory after reaching the V_{PORUP} level specified in the [Power-On-Reset Voltage](#) table in the [DC and Switching Characteristics](#) section of this data sheet. For “C” devices with voltage regulators, V_{CCINT} is regulated from the V_{CC} supply voltage. From this voltage reference, the time taken for configuration and entry into user mode is specified as Flash Download Time ($t_{REFRESH}$) in the [DC and Switching Characteristics](#) section of this data sheet. Before and during configuration, the I/O are held in tri-state. I/O are released to user functionality once the device has finished configuration. Note that for C devices, a separate POR circuit monitors external V_{CC} voltage in addition to the POR circuit that monitors the internal post-regulated power supply voltage level.

Once the device enters into user mode, the POR circuitry can optionally continue to monitor V_{CCINT} levels. If V_{CCINT} drops below $V_{PORDNBG}$ level (with the bandgap circuitry switched on) or below $V_{PORDNSRAM}$ level (with the bandgap circuitry switched off to conserve power) device functionality cannot be guaranteed. In such a situation the POR issues a reset and begins monitoring the V_{CCINT} and V_{CCIO} voltage levels. $V_{PORDNBG}$ and $V_{PORDNSRAM}$ are both specified in the [Power-On-Reset Voltage](#) table in the [DC and Switching Characteristics](#) section of this data sheet.

When the bandgap circuitry is switched off, the POR circuitry also shuts down. The device is designed such that a minimal, low power POR circuit is still operational (this corresponds to the $V_{PORDNSRAM}$ reset point described in the paragraph above). However, this circuit is not as accurate as the one that operates when the bandgap is switched on. The low power POR circuit emulates an SRAM cell and is biased to trip before the vast majority of SRAM cells flip. If you are concerned about the V_{CC} supply dropping below $V_{CC}(\min)$, you should not shut down the bandgap or POR circuit.

2.17. Configuration and Testing

This section describes the configuration and testing features of the MachXO4 RoT devices.

2.17.1. IEEE 1149.1-Compliant Boundary Scan Testability

All MachXO4 RoT devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/O: TDI, TDO, TCK and TMS. The test access port shares its power supply with V_{CCIO} Bank 0 and can operate with LVCMOS3.3, 2.5, 1.8, 1.5, and 1.2 standards.

For more details on boundary scan test, see [Boundary Scan Testability with Lattice sysI/O Capability \(AN8066\)](#) and [Minimizing System Interruption During Configuration Using TransFR Technology \(FPGA-TN-02198\)](#).

2.17.2. Device Configuration

All MachXO4 RoT devices contain two ports that can be used for device configuration. These are the Test Access Port (TAP), which supports bit-wide configuration and the sysCONFIG port, which supports serial configuration through I2C or SPI. The TAP supports both the IEEE Standard 1149.1 Boundary Scan specification and the IEEE Standard 1532 In-System Configuration specification. There are various ways to configure a MachXO4 RoT device:

- Internal Flash Download
- JTAG
- Standard Serial Peripheral Interface (Master SPI mode) – interface to boot PROM memory
- System microprocessor to drive a serial slave SPI port (SSPI mode)
- Standard I2C Interface to system microprocessor

Upon power-up, the configuration SRAM is ready to be configured using the selected sysCONFIG port. Once a configuration port is selected, it remains active throughout that configuration cycle. The IEEE 1149.1 port can be activated any time after power-up by sending the appropriate command through the TAP port. Optionally, the device can run a CRC check upon entering the user mode. This ensures that the device is configured correctly.

The sysCONFIG port has 10 dual-function pins, which can be used as general purpose I/O, if they are not required for configuration.

Lattice design software uses proprietary compression technology to compress bitstreams for use in MachXO4 RoT devices. Use of this technology allows Lattice Semiconductor to provide a lower cost solution. In the unlikely event that this technology is unable to compress bitstreams to fit into the amount of on-chip Flash, there are a variety of techniques that can be used to allow the bitstream to fit in the on-chip Flash.

2.17.2.1. Encryption and Authentication

With the Cryptographic Engine, MachXO4 RoT device can provide highly secured control for the device programming and configuration. It uses ECDSA256 algorithm for Configuration Image Authentication. It has the AES256 encryption for additional security and IP protection.

2.17.2.2. Transparent Field Reconfiguration (TransFR)

TransFR is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a push-button solution. For more details, refer to [Minimizing System Interruption During Configuration Using TransFR Technology \(FPGA-TN-02198\)](#).

2.17.2.3. Lock Bits and Lock Control Policy

MachXO4 RoT device has read, program, and erase permission control for external CFG ports and for internal WISHBONE bus to access Flash sectors. External CFG ports include JTAG, slave SPI, and slave I2C. The way to support this feature is to deploy three permission control setting bits for each sectors as SEC_READ, SEC_PROG, and SEC_ERASE.

- SEC_READ — Disable the READ access. This prevents user content from being exposed to external CFG port.
- SEC_PROG— Disable the PROGRAM access. This prevents unexpected incremental programming to modify the current user setting, such as AES KEY, ECDSA PUBLIC KEY or authenticated Bitstream, and others.
- SEC_ERASE— Disable the ERASE access. This prevents unexpected incremental programming to modify the current user setting, such as AES KEY, ECDSA PUBLIC KEY or authenticated Bitstream, and others. This also ensures a safe boot up.

MachXO4 RoT device also provides *Hard Lock* and *Soft Lock* modes for flexible permission control. *Soft Lock* means the security setting bits can be modified by internal WISHBONE bus. In this way, user logic can enable or disable the access by altering the security control bits through internal WISHBONE Bus. *Hard Lock* mode means user logic cannot alter permission control bits through internal WISHBONE bus. The SEC_HLOCK bit is used to choose between the *Soft Lock* and *Hard Lock* modes.

For detailed information regarding Lock Bits and Lock Control Policy, refer to [MachXO4 Programming and Configuration Usage Guide \(FPGA-TN-02393\)](#).

2.17.2.4. Tamper Detection and Response

Configuration logic automatically detects a variety of threats from configuration ports. These threats include any commands/instructions that:

- Try to access Flash/SRAM without entering password or with entering wrong password, if password protection is enabled.
- Try to access Flash/SRAM that is under Soft/Hard Lock protection.
- Attempt to enter MANUFACTURE mode.
- Shift in a wrong password by LSC_SHIFT_PASSWORD.

The Configuration module asserts *threat detect* to user logic once the enabled type of threat has been detected. Also, the Configuration module reports which type of threat is detected and from which configuration port the threat comes.

Once a certain threat has been detected, user logic may inform the Configuration module to disable configuration ports to avoid a dictionary style attack.

2.17.2.5. Password

The MachXO4 RoT device maintains the legacy support, as in the previous generation, for password-based security access feature also known as Flash Protect Key. The Flash Protect Key feature provides a method of controlling access to the Configuration and Programming modes of the device. When enabled, the Configuration and Programming edit mode operations including Write, Verify and Erase operations are allowed only when coupled with a Flash Protect Key, which matches that expected by the device. Without a valid Flash Protect Key, you can perform only rudimentary non-configuration operations such as Read Device ID.

2.17.2.6. On-chip Dual-Boot

MachXO4 RoT devices can optionally boot from two patterns, a primary bitstream and a golden bitstream. If the primary bitstream is found to be corrupt while being downloaded into the SRAM, the device automatically reboots from the golden bitstream. MachXO4 RoT device also supports the option to boot from the latest image in a ping-pong style, or user select for the boot image.

Beyond the On-chip boot, MachXO4 RoT device also provides the external SPI flash boot option. Together with the On-chip boot flash, MachXO4 RoT device can enable the flexible multi-boot function.

2.17.2.7. Soft Error Detection (SED)

The Soft Error Detection (SED) feature is a CRC check of the SRAM cells after the device is configured. This check ensures that the SRAM cells were configured successfully. This feature is enabled by a configuration bit option. The SED can also be initiated in user mode through an input to the fabric. The clock for the SED circuit is generated using a

dedicated divider. The undivided clock from the on-chip oscillator is the input to this divider. For low power applications, you can switch off the Soft Error Detection circuit.

2.17.2.8. Soft Error Correction

The MachXO4 RoT device supports Soft Error Correction (SEC). When BACKGROUND_RECONFIG is enabled using the Lattice Radiant software in a design, asserting the PROGRAMN pin or issuing the REFRESH sysConfig command refreshes the SRAM array from configuration memory. Only the detected error bit is corrected. No other SRAM cells are changed, allowing the user design to function uninterrupted.

During the project design phase, if the overall system cannot guarantee containment of the error or its subsequent effects on downstream data or control paths, Lattice Semiconductor recommends using SED only. MachXO4 RoT device can then be soft-reset by asserting PROGRAMN or issuing the Refresh command over a sysConfig port in response to SED. Soft-reset additionally erases the SRAM array prior to the SRAM refresh, and asserts internal Reset circuitry to guarantee a known state.

2.18. TraceID

Each MachXO4 RoT device contains a unique (per device) TraceID that can be used for tracking purposes or for IP security applications. The TraceID is 64 bits long. Eight out of 64 bits are user-programmable, the remaining 56 bits are factory-programmed. The TraceID is accessible through the EFB WISHBONE interface and can also be accessed through the SPI, I2C, or JTAG interfaces.

2.19. Density Shifting

The MachXO4 RoT family has been designed to enable density migration within the same package. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization impact the likely success in each case. When migrating from lower to higher density or higher to lower density, ensure to review all the power supplies and NC pins of the chosen devices.

3. DC and Switching Characteristics

3.1. Absolute Maximum Rating

Table 3.1. Absolute Maximum Rating^{1, 2, 3}

	LFMXO4D ZC/HC (2.5 V/3.3 V)	LFMXO4D HE (1.2 V)
Supply Voltage V_{CC}	–0.5 V to 3.75 V	–0.5 V to 1.32 V
Output Supply Voltage V_{CCIO}	–0.5 V to 3.75 V	–0.5 V to 3.75 V
I/O Tri-state Voltage Applied ^{4, 5}	–0.5 V to 3.75 V	–0.5 V to 3.75 V
Dedicated Input Voltage Applied ⁴	–0.5 V to 3.75 V	–0.5 V to 3.75 V
Storage Temperature (Ambient)	–55 °C to 125 °C	–55 °C to 125 °C
Junction Temperature (T_J)	–40 °C to 125 °C	–40 °C to 125 °C

Notes:

1. Stress above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice [Thermal Management \(FPGA-TN-02044\)](#) document is required.
3. All voltages referenced to GND.
4. Overshoot and undershoot of –2 V to ($V_{IHMAX} + 2$) volts is permitted for a duration of <20 ns.
5. The dual-function I2C pins SCL and SDA are limited to –0.25 V to 3.75 V or to –0.3 V with a duration of <20 ns.

3.2. Recommended Operating Conditions

Table 3.2. Recommended Operating Conditions¹

Symbol	Parameter	Min.	Max.	Unit
$V_{CC} (HC/ZC)^1$	Core Supply Voltage for 2.5 V/3.3 V Devices	2.375	3.465	V
$V_{CC} (HE)^2$	Core Supply Voltage for 1.2 V Devices	1.14	1.26	V
$V_{CCIO}^{1, 3, 4}$	I/O Driver Supply Voltage	1.14	3.465	V
t_{JCOM}	Junction Temperature Commercial Operation	0	85	°C
t_{JIND}	Junction Temperature Industrial Operation	–40	100	°C
t_{JAUTO}	Junction Temperature Automotive Operation	–40	125	°C

Notes:

1. On HC and ZC devices, like power supplies must be tied together. For example, if V_{CCIO} and V_{CC} are both the same voltage, they must also be the same supply.
2. On HE devices, V_{CC} needs to be powered-up prior V_{CCIO} with fast ramp rate applied on V_{CC} and at least 20 ms delay before V_{CCIO} is powered up.
3. See recommended voltages by I/O standard in subsequent table.
4. V_{CCIO} pins of unused I/O banks should be connected to the V_{CC} power supply on boards.

3.3. Power Supply Ramp Rates

Table 3.3. Power Supply Ramp Rates¹

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{RAMP}	Power supply ramp rates for all power supplies.	0.01	—	40	V/ms

Note:

1. Assumes monotonic ramp rates.

3.4. Power-On-Reset Voltage Levels

Table 3.4. Power-On Reset Voltage Levels^{1, 2, 3, 4}

Symbol	Parameter	Commercial/Industrial			Automotive			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V _{PORUP}	Power-On-Reset ramp up trip point (band gap based circuit monitoring V _{CCINT} and V _{CCIO0})	0.90	—	1.06	0.90	—	1.06	V
V _{PORUPEXT}	Power-On-Reset ramp up trip point (band gap based circuit monitoring external V _{CC} power supply)	1.50	—	2.10	1.50	—	2.10	V
V _{PORNBG}	Power-On-Reset ramp down trip point (band gap based circuit monitoring V _{CCINT})	0.75	—	1.04	0.75	—	1.06	V
V _{PORDNBGEXT}	Power-On-Reset ramp down trip point (band gap based circuit monitoring V _{CC})	0.98	—	1.44	0.98	—	1.47	V
V _{PORDNSRAM}	Power-On-Reset ramp down trip point (SRAM based circuit monitoring V _{CCINT})	—	0.84	—	—	0.84	—	V
V _{PORDNSRAMEXT}	Power-On-Reset ramp down trip point (SRAM based circuit monitoring V _{CC})	—	1.16	—	—	1.16	—	V

Notes:

- These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.
- For devices without voltage regulators V_{CCINT} is the same as the V_{CC} supply voltage. For devices with voltage regulators, V_{CCINT} is regulated from the V_{CC} supply voltage.
- Note that V_{PORUP} (min.) and V_{PORNBG} (max.) are in different process corners. For any given process corner V_{PORNBG} (max.) is always 12.0 mV below V_{PORUP} (min.).
- V_{CCIO0} does not have a Power-On-Reset ramp down trip point. V_{CCIO0} must remain within the Recommended Operating Conditions to ensure proper operation.

3.5. Hot Socketing Specifications

Table 3.5. Hot Socketing Specifications^{1, 2, 3, 4}

Symbol	Parameter	Condition	Commercial/Industrial	Automotive	Unit
			Max.		
I _{DK}	Input or I/O leakage Current	0 < V _{IN} < V _{IH} (MAX)	±350	±400	μA

Notes:

- Insensitive to sequence of V_{CC} and V_{CCIO}. However, assumes monotonic rise/fall rates for V_{CC} and V_{CCIO}.
- 0 < V_{CC} < V_{CC} (MAX), 0 < V_{CCIO} < V_{CCIO} (MAX).
- I_{DK} is additive to I_{PU}, I_{PD} or I_{BH}.
- Clamp option is set to OFF.

3.6. Programming/Erase Specifications

Table 3.6. Programming/Erase Specifications

Symbol	Parameter	Commercial/Industrial		Automotive		Unit
		Min.	Max.	Min.	Max.	
N _{PROGCYC}	Flash Programming cycles per t _{RETENTION} ¹	—	10,000	—	1,000	Cycles
	Flash Write/Erase cycles ²	—	10,000	—	10,000	
t _{RETENTION}	Data retention at 125 °C junction temperature	—	—	2	—	Years
	Data retention at 100 °C junction temperature	10	—	—	—	
	Data retention at 85 °C junction temperature	20	—	—	—	

Notes:

- Maximum Flash memory reads are limited to 7.5E13 cycles over the lifetime of the product.
- A Write/Erase cycle is defined as any number of writes over time followed by any erase cycle.

3.7. ESD Performance

Refer to the MachXO4 RoT Product Family Qualification Summary for complete qualification data, including ESD performance. The MachXO4 RoT Family Qualification Summary can be requested from Lattice's Quality and Reliability Team.

3.8. DC Electrical Characteristics

Over Recommended Operating Conditions

Table 3.7. DC Electrical Characteristics

Symbol	Parameter	Condition	Commercial/Industrial			Automotive			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
$I_{IL}, I_{IH}^{1,4}$	Input or I/O Leakage	Clamp OFF and $V_{CCIO} < V_{IN} < V_{IH} \text{ (MAX)}$	—	—	175	—	—	175	μA
		Clamp OFF and $V_{IN} = V_{CCIO}$	–10	—	10	–10	—	11	μA
		Clamp OFF and $V_{CCIO} - 0.97 \text{ V} < V_{IN} < V_{CCIO}$	–175	—	—	–175	—	—	μA
		Clamp OFF and $0 \text{ V} < V_{IN} < V_{CCIO} - 0.97 \text{ V}$	—	—	10	—	—	10	μA
		Clamp OFF and $V_{IN} = \text{GND}$	—	—	10	—	—	10	μA
		Clamp ON and $0 \text{ V} < V_{IN} < V_{CCIO}$	—	—	10	—	—	11	μA
I_{PU}	I/O Active Pull-up Current	$0 < V_{IN} < 0.7 V_{CCIO}$	–30	—	–309	–26	—	–309	μA
I_{PD}	I/O Active Pull-down Current	$V_{IL} \text{ (MAX)} < V_{IN} < V_{CCIO}$	30	—	305	30	—	305	μA
I_{BHLS}	Bus Hold Low sustaining current	$V_{IN} = V_{IL} \text{ (MAX)}$	30	—	—	30	—	—	μA
I_{BHHS}	Bus Hold High sustaining current	$V_{IN} = 0.7V_{CCIO}$	–30	—	—	–27	—	—	μA
I_{BHLO}	Bus Hold Low Overdrive current	$0 \leq V_{IN} \leq V_{CCIO}$	—	—	305	—	—	305	μA
I_{BHHO}	Bus Hold High Overdrive current	$0 \leq V_{IN} \leq V_{CCIO}$	—	—	–309	—	—	–309	μA
V_{BHT}^3	Bus Hold Trip Points	—	$V_{IL} \text{ (MAX)}$	—	$V_{IH} \text{ (MIN)}$	$V_{IL} \text{ (MAX)}$	—	$V_{IH} \text{ (MIN)}$	V
C_1	I/O Capacitance ²	$V_{CCIO} = 3.3 \text{ V}, 2.5 \text{ V}, 1.8 \text{ V}, 1.5 \text{ V}, 1.2 \text{ V}$, $V_{CC} = \text{Typ.}, V_{IO} = 0 \text{ to } V_{IH} \text{ (MAX)}$	3	5	9	3	5	9	pf
V_{HYST}^3	Hysteresis for Schmitt Trigger Inputs ⁵	$V_{CCIO} = 3.3 \text{ V}$, Hysteresis = Large	—	450	—	—	450	—	mV
		$V_{CCIO} = 2.5 \text{ V}$, Hysteresis = Large	—	250	—	—	250	—	mV
		$V_{CCIO} = 1.8 \text{ V}$, Hysteresis = Large	—	125	—	—	125	—	mV
		$V_{CCIO} = 1.5 \text{ V}$, Hysteresis = Large	—	100	—	—	100	—	mV
		$V_{CCIO} = 3.3 \text{ V}$, Hysteresis = Small	—	250	—	—	250	—	mV
		$V_{CCIO} = 2.5 \text{ V}$, Hysteresis = Small	—	150	—	—	150	—	mV
		$V_{CCIO} = 1.8 \text{ V}$, Hysteresis = Small	—	60	—	—	60	—	mV
		$V_{CCIO} = 1.5 \text{ V}$, Hysteresis = Small	—	40	—	—	40	—	mV

Notes:

- Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
- $T_A = 25^\circ\text{C}$, $f = 1.0 \text{ MHz}$.
- Refer to V_{IL} and V_{IH} in [Table 3.11](#).
- When V_{IH} is higher than V_{CCIO} , a transient current typically of 30 ns in duration or less with a peak current of 6 mA can occur on the high-to-low transition. For true LVDS output pins in MachXO4 RoT devices, V_{IH} must be less than or equal to V_{CCIO} .
- With bus keeper circuit turned on.

3.9. Static Supply Current

Table 3.8. Static Supply Current^{1, 2, 3, 6}

Symbol	Parameter	Device	Typ. ⁴	Unit
I _{CC}	Core Power Supply	LFMXO4D-040HC	13	mA
		LFMXO4D-040ZC	10	mA
		LFMXO4D-050HC	13	mA
		LFMXO4D-050ZC	10	mA
		LFMXO4D-080HC	20	mA
		LFMXO4D-080ZC	12	mA
		LFMXO4D-080HE	6	mA
		LFMXO4D-110HC	20	mA
		LFMXO4D-110ZC	12	mA
		LFMXO4D-110HE	6	mA
I _{CCIO}	Bank Power Supply ⁵ V _{CCIO} = 2.5 V	All devices	10	uA

Notes:

1. Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at V_{CCIO} or GND, on-chip oscillator is off, on-chip PLL is off.
2. Frequency = 0 MHz.
3. T_j = 25 °C, power supplies at nominal voltage.
4. Does not include pull-up/pull-down.
5. To determine the MachXO4 RoT peak start-up current data, use the Power Calculator tool.
6. Determination of safe ambient operating conditions requires use of the Lattice Radiant Power Calculator tool.

3.10. Programming and Erase Supply Current

Table 3.9. Programming and Erase Supply Current^{1, 2, 3, 4}

Symbol	Parameter	Device	Typ. ⁴	Unit
I _{CC}	Core Power Supply	LFMXO4D-040HC	51.8	mA
		LFMXO4D-040ZC	49.4	mA
		LFMXO4D-050HC	51.8	mA
		LFMXO4D-050ZC	49.4	mA
		LFMXO4D-080HC	71	mA
		LFMXO4D-080ZC	64	mA
		LFMXO4D-080HE	60	mA
		LFMXO4D-110HC	71	mA
		LFMXO4D-110ZC	64	mA
		LFMXO4D-110HE	60	mA
I _{CCIO}	Bank Power Supply ⁵ V _{CCIO} = 2.5 V	All devices	10	uA

Notes:

1. Assumes all inputs are held at V_{CCIO} or GND and all outputs are tri-stated.
2. Typical user pattern.
3. JTAG programming is at 25 MHz.
4. T_j = 25 °C, power supplies at nominal voltage.
5. Per bank. V_{CCIO} = 2.5 V. Does not include pull-up/pull-down.

3.11. sysI/O Recommended Operating Conditions

Table 3.10. sysI/O Recommended Operating Conditions

Standard	V _{CCIO} (V)			V _{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVC MOS 3.3	3.135	3.3	3.465	—	—	—
LVC MOS 2.5	2.375	2.5	2.625	—	—	—
LVC MOS 1.8	1.71	1.8	1.89	—	—	—
LVC MOS 1.5	1.425	1.5	1.575	—	—	—
LVC MOS 1.2	1.14	1.2	1.26	—	—	—
LVTTL	3.135	3.3	3.465	—	—	—
LVDS25 ^{1, 2}	2.375	2.5	2.625	—	—	—
LVDS33 ^{1, 2}	3.135	3.3	3.465	—	—	—
LVPECL ¹	3.135	3.3	3.465	—	—	—
BLVDS ¹	2.375	2.5	2.625	—	—	—
MIPI ³	2.375	2.5	2.625	—	—	—
MIPI_LP ³	1.14	1.2	1.26	—	—	—
I3C33	3.135	3.3	3.465	—	—	—
I3C18	1.71	1.8	1.89	—	—	—
I3C12	1.14	1.2	1.26	—	—	—
LVC MOS25R33	3.135	3.3	3.465	1.1	1.25	1.4
LVC MOS18R33	3.135	3.3	3.465	0.75	0.9	1.05
LVC MOS18R25	2.375	2.5	2.625	0.75	0.9	1.05
LVC MOS15R33	3.135	3.3	3.465	0.6	0.75	0.9
LVC MOS15R25	2.375	2.5	2.625	0.6	0.75	0.9
LVC MOS12R33 ⁴	3.135	3.3	3.465	0.45	0.6	0.75
LVC MOS12R25 ⁴	2.375	2.5	2.625	0.45	0.6	0.75
LVC MOS10R33 ⁴	3.135	3.3	3.465	0.35	0.5	0.65
LVC MOS10R25 ⁴	2.375	2.5	2.625	0.35	0.5	0.65

Notes:

1. Inputs on-chip. Outputs are implemented with the addition of external resistors.
2. For the dedicated LVDS buffers.
3. Requires the addition of external resistors.
4. Supported only for inputs and BIDs for –6 speed grade devices.

3.12. sysI/O Single-Ended DC Electrical Characteristics

Table 3.11. sysI/O Single-Ended DC Electrical Characteristics^{1, 2}

Input/Output Standard	V _{IL}		V _{IH}		Commercial/Industrial		Automotive		IOL Max. ⁴ (mA)	IOH Max. ⁴ (mA)
	Min. (V) ³	Max. (V)	Min. (V)	Max. (V)	VOL Max. (V)	VOH Min. (V)	VOL Max. (V)	VOH Min. (V)		
LVCMOS 3.3 LVTTL	-0.3	0.8	2.0	3.6	0.4	V _{CCIO} - 0.4	0.4	V _{CCIO} - 0.4	4	-4
									8	-8
									12	-12
									16	-16
					0.2	V _{CCIO} - 0.2	0.2	V _{CCIO} - 0.2	0.1	-0.1
LVCMOS 2.5	-0.3	0.7	1.7	3.6	0.4	V _{CCIO} - 0.4	0.4	V _{CCIO} - 0.4	4	-4
									8	-8
									12	-12
					0.2	V _{CCIO} - 0.2	0.2	V _{CCIO} - 0.2	0.1	-0.1
LVCMOS 1.8	-0.3	0.35 V _{CCIO}	0.65 V _{CCIO}	3.6	0.4	V _{CCIO} - 0.4	0.4	V _{CCIO} - 0.4	4	-4
									8	-8
									12	-12
					0.2	V _{CCIO} - 0.2	0.2	V _{CCIO} - 0.2	0.1	-0.1
LVCMOS 1.5	-0.3	0.35 V _{CCIO}	0.65 V _{CCIO}	3.6	0.4	V _{CCIO} - 0.4	0.4	V _{CCIO} - 0.4	4	-4
									8	-8
					0.2	V _{CCIO} - 0.2	0.2	V _{CCIO} - 0.2	0.1	-0.1
LVCMOS 1.2	-0.3	0.35 V _{CCIO}	0.65 V _{CCIO}	3.6	0.4	V _{CCIO} - 0.4	0.4	V _{CCIO} - 0.4	4	-2
									8	-6
					0.2	V _{CCIO} - 0.2	0.2	V _{CCIO} - 0.2	0.1	-0.1
I3C33	-0.3	0.8	2.0	3.6	0.27	V _{CCIO} - 0.27	0.27	V _{CCIO} - 0.27	4	-4
I3C18	-0.3	0.35 V _{CCIO}	0.65 V _{CCIO}	3.6	0.27	V _{CCIO} - 0.27	0.27	V _{CCIO} - 0.27	4	-4
I3C12	-0.3	0.35 V _{CCIO}	0.65 V _{CCIO}	3.6	0.18	V _{CCIO} - 0.19	0.18	V _{CCIO} - 0.20	2	-2
LVCMOS25R33	-0.3	V _{REF} - 0.1	V _{REF} + 0.1	3.6	NA	NA	NA	NA	NA	NA
LVCMOS18R33	-0.3	V _{REF} - 0.1	V _{REF} + 0.1	3.6	NA	NA	NA	NA	NA	NA
LVCMOS18R25	-0.3	V _{REF} - 0.1	V _{REF} + 0.1	3.6	NA	NA	NA	NA	NA	NA
LVCMOS15R33	-0.3	V _{REF} - 0.1	V _{REF} + 0.1	3.6	NA	NA	NA	NA	NA	NA
LVCMOS15R25	-0.3	V _{REF} - 0.1	V _{REF} + 0.1	3.6	NA	NA	NA	NA	NA	NA
LVCMOS12R33	-0.3	V _{REF} - 0.1	V _{REF} + 0.1	3.6	0.4	NA	0.4	NA	24, 16, 12, 8, 4	NA
LVCMOS12R25	-0.3	V _{REF} - 0.1	V _{REF} + 0.1	3.6	0.4	NA	0.4	NA	16, 12, 8, 4	NA
LVCMOS10R33	-0.3	V _{REF} - 0.1	V _{REF} + 0.1	3.6	0.4	NA	0.4	NA	24, 16, 12, 8, 4	NA
LVCMOS10R25	-0.3	V _{REF} - 0.1	V _{REF} + 0.1	3.6	0.4	NA	0.4	NA	16, 12, 8, 4	NA

Notes:

1. MachXO4 RoT devices allow LVCMOS inputs to be placed in I/O banks where VCCIO is different from what is specified in the applicable JEDEC specification. This is referred to as a ratioed input buffer. In a majority of cases, this operation follows or exceeds the applicable JEDEC specification.
2. MachXO4 RoT devices allow for LVCMOS referenced I/O, which follow applicable JEDEC specifications.
3. The dual-function I2C pins SCL and SDA are limited to a V_{IL} min of -0.25 V or to -0.3 V with a duration of <10 ns.

- For electromigration, the average DC current sourced or sunk by I/O pads between two consecutive V_{CCIO} or GND pad connections, or between the last V_{CCIO} or GND in an I/O bank and the end of an I/O bank, as shown in the Logic Signal Connections table (also shown as I/O grouping) shall not exceed a maximum of $n * 8$ mA. “n” is the number of I/O pads between the two consecutive bank V_{CCIO} or GND connections or between the last V_{CCIO} and GND in a bank and the end of a bank. I/O Grouping can be found in the Data Sheet Pin Tables, which can also be generated from the Lattice Radiant software.

3.13. sysI/O Differential Electrical Characteristics

The LVDS differential output buffers are available on the top side of the MachXO4 RoT FPGA family.

3.13.1. LVDS

Over Recommended Operating Conditions.

Table 3.12. LVDS

Parameter Symbol	Parameter Description	Test Condition	Min.	Typ.	Max.	Unit
V_{INP}, V_{INM}	Input Voltage	$V_{CCIO} = 3.3$ V	0	—	2.6	V
		$V_{CCIO} = 2.5$ V	0	—	2.0	V
V_{THD}	Differential Input Threshold	—	± 100	—		mV
V_{CM}	Input Common Mode Voltage	$V_{CCIO} = 3.3$ V	0.05	—	2.6	V
		$V_{CCIO} = 2.5$ V	0.05	—	2.0	V
I_{IN}	Input current	Power on	—	—	± 10	μ A
V_{OH}	Output high voltage for V_{OP} or V_{OM}	$R_T = 100$ Ω	—	1.375	—	V
V_{OL}	Output low voltage for V_{OP} or V_{OM}	$R_T = 100$ Ω	0.9	1.025	—	V
V_{OD}	Output voltage differential	$(V_{OP} - V_{OM}), R_T = 100$ Ω	250	350	450	mV
ΔV_{OD}	Change in V_{OD} between high and low	—	—	—	50	mV
V_{OS}	Output voltage offset	$(V_{OP} - V_{OM})/2, R_T = 100$ Ω	1.1	1.20	1.395	V
ΔV_{OS}	Change in V_{OS} between H and L	—	—	—	50	mV
I_{OSD}	Output short circuit current	$V_{OD} = 0$ V driver outputs shorted	—	—	24	mA

3.13.2. LVDS Emulation

MachXO4 RoT devices can support LVDS outputs through emulation (LVDS25E). The output is emulated using complementary LVC MOS outputs in conjunction with resistors across the driver outputs on all devices. The scheme shown in Figure 3.1 is one possible solution for LVDS standard implementation. Resistor values in Figure 3.1 are industry standard values for 1% resistors.

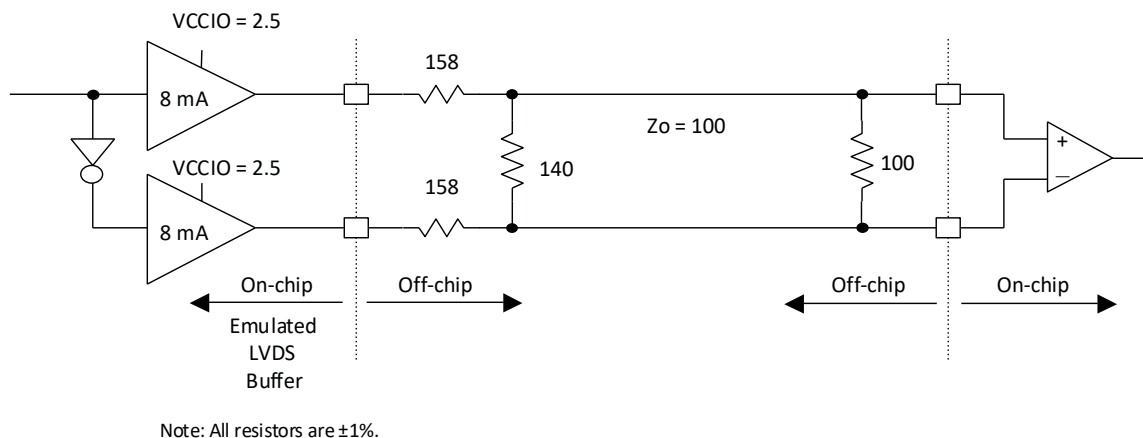


Figure 3.1. LVDS Using External Resistors (LVDS25E)

3.13.3. LVDS25E DC Conditions

Over Recommended Operating Conditions

Table 3.13. LVDS25E DC Conditions

Parameter	Description	Typ.	Unit
Z_{OUT}	Output impedance	20	Ω
R_S	Driver series resistor	158	Ω
R_P	Driver parallel resistor	140	Ω
R_T	Receiver termination	100	Ω
V_{OH}	Output high voltage	1.43	V
V_{OL}	Output low voltage	1.07	V
V_{OD}	Output differential voltage	0.35	V
V_{CM}	Output common mode voltage	1.25	V
Z_{BACK}	Back impedance	100	Ω
I_{DC}	DC output current	6.03	mA

3.13.4. BLVDS

The MachXO4 RoT device supports the BLVDS standard through emulation. The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs. The input standard is supported by the LVDS differential input buffer. BLVDS is intended for use when multi-drop and bidirectional multi-point differential signaling is required. The scheme shown in Figure 3.2 is one possible solution for bidirectional multi-point differential signals.

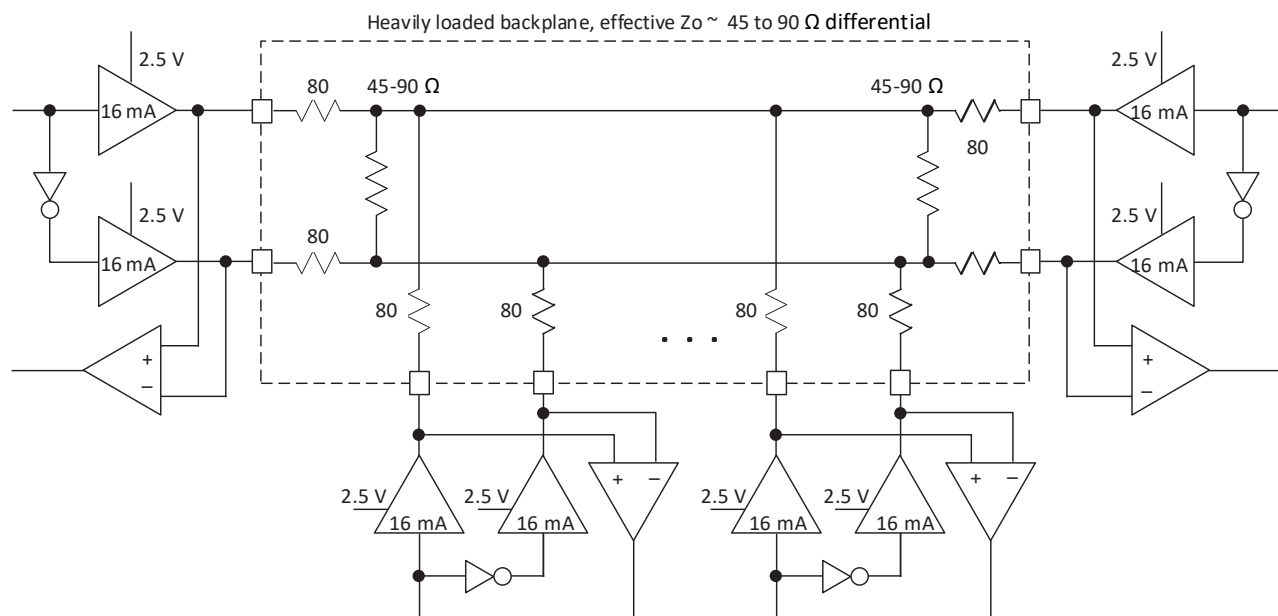


Figure 3.2. BLVDS Multi-point-Output Example

3.13.5. BLVDS DC Condition

Over Recommend Operating Conditions

Table 3.14. BLVDS DC Conditions

Symbol	Description	Nominal		Unit
		Zo = 45	Zo = 90	
Z _{OUT}	Output impedance	20	20	Ω
R _S	Driver series resistance	80	80	Ω
R _{TLEFT}	Left end termination	45	90	Ω
R _{TRIGHT}	Right end termination	45	90	Ω
V _{OH}	Output high voltage	1.375	1.480	V
V _{OL}	Output low voltage	1.125	1.020	V
V _{OD}	Output differential voltage	0.25	0.46	V
V _{CM}	Output common mode voltage	1.250	1.250	V
I _{DC}	DC output current	11.24	10.20	mA

Note:

1. For input buffer, see [Table 3.12](#).

3.13.6. LVPECL

The MachXO4 RoT device supports the differential LVPECL standard through emulation. This output standard is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all the devices. The LVPECL input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3.3 is one possible solution for point-to-point signals.

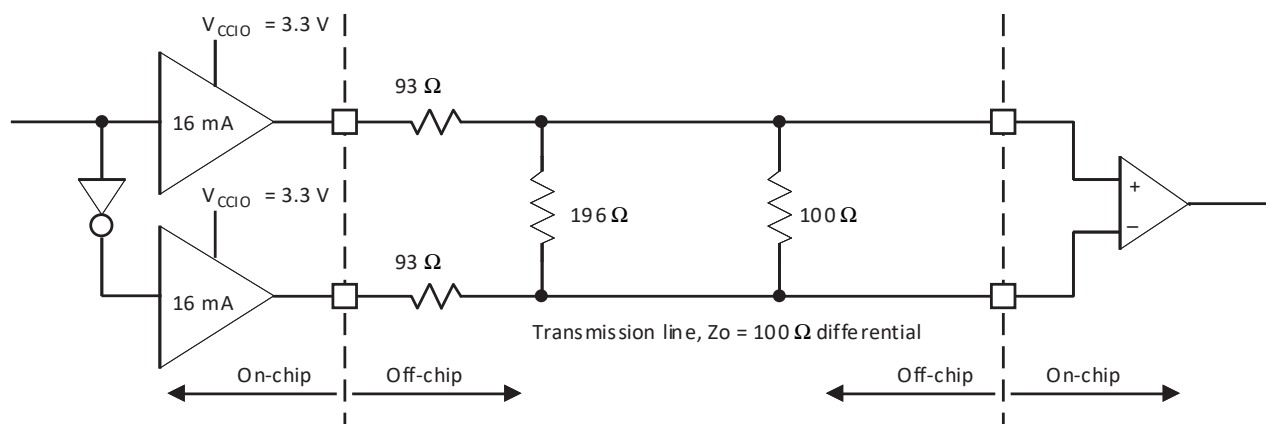


Figure 3.3. Differential LVPECL

3.13.7. LVPECL DC Conditions

Over Recommended Operating Conditions

Table 3.15. LVPECL DC Conditions¹

Symbol	Description	Nominal	Unit
Z _{OUT}	Output impedance	20	Ω
R _S	Driver series resistor	93	Ω
R _P	Driver parallel resistor	196	Ω
R _T	Receiver termination	100	Ω
V _{OH}	Output high voltage	2.05	V
V _{OL}	Output low voltage	1.25	V
V _{OD}	Output differential voltage	0.80	V
V _{CM}	Output common mode voltage	1.65	V
Z _{BACK}	Back impedance	100	Ω
I _{DC}	DC output current	12.11	mA

Note:

1. For input buffer, see [Table 3.12](#).

For further information on LVPECL, BLVDS, and other differential interfaces, see details of additional technical documentation at the end of the data sheet.

3.13.8. MIPI D-PHY Emulation

MachXO4 RoT devices can support MIPI D-PHY unidirectional High Speed (HS) and bidirectional Low Power (LP) inputs and outputs through emulation. In conjunction with external resistors, High Speed I/O use the LVDS25E buffer and Low Power I/O use the LVCMOS buffers. The scheme shown in [Figure 3.4](#) is one possible solution for MIPI D-PHY Receiver implementation. The scheme shown in [Figure 3.5](#) is one possible solution for MIPI D-PHY Transmitter implementation.

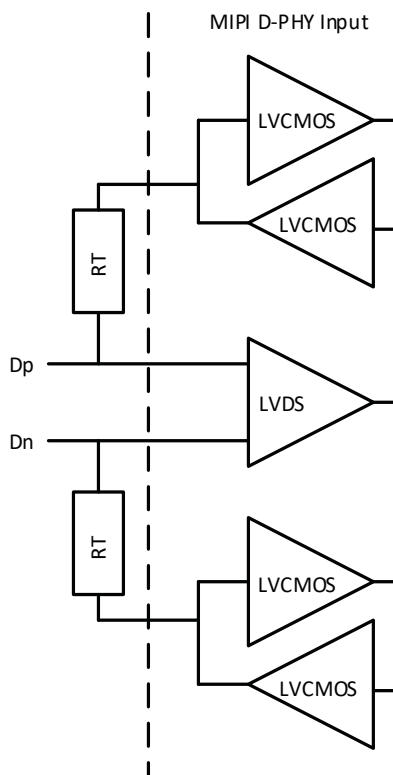


Figure 3.4. MIPI D-PHY Input Using External Resistors

Over recommended operating conditions.

Table 3.16. MIPI DC Conditions

Symbol	Description	Min.	Typ.	Max.	Unit
Receiver					
External Termination					
RT	1% external resistor with $V_{CCIO}=2.5\text{ V}$	—	50	—	Ω
	1% external resistor with $V_{CCIO}=3.3\text{ V}$	—	50	—	Ω
High Speed					
V_{CCIO}	V_{CCIO} of the Bank with LVDS Emulated input buffer	—	2.5	—	V
	V_{CCIO} of the Bank with LVDS Emulated input buffer	—	3.3	—	V
V_{CMRX}	Common-mode voltage HS receive mode	150	200	250	mV
V_{IDTH}	Differential input high threshold	—	—	100	mV
V_{IDTL}	Differential input low threshold	–100	—	—	mV
V_{IHHS}	Single-ended input high voltage	—	—	300	mV
V_{ILHS}	Single-ended input low voltage	100	—	—	mV
ZID	Differential input impedance	80	100	120	Ω
Low Power					
V_{CCIO}	V_{CCIO} of the Bank with LVCMOS12D 6 mA drive bidirectional I/O buffer	—	1.2	—	V
V_{IH}	Logic 1 input voltage	—	—	0.88	V
V_{IL}	Logic 0 input voltage, not in ULP State	0.55	—	—	V
V_{HYST}	Input hysteresis	25	—	—	mV

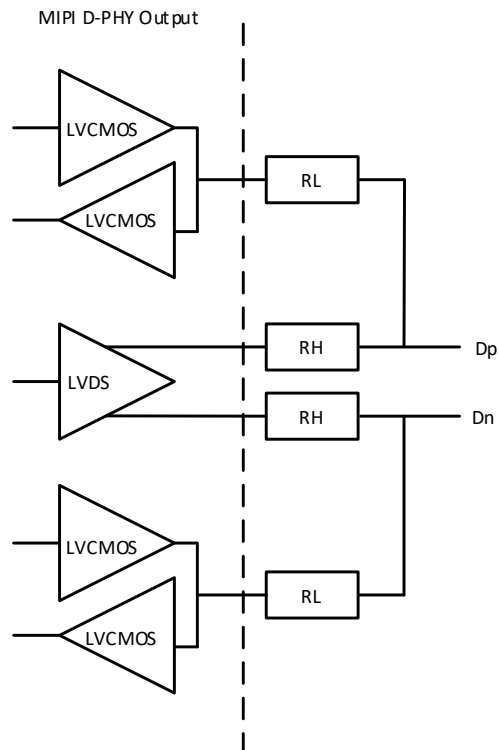


Figure 3.5. MIPI D-PHY Output Using External Resistors

Over recommended operating conditions.

Table 3.17. MIPI D-PHY Output DC Conditions

Symbol	Description	Min.	Typ.	Max.	Unit
Transmitter					
External Termination					
R_L	1% external resistor with $V_{CCIO} = 2.5$ V	—	50	—	Ω
	1% external resistor with $V_{CCIO} = 3.3$ V	—	50	—	
R_H	1% external resistor with performance up to 800 Mbps or with performance up 900 Mbps when $V_{CCIO} = 2.5$ V	—	330	—	Ω
	1% external resistor with performance between 800 Mbps to 900 Mbps when $V_{CCIO} = 3.3$ V	—	464	—	Ω
High Speed					
V_{CCIO}	V_{CCIO} of the Bank with LVDS Emulated output buffer	—	2.5	—	V
	V_{CCIO} of the Bank with LVDS Emulated output buffer	—	3.3	—	V
V_{CMTX}	HS transmit static common mode voltage	150	200	250	mV
V_{OD}	HS transmit differential voltage	140	200	270	mV
V_{OHHS}	HS output high voltage	—	—	360	mV
ZOS	Single-ended output impedance	—	50	—	Ω
ΔZOS	Single-ended output impedance mismatch	—	—	10	%
Low Power					
V_{CCIO}	V_{CCIO} of the Bank with LVCMOS12D 6 mA drive bidirectional I/O buffer	—	1.2	—	V
V_{OH}	Output high level	1.1	1.2	1.3	V
V_{OL}	Output low level	–50	0	50	mV
$ZOLP$	Output impedance of LP transmitter	110	—	—	Ω

3.13.9. Comparator Function

MachXO4 RoT devices can support a limited comparator function using the 3.3 V referenced input buffers. The scheme is shown in Figure 3.6.

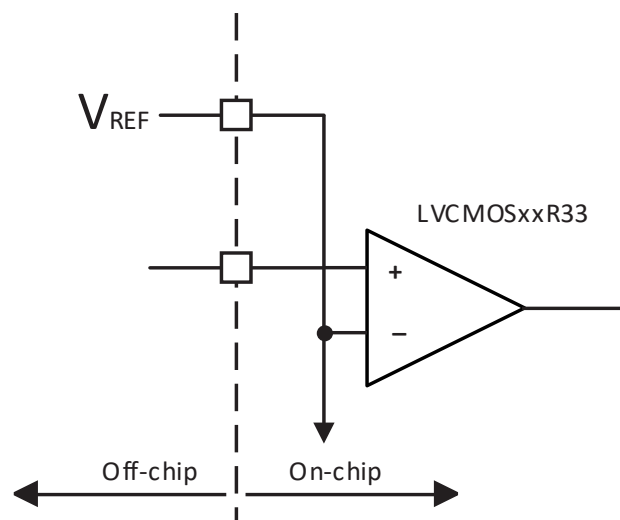


Figure 3.6. Comparator Function Using Referenced Input Buffers

Over recommended operating conditions.

Table 3.18. Comparator Specifications¹

Parameter	Description	Test Condition	–6/–5 (Commercial/Industrial)		–5 (Automotive)		Unit
			Min.	Max.	Min.	Max.	
V _{IH}	Single-Ended input	V _{CCIO} = 3.3 V	V _{REF} + 0.1	3.6	V _{REF} + 0.1	3.6	MHz
V _{IL}			–0.3	V _{REF} – 0.1	–0.3	V _{REF} – 0.1	
V _{ref}	Voltage Ref input	V _{CCIO} = 3.3 V	0.05	2.605	0.05	2.605	V
t _{W_PRI}	Propagation Delay	V _{CCIO} = 3.3 V	—	10	—	10	ns
V _{OS}	Input Offset Voltage	V _{CCIO} = 3.3 V	–100	100	–105	105	mV

Note:

1. Comparator function supported for 3.3 V Referenced Input Buffer types LVCMOS25R33, LVCMOS18R33, LVCMOS15R33, LVCMOS12R33, and LVCMOS10R33.

3.14. Typical Building Block Function Performance

3.14.1. Pin-to-Pin Performance (LVCMOS25 12 mA Drive)

Table 3.19. Pin-to-Pin Performance (LVCMOS25 12 mA Drive)

Function	–6 Timing	–3 Timing	Unit
Basic Function			
16-bit decoder	7.9	13.0	ns
4:1 MUX	6.6	9.9	ns
16:1 MUX	7.8	13.3	ns

3.14.2. Register-to-Register Performance

Table 3.20. Register-to-Register Performance

Function	–6 Timing	–3 Timing	Unit
Basic Function			
16:1 MUX	423	191	MHz
16-bit adder	277	125	MHz
16-bit counter	325	149	MHz
64-bit counter	161	77	MHz
Embedded Memory Function			
1024x9 True Dual-Port RAM (Write Through or Normal, EBR output registers)	182	90	MHz
Distributed Memory Function			
16x4 Pseudo Dual-Port RAM (one PFU)	500	400	MHz

Note: The above timing numbers in Table 3.19 and Table 3.20 are generated using the Lattice Radiant design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Lattice Radiant software.

3.15. Derating Logic Timing

Logic timing provided in the following sections of the data sheet and the Lattice design tools are worst case numbers in the operating range. Actual delays may be much faster. Lattice design tools can provide logic timing numbers at a particular temperature and voltage.

3.16. Maximum sysI/O Buffer Performance

Table 3.21. Maximum sysI/O Buffer Performance

I/O Standard	Maximum Speed	Unit
MIPI	450	MHz
LVDS25	400	MHz
LVDS25E	150	MHz
BLVDS25	150	MHz
BLVDS25E	150	MHz
MLVDS25	150	MHz
MLVDS25E	150	MHz
LVPECL33	150	MHz
LVPECL33E	150	MHz
LVTTL33	150	MHz
LVTTL33D	150	MHz
LVC MOS33	150	MHz
LVC MOS33D	150	MHz
LVC MOS25	150	MHz
LVC MOS25D	150	MHz
LVC MOS18	150	MHz
LVC MOS18D	150	MHz
LVC MOS15	150	MHz
LVC MOS15D	150	MHz
LVC MOS12	91	MHz
LVC MOS12D	91	MHz
I3C33	12.5	MHz
I3C18	12.5	MHz
I3C12	12.5	MHz

3.17. MachXO4 RoT External Switching Characteristics – HE/HC Devices

Over Recommended Operating Conditions.

Table 3.22. MachXO4 RoT External Switching Characteristics – HE/HC Devices^{1, 2, 3, 4, 5, 6, 10}

Parameter	Description	Device	–6 (Commercial/ Industrial)		–5 (Commercial/ Industrial)		–5 (Automotive) Preliminary		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Clocks									
Primary Clocks									
f _{MAX_PRI} ⁷	Frequency for Primary Clock Tree	All MachXO4 RoT devices	—	390	—	320	—	320	MHz
t _{W_PRI}	Clock Pulse Width for Primary Clock	All MachXO4 RoT devices	0.5	—	0.6	—	0.6	—	ns
t _{SKEW_PRI}	Primary Clock Skew Within a Device	LFMXO4D-040, LFMXO4D-050	—	611	—	748	—	1458	ps
		LFMXO4D-080, LFMXO4D-110	—	1423	—	1432	—	1432	ps
Edge Clock									
f _{MAX_EDGE} ⁷	Frequency for Edge Clock	MachXO4 RoT	—	400	—	333	—	333	MHz
Pin-LUT-Pin Propagation Delay									
t _{PD}	Best case propagation delay through one LUT-4	All MachXO4 RoT devices	—	6.70	—	7.00	—	7.00	ns
General I/O Pin Parameters (Using Primary Clock without PLL)									
t _{CO}	Clock to Output – PIO Output Register	LFMXO4D-040, LFMXO4D-050	—	6.345	—	6.664	—	7.79	ns
		LFMXO4D-080, LFMXO4D-110	—	7.53	—	7.83	—	7.83	ns
t _{SU}	Clock to Data Setup – PIO Input Register	LFMXO4D-040, LFMXO4D-050	–0.546	—	–0.546	—	–0.546	—	ns
		LFMXO4D-080, LFMXO4D-110	–0.24	—	–0.24	—	–0.24	—	ns
t _H	Clock to Data Hold – PIO Input Register	LFMXO4D-040, LFMXO4D-050	2.838	—	3.004	—	3.035	—	ns
		LFMXO4D-080, LFMXO4D-110	1.99	—	2.24	—	3.1	—	ns
t _{SU_DEL}	Clock to Data Setup – PIO Input Register with Data Input Delay	LFMXO4D-040, LFMXO4D-050	1.865	—	1.989	—	2.126	—	ns
		LFMXO4D-080, LFMXO4D-110	1.65	—	1.80	—	1.96	—	ns

Parameter	Description	Device	–6 (Commercial/ Industrial)		–5 (Commercial/ Industrial)		–5 (Automotive) Preliminary		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t _{H_DEL}	Clock to Data Hold – PIO Input Register with Input Data Delay	LFMXO4D-040, LFMXO4D-050	0.363	—	0.363	—	0	—	ns
		LFMXO4D-080, LFMXO4D-110	–0.24	—	–0.24	—	–0.14	—	ns
f _{MAX_IO}	Clock Frequency of I/O and PFU Register	All MachXO4 RoT devices	—	390	—	320	—	320	MHz
General I/O Pin Parameters (Using Edge Clock without PLL)									
T _{COE}	Clock to Output – PIO Output Register	LFMXO4D-040, LFMXO4D-050	—	7.45	—	7.68	—	7.68	ns
		LFMXO4D-080, LFMXO4D-110	—	8.93	—	9.35	—	9.35	ns
t _{SUE}	Clock to Data Setup – PIO Input Register	LFMXO4D-040, LFMXO4D-050	–0.16	—	–0.16	—	–0.16	—	ns
		LFMXO4D-080, LFMXO4D-110	–0.20	—	–0.20	—	–0.20	—	ns
t _{HE}	Clock to Data Hold – PIO Input Register	LFMXO4D-040, LFMXO4D-050	1.89	—	2.16	—	2.16	—	ns
		LFMXO4D-080, LFMXO4D-110	1.98	—	2.25	—	2.25	—	ns
t _{SU_DELE}	Clock to Data Setup – PIO Input Register with Data Input Delay	LFMXO4D-040, LFMXO4D-050	1.74	—	1.88	—	1.88	—	ns
		LFMXO4D-080, LFMXO4D-110	1.71	—	1.85	—	1.85	—	ns
t _{H_DELE}	Clock to Data Hold – PIO Input Register with Input Data Delay	LFMXO4D-040, LFMXO4D-050	–0.34	—	–0.34	—	–0.34	—	ns
		LFMXO4D-080, LFMXO4D-110	–0.30	—	–0.30	—	–0.30	—	ns
General I/O Pin Parameters (Using Primary Clock with PLL)									
t _{COPLL}	Clock to Output – PIO Output Register	LFMXO4D-040, LFMXO4D-050	—	4.467	—	4.661	—	5.01	ns
		LFMXO4D-080, LFMXO4D-110	—	5.55	—	6.13	—	6.13	ns
t _{SUPLL}	Clock to Data Setup – PIO Input Register	LFMXO4D-040, LFMXO4D-050	0.357	—	0.357	—	0.726	—	ns
		LFMXO4D-080, LFMXO4D-110	0.33	—	0.33	—	0.53	—	ns
t _{HPLL}	Clock to Data Hold – PIO Input Register	LFMXO4D-040, LFMXO4D-050	0.882	—	0.882	—	0.882	—	ns
		LFMXO4D-080, LFMXO4D-110	0.47	—	0.55	—	0.67	—	ns
t _{SU_DELPLL}	Clock to Data Setup – PIO Input Register with Data Input Delay	LFMXO4D-040, LFMXO4D-050	3.546	—	3.814	—	3.903	—	ns
		LFMXO4D-080, LFMXO4D-110	3.06	—	3.37	—	4.12	—	ns

Parameter	Description	Device	–6 (Commercial/ Industrial)		–5 (Commercial/ Industrial)		–5 (Automotive) Preliminary		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t _{H_DELP}	Clock to Data Hold – PIO	LFMXO4D-040, LFMXO4D-050	–0.447	—	–0.447	—	–0.447	—	ns
	Input Register with Input Data Delay	LFMXO4D-080, LFMXO4D-110	–0.93	—	–0.93	—	–0.93	—	ns
Generic DDRX1 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDR1_RX.SCLK.Aligned ^{8, 9, 13}									
t _{DVA}	Input Data Valid After CLK	All MachXO4 RoT devices, all sides	—	0.317	—	0.344	—	0.344	UI
t _{DVE}	Input Data Hold After CLK		0.742	—	0.702	—	0.702	—	UI
f _{DATA}	DDRX1 Input Data Speed		—	300	—	250	—	250	Mbps
f _{DDRX1}	DDRX1 SCLK Frequency		—	150	—	125	—	125	MHz
Generic DDRX1 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDR1_RX.SCLK.Centered ^{8, 9, 13}									
t _{SU}	Input Data Setup Before CLK	All MachXO4 RoT devices, all sides	0.566	—	0.566	—	0.56	—	ns
t _{HO}	Input Data Hold After CLK		0.778	—	0.879	—	0.879	—	ns
f _{DATA}	DDRX1 Input Data Speed		—	300	—	250	—	250	Mbps
f _{DDRX1}	DDRX1 SCLK Frequency		—	150	—	125	—	125	MHz
Generic DDRX2 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDR2_RX.ECLK.Aligned ^{8, 9}									
t _{DVA}	Input Data Valid After CLK	MachXO4 RoT devices, bottom side only	—	0.316	—	0.342	—	0.342	UI
t _{DVE}	Input Data Hold After CLK		0.710	—	0.675	—	0.681	—	UI
f _{DATA}	DDRX2 Serial Input Data Speed		—	664	—	554	—	554	Mbps
f _{DDRX2}	DDRX2 ECLK Frequency		—	332	—	277	—	277	MHz
f _{SCLK}	SCLK Frequency		—	166	—	139	—	139	MHz

Parameter	Description	Device	–6 (Commercial/ Industrial)		–5 (Commercial/ Industrial)		–5 (Automotive) Preliminary		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Generic DDRX2 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX2_RX.ECLK.Centered ^{8, 9}									
t _{SU}	Input Data Setup Before CLK	MachXO4 RoT devices, bottom side only	0.233	—	0.233	—	0.233	—	ns
t _{HO}	Input Data Hold After CLK		0.287	—	0.287	—	0.287	—	ns
f _{DATA}	DDRX2 Serial Input Data Speed		—	664	—	554	—	554	Mbps
f _{DDRX2}	DDRX2 ECLK Frequency		—	332	—	277	—	277	MHz
f _{SCLK}	SCLK Frequency		—	166	—	139	—	139	MHz
Generic DDR4 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDR4_RX.ECLK.Aligned ⁸									
t _{DVA}	Input Data Valid After ECLK	LFMXO4D-040, LFMXO4D-050 devices, bottom side only	—	0.359	—	0.383	—	0.32	UI
		LFMXO4D-080, LFMXO4D-110 devices, bottom side only	—	0.307	—	0.320	—	0.320	
t _{DVE}	Input Data Hold After ECLK	LFMXO4D-040, LFMXO4D-050 devices, bottom side only	0.837	—	0.765	—	0.774	—	UI
		LFMXO4D-080, LFMXO4D-110 devices, bottom side only	0.782	—	0.699	—	0.774	—	
f _{DATA}	DDR4 Serial Input Data Speed	MachXO4 RoT devices, bottom side only	—	800	—	630	—	630	Mbps
f _{DDR4}	DDR4 ECLK Frequency		—	400	—	315	—	315	MHz
f _{SCLK}	SCLK Frequency		—	100	—	79	—	79	MHz

Parameter	Description	Device	–6 (Commercial/ Industrial)		–5 (Commercial/ Industrial)		–5 (Automotive) Preliminary		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Generic DDR4 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDR4_RX.ECLK.Centered ⁸									
t _{SU}	Input Data Setup Before ECLK	MachXO4 RoT devices, bottom side only	0.233	—	0.233	—	0.241	—	ns
t _{HO}	Input Data Hold After ECLK		0.287	—	0.287	—	0.291	—	ns
f _{DATA}	DDR4 Serial Input Data Speed		—	800	—	630	—	630	Mbps
f _{DDR4}	DDR4 ECLK Frequency		—	400	—	315	—	315	MHz
f _{SCLK}	SCLK Frequency		—	100	—	79	—	79	MHz
7:1 LVDS Inputs (GDDR71_RX.ECLK.7:1) ⁹									
t _{DVA}	Input Data Valid After ECLK (See Figure 3.7)	LFMXO4D-040, LFMXO4D-050 devices, bottom side only	—	0.367	—	0.405	—	0.243	UI
		LFMXO4D-080, LFMXO4D-110 devices, bottom side only	—	0.290	—	0.320	—	0.243	
t _{DVE}	Input Data Hold After ECLK (See Figure 3.7)	LFMXO4D-040, LFMXO4D-050 devices, bottom side only	0.818	—	0.791	—	0.703	—	UI
		LFMXO4D-080, LFMXO4D-110 devices, bottom side only	0.739	—	0.699	—	0.703	—	
f _{DATA}	DDR71 Serial Input Data Speed	MachXO4 RoT devices, bottom side only	—	756	—	630	—	630	Mbps
f _{DDR71}	DDR71 ECLK Frequency		—	378	—	315	—	315	MHz
f _{CLKIN}	7:1 Input Clock Frequency (SCLK) (minimum limited by PLL)		—	108	—	90	—	90	MHz

Parameter	Description	Device	–6 (Commercial/ Industrial)		–5 (Commercial/ Industrial)		–5 (Automotive) Preliminary		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
MIPI D-PHY Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input - GDDR4_RX.ECLK.Centered ^{10, 11, 12}									
t _{SU} ¹⁶	Input Data Setup Before ECLK	All MachXO4 RoT devices, bottom side only	0.200	—	0.200	—	0.312	—	UI
t _{HO} ¹⁶	Input Data Hold After ECLK		0.200	—	0.200	—	0.367	—	UI
f _{DATA} ¹⁵	MIPI D-PHY Input Data Speed		—	900	—	900	—	900	Mbps
f _{DDR4} ¹⁵	MIPI D-PHY ECLK Frequency		—	450	—	450	—	450	MHz
f _{SCLK} ¹⁵	SCLK Frequency		—	112.5	—	112.5	—	112.5	MHz
Generic DDR Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDR1_TX.SCLK.Aligned ^{8, 13}									
t _{DIA}	Output Data Invalid After CLK Output	All MachXO4 RoT devices, all sides	—	0.52	—	0.55	—	0.55	ns
t _{DIB}	Output Data Invalid Before CLK Output		—	0.52	—	0.55	—	0.55	ns
f _{DATA}	DDR1 Output Data Speed		—	300	—	250	—	250	Mbps
f _{DDR1}	DDR1 SCLK frequency		—	150	—	125	—	125	MHz
Generic DDR Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDR1_TX.SCLK.Centered ^{8, 13}									
t _{DVB}	Output Data Valid Before CLK Output	All MachXO4 RoT devices, all sides	1.210	—	1.510	—	1.510	—	ns
t _{DVA}	Output Data Valid After CLK Output		1.210	—	1.510	—	1.510	—	ns
f _{DATA}	DDR1 Output Data Speed		—	300	—	250	—	250	Mbps
f _{DDR1}	DDR1 SCLK Frequency (minimum limited by PLL)		—	150	—	125	—	125	MHz

Parameter	Description	Device	–6 (Commercial/ Industrial)		–5 (Commercial/ Industrial)		–5 (Automotive) Preliminary		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Generic DDRX2 Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDR2_TX.ECLK.Aligned ⁸									
t _{DIA}	Output Data Invalid After CLK Output	MachXO4 RoT devices, top side only	—	0.200	—	0.215	—	0.215	ns
t _{DIB}	Output Data Invalid Before CLK Output		—	0.200	—	0.215	—	0.215	ns
f _{DATA}	DDR2 Serial Output Data Speed		—	664	—	554	—	554	Mbps
f _{DDR2}	DDR2 ECLK frequency		—	332	—	277	—	277	MHz
f _{SCLK}	SCLK Frequency		—	166	—	139	—	139	MHz
Generic DDRX2 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDR2_TX.ECLK.Centered ^{8, 9}									
t _{DVB}	Output Data Valid Before CLK Output	MachXO4 RoT devices, top side only	0.535	—	0.670	—	0.670	—	ns
t _{DVA}	Output Data Valid After CLK Output		0.535	—	0.670	—	0.670	—	ns
f _{DATA}	DDR2 Serial Output Data Speed		—	664	—	554	—	554	Mbps
f _{DDR2}	DDR2 ECLK Frequency (minimum limited by PLL)		—	332	—	277	—	277	MHz
f _{SCLK}	SCLK Frequency		—	166	—	139	—	139	MHz
Generic DDRX4 Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDR4_TX.ECLK.Aligned ^{8, 9}									
t _{DIA}	Output Data Invalid After CLK Output	MachXO4 RoT devices, top side only	—	0.200	—	0.215	—	0.215	ns
t _{DIB}	Output Data Invalid Before CLK Output		—	0.200	—	0.215	—	0.215	ns
f _{DATA}	DDR4 Serial Output Data Speed		—	800	—	630	—	630	Mbps
f _{DDR4}	DDR4 ECLK Frequency		—	400	—	315	—	315	MHz
f _{SCLK}	SCLK Frequency		—	100	—	79	—	79	MHz

Parameter	Description	Device	–6 (Commercial/ Industrial)		–5 (Commercial/ Industrial)		–5 (Automotive) Preliminary		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Generic DDRX4 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDR4_TX.ECLK.Centered ^{8,9}									
t _{DVB}	Output Data Valid Before CLK Output	MachXO4 RoT devices, top side only	0.455	—	0.570	—	0.570	—	ns
t _{DVA}	Output Data Valid After CLK Output		0.455	—	0.570	—	0.570	—	ns
f _{DATA}	DDR4 Serial Output Data Speed		—	800	—	630	—	630	Mbps
f _{DDR4}	DDR4 ECLK Frequency (minimum limited by PLL)		—	400	—	315	—	315	MHz
f _{SCLK}	SCLK Frequency		—	100	—	79	—	79	MHz
7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1 ^{8,9}									
t _{DIB}	Output Data Invalid Before CLK Output (See Figure 3.8)	MachXO4 RoT devices, top side only	—	0.160	—	0.180	—	0.180	ns
t _{DIA}	Output Data Invalid After CLK Output (See Figure 3.8)		—	0.160	—	0.180	—	0.180	ns
f _{DATA}	DDR71 Serial Output Data Speed		—	756	—	630	—	630	Mbps
f _{DDR71}	DDR71 ECLK Frequency		—	378	—	315	—	315	MHz
f _{CLKOUT}	7:1 Output Clock Frequency (SCLK) (minimum limited by PLL)		—	108	—	90	—	90	MHz

Parameter	Description	Device	–6 (Commercial/ Industrial)		–5 (Commercial/ Industrial)		–5 (Automotive) Preliminary		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
MIPI D-PHY Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDR4_TX.ECLK.Centered ^{10, 11, 12}									
t _{DVB}	Output Data Valid Before CLK Output	All MachXO4 RoT devices, top side only	0.200	—	0.200	—	0.200	—	UI
t _{DVA}	Output Data Valid After CLK Output		0.200	—	0.200	—	0.200	—	UI
f _{DATA}	MIPI D-PHY Output Data Speed		—	900	—	900	—	900	Mbps
F _{DDR4}	MIPI D-PHY ECLK Frequency (minimum limited by PLL)		—	450	—	450	—	450	MHz
f _{SCLK}	SCLK Frequency		—	112.5	—	112.5	—	112.5	MHz

Notes:

- Exact performance may vary with device and design implementation. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Lattice Radiant software.
- General I/O timing numbers based on LVCMOS 2.5, 8 mA, 0pf load, fast slew rate.
- Generic DDR timing numbers based on LVDS I/O (for input, output, and clock ports).
- 7:1 LVDS (GDDR71) uses the LVDS I/O standard (for input, output, and clock ports).
- For Generic DDRX1 mode $t_{SU} = t_{HO} = (t_{DVE} - t_{DVA} - 0.03 \text{ ns})/2$.
- The t_{SU}_DEL and t_H_DEL values use the SCLK_ZERHOLD default step size. Each step is 105 ps (–6), 113 ps (–5).
- This number for general purpose usage. Duty cycle tolerance is +/–10%.
- Duty cycle is +/– 5% for system usage.
- Performance is calculated with 0.225 UI.
- Performance is calculated with 0.20 UI.
- Performance for Industrial devices are only supported with VCC between 1.16 V to 1.24 V.
- Performance for Industrial devices and –5 devices are not modeled in the Lattice Radiant design tool.
- GDDR1 is not recommended to mix top banks with other banks in applications. Or, the related clock skew is increased significantly.
- The above timing numbers are generated using the Lattice Radiant design tool. Exact performance may vary with the device selected.
- Above 800 Mbps is only supported with WLCSP and csfBGA packages.
- Between 800 Mbps to 900 Mbps:
VIDTH exceeds the MIPI D-PHY Input DC Conditions (Table 3.16) and can be calculated with the equation t_{SU} or $t_H = -0.0005 \times \text{VIDTH} + 0.3284$
Example calculations
 - t_{SU} and t_{HO} = 0.28 with VIDTH = 100 mV
 - t_{SU} and t_{HO} = 0.25 with VIDTH = 170 mV
 - t_{SU} and t_{HO} = 0.20 with VIDTH = 270 mV

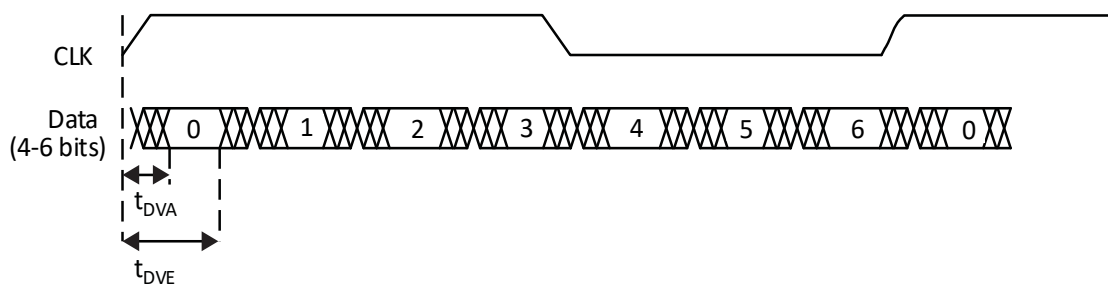


Figure 3.7. Receiver GDDR71_RX. Waveforms

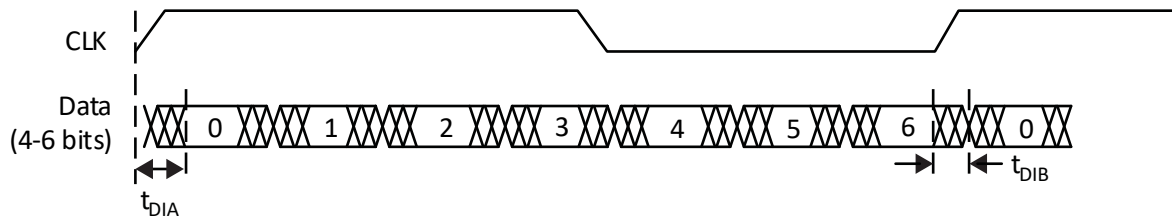


Figure 3.8. Transmitter GDDR71_TX. Waveforms

3.18. MachXO4 RoT External Switching Characteristics – ZC Devices

Over Recommended Operating Conditions

Table 3.23. MachXO4 RoT External Switching Characteristics – ZC Devices^{1, 2, 3, 4, 5, 6}

Parameter	Description	Device	–3 (Commercial/ Industrial)		–2 (Commercial/ Industrial)		–2 (Automotive) Preliminary		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Clocks									
Primary Clocks									
f _{MAX_PRI} ⁷	Frequency for Primary Clock Tree	All MachXO4 RoT devices	—	150	—	125	—	125	MHz
t _{W_PRI}	Clock Pulse Width for Primary Clock	All MachXO4 RoT devices	1.0	—	1.2	—	1.2	—	ns
t _{SKEW_PRI}	Primary Clock Skew Within a Device	LFMXO4D-040, LFMXO4D-050	—	1264.72	—	1309.17	—	1309.17	ps
		LFMXO4D-080, LFMXO4D-110	—	1673	—	1682	—	2718	ps
Edge Clock									
f _{MAX_EDGE} ⁷	Frequency for Edge Clock	MachXO4 RoT	—	210	—	175	—	175	MHz
Pin-LUT-Pin Propagation Delay									
t _{PD}	Best case propagation delay through one LUT-4	All MachXO4 RoT devices	—	6.70	—	7.00	—	7.00	ns
General I/O Pin Parameters (Using Primary Clock without PLL)									
t _{CO}	Clock to Output – PIO Output Register	LFMXO4D-040, LFMXO4D-050	—	9.969	—	10.415	—	10.467	ns
		LFMXO4D-080, LFMXO4D-110	—	11.22	—	11.76	—	12.57	ns
t _{SU}	Clock to Data Setup – PIO Input Register	LFMXO4D-040, LFMXO4D-050	–0.148	—	–0.148	—	–0.12	—	ns
		LFMXO4D-080, LFMXO4D-110	–0.33	—	–0.33	—	–0.33	—	ns
t _H	Clock to Data Hold – PIO Input Register	LFMXO4D-040, LFMXO4D-050	5.493	—	5.750	—	5.750	—	ns
		LFMXO4D-080, LFMXO4D-110	5.573	—	5.835	—	6.3	—	ns
t _{SU_DEL}	Clock to Data Setup – PIO Input Register with Data Input Delay	LFMXO4D-040, LFMXO4D-050	4.372	—	4.573	—	4.689	—	ns
		LFMXO4D-080, LFMXO4D-110	2.17	—	2.33	—	3.47	—	ns

Parameter	Description	Device	–3 (Commercial/ Industrial)		–2 (Commercial/ Industrial)		–2 (Automotive) Preliminary		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{H_DEL}	Clock to Data Hold – PIO	LFMXO4D-040, LFMXO4D-050	0.601	—	0.601	—	0.601	—	ns
	Input Register with Input Data Delay	LFMXO4D-080, LFMXO4D-110	–0.21	—	–0.21	—	–0.21	—	ns
f_{MAX_IO}	Clock Frequency of I/O and PFU Register	All MachXO4 RoT devices	—	150	—	125	—	125	MHz
General I/O Pin Parameters (Using Primary Clock with PLL)									
t_{COPLL}	Clock to Output – PIO	LFMXO4D-040, LFMXO4D-050	—	6.045	—	6.278	—	6.371	ns
	Output Register	LFMXO4D-080, LFMXO4D-110	—	8.02	—	8.14	—	8.14	ns
t_{SUPLL}	Clock to Data Setup – PIO	LFMXO4D-040, LFMXO4D-050	0.754	—	0.754	—	—	0.754	ns
	Input Register	LFMXO4D-080, LFMXO4D-110	0.83	—	0.83	—	0.89	—	ns
t_{HPLL}	Clock to Data Hold – PIO	LFMXO4D-040, LFMXO4D-050	1.203	—	1.203	—	1.203	—	ns
	Input Register	LFMXO4D-080, LFMXO4D-110	0.73	—	0.74	—	0.9	—	ns
t_{SU_DELPLL}	Clock to Data Setup – PIO	LFMXO4D-040, LFMXO4D-050	7.776	—	8.193	—	8.261	—	ns
	Input Register with Data Input Delay	LFMXO4D-080, LFMXO4D-110	5.15	—	5.71	—	7.39	—	ns
t_{H_DELPLL}	Clock to Data Hold – PIO	LFMXO4D-040, LFMXO4D-050	–0.52	—	–0.52	—	–0.52	—	ns
	Input Register with Input Data Delay	LFMXO4D-080, LFMXO4D-110	–1.41	—	–1.41	—	–1.41	—	ns
Generic DDRX1 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX1_RX.SCLK.Aligned^{8, 9, 10}									
t_{DVA}	Input Data Valid After CLK	All MachXO4 RoT devices, all sides	—	0.382	—	0.401	—	0.384	UI
t_{DVE}	Input Data Hold After CLK		0.670	—	0.684	—	0.684	—	UI
f_{DATA}	DDR1 Input Data Speed		—	140	—	116	—	116	Mbps
f_{DDR1}	DDR1 SCLK Frequency		—	70	—	58	—	58	MHz

Parameter	Description	Device	–3 (Commercial/ Industrial)		–2 (Commercial/ Industrial)		–2 (Automotive) Preliminary		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Generic DDRX1 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDR1_RX.SCLK.Centered ^{8, 9, 10}									
t _{SU}	Input Data Setup Before CLK	All MachXO4 RoT devices, all sides	1.319	—	1.412	—	1.412	—	ns
t _{HO}	Input Data Hold After CLK		0.717	—	1.010	—	1.010	—	ns
f _{DATA}	DDRX1 Input Data Speed		—	140	—	116	—	116	Mbps
f _{DDRX1}	DDRX1 SCLK Frequency		—	70	—	58	—	58	MHz
Generic DDRX2 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDR2_RX.ECLK.Aligned ^{8, 9}									
t _{DVA}	Input Data Valid After CLK	MachXO4 RoT devices, bottom side only	—	0.361	—	0.346	—	0.346	UI
t _{DVE}	Input Data Hold After CLK		0.602	—	0.625	—	0.625	—	UI
f _{DATA}	DDRX2 Serial Input Data Speed		—	280	—	234	—	234	Mbps
f _{DDRX2}	DDRX2 ECLK Frequency		—	140	—	117	—	117	MHz
f _{SCLK}	SCLK Frequency		—	70	—	59	—	59	MHz
Generic DDRX2 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDR2_RX.ECLK.Centered ^{8, 9}									
t _{SU}	Input Data Setup Before CLK	MachXO4 RoT devices, bottom side only	0.472	—	0.672	—	0.672	—	ns
t _{HO}	Input Data Hold After CLK		0.363	—	0.501	—	0.501	—	ns
f _{DATA}	DDRX2 Serial Input Data Speed		—	280	—	234	—	234	Mbps
f _{DDRX2}	DDRX2 ECLK Frequency		—	140	—	117	—	117	MHz
f _{SCLK}	SCLK Frequency		—	70	—	59	—	59	MHz

Parameter	Description	Device	–3 (Commercial/ Industrial)		–2 (Commercial/ Industrial)		–2 (Automotive) Preliminary		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Generic DDR4 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDR4_RX.ECLK.Aligned ⁸									
t _{DVA}	Input Data Valid After ECLK	MachXO4 RoT devices, bottom side only	—	0.293	—	0.316	—	0.316	UI
t _{DVE}	Input Data Hold After ECLK		0.662	—	0.650	—	0.650	—	UI
f _{DATA}	DDR4 Serial Input Data Speed		—	420	—	352	—	352	Mbps
f _{DDR4}	DDR4 ECLK Frequency		—	210	—	176	—	176	MHz
f _{SCLK}	SCLK Frequency		—	53	—	44	—	44	MHz
Generic DDR4 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDR4_RX.ECLK.Centered ⁸									
t _{SU}	Input Data Setup Before ECLK	MachXO4 RoT devices, bottom side only	0.434	—	0.535	—	0.616	—	ns
t _{HO}	Input Data Hold After ECLK		0.385	—	0.395	—	0.395	—	ns
f _{DATA}	DDR4 Serial Input Data Speed		—	420	—	352	—	352	Mbps
f _{DDR4}	DDR4 ECLK Frequency		—	210	—	176	—	176	MHz
f _{SCLK}	SCLK Frequency		—	53	—	44	—	44	MHz
7:1 LVDS Inputs (GDDR71_RX.ECLK.7:1) ⁹									
t _{DVA}	Input Data Valid After ECLK	MachXO4 RoT devices, bottom side only	—	0.307	—	0.316	—	0.282	UI
t _{DVE}	Input Data Hold After ECLK		0.740	—	0.702	—	0.702	—	UI
f _{DATA}	DDR71 Serial Input Data Speed		—	420	—	352	—	352	Mbps
f _{DDR71}	DDR71 ECLK Frequency		—	210	—	176	—	176	MHz
f _{CLKIN}	7:1 Input Clock Frequency (SCLK) (minimum limited by PLL)		—	60	—	50	—	50	MHz

Parameter	Description	Device	–3 (Commercial/ Industrial)		–2 (Commercial/ Industrial)		–2 (Automotive) Preliminary		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Generic DDR Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDR1_TX.SCLK.Aligned ^{8, 10}									
t _{DIA}	Output Data Invalid After CLK Output	All MachXO4 RoT devices, all sides	—	0.850	—	0.910	—	0.910	ns
t _{DIB}	Output Data Invalid Before CLK Output		—	0.850	—	0.910	—	0.910	ns
f _{DATA}	DDR1 Output Data Speed		—	140	—	117	—	117	Mbps
f _{DDR1}	DDR1 SCLK frequency		—	70	—	58	—	58	MHz
Generic DDR Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDR1_TX.SCLK.Centered ^{8, 10}									
t _{DVB}	Output Data Valid Before CLK Output	All MachXO4 RoT devices, all sides	2.720	—	3.380	—	3.380	—	ns
t _{DVA}	Output Data Valid After CLK Output		2.720	—	3.380	—	3.380	—	ns
f _{DATA}	DDR1 Output Data Speed		—	140	—	117	—	117	Mbps
f _{DDR1}	DDR1 SCLK Frequency (minimum limited by PLL)		—	70	—	58	—	58	MHz
Generic DDR2 Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDR2_TX.ECLK.Aligned ⁸									
t _{DIA}	Output Data Invalid After CLK Output	MachXO4 RoT devices, top side only	—	0.270	—	0.300	—	0.300	ns
t _{DIB}	Output Data Invalid Before CLK Output		—	0.270	—	0.300	—	0.300	ns
f _{DATA}	DDR2 Serial Output Data Speed		—	280	—	224	—	224	Mbps
f _{DDR2}	DDR2 ECLK frequency		—	140	—	112	—	112	MHz
f _{SCLK}	SCLK Frequency		—	70	—	56	—	56	MHz

Parameter	Description	Device	–3 (Commercial/ Industrial)		–2 (Commercial/ Industrial)		–2 (Automotive) Preliminary		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Generic DDRX2 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX2_TX.ECLK.Centered ^{8, 9}									
t _{DVB}	Output Data Valid Before CLK Output	MachXO4 RoT devices, top side only	1.445	—	1.760	—	1.760	—	ns
t _{DVA}	Output Data Valid After CLK Output		1.445	—	1.760	—	1.760	—	ns
f _{DATA}	DDRX2 Serial Output Data Speed		—	280	—	224	—	224	Mbps
f _{DDRX2}	DDRX2 ECLK Frequency (minimum limited by PLL)		—	140	—	112	—	112	MHz
f _{SCLK}	SCLK Frequency		—	70	—	56	—	56	MHz
Generic DDRX4 Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX4_TX.ECLK.Aligned ^{8, 9}									
t _{DIA}	Output Data Invalid After CLK Output	MachXO4 RoT devices, top side only	—	0.270	—	0.300	—	0.300	ns
t _{DIB}	Output Data Invalid Before CLK Output		—	0.270	—	0.300	—	0.300	ns
f _{DATA}	DDRX4 Serial Output Data Speed		—	420	—	350	—	350	Mbps
f _{DDRX4}	DDRX4 ECLK Frequency		—	210	—	175	—	175	MHz
f _{SCLK}	SCLK Frequency		—	53	—	44	—	44	MHz
Generic DDRX4 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX4_TX.ECLK.Centered ^{8, 9}									
t _{DVB}	Output Data Valid Before CLK Output	MachXO4 RoT devices, top side only	0.873	—	1.067	—	1.067	—	ns
t _{DVA}	Output Data Valid After CLK Output		0.873	—	1.067	—	1.067	—	ns
f _{DATA}	DDRX4 Serial Output Data Speed		—	420	—	350	—	350	Mbps
f _{DDRX4}	DDRX4 ECLK Frequency (minimum limited by PLL)		—	210	—	175	—	175	MHz
f _{SCLK}	SCLK Frequency		—	53	—	44	—	44	MHz

Parameter	Description	Device	–3 (Commercial/ Industrial)		–2 (Commercial/ Industrial)		–2 (Automotive) Preliminary		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1 ^{8,9}									
t _{DIB}	Output Data Invalid Before CLK Output	MachXO4 RoT devices, top side only	—	0.240	—	0.270	—	0.270	ns
t _{DIA}	Output Data Invalid After CLK Output		—	0.240	—	0.270	—	0.270	ns
f _{DATA}	DDR71 Serial Output Data Speed		—	420	—	350	—	350	Mbps
f _{DDR71}	DDR71 ECLK Frequency		—	210	—	175	—	175	MHz
f _{CLKOUT}	7:1 Output Clock Frequency (SCLK) (minimum limited by PLL)		—	60	—	50	—	50	MHz

Notes:

- Exact performance may vary with device and design implementation. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Lattice Radiant software.
- General I/O timing numbers based on LVCMOS 2.5, 8 mA, 0pf load, fast slew rate.
- Generic DDR timing numbers based on LVDS I/O (for input, output, and clock ports).
- 7:1 LVDS (GDDR71) uses the LVDS I/O standard (for input, output, and clock ports).
- For Generic DDRX1 mode $t_{SU} = t_{HO} = (t_{DVE} - t_{DVA} - 0.03 \text{ ns})/2$.
- The t_{SU}_DEL and t_H_DEL values use the SCLK_ZERHOLD default step size.
- This number for general purpose usage. Duty cycle tolerance is +/–10%.
- Duty cycle is +/– 5% for system usage.
- Performance is calculated with 0.225 UI.
- GDDR71 is not recommended to mix top banks with other banks in applications. Or, the related clock skew is increased significantly.

3.19. sysCLOCK PLL Timing

Over Recommended Operating Conditions.

Table 3.24. sysCLOCK PLL Timing

Parameter	Description	Condition	Commercial/ Industrial		Automotive		Unit
			Min.	Max.	Min.	Max.	
f_{IN}	Input Clock Frequency (CLKI, CLKFB)	—	7	400	7	400	MHz
f_{OUT}	Output Clock Frequency (CLKOP, CLKOS, CLKOS2)	—	1.5625	400	1.5625	400	MHz
f_{OUT2}	Output Frequency (CLKOS3 cascaded from CLKOS2)	—	0.0122	400	0.0122	400	MHz
f_{VCO}^9	PLL VCO Frequency	—	200	800	200	800	MHz
f_{PFD}	Phase Detector Input Frequency	—	7	400	7	400	MHz
AC Characteristics							
t_{DT}	Output Clock Duty Cycle	Without duty trim selected ³	40	60	40	60	%
$t_{DT_TRIM}^7$	Edge Duty Trim Accuracy	—	–75	75	N/A	N/A	%
t_{PH}^4	Output Phase Accuracy	—	–6	6	–6	6	%
$t_{OPJIT}^{1,8}$	Output Clock Period Jitter for LFMXO4D-040, LFMXO4D-050	$f_{OUT} > 100$ MHz	—	352	—	367	ps p-p
		$f_{OUT} < 100$ MHz	—	0.032	—	0.034	UIPP
	Output Clock Cycle-to-cycle Jitter for LFMXO4D-040, LFMXO4D-050	$f_{OUT} > 100$ MHz	—	649	—	666	ps p-p
		$f_{OUT} < 100$ MHz	—	0.05	—	0.053	UIPP
	Output Clock Phase Jitter for LFMXO4D-040, LFMXO4D-050	$f_{PFD} > 100$ MHz	—	218	—	218	ps p-p
		$f_{PFD} < 100$ MHz	—	0.016	—	0.017	UIPP
	Output Clock Period Jitter (Fractional-N) for LFMXO4D-040, LFMXO4D-050	$f_{OUT} > 100$ MHz	—	660	—	740	ps p-p
		$f_{OUT} < 100$ MHz	—	0.38	—	0.38	UIPP
	Output Clock Cycle-to-cycle Jitter (Fractional-N) for LFMXO4D-040, LFMXO4D-050	$f_{OUT} > 100$ MHz	—	875	—	955	ps p-p
		$f_{OUT} < 100$ MHz	—	0.44	—	0.44	UIPP
	Output Clock Period Jitter for LFMXO4D-080, LFMXO4D-110	$f_{OUT} > 100$ MHz	—	210	—	210	ps p-p
		$f_{OUT} < 100$ MHz	—	0.014	—	0.0142	UIPP
	Output Clock Cycle-to-cycle Jitter for LFMXO4D-080, LFMXO4D-110	$f_{OUT} > 100$ MHz	—	390	—	390	ps p-p
		$f_{OUT} < 100$ MHz	—	0.025	—	0.026	UIPP
	Output Clock Phase Jitter for LFMXO4D-080, LFMXO4D-110	$f_{PFD} > 100$ MHz	—	160	—	160	ps p-p
		$f_{PFD} < 100$ MHz	—	0.011	—	0.011	UIPP
	Output Clock Period Jitter (Fractional-N) for LFMXO4D-080, LFMXO4D-110	$f_{OUT} > 100$ MHz	—	320	—	320	ps p-p
		$f_{OUT} < 100$ MHz	—	0.38	—	0.38	UIPP
	Output Clock Cycle-to-cycle Jitter (Fractional-N) for LFMXO4D-080, LFMXO4D-110	$f_{OUT} > 100$ MHz	—	365	—	388	ps p-p
		$f_{OUT} < 100$ MHz	—	0.44	—	0.44	UIPP
t_W	Output Clock Pulse Width	At 90% or 10% ³	0.9	—	0.9	—	ns
$t_{LOCK}^{2,5}$	PLL Lock-in Time	—	—	15	—	15	ms
t_{UNLOCK}	PLL Unlock Time	—	—	50	—	50	ns
t_{IPJIT}^6	Input Clock Period Jitter	$f_{PFD} \geq 20$ MHz	—	1,000	—	1,000	ps p-p
		$f_{PFD} < 20$ MHz	—	0.02	—	0.02	UIPP
t_{HI}	Input Clock High Time	90% to 90%	0.75	—	0.75	—	ns
t_{LO}	Input Clock Low Time	10% to 10%	0.7	—	0.7	—	ns
t_{STABLE}^5	STANDBY High to PLL Stable	—	—	15	—	15	ms

Parameter	Description	Condition	Commercial/ Industrial		Automotive		Unit
			Min.	Max.	Min.	Max.	
t_{RST}	RST/RESETM Pulse Width	—	1	—	1	—	ns
t_{RST_DIV}	RESETC/D Pulse Width	—	10	—	10	—	ns
t_{ROTATE_SETUP}	PHASESTEP Setup Time	—	10	—	10	—	ns
t_{ROTATE_WD}	PHASESTEP Pulse Width	—	4	—	4	—	VCO Cycles

Notes:

1. Period jitter sample is taken over 10,000 samples of the primary PLL output with a clean reference clock. Cycle-to-cycle jitter is taken over 1000 cycles. Phase jitter is taken over 2000 cycles. All values per JESD65B.
2. Output clock is valid after tLOCK for PLL reset and dynamic delay adjustment.
3. Using LVDS output buffers.
4. CLKOS as compared to CLKOP output for one phase step at the maximum VCO frequency. See [MachXO4 sysCLOCK PLL Design and Usage Guide \(FPGA-TN-02391\)](#) for more details.
5. At minimum fPPD. As the fPPD increases, the time decreases to approximately 60% the value listed.
6. Maximum allowed jitter on an input clock. PLL unlock may occur if the input jitter exceeds this specification. Jitter on the input clock may be transferred to the output clocks, resulting in jitter measurements outside the output specifications listed in this table.
7. Edge Duty Trim Accuracy is a percentage of the setting value. For Commercial/Industrial devices, valid trim settings are 0 ps, 140 ps and 280 ps or Delay Multipliers of "0", "2" and "4", respectively.
8. Jitter values measured with the internal oscillator operating. The jitter values increase with loading of the FPGA fabric and in the presence of SSO noise.
9. Optimal VCO range for best operation of the PLL. PLL can work outside the range, but the clock output could have increased jitter.

3.20. Oscillator

Table 3.25. Oscillator

Symbol	Parameter		Commercial/Industrial Grade Devices (–40 °C to 100 °C)			Automotive Grade Devices (–40 °C to 125 °C)			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{MAX}	Oscillator Output Frequency		124.355	133	141.645	122.360	133	143.640	MHz
t_{DT}	Output Clock Duty Cycle		43	50	57	42	50	58	%
t_{OPJIT}	Output Clock Period Jitter	XO4D-080, XO4D-110	—	—	0.031	—	—	0.034	UIPP
		XO4D-040, XO4D-050	—	—	0.38	—	—	0.04	UIPP
$t_{STABLEOSC}$	STDBY Low to Oscillator Stable		—	—	0.1	—	—	0.1	us

3.21. Flash Download Time

Table 3.26. Flash Download Time

Symbol	Parameter	Device	Typ.	Unit
$t_{REFRESH}$	POR to Device I/O Active	LFMXO4D-040, LFMXO4D-050	—	ms
		LFMXO4D-080, LFMXO4D-110	5.2	ms

Notes:

- Assumes sysMEM EBR initialized to an all zero pattern if they are used.
- The NVCM/Flash download time is measured starting from the maximum voltage of POR trip point.
- The worst case can be up to 1.75 times the Typ value.

3.22. JTAG Port Timing Specifications

Table 3.27. JTAG Port Timing Specifications

Symbol	Parameter	Min.	Max.	Unit
f_{MAX}	TCK clock frequency	—	25	MHz
t_{BTCPH}	TCK [BSCAN] clock pulse width high	20	—	ns
t_{BTCPL}	TCK [BSCAN] clock pulse width low	20	—	ns
t_{BTS}	TCK [BSCAN] setup time	10	—	ns
t_{BTH}	TCK [BSCAN] hold time	10	—	ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
$t_{BTCODIS}$	TAP controller falling edge of clock to valid disable	—	12	ns
t_{BTCOEN}	TAP controller falling edge of clock to valid enable	—	12	ns
t_{BTCRS}	BSCAN test capture register setup time	8	—	ns
t_{BTCRH}	BSCAN test capture register hold time	20	—	ns
t_{BUTCO}	BSCAN test update register, falling edge of clock to valid output	—	25	ns
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to valid disable	—	27	ns
$t_{BTUPOEN}$	BSCAN test update register, falling edge of clock to valid enable	—	25	ns

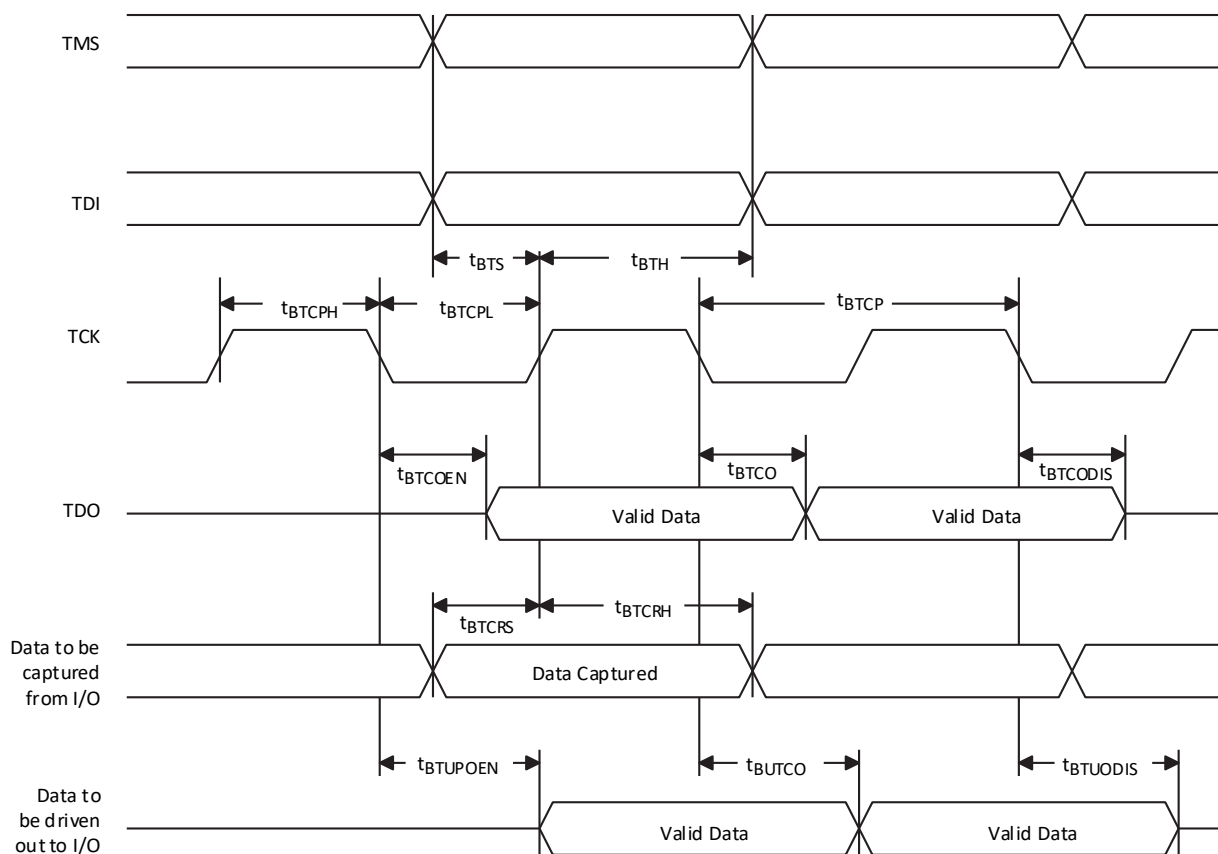


Figure 3.9. JTAG Port Timing Waveforms

3.23. sysCONFIG Port Timing Specifications

Table 3.28. sysCONFIG Port Timing Specifications

Symbol	Parameter	Min.	Max.	Unit
All Configuration Mode				
t_{PRGM}	PROGRAMN low pulse accept	109	—	ns
t_{PRGMJ}	PROGRAMN low pulse rejection	—	60	ns
t_{INITL}	INITN low time	LFMXO4D-040, LFMXO4D-050	130	us
		LFMXO4D-080, LFMXO4D-110	175	us
$t_{DPPINIT}$	PROGRAMN low to INITN low	—	150	ns
$t_{DPPDONE}$	PROGRAMN low to DONE low	—	165	ns
t_{IODISS}	PROGRAMN low to I/O disable	—	196	ns
Slave SPI				
f_{MAX}	CCLK clock frequency	—	66	MHz
t_{CCLKH}	CCLK clock pulse width high	7.5	—	ns
t_{CCLKL}	CCLK clock pulse width low	7.5	—	ns
t_{STSU}	CCLK setup time	2	—	ns
t_{STH}	CCLK hold time	0	—	ns
t_{STCO}	CCLK falling edge to valid output	—	14	ns
t_{STOZ}	CCLK falling edge to valid disable	—	12	ns
t_{STOV}	CCLK falling edge to valid enable	—	14	ns
t_{SCS}	Chip select high time	25	—	ns
t_{SCSS}	Chip select setup time	3	—	ns
t_{SCSH}	Chip select hold time	3	—	ns
Master SPI				
f_{MAX}	MCLK clock frequency	—	66	MHz
t_{MCLKH}	MCLK clock pulse width high	7.5	—	ns
t_{MCLKL}	MCLK clock pulse width low	7.5	—	ns
t_{STSU}	MCLK setup time	6	—	ns
t_{STH}	MCLK hold time	Commercial/Industrial	2	ns
		Automotive	3	ns
t_{CSSPI}	INITN high to chip select low	100	200	ns
t_{MCLK}	INITN high to first MCLK edge	0.75	1	us

3.24. I2C Port Timing Specifications

Table 3.29. I2C Port Timing Specification^{1, 2}

Symbol	Parameter	Min.	Max.	Unit
f_{MAX}	Maximum SCL clock frequency	—	400	kHz

Notes:

- MachXO4 RoT device supports the following modes:
 - Standard-mode (Sm), with a bit rate up to 100 kb/s (user and configuration mode)
 - Fast-mode (Fm), with a bit rate up to 400 kb/s (user and configuration mode)
- Refer to the I2C specification for timing requirements.

3.25. SPI Port Timing Specifications

Table 3.30. SPI Port Timing Specifications

Symbol	Parameter	Min.	Max.	Unit
f_{MAX}	Maximum SCK clock frequency	—	45	MHz

Note: Applies to user mode only. For configuration mode timing specifications, refer to [sysCONFIG Port Timing Specifications](#) table in this data sheet.

3.26. Switching Test Conditions

Figure 3.10 shows the output test load used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3.31.

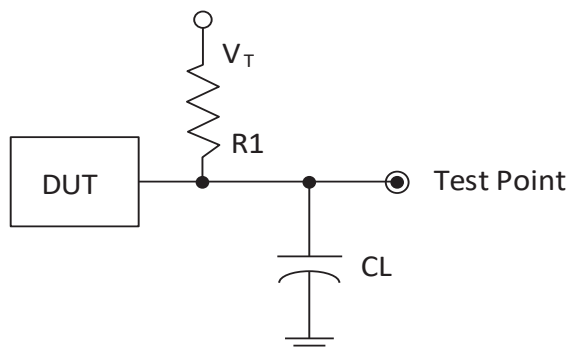


Figure 3.10. Output Test Load, LVTTTL and LVCMOS Standards

Table 3.31. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R1	CL	Timing Ref.	VT
LVTTTL and LVCMOS settings (L -> H, H -> L)	∞	0 pF	LVTTTL, LVCMOS 3.3 = 1.5 V	—
			LVCMOS 2.5 = $V_{CCIO}/2$	—
			LVCMOS 1.8 = $V_{CCIO}/2$	—
			LVCMOS 1.5 = $V_{CCIO}/2$	—
			LVCMOS 1.2 = $V_{CCIO}/2$	—
LVTTTL and LVCMOS 3.3 (Z -> H)	188	0 pF	1.5	VOL
LVTTTL and LVCMOS 3.3 (Z -> L)			1.5	VOH
Other LVCMOS (Z -> H)			$V_{CCIO}/2$	VOL
Other LVCMOS (Z -> L)			$V_{CCIO}/2$	VOH
LVTTTL + LVCMOS (H -> Z)			$V_{OH} - 0.15$	VOL
LVTTTL + LVCMOS (L -> Z)			$V_{OL} - 0.15$	VOH

Note: Output test conditions for all other interfaces are determined by the respective standards.

4. Signal Descriptions

Table 4.1. Signal Descriptions

Signal Name	I/O	Description
General Purpose		
P[Edge] [Row/Column Number]_[A/B/C/D]	I/O	[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top). [Row/Column Number] indicates the PFU row or the column of the device on which the PIO Group exists. When Edge is T (Top) or (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number. [A/B/C/D] indicates the PIO within the group to which the pad is connected. Some of these user-programmable pins are shared with special function pins. When not used as special function pins, these pins can be programmed as I/O for user logic. During configuration of the user-programmable I/O, you have an option to tri-state the I/O and enable an internal pull-up, pull-down or buskeeper resistor. This option also applies to unused pins (or those not bonded to a package pin). The default during configuration is for user-programmable I/O to be tri-stated with an internal pull-down resistor enabled. When the device is erased, I/O is tri-stated with an internal pull-down resistor enabled. Some pins, such as PROGRAMN and JTAG pins, default to tri-stated I/O with pull-up resistors enabled when the device is erased.
NC	—	No connect.
GND	—	GND – Ground. Dedicated pins. It is recommended that all GNDs are tied together.
V _{CC}	—	V _{CC} – The power supply pins for core logic. Dedicated pins. It is recommended that all V _{CC} s are tied to the same supply.
V _{CCIOX}	—	V _{CCIO} – The power supply pins for I/O Bank x. Dedicated pins. It is recommended that all V _{CCIO} s located in the same bank are tied to the same supply.
PLL and Clock Function (Used as user-programmable I/O pins when not used for PLL or clock pins)		
[LOC]_GPLL[T, C]_IN	—	Reference Clock (PLL) input pads: [LOC] indicates location. Valid designations are L (Left PLL) and R (Right PLL). T = true and C = complement.
[LOC]_GPLL[T, C]_FB	—	Optional Feedback (PLL) input pads: [LOC] indicates location. Valid designations are L (Left PLL) and R (Right PLL). T = true and C = complement.
PCLK [n]_[2:0]	—	Primary Clock pads. One to three clock pads per side.
Test and Programming (Dual-function pins used for test access port and during sysCONFIG™)		
TMS	I	Test Mode Select input pin, used to control the 1149.1 state machine.
TCK	I	Test Clock input pin, used to clock the 1149.1 state machine.
TDI	I	Test Data input pin, used to load data into the device using an 1149.1 state machine.
TDO	O	Output pin – Test Data output pin used to shift data out of the device using 1149.1.
JTAGENB	I	Optionally controls behavior of TDI, TDO, TMS, TCK. If the device is configured to use the JTAG pins (TDI, TDO, TMS, TCK) as general purpose I/O, then: If JTAGENB is low: TDI, TDO, TMS and TCK can function a general purpose I/O. If JTAGENB is high: TDI, TDO, TMS and TCK function as JTAG pins.
Configuration (Dual-function pins used during sysCONFIG)		
PROGRAMN	I	Initiates configuration sequence when asserted low. This pin always has an active pull-up.
INITN	I/O	Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled.
DONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the start-up sequence is in progress.
MCLK/CCLK	I/O	Input Configuration Clock for configuring an FPGA in Slave SPI mode. Output Configuration Clock for configuring an FPGA in SPI and SPIIm configuration modes.
SN	I	Slave SPI active low chip select input.
CSSPIN	I/O	Master SPI active low chip select output.
SI/SPISI	I/O	Slave SPI serial data input and master SPI serial data output.
SO/SPISO	I/O	Slave SPI serial data output and master SPI serial data input.

Signal Name	I/O	Description
SCL	I/O	Slave I2C clock input and master I2C clock output.
SDA	I/O	Slave I2C data input and master I2C data output.

4.1. Pin Information Summary

Table 4.2. LFMXO4D-040 Pin Summary

	LFMXO4D-040			
	BSG132	TSG144	BFG256	BBG256/BTG256
General Purpose I/O per Bank				
Bank 0	24	26	49	49
Bank 1	26	29	52	52
Bank 2	28	29	52	52
Bank 3	7	9	16	16
Bank 4	8	10	16	16
Bank 5	10	10	20	20
Total General Purpose Single-Ended I/O	103	113	205	205
Minimum Reserved for Configuration*	1	1	1	1
Maximum Programmable Single-Ended I/O	102	112	204	204
Differential I/O per Bank				
Bank 0	11	12	23	23
Bank 1	13	14	26	26
Bank 2	14	14	26	26
Bank 3	3	4	8	8
Bank 4	4	5	8	8
Bank 5	5	5	10	10
Total General Purpose Differential I/O	50	54	101	101
Dual-Function I/O	37	37	37	37
Number 7:1 or 8:1 Gearboxes				
Number of 7:1 or 8:1 Output Gearboxes Available (Bank 0)	6	7	16	16
Number of 7:1 or 8:1 Input Gearboxes Available (Bank 2)	14	14	18	18
High-speed Differential Outputs				
Bank 0	6	7	16	16
VCCIO Pins				
Bank 0	4	4	5	5
Bank 1	3	3	4	4
Bank 2	3	3	4	4
Bank 3	1	1	1	1
Bank 4	1	1	2	2
Bank 5	1	1	1	1
VCC	4	4	8	8
GND	11	13	25	25
NC	1	1	1	1

	LFMXO4D-040			
	BSG132	TSG144	BFG256	BBG256/BTG256
Total Count of Bonded Pins	132	144	256	256

***Note:** One pin for JTAGENB or four pins for JTAG.

Table 4.3. LFMXO4D-050 Pin Summary

	LFMXO4D-050			
	BSG132	TSG144	BFG256	BBG256/BTG256
General Purpose I/O per Bank				
Bank 0	24	26	49	49
Bank 1	26	29	52	52
Bank 2	28	29	52	52
Bank 3	7	9	16	16
Bank 4	8	10	16	16
Bank 5	10	10	20	20
Total General Purpose Single-Ended I/O	103	113	205	205
Minimum Reserved for Configuration*	1	1	1	1
Maximum Programmable Single-Ended I/O	102	112	204	204
Differential I/O per Bank				
Bank 0	11	12	23	23
Bank 1	13	14	26	26
Bank 2	14	14	26	26
Bank 3	3	4	8	8
Bank 4	4	5	8	8
Bank 5	5	5	10	10
Total General Purpose Differential I/O	50	54	101	101
Dual-Function I/O	37	37	37	37
Number 7:1 or 8:1 Gearboxes				
Number of 7:1 or 8:1 Output Gearboxes Available (Bank 0)	6	7	16	16
Number of 7:1 or 8:1 Input Gearboxes Available (Bank 2)	14	14	18	18
High-speed Differential Outputs				
Bank 0	6	7	16	16
VCCIO Pins				
Bank 0	4	4	5	5
Bank 1	3	3	4	4
Bank 2	3	3	4	4
Bank 3	1	1	1	1
Bank 4	1	1	2	2
Bank 5	1	1	1	1
VCC	4	4	8	8
GND	11	13	25	25
NC	1	1	1	1
Total Count of Bonded Pins	132	144	256	256

***Note:** One pin for JTAGENB or four pins for JTAG.

Table 4.4. LFMXO4D-080 Pin Summary

	LFMXO4D-080		
	UTG69	BBG256/BTG256	BBG400/BTG400
General Purpose I/O per Bank			
Bank 0	19	49	82
Bank 1	13	52	84
Bank 2	17	52	84
Bank 3	9	16	28
Bank 4	—	16	24
Bank 5	—	20	32
Total General Purpose Single Ended I/O	58	205	334
Minimum Reserved for Configuration*	1	1	1
Maximum Programmable Single Ended I/O	57	204	333
Differential I/O per Bank			
Bank 0	9	23	40
Bank 1	5	26	42
Bank 2	8	26	42
Bank 3	4	8	14
Bank 4	—	8	12
Bank 5	—	10	16
Total General Purpose Differential I/O	26	101	166
Dual-Function I/O	31	37	37
Number 7:1 or 8:1 Gearboxes			
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	4	18	20
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	8	20	22
High-speed Differential Outputs			
Bank 0	4	18	20
VCCIO Pins			
Bank 0	2	5	6
Bank 1	1	4	5
Bank 2	1	4	5
Bank 3	1	1	2
Bank 4	—	2	2
Bank 5	—	1	2
VCC	2	8	10
GND	4	25	34
NC	—	1	—
Total Count of Bonded Pins	69	256	400

*Note: One pin for JTAGENB or four pins for JTAG.

Table 4.5. LFMXO4D-110 Pin Summary

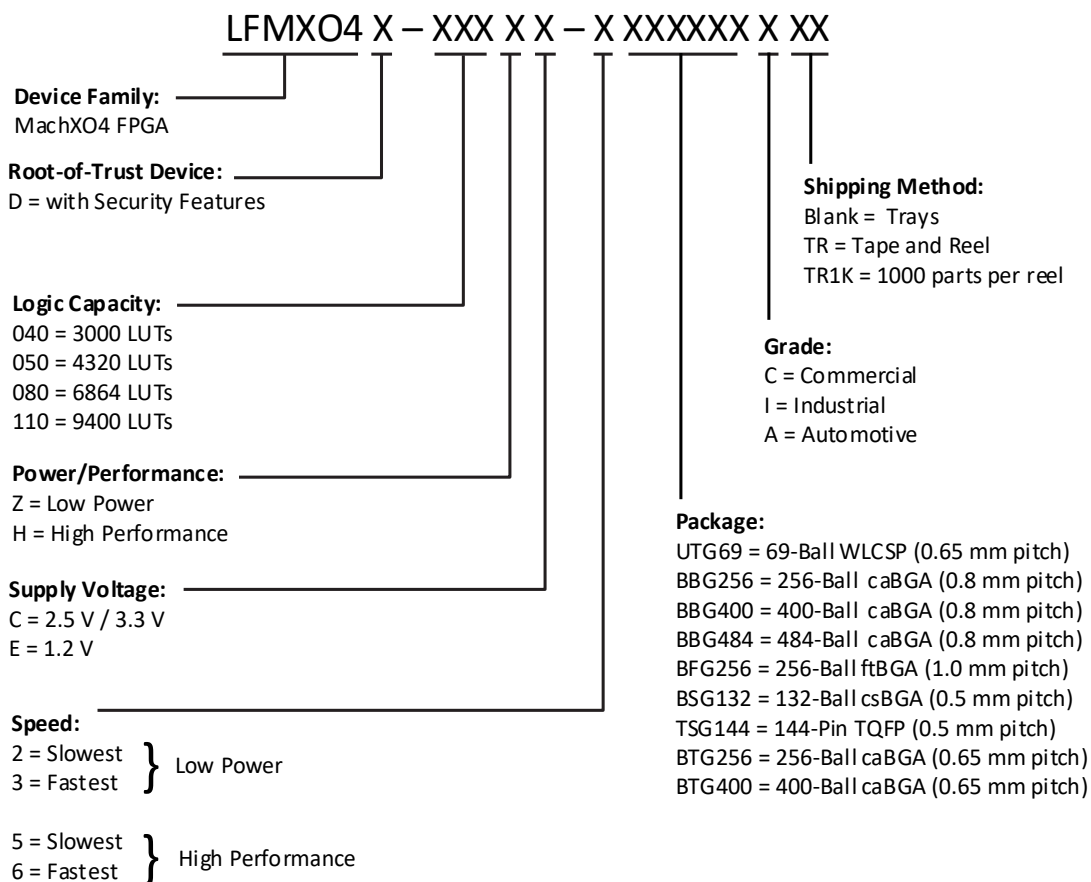
	LFMXO4D-110			
	UTG69	BBG256/BTG256	BBG400/BTG400	BBG484
General Purpose I/O per Bank				
Bank 0	19	49	82	94
Bank 1	13	52	84	96
Bank 2	17	52	84	96
Bank 3	9	16	28	36

	LFMXO4D-110			
	UTG69	BBG256/BTG256	BBG400/BTG400	BBG484
Bank 4	—	16	24	24
Bank 5	—	20	32	36
Total General Purpose Single Ended I/O	58	205	334	382
Minimum Reserved for Configuration*	1	1	1	1
Maximum Programmable Single Ended I/O	57	204	333	381
Differential I/O per Bank				
Bank 0	9	23	40	46
Bank 1	5	26	42	48
Bank 2	8	26	42	48
Bank 3	4	8	14	18
Bank 4	—	8	12	12
Bank 5	—	10	16	18
Total General Purpose Differential I/O	26	101	166	190
Dual-Function I/O	31	37	37	43
Number 7:1 or 8:1 Gearboxes				
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	4	18	20	22
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	8	20	22	24
High-speed Differential Outputs				
Bank 0	4	18	20	22
VCCIO Pins				
Bank 0	2	5	6	10
Bank 1	1	4	5	9
Bank 2	1	4	5	9
Bank 3	1	1	2	3
Bank 4	—	2	2	3
Bank 5	—	1	2	3
VCC	2	8	10	12
GND	4	25	34	53
NC	—	1	—	—
Total Count of Bonded Pins	69	256	400	484

*Note: One pin for JTAGENB or four pins for JTAG.

5. Ordering Information

5.1. LFMXO4D Part Number Description

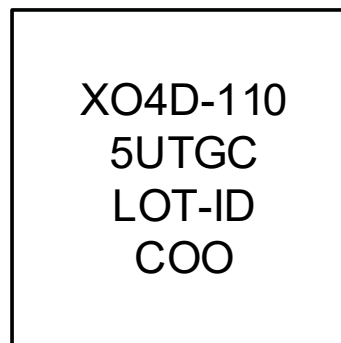


5.2. Ordering Information

- Except for WLCSP packages, all MachXO4 RoT devices have top-side marking as shown below.



- For all MachXO4 RoT devices in WLCSP packages, the markings are abbreviated and adhered to the sample format shown below.



5.3. LFMXO4D Low Power Commercial Grade Devices Packaging

Part Number	LUTs	Supply Voltage	Speed	Package	Pins	Temp. Grade
LFMXO4D-040ZC-2BBG256C	3000	2.5 V/3.3 V	2	BBG256	256	Commercial
LFMXO4D-040ZC-3BBG256C	3000	2.5 V/3.3 V	3	BBG256	256	Commercial
LFMXO4D-040ZC-2BFG256C	3000	2.5 V/3.3 V	2	BFG256	256	Commercial
LFMXO4D-040ZC-3BFG256C	3000	2.5 V/3.3 V	3	BFG256	256	Commercial

Part Number	LUTs	Supply Voltage	Speed	Package	Pins	Temp. Grade
LFMXO4D-050ZC-2BBG256C	4320	2.5 V/3.3 V	2	BBG256	256	Commercial
LFMXO4D-050ZC-3BBG256C	4320	2.5 V/3.3 V	3	BBG256	256	Commercial
LFMXO4D-050ZC-2BFG256C	4320	2.5 V/3.3 V	2	BFG256	256	Commercial
LFMXO4D-050ZC-3BFG256C	4320	2.5 V/3.3 V	3	BFG256	256	Commercial

Part Number	LUTs	Supply Voltage	Speed	Package	Pins	Temp. Grade
LFMXO4D-080ZC-2BBG256C	6864	2.5 V/3.3 V	2	BBG256	256	Commercial
LFMXO4D-080ZC-3BBG256C	6864	2.5 V/3.3 V	3	BBG256	256	Commercial
LFMXO4D-080ZC-2BBG400C	6864	2.5 V/3.3 V	2	BBG400	400	Commercial
LFMXO4D-080ZC-3BBG400C	6864	2.5 V/3.3 V	3	BBG400	400	Commercial

Part Number	LUTs	Supply Voltage	Speed	Package	Pins	Temp. Grade
LFMXO4D-110ZC-2BBG256C	9400	2.5 V/3.3 V	2	BBG256	256	Commercial
LFMXO4D-110ZC-3BBG256C	9400	2.5 V/3.3 V	3	BBG256	256	Commercial
LFMXO4D-110ZC-2BBG400C	9400	2.5 V/3.3 V	2	BBG400	400	Commercial
LFMXO4D-110ZC-3BBG400C	9400	2.5 V/3.3 V	3	BBG400	400	Commercial
LFMXO4D-110ZC-2BBG484C	9400	2.5 V/3.3 V	2	BBG484	484	Commercial
LFMXO4D-110ZC-3BBG484C	9400	2.5 V/3.3 V	3	BBG484	484	Commercial

5.4. LFMXO4D High Performance Commercial Grade Devices Packaging

Part Number	LUTs	Supply Voltage	Speed	Package	Pins	Temp. Grade
LFMXO4D-040HC-5BBG256C	3000	2.5 V/3.3 V	5	BBG256	256	Commercial
LFMXO4D-040HC-6BBG256C	3000	2.5 V/3.3 V	6	BBG256	256	Commercial
LFMXO4D-040HC-5BFG256C	3000	2.5 V/3.3 V	5	BFG256	256	Commercial
LFMXO4D-040HC-6BFG256C	3000	2.5 V/3.3 V	6	BFG256	256	Commercial

Part Number	LUTs	Supply Voltage	Speed	Package	Pins	Temp. Grade
LFMXO4D-050HC-5BBG256C	4320	2.5 V/3.3 V	5	BBG256	256	Commercial
LFMXO4D-050HC-6BBG256C	4320	2.5 V/3.3 V	6	BBG256	256	Commercial
LFMXO4D-050HC-5BFG256C	4320	2.5 V/3.3 V	5	BFG256	256	Commercial
LFMXO4D-050HC-6BFG256C	4320	2.5 V/3.3 V	6	BFG256	256	Commercial

Part Number	LUTs	Supply Voltage	Speed	Package	Pins	Temp. Grade
LFMXO4D-080HE-5UTG69C	6864	1.2 V	5	UTG69	69	Commercial
LFMXO4D-080HE-5BBG256C	6864	1.2 V	5	BBG256	256	Commercial
LFMXO4D-080HE-6BBG256C	6864	1.2 V	6	BBG256	256	Commercial
LFMXO4D-080HE-5BBG400C	6864	1.2 V	5	BBG400	400	Commercial
LFMXO4D-080HE-6BBG400C	6864	1.2 V	6	BBG400	400	Commercial
LFMXO4D-080HE-5UTG69CTR1K	6864	1.2 V	5	UTG69	69	Commercial
LFMXO4D-080HC-5BBG256C	6864	2.5 V/3.3 V	5	BBG256	256	Commercial
LFMXO4D-080HC-6BBG256C	6864	2.5 V/3.3 V	6	BBG256	256	Commercial
LFMXO4D-080HC-5BBG400C	6864	2.5 V/3.3 V	5	BBG400	400	Commercial
LFMXO4D-080HC-6BBG400C	6864	2.5 V/3.3 V	6	BBG400	400	Commercial

Part Number	LUTs	Supply Voltage	Speed	Package	Pins	Temp. Grade
LFMXO4D-110HE-5UTG69C	9400	1.2 V	5	UTG69	69	Commercial
LFMXO4D-110HE-5UTG69CTR1K	9400	1.2 V	5	UTG69	69	Commercial
LFMXO4D-110HE-5BBG256C	9400	1.2 V	5	BBG256	256	Commercial
LFMXO4D-110HE-6BBG256C	9400	1.2 V	6	BBG256	256	Commercial
LFMXO4D-110HE-5BBG400C	9400	1.2 V	5	BBG400	400	Commercial
LFMXO4D-110HE-6BBG400C	9400	1.2 V	6	BBG400	400	Commercial
LFMXO4D-110HE-5BBG484C	9400	1.2 V	5	BBG484	484	Commercial
LFMXO4D-110HE-6BBG484C	9400	1.2 V	6	BBG484	484	Commercial
LFMXO4D-110HC-5BBG256C	9400	2.5 V/3.3 V	5	BBG256	256	Commercial
LFMXO4D-110HC-6BBG256C	9400	2.5 V/3.3 V	6	BBG256	256	Commercial
LFMXO4D-110HC-5BBG400C	9400	2.5 V/3.3 V	5	BBG400	400	Commercial
LFMXO4D-110HC-6BBG400C	9400	2.5 V/3.3 V	6	BBG400	400	Commercial
LFMXO4D-110HC-5BBG484C	9400	2.5 V/3.3 V	5	BBG484	484	Commercial
LFMXO4D-110HC-6BBG484C	9400	2.5 V/3.3 V	6	BBG484	484	Commercial

5.5. LFMXO4D Low Power Industrial Grade Devices Packaging

Part Number	LUTs	Supply Voltage	Speed	Package	Pins	Temp. Grade
LFMXO4D-040ZC-2BBG256I	3000	2.5 V/3.3 V	2	BBG256	256	Industrial
LFMXO4D-040ZC-3BBG256I	3000	2.5 V/3.3 V	3	BBG256	256	Industrial
LFMXO4D-040ZC-2BFG256I	3000	2.5 V/3.3 V	2	BFG256	256	Industrial
LFMXO4D-040ZC-3BFG256I	3000	2.5 V/3.3 V	3	BFG256	256	Industrial

Part Number	LUTs	Supply Voltage	Speed	Package	Pins	Temp. Grade
LFMXO4D-050ZC-2BBG256I	4320	2.5 V/3.3 V	2	BBG256	256	Industrial
LFMXO4D-050ZC-3BBG256I	4320	2.5 V/3.3 V	3	BBG256	256	Industrial
LFMXO4D-050ZC-2BFG256I	4320	2.5 V/3.3 V	2	BFG256	256	Industrial
LFMXO4D-050ZC-3BFG256I	4320	2.5 V/3.3 V	3	BFG256	256	Industrial

Part Number	LUTs	Supply Voltage	Speed	Package	Pins	Temp. Grade
LFMXO4D-080ZC-2BBG256I	6864	2.5 V/3.3 V	2	BBG256	256	Industrial
LFMXO4D-080ZC-3BBG256I	6864	2.5 V/3.3 V	3	BBG256	256	Industrial
LFMXO4D-080ZC-2BBG400I	6864	2.5 V/3.3 V	2	BBG400	400	Industrial
LFMXO4D-080ZC-3BBG400I	6864	2.5 V/3.3 V	3	BBG400	400	Industrial

Part Number	LUTs	Supply Voltage	Speed	Package	Pins	Temp. Grade
LFMXO4D-110ZC-2BBG256I	9400	2.5 V/3.3 V	2	BBG256	256	Industrial
LFMXO4D-110ZC-3BBG256I	9400	2.5 V/3.3 V	3	BBG256	256	Industrial
LFMXO4D-110ZC-2BBG400I	9400	2.5 V/3.3 V	2	BBG400	400	Industrial
LFMXO4D-110ZC-3BBG400I	9400	2.5 V/3.3 V	3	BBG400	400	Industrial
LFMXO4D-110ZC-2BBG484I	9400	2.5 V/3.3 V	2	BBG484	484	Industrial
LFMXO4D-110ZC-3BBG484I	9400	2.5 V/3.3 V	3	BBG484	484	Industrial

5.6. LFMXO4D High Performance Industrial Grade Devices Packaging

Part Number	LUTs	Supply Voltage	Speed	Package	Pins	Temp. Grade
LFMXO4D-040HC-5BBG256I	3000	2.5 V/3.3 V	5	BBG256	256	Industrial
LFMXO4D-040HC-6BBG256I	3000	2.5 V/3.3 V	6	BBG256	256	Industrial
LFMXO4D-040HC-5BFG256I	3000	2.5 V/3.3 V	5	BFG256	256	Industrial
LFMXO4D-040HC-6BFG256I	3000	2.5 V/3.3 V	6	BFG256	256	Industrial

Part Number	LUTs	Supply Voltage	Speed	Package	Pins	Temp. Grade
LFMXO4D-050HC-5BBG256I	4320	2.5 V/3.3 V	5	BBG256	256	Industrial
LFMXO4D-050HC-6BBG256I	4320	2.5 V/3.3 V	6	BBG256	256	Industrial
LFMXO4D-050HC-5BFG256I	4320	2.5 V/3.3 V	5	BFG256	256	Industrial
LFMXO4D-050HC-6BFG256I	4320	2.5 V/3.3 V	6	BFG256	256	Industrial

Part Number	LUTs	Supply Voltage	Speed	Package	Pins	Temp. Grade
LFMXO4D-080HE-5UTG69I	6864	1.2 V	5	UTG69	69	Industrial
LFMXO4D-080HE-5BBG256I	6864	1.2 V	5	BBG256	256	Industrial
LFMXO4D-080HE-6BBG256I	6864	1.2 V	6	BBG256	256	Industrial
LFMXO4D-080HE-5BBG400I	6864	1.2 V	5	BBG400	400	Industrial
LFMXO4D-080HE-6BBG400I	6864	1.2 V	6	BBG400	400	Industrial
LFMXO4D-080HE-5UTG69ITR1K	6864	1.2 V	5	UTG69	69	Industrial

Part Number	LUTs	Supply Voltage	Speed	Package	Pins	Temp. Grade
LFMXO4D-080HC-5BBG256I	6864	2.5 V/3.3 V	5	BBG256	256	Industrial
LFMXO4D-080HC-6BBG256I	6864	2.5 V/3.3 V	6	BBG256	256	Industrial
LFMXO4D-080HC-5BBG400I	6864	2.5 V/3.3 V	5	BBG400	400	Industrial
LFMXO4D-080HC-6BBG400I	6864	2.5 V/3.3 V	6	BBG400	400	Industrial

Part Number	LUTs	Supply Voltage	Speed	Package	Pins	Temp. Grade
LFMXO4D-110HE-5UTG69I	9400	1.2 V	5	UTG69	69	Industrial
LFMXO4D-110HE-5UTG69ITR1K	9400	1.2 V	5	UTG69	69	Industrial
LFMXO4D-110HE-5BBG256I	9400	1.2 V	5	BBG256	256	Industrial
LFMXO4D-110HE-6BBG256I	9400	1.2 V	6	BBG256	256	Industrial
LFMXO4D-110HE-5BBG400I	9400	1.2 V	5	BBG400	400	Industrial
LFMXO4D-110HE-6BBG400I	9400	1.2 V	6	BBG400	400	Industrial
LFMXO4D-110HE-5BBG484I	9400	1.2 V	5	BBG484	484	Industrial
LFMXO4D-110HE-6BBG484I	9400	1.2 V	6	BBG484	484	Industrial
LFMXO4D-110HC-5BBG256I	9400	2.5 V/3.3 V	5	BBG256	256	Industrial
LFMXO4D-110HC-6BBG256I	9400	2.5 V/3.3 V	6	BBG256	256	Industrial
LFMXO4D-110HC-5BBG400I	9400	2.5 V/3.3 V	5	BBG400	400	Industrial
LFMXO4D-110HC-6BBG400I	9400	2.5 V/3.3 V	6	BBG400	400	Industrial
LFMXO4D-110HC-5BBG484I	9400	2.5 V/3.3 V	5	BBG484	484	Industrial
LFMXO4D-110HC-6BBG484I	9400	2.5 V/3.3 V	6	BBG484	484	Industrial

5.7. LFMXO4D Low Power Automotive Grade Devices Packaging

Part Number	LUTs	Supply Voltage	Speed	Package	Pins	Temp. Grade
LFMXO4D-080ZC-2BBG256A	6864	2.5 V/3.3 V	2	BBG256	256	Automotive
LFMXO4D-110ZC-2BBG256A	9400	2.5 V/3.3 V	2	BBG256	256	Automotive
LFMXO4D-110ZC-2BBG484A	9400	2.5 V/3.3 V	2	BBG484	484	Automotive

5.8. LFMXO4D High Performance Automotive Grade Devices Packaging

Part Number	LUTs	Supply Voltage	Speed	Package	Pins	Temp. Grade
LFMXO4D-040HC-5BBG256A	3000	2.5 V/3.3 V	5	BBG256	256	Automotive
LFMXO4D-050HC-5BBG256A	4320	2.5 V/3.3 V	5	BBG256	256	Automotive
LFMXO4D-080HE-5BBG256A	6864	1.2 V	5	BBG256	256	Automotive
LFMXO4D-110HE-5BBG256A	9400	1.2 V	5	BBG256	256	Automotive
LFMXO4D-110HE-5BBG484A	9400	1.2 V	5	BBG484	484	Automotive

References

A variety of technical notes for the MachXO4 RoT family are available on the Lattice website.

- [MachXO4 sysCLOCK PLL Design and Usage Guide \(FPGA-TN-02391\)](#)
- [MachXO4 Implementing High-Speed I/O Interface \(FPGA-TN-02410\)](#)
- [MachXO4 sysI/O User Guide \(FPGA-TN-02398\)](#)
- [MachXO4 Programming and Configuration User Guide \(FPGA-TN-02393\)](#)
- [PCB Layout Recommendations for BGA Packages \(FPGA-TN-02024\)](#)
- [Minimizing System Interruption During Configuration Using TransFR Technology \(FPGA-TN-02198\)](#)
- [Boundary Scan Testability with Lattice sysI/O Capability \(AN8066\)](#)
- [Thermal Management document \(FPGA-TN-02044\)](#)
- [FPGA Design Software](#)
- [MachXO4 web page](#)
- [Lattice Insights](#) for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at
<https://www.latticesemi.com/Support/AnswerDatabase>.

For Quality and Reliability documents, email requests may be sent to custreq@latticesemi.com

Revision History

Revision 1.1, September 2026

Section	Change Summary
All	Made editorial fixes.
Introduction	Updated the package status classification in Table 1.1. Specification Status for MachXO4 RoT Devices to align with the current product qualification and validation status.
Ordering Information	- Updated the two marking diagrams in the Ordering Information section. - Added the following OPNs to the LFMXO4D High Performance Commercial Grade Devices Packaging section: - LFMXO4D-080HE-5BBG256C - LFMXO4D-080HE-6BBG256C - LFMXO4D-080HE-5BBG400C - LFMXO4D-080HE-6BBG400C - LFMXO4D-110HE-5BBG256C - LFMXO4D-110HE-6BBG256C - LFMXO4D-110HE-5BBG400C - LFMXO4D-110HE-6BBG400C - LFMXO4D-110HE-5BBG484C - LFMXO4D-110HE-6BBG484C - Added the following OPNs to the LFMXO4D High Performance Industrial Grade Devices Packaging section: - LFMXO4D-080HE-5BBG256I - LFMXO4D-080HE-6BBG256I - LFMXO4D-080HE-5BBG400I - LFMXO4D-080HE-6BBG400I - LFMXO4D-110HE-5BBG256I - LFMXO4D-110HE-6BBG256I - LFMXO4D-110HE-5BBG400I - LFMXO4D-110HE-6BBG400I - LFMXO4D-110HE-5BBG484I - LFMXO4D-110HE-6BBG484I

Revision 1.0, September 2025

Section	Change Summary
All	- Changed <i>MachXO4D</i> to <i>LFMXO4D</i> globally. - Replaced <i>ESB</i> with <i>CRE</i> and replaced <i>Embedded Security Block</i> with <i>Cryptographic Engine</i> globally. - Updated software tool references throughout the document.
Introduction	- Changed <i>The MachXO4 family consists of low-power, instant-on, non-volatile, and Flash-based FPGAs with 10 devices, featuring densities ranging from 896 to 9400 Look-Up Tables (LUTs)</i> to <i>The MachXO4 RoT devices consist of low-power, instant-on, non-volatile, and Flash-based FPGAs with four devices, featuring densities ranging from 3000 to 9400 Look-Up Tables (LUTs).</i> - Changed <i>These FPGAs are available in a range of advanced halogen-free packages, from the compact 2.5 x 2.5 mm WLCSP to the 20 x 20 mm TQFP</i> to <i>These RoT FPGAs are available in a range of advanced halogen-free packages, from the compact 5.2 x 6.2 mm WLCSP to the 19 x 19 mm BGA.</i> - In the Low Power and Programmable Architecture section: - changed <i>Logic Density ranging from 896 to 9.4k LUT4</i> to <i>Logic Density ranging from 3k to 9.4k LUT4;</i> - changed <i>64 to 432 kb of embedded memory (EBR)</i> to

Section	Change Summary
	80 to 432 kb of embedded memory (EBR); - changed Up to 54 kbits Distributed RAM to Up to 73 kbits Distributed RAM. - In the Broad Range of Advanced Packaging section: - changed Compact packages with high I/O-to-LUT ratio up to 382 I/O to Compact packages with high I/O-to-LUT ratio up to 381 I/O; - removed the description of the 0.4 mm pitch; - updated descriptions of the 0.5 mm pitch, 0.65 mm pitch, 0.8 mm pitch, and 1.0 mm pitch. - In Table 1.2. MachXO4 Family RoT Devices Selection Guide, removed the HE (VCC = 1.2 V) Device Option for LFMXO4D-040 and LFMXO4D-050 devices. - Newly added Table 1.1. Specification Status for MachXO4 RoT Devices.
Architecture	Updated Figure 2.2. PFU Block Diagram and Figure 2.3. Slice Diagram.
DC and Switching Characteristics	- In Table 3.1. Absolute Maximum Rating^{1, 2, 3}, added a column for LFMXO4D HE (1.2 V). - Removed MachXO4D-040HE and MACHXO4D-050HE devices from Table 3.8. Static Supply Current^{1, 2, 3, 6} and Table 3.9. Programming and Erase Supply Current^{1, 2, 3, 4}. - Table 3.22. MachXO4 RoT External Switching Characteristics – HE/HC Devices^{1, 2, 3, 4, 5, 6, 10}: under the 7:1 LVDS Inputs (GDDR71_RX.ECLK.7:1)⁹ section, changed the repeated MachXO4D-040, MachXO4D-050 devices, bottom side only description to LFMXO4D-080, LFMXO4D-110 devices, bottom side only for the t_{DVE} parameter.
Signal Descriptions	- Updated headers of below tables to align with LFMXO4D devices packages: Table 4.2. LFMXO4D-040 Pin Summary, Table 4.3. LFMXO4D-050 Pin Summary, Table 4.4. LFMXO4D-080 Pin Summary, Table 4.5. LFMXO4D-110 Pin Summary. - Added UTG69 related pin information in Table 4.4. LFMXO4D-080 Pin Summary. - Added UTG69 and BBG484 related pin information in Table 4.5. LFMXO4D-110 Pin Summary.
Ordering Information	- Updated LFMXO4D Part Number Description: - updated the slowest Speed number from 4 to 5 for High Performance parts; - removed TR50 = 50 parts per reel from Shipping Method; - added BSG132, TSG144, BTG256, and BTG400 related descriptions to Package. - Removed the following OPNs from the LFMXO4D High Performance Commercial Grade Devices Packaging section: LFMXO4D-040HE-5BBG256C LFMXO4D-040HE-6BBG256C LFMXO4D-040HE-5BFG256C LFMXO4D-040HE-6BFG256C LFMXO4D-050HE-5BBG256C LFMXO4D-050HE-6BBG256C LFMXO4D-050HE-5BFG256C LFMXO4D-050HE-6BFG256C LFMXO4D-080HE-5BBG400C LFMXO4D-080HE-6BBG400C LFMXO4D-080HE-5BBG256C LFMXO4D-080HE-6BBG256C LFMXO4D-110HE-5BBG484C LFMXO4D-110HE-6BBG484C LFMXO4D-110HE-5BBG400C LFMXO4D-110HE-6BBG400C LFMXO4D-110HE-5BBG256C LFMXO4D-110HE-6BBG256C - Newly added the following OPNs to the LFMXO4D High Performance Commercial Grade Devices Packaging section: LFMXO4D-080HE-5UTG69CTR1K LFMXO4D-110HE-5UTG69CTR1K

Section	Change Summary
	- Removed the following OPNs from the LFMXO4D High Performance Industrial Grade Devices Packaging section: LFMXO4D-040HE-5BBG256I LFMXO4D-040HE-6BBG256I LFMXO4D-040HE-5BFG256I LFMXO4D-040HE-6BFG256I LFMXO4D-050HE-5BBG256I LFMXO4D-050HE-6BBG256I LFMXO4D-050HE-5BFG256I LFMXO4D-050HE-6BFG256I LFMXO4D-080HE-5BBG400I LFMXO4D-080HE-6BBG400I LFMXO4D-080HE-5BBG256I LFMXO4D-080HE-6BBG256I LFMXO4D-110HE-5BBG484I LFMXO4D-110HE-6BBG484I LFMXO4D-110HE-5BBG400I LFMXO4D-110HE-6BBG400I LFMXO4D-110HE-5BBG256I LFMXO4D-110HE-6BBG256I - Newly added the following OPNs from the LFMXO4D High Performance Industrial Grade Devices Packaging section: LFMXO4D-080HE-5UTG69ITR1K LFMXO4D-110HE-5UTG69ITR1K

Revision 0.70, July 2025

Section	Change Summary
All	Initial Advance release.



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