

Lattice Radiant Known Issues

2026.1 Known Issues

The following are known issues for Radiant Software 2026.1. If no workaround is available, please contact Lattice Technical Support for further assistance.

Radiant 2026.1 and the 2026.1 standalone tools cannot be uninstalled using the Windows Add or Remove Programs interface.

Workaround: To uninstall Radiant 2026.1 or 2026.1 standalone tools (such as Reveal Analyzer, Programmer, or Power Calculator), navigate to the installation directory and run uninstaller.exe.

Devices affected: All devices

Reference number: DNG-33155

Hold Time Violations May Occur in LAV-AT Designs When Using the MPPHY Module.

Radiant software automatically inserts LMMI arbiter logic to enable access to the MPPHY LMMI interface.

This implementation introduces a LUT4-based clock multiplexer in the LMMI clock path to enable Reveal Controller access to the MPPHY LMMI interface. The additional LUT4 logic can introduce significant clock skew, which may result in hold time violations in user designs.

This issue applies to the following Lattice IPs that incorporate the MPPHY module:

- DisplayPort IP
- JESD204B IP
- PCIe x8 IP
- Ethernet IPs (Tri-Speed, 2.5G, 5G, 10G, and 25G)

Workaround:

Try running your design using different Lattice Radiant tool settings such as Impose Hold Timing Correction or seeds. For further assistance, contact Lattice support.

For the latest update, refer to the Lattice Knowledge Base article.

Devices affected: Lattice Avant (LAV-AT)

Reference number: DNG-29323

SEDC May Fail to Detect Errors After 1-Bit or 2-Bit SEI Bitstream Injection on Avant Devices.

Some 1-bit and 2-bit Soft Error Injection (SEI) bitstreams do not function correctly on Avant devices. After the SEI bitstream is injected, the Soft Error Detection and Correction (SEDC) logic may fail to detect the injected error, report an incorrect error bit location, or return zero for the error bit location. The error frame location is typically reported correctly. The failure pattern depends on the target block (PFU, DSP, routing, or mixed-block injection).

Devices affected: Lattice Avant (LAV-AT)

Reference number: DNG-26267

SEI Bitstream Error Bit and Region Locations May Differ Between Hardware and Software on Avant Devices.

When using Soft Error Injection (SEI) bitstreams for Soft Error Detection and Correction (SEDC) testing, the error bit location and error region location reported by the hardware do not match the values specified by the software-generated SEI bitstream profile. The error frame location is reported correctly.

Devices affected: Lattice Avant (LAV-AT)

Reference number: DNG-26257

Synplify Pro May Ignore SDC create_clock Constraints in Designs Using PLLs.

In Synplify Pro, create_clock constraints defined in an SDC file may not be recognized for designs that use one or more PLLs, resulting in near-zero timing constraint coverage. The same constraints are recognized correctly when using the Lattice Synthesis Engine (LSE).

Devices affected: All devices

Reference number: DNG-25214

Power Calculator Reports 100 Percent Utilization for MPPHY with Partial Lane Usage.

The Power Calculator displays 100 percent resource utilization for an MPPHY when fewer than all four lanes are in use. The displayed value does not reflect the actual percentage based on the number of lanes used. For example, using three of four lanes shows 100 percent instead of the expected 75 percent.

Devices affected: Lattice Avant (LAV-AT)

Reference number: DNG-23785

Power Calculator Reports Incorrect Available MPPHY Quad Count for LAV-AT-X70 FBG644 Package.

The Power Calculator MPPHY tab reports an incorrect number of available MPPHY Quads for the LAV-AT-X70 FBG644 package. For example, MAP reports that 2 MPPHY Quads are available for this package, but the Power Calculator displays 7, which is incorrect.

Devices affected: Lattice Avant (LAV-AT-X70)

Reference number: DNG-32825

Bitstream Generation Produces Incorrect Configuration for Designs Using IMON with DelayC.

Bitstream Generation may produce an incorrect bitstream for designs that use IMON (current monitoring) with DelayC on LIFCL devices. In such cases, the MIBMEM_56/MC1_SEL_FINE_DELAY_CODE_REG_OR_BYPASS_ENABLE_A setting may not be properly enabled, which can lead to device hardware failure.

Devices affected: Certus-NX (LFD2NX), CertusPro-NX (LFCPNX), CrossLink-NX (LIFCL)

Reference number: DNG-32594

Simulation Model Incorrectly Maps RX/TX Polarity Inversion Parameters in PCS Core and EOM Control Parameters in PCIe Core.

The simulation model for the PCS_CORE incorrectly maps the RX_POLINV and TX_POLINV polarity inversion parameters to the wrong register bit indices, causing simulation results to not reflect the configured polarity inversion behavior. In addition, the simulation model for the PCIE Core incorrectly maps the EOMMODE, EOMRDSEL, EOMDIVDIS, and EOMCTRL0_LOW parameters to the wrong register bit indices, causing simulation results to not reflect the configured EOM control behavior defined in the specification.

Devices affected: CertusPro-NX (LFCPNX)

Reference number: DNG-32515

ECO Does Not Update RAM_DP Memory Content Correctly When Using Byte Enable with Byte Size 8.

ECO flow may incorrectly update RAM_DP memory content when byte enable is used with a byte size of 8, resulting in incorrect memory initialization after the ECO operation.

Workaround:

Use one of the following alternatives:

1. Do not use the ECO flow — regenerate the design if a memory content change is required.
2. Use a byte size of 9 instead of 8.

3. Use RAM_DP_TRUE instead of RAM_DP (the problem is specific to PDPW8KC primitive).

Devices affected: MachXO4 (LFMXO4)

Reference number: DNG-32505

Exported Pin Layout File Shows Package Delay and Trace Length as -1 for LAV-AT-X30 and LN2-CT-20 LFG676 Packages.

Package delay and trace length values are displayed as -1 in the exported pin layout file for LAV-AT-X30 and LN2-CT-20 LFG676 packages.

Workaround: Obtain the latest package data information from the Lattice website.

Devices affected: Lattice Avant (LAV-AT-X30), Certus-N2 (LN2-CT-20)

Reference number: DNG-32472

Missing Timing Arcs for JTAG Primitive May Cause Functional Failures on Nexus Devices.

Timing Analysis may not report timing violations for designs using the JTAG interface on Nexus devices because timing arcs for the JTAG primitive are incomplete, which may lead to functional failures on the hardware even when timing analysis reports no violations.

Workaround: If functional failures are seen when using Reveal or other modules that include the JTAG block, and timing analysis does not report violations, re-run Place and Route with a different placement seed, as changing the seed may result in the design passing on hardware.

Devices affected: All Nexus devices

Reference number: DNG-32467

Post-Place and Route Simulation Shows Incorrect Memory Initialization for EBR Primitives with Non-Zero INITVAL.

The Post-Place and Route Simulation Model returns incorrect data at the initial addresses of EBR memory primitives (SP8KC, DP8KC, PDP8KC) when non-zero INITVAL attributes are configured.

Devices affected: MachXO4 (LFMXO4)

Reference number: DNG-31327

Simulation Model Returns Incorrect Read Data for PDP8KC Primitive in 2-Bit Read Mode.

Simulation Model for the PDP8KC memory primitive returns corrupted read data when configured in mixed-width mode with a 2-bit read width (`DATA_WIDTH_R = 2`), where bit-1 of every 5th read data value in an 8-address segment does not reflect the data that was written.

Devices affected: MachXO4 (LFMXO4)

Reference number: DNG-30663

Synplify Pro Does Not Correctly Apply the `add_delay` Option for `set_output_delay` and `set_input_delay` Constraints.

Synplify Pro does not correctly apply the `add_delay` option for `set_output_delay` and `set_input_delay` constraints when multiple clocks are defined, resulting in incorrect timing analysis results.

Workaround: Ensure that constraints are defined in the correct order within the SDC file.

Devices affected: All devices

Reference number: DNG-31290

DDRDLA Primitive Takes Extended Time to Lock in Simulation.

The DDRDLA primitive simulation model may require more than 300 microseconds of simulation time (approximately 10 minutes of real time) to assert the `ready_o` signal when using the default `DIV="1"` setting. This behavior can significantly increase overall simulation runtime.

Devices affected: Lattice Avant (LAV-AT), Certus-N2 (LN2-CT)

Reference number: DNG-31228

Synplify Pro May Not Infer IO Registers When `syn_useioff` Is Applied Directly to Top-Level Ports.

When using Synplify Pro for synthesis, applying the `syn_useioff` attribute directly on top-level ports may not infer IO registers, which is a change in behavior compared to previous Radiant releases.

Workaround: Apply the `syn_useioff` attribute on intermediate signals instead of directly on top-level ports.

Devices affected: CrossLink-NX (LIFCL), Lattice Avant (LAV-AT)

Reference number: DNG-32343

Physical Designer Displays Incorrect SLICE Configuration Values and Missing Connection Highlights.

In Physical Designer, SLICE LUT INIT values may not accurately reflect their corresponding logic equations, and some internal SLICE connections may not be highlighted in Routing Mode.

Devices affected: Lattice Avant (LAV-AT)

Reference number: DNG-31474

DDR Memory Controller IP Generation Failure on Linux.

The import construct is not supported in the IP Generation Engine on some Linux OS versions. This may cause the DDR Memory Controller IP to fail to generate.

Workaround: Avoid using the import construct and reference everything explicitly.

Devices affected: Lattice Avant (LAV-AT)

Reference number: DNG-31278

Synplify Pro Ignores the `syn_useioff` Attribute in User VHDL Code.

In certain VHDL designs, Synplify Pro does not pack registers into I/O pad cells when the `syn_useioff` attribute is specified. As a result, the Map report indicates zero input/output I/O registers used. In contrast, LSE recognizes and applies the attribute as expected.

Workaround: Apply the `syn_useioff` attribute directly to the I/O signals.

Devices affected: CrossLink-NX (LIFCL)

Reference number: DNG-30879

Place and Route Places Clock Buffer Instances Outside the Placement Group Boundary

For designs using regional clocks, the clock sources are restricted to specific device locations due to architectural limitations. If such a source is assigned to a PGROUP that does not include any valid placement locations, placement issues may occur.

Workaround: This is not a functional issue but may appear as a quality issue. If you see WARNING <61293316> - par: discard locked instance messages in the log file and observe poor WNS after placement, it is recommended to avoid using PGROUPs.

Devices affected: Lattice Avant (LAV-AT)

Reference number: DNG-30821

Timing Analysis Reports Incorrect Delay Values for Certain DELAYA Paths.

The timing model for certain DELAYA paths contains incorrect delay values (~6 ns vs. the expected 0.4–1 ns range), causing Timing Analysis to report false timing violations on designs that use these paths.

Workaround: Set the affected DELAYA timing paths as false paths.

Devices affected: Certus-NX (LFD2NX)

Reference number: DNG-29460

Net Display is Incorrect in Logic Block View in Physical Designer.

In the Radiant Physical Designer GUI, certain nets may display incorrectly in the Logic Block View, showing inaccurate signal connections. This is a visual display issue only and does not affect design functionality.

Devices affected: Lattice Avant (LAV-AT)

Reference number: DNG-23192

Physical Designer IO Mode Pin Labels Overlap and Are Unreadable on LFMXO4-050 and LFMXO4-080 Devices.

In the Radiant Physical Designer GUI, when viewing IO mode for LFMXO4-050 and LFMXO4-080 devices, pin name labels overlap each other, rendering them unreadable. Users cannot clearly identify specific pins or their locations in IO mode. This issue is observed specifically on LFMXO4-050HC and LFMXO4-080HC does not appear on other devices.

Devices affected: MachXO4 (LFMXO4)

Reference number: DNG-32777

Certus-N2 Devices Missing IBIS HW Data Status in .ibs Report.

Certus-N2 (LN2-CT) devices are missing IBIS hardware data status entries in the generated .ibs report. This issue is caused by the IBIS generator referencing incorrect master IBIS files for these devices, leading to absent status information.

Devices affected: Certus-N2 (LN2-CT)

Reference number: DNG-32156

Synplify Pro Does Not Report an Error When Memory Initialization File Is Missing.

Synplify Pro in Radiant reports missing data files used by readmemh/readmemb as warnings instead of errors. Due to the large number of synthesis warnings, this can be easily overlooked and may lead to incorrect results.

Workaround: Explicitly provide the data file specified in readmemh (or readmemb). Also, monitor warning message WARNING <2012641> - CG371: Cannot find data file ... for task \$readmemh and add the missing data file if it appears.

Devices affected: All devices

Reference number: DNG-31492

Physical Designer Displays Incorrect Rendering for IFD1P3BX Primitive.

In Radiant Physical Designer, the IFD1P3BX primitive may be displayed incorrectly in the GUI during routing mode, with some ports shown inverted or not filled as expected. This is a display-only issue and does not affect design functionality or results. Similar display inconsistencies may also appear for other logic block primitives.

Devices affected: Lattice Avant (LAV-AT)

Reference number: DNG-14531

Programmer GUI Theme Displays Incorrectly when Windows and Radiant Use Different Themes

In the Programmer tool, the GUI theme colors display inconsistently when Windows is set to Dark mode while Radiant is configured to Light mode. This results in mixed styling and reduces readability of GUI elements.

Workaround: Set the Radiant theme to match the Windows theme. If the Windows theme is Dark, select the Dark theme for Radiant as well.

Devices affected: All devices

Reference number: DNG-32395

LSE Incorrectly Initializes a VHDL Boolean Register to SET Instead of RESET when syn_keep Attribute is Applied

In Lattice Synthesis (LSE), a VHDL boolean register with the `syn_keep` attribute is incorrectly mapped to a preset flip-flop (power-on state = 1) instead of a reset flip-flop (power-on state = 0), causing the register to initialize to the wrong value in both simulation and on hardware.

Workaround: Remove the `syn_keep` attribute from the affected signals.

Devices affected: Lattice Avant (LAV-AT)

Reference number: DNG-32576

UFM JED File Cannot Be Generated for MachXO5-NX Devices

In the Deployment Tool (Bitstream Generation), the UFM-specific JED file cannot be generated for LFMXO5-35/T and LFMXO5-65/T devices, preventing users from programming user data to the internal flash using a UFM JED file.

Devices affected: MachXO5-NX (LFMXO5)

Reference number: DNG-32987

Run All Button Does Not Execute the Design Flow for EAPR Devices

In the Radiant GUI, clicking the Run All button on EAPR (Early Access Program) devices does not run any process (Synthesis, Map, and Place & Route). This is because the tool incorrectly requires the Export/Bitstream stage which is not available on these devices.

Workaround: For devices that do not support the Export stage, the Export step is treated as a no-op. The Run All action now executes the flow through PAR and no longer fails due to missing or empty Bitgen tasks. When running Run All, a warning is issued to indicate that Export is disabled:

WARNING: Export Files is not available for this device.

Devices affected:

- Certus-N2 (LN2-CT-20ES)
- Lattice Avant (LAV-AT-E70ES1/E70/E50)
- MachXO5-NX (LFMXO5-25/35T/55T/65T/100T)
- Certus-NX (LFD2NX-9/15/17/25/28/35/40/65)
- MachXO4 (LFMXO4-010HE/HC, 015HE/HC, 025HE/HC, 050HE/HC; 080HE/HC, 110HE/HC)

Reference number: DNG-32987, DNG-31168

Device Provisioning of the MachXO5-55TD Using UFM with STAPL is Not Functioning.

When using the Programmer to generate a STAPL file for device provisioning (Erase, Program, Verify, Refresh) with UFM on MachXO5-55TD devices, the file generation fails.

Workaround: Use Programmer Direct Programming mode to program UFM instead of generating a STAPL file.

Devices affected: MachXO5-NX (LFMXO5)

Reference number: DNG-33024

When the Signals Column is Empty, clicking MSB/LSB Removes Virtual SW/LED Entries.

In Reveal Inserter, an empty signals column for multiple virtual switches/LEDs causes incorrect GUI behavior. When the LSB and MSB buttons are clicked, other virtual switches or LEDs are removed from the display.

Devices affected: All devices

Reference number: DNG-32369

PAR Fails When Implementation Directory Path Contains './' in the Radiant Project File.

In Radiant project (.rdf) files, inclusion of './' in the implementation directory value, whether manually specified or assigned via Tcl, results in incorrect path resolution. An extra './' is introduced, leading to PAR failure.

Workaround: Manually update the .rdf file and remove './' from the implementation directory path.

Devices affected: All devices

Reference number: DNG-33083

Placer Error Due to Carry Chain Clock Driver in Synplify Pro.

In Radiant 2026.1, Synplify Pro may generate a carry chain output as a clock driver, which is not supported by Place and Route, causing a placer error during implementation.

Workaround: A patch is available to address this issue. For assistance and to obtain the patch, please contact Lattice Technical Support.

Devices affected: CrossLink-NX (LIFCL)

Reference number: DNG-32781

DELAYB Delay Reports as Zero in Hold Timing Analysis.

In Timing Analysis, the DELAYB primitive delay is incorrectly reported as zero during hold time analysis when using the "m" speed grade, regardless of the DEL_VALUE and COARSE_DELAY settings, leading to inaccurate hold timing results.

Devices affected: CertusPro-NX (LFCPNX)

Reference number: DNG-32000

IDDRX2 Produces Incorrect Output in Gate-Level Simulation.

Timing simulation encounters clock domain crossing issue due to intrinsic delay mismatch on DQSBUF output signals – write pointer and clock DQSR90 that are used to drive subsequent IO Logic. If not fixed, the clock domain crossing issue will cause the RXDATA/output to be incorrect for IDDRX2 design.

Devices affected: CrossLink-NX (LIFCL)

Reference number: DNG-31855

Incorrect Auto-Generated Clock Constraint for PCIe x8 IP on Avant.

In Timing Analysis, the auto-generated clock constraint for the PCIe x8 IP link0_clk_usr_o output on Avant devices is set to an incorrect frequency (e.g., 50 MHz instead of the expected 250 MHz for Gen4x8), due to missing timing arcs from REFCLK to TXOUTCLK in the device timing model.

Devices affected: Lattice Avant (LAV-AT)

Reference number: DNG-28241

Power Calculator Does Not Constrain RAMX16/RAMX32 Count by Existing LUT Usage.

In the Power Calculator estimation mode, the maximum allowable count for RAMX16 and RAMX32 entries is not adjusted based on existing LUT usage for Avant and Khronos devices, allowing users to enter RAM values that exceed the device's actual available resources and producing misleading power estimates.

Devices affected: Lattice Avant (LAV-AT)

Reference number: DNG-31896

CONFIG_LMMID Simulation Model Does Not Fully Align with LMMI Specification.

The CONFIG_LMMID primitive simulation model (HW SIM Model) may not fully reflect silicon behavior when processing configuration commands, which can cause simulation results to differ from actual device operation.

Devices affected: Lattice Avant (LAV-AT), Certus-N2 (LN2-CT), Mach-N2 (LN2-MH)

Reference number: DNG-30574

Missing Timing Arcs in CONFIG_CLKRST_CORE.

In Timing Analysis, timing arcs are missing for the CONFIG_CLKRST_CORE block when using the OSC_CRE CFG_CLK with manually defined constraints, and the auto-generated constraints for CFG_CLK and LMMI_CLK are also absent, resulting in incomplete timing coverage.

Devices affected: MachXO5-NX (LFMXO5)

Reference number: DNG-28315

Timing Fails After Relaxing IO Slew Rate Constraint.

In Place and Route, changing an output IO's slew rate from FAST to MED increases the clock path delay significantly, causing hold violations that the router attempts to fix by detouring data paths, which in turn degrades setup timing and results in setup failures.

Devices affected: CrossLink-NX (LIFCL)

Reference number: DNG-29537

Power Calculator Selects Incorrect Default Device for Unsupported Avant PLC L-Variant.

When loading a Power Calculator project file (.pcf) that targets an Avant PLC L-variant device into a Radiant version released before the device is enabled, the Power Calculator silently selects a different default Avant device without issuing a warning, resulting in incorrect power estimates.

Devices affected: Lattice Avant (LAV-AT)

Reference number: DNG-32443

Intermittent Radiant Crash when Launching Device Constraint Editor.

Radiant may intermittently crash when launching the Device Constraint Editor (DCE) or when a design compilation is triggered from the DCE, due to a race condition when loading device data files (GUI).

Workaround: Close the Device Constraint Editor before starting design compilation. If the crash occurs during DCE launch, re-launch Radiant and try again.

Devices affected: All devices

Reference number: DNG-28678

Place and Route Failure when Using Four MIPI RX DPHY Interfaces in the Same I/O Bank on Avant Devices.

Place and Route may fail with a routing error when four MIPI DPHY RX IP instances are placed in the same I/O bank on Avant devices, due to limited clock routing resources for edge clocks within a single bank (Place and Route).

Devices affected: Lattice Avant (LAV-AT)

Reference number: DNG-32974

SDC `set_multicycle_path -setup` Constraint Dropped when Using Encrypted IP.

When using Synplify Pro, a `set_multicycle_path -setup` constraint defined in the SDC file is dropped during post-synthesis constraint processing when the target paths reside inside an encrypted IP block, while the corresponding `-hold` constraint is preserved.

Workaround: Define the multicycle path constraints in the physical design constraints (pdc) file instead of the SDC file, as PDC constraints are applied after mapping when the encrypted paths become visible.

Devices affected: CertusPro-NX (LFCPNX)

Reference number: DNG-31443

Spurious Hold Timing Failure on D-PHY RX Internal Path.

When using the CSI-2/DSI D-PHY Receiver IP on Nexus devices, Timing Analysis reports a spurious hold timing violation on an internal path from INLP to LSR, because the IP's embedded false path constraint does not take effect.

Workaround: Add the following false path constraint in the physical design constraints (.pdc) file using the full hierarchical net and pin path:

```
set_false_path -through [get_nets -hierarchical  
{mipi_rx_inst/u_dphyrx_ip/lscd_dphy_rx_inst/NOCIL_TOP.u_dphy_rx_core/rx_global_ctrl_inst/LP_HS_CLK_CONTROL.lp_hs_ctrl_clk/lp11_reset_n_i}] \  
-to [get_pins -hierarchical  
{mipi_rx_inst/u_dphyrx_ip/lscd_dphy_rx_inst/NOCIL_TOP.u_dphy_rx_core/rx_global_ctrl_inst/LP_HS_CLK_CONTROL.lp_hs_ctrl_clk/hs_en_off_inst/LSR}]
```

Devices affected: All Nexus devices

Reference number: DNG-30147

Place and Route Assigns CDR SGMIIN Input to an Unbonded I/O Site.

The Place and Route tool incorrectly assigns the SGMIIN CDR input to an unbonded I/O site (PB10A) on LFD2NX-15P and LFD2NX-25P devices. This results in a placement error that prevents successful design completion.

Workaround: Use the `ldc_set_location` constraint to manually place the CDR SGMIIN I/O.

Devices affected: Certus-NX (LFD2NX-15P, LFD2NX-25P)

Reference number: DNG-33068

Incorrect PLL Timing Model for iCE40UP Devices in Radiant.

In Timing Analysis, the PLL timing model for iCE40UP devices in Radiant is incomplete, with missing PLL intrinsic delay, missing derating on PLL tap delay, incorrect delay from PLL to global clock mux, and incorrect clock B adjustment, resulting in inaccurate timing analysis results.

Workaround: Use iCECube2 instead of Radiant for timing closure on iCE40UP designs.

Devices affected: iCE40 UltraPlus (iCE40UP)

Reference number: DNG-33029

Place and Route Errors Out on Designs with Unbalanced Wide LUT.

Place and Route encounters an error when processing designs that contain unbalanced wide LUTs, preventing the design from completing successfully.

Devices affected: MachXO4 (LFMXO4)

Reference number: DNG-33063

Lattice Synthesis (LSE) Intermittently Crashes During Synthesis.

LSE intermittently crashes with a segmentation violation or unknown signal error during synthesis, causing the design to fail with "error code 1" approximately 50% of the time.

Devices affected: Certus-NX (LFD2NX)

Reference number: DNG-31070

iCE40 PLL Timing Is Not Modeled Correctly in Radiant.

Timing Analysis reports significantly different PLL timing values for iCE40UP devices compared to iCEcube2, which may result in inaccurate timing closure.

Workaround: Use iCECube2 for timing analysis.

Devices affected: iCE40UP (iCE40 UltraPlus)

Reference number: DNG-32321

DSP PREADD9 Asynchronous Reset Causes Functional Failure on Hardware.

DSP block's PREADD9 multiplier output is stuck at all-zero on hardware when the RESET property is set to ASYNC.

Workaround: Use dynamic reset or synchronous mode instead.

Devices affected: CertusPro-NX (LFCPNX), CrossLink-NX (LIFCL-40, LIFCL-33), Certus-NX (LFD2NX-35, LFD2NX-65), MachXO5 (LFMXO5-35T, LFMXO5-65T)

Reference number: DNG-32692, DNG-32693, DNG-32694, DNG-32695

2025.2.1 Known Issues

The following are known issues for Radiant Software 2025.2.1. If no workaround is available, please contact Lattice Technical Support for further assistance.

DELAYE Used on a Clock Path Can Cause the Delayed Output to be Stuck Low in Hardware.

For Avant devices, a design that routes a clock through a DELAYE element to drive a delayed output can result in the delayed output pin being stuck low in hardware, even though post-map and post-PAR simulation waveforms appear correct. The issue is related to an incorrect DELAYMUX selection for the DELAYE path in the generated bitstream.

Devices affected: Lattice Avant (LAV-AT)

Reference number: DNG-31260

Timing Report Shows Infinite Slack on Output Paths When Set_Max_Delay Uses Datapath_Only.

In some designs that use a generated clock on an output port, applying a set_max_delay constraint with the datapath_only option on output paths can cause the timing report to show INF (infinite) slack for those paths. The affected paths are not reported as violating even when they should, because the tool initializes timing at the generated clock output with a default clock phase that does not match the generated clock definition.

Devices affected: CertusPro-NX (LFCPNX)

Reference number: DNG-29538

GDDR Aligned Mode Capture Clock Phase Not Configured for Avant Device.

When GDDR RX in Avant devices is configured to Aligned mode, the capture clock lacks the expected phase shift or delay, which can cause timing analysis failures.

Devices affected: Lattice Avant (LAV-AT)

Reference number: DNG-31269

PCIe Primitive Parameter Overrides Do Not Take Effect.

PCIe primitive parameters set in the PCIE.v module are not correctly applied to the PCIe core registers in hardware or simulation. As a result, the PCIe link may fail to train or link up.

Devices affected: CrossLink-NX (LIFCL)

Reference number: DNG-28201

You May Encounter a Large RAM DP True Synthesis Error When Port B Byte Enable is Used.

The Large RAM DP True (LRAM_DP_TRUE) IP can fail synthesis when Port B byte enable is enabled with 16-bit data width and output registers on both ports. The generated RTL creates an invalid `ben_b_w` part select, leading to errors such as index out of range and multiple non tristate drivers on `ben_b_i[1]`.

Workaround: Do not use LRAM_DP_TRUE with byte enable enabled on both ports and output registers enabled on both ports. If the design allows, temporarily disable byte enable or the output register on one or both ports.

If you must use this configuration, a temporary RTL edit can be used: locate the generated RTL file for the instance, find the assign statement that defines the overflow padding for `ben_b_w`, and modify it to remove the extra +1 and match the `ben_a_w` form, for example:

```
assign ben_b_w[(BWID_B - 1):(BYTE_WIDTH_B - (BWID_B * i1))] = {(BYTE_WIDTH_B - (BWID_B * i1))}{1'b1};
```

Then rebuild the project using the edited RTL.

Devices affected: Certus-NX (LFD2NX)

Reference number: DNG-31307

DQSBUF Delay Values in Timing Analyzer Does Not Match with Post PAR Simulation.

For LFCPNX designs, DQSBUF shifted clock delays (`DQSI2DQSR_DEL`, `S2DQSW_DEL`) reported in Static Timing Analysis can differ significantly from post PAR simulation values. The STA reports about 0.5 ns larger delay than post PAR for arcs such as DQSI to DQSR90 and ECLKIN to DQSW270, which can cause confusion when correlating STA and simulation results.

Devices affected: CertusPro-NX (LFCPNX)

Reference number: DNG-30385

There Are Missing AXI4 Lite Constraints When Using Encrypted IP for Avant Devices.

For encrypted AXI4 Lite IP used with Avant devices in Radiant 2025.2, some dpram related false path constraints are not applied, causing hold timing violations. The same constraints are applied correctly, and timing violations do not occur when using the unencrypted IP with the same configuration.

Workaround: Update the AXI4 Lite constraints to replace the encrypted portion of the instance path (for example `gen_pmi.gen_async.u_fifo`) with a wildcard (`/`) so the constraints match the renamed instances in the encrypted IP. Use this with care to avoid unintentionally setting false paths on other parts of the design.

Devices affected: Lattice Avant (LAV-AT)

Reference number: DNG-29853

LRAM Initialization from ECO Editor Sets Only 8 Bits Out of 32.

When initializing a 65536x8 LRAM from ECO Editor (all 1s or from a `.mem` file), only the first 8 bits of every 32 bit word are initialized correctly and the remaining 24 bits are left as 0 in the bitstream.

Devices affected: CrossLink-NX (LIFCL)

Reference number: DNG-29226

Bounding Box Selected Instance Resource Count Does Not Report Register Usage Correctly.

In the Bounding Box user interface, Selected Instance Resource Count can show zero usage for selected registers or flops because the count is taken from the MAP resource usage report, which does not include these instances for the affected designs.

Devices affected: MachXO5-NX (LFMXO5)

Reference number: DNG-26318

There is an IBIS Model Mismatch for Pull Mode and Series Resistance When Using the LFMXO4 Device.

In the LFMXO4 device family, pull mode and series resistance are not loaded correctly during IBIS report generation, which prevents the system from finding a matching IBIS model. When this issue occurs, you will see warning 1191010, and the affected input pins will not have IBIS information listed in the IBIS report.

Devices affected: MachXO4 (LFMXO4)

Reference number: DNG-31303

In Radiant 2025.2, PAR Ignores User Location Constraints for Instantiated DCC and Performs Automatic Placements of the Instantiated DCCs.

The `Idc_set_location` constraint is not supported for DCC instances in PAR because of hardware limitations.

Devices affected: Lattice Avant (LAV-AT)

Reference number: DNG-30001

Power Calculator DDRPHY Tab Activity Inputs Use AF And EF Instead of RX/TX/IDLE.

In the Power Calculator DDRPHY tab, the AF and EF fields are still displayed instead of the RX percent, TX percent, IDLE percent, and `data_H/data_L` percentages. The RX, TX, and IDLE percentages must sum to 100%.

Devices affected: Lattice Avant (LAV-AT)

Reference number: DNG-31469

Maximum Slack Limit Option in Timing Analyzer Has No Effect on Reported Paths.

In the Timing Analyzer, the Maximum Slack Limit setting is currently non-functional. Paths are reported regardless of the configured slack limit.

Devices affected: All devices

Reference number: DNG-30518

LOC Attribute May Be Ignored for Output Ports Declared as Reg When Using Synplify Pro.

In Synplify Pro, a LOC attribute attached to an output port declared as a reg and driving a flip flop can be ignored. As a result, PAR may place the output on a different package pin than specified by the LOC. The issue is not seen with LSE or when the output is declared as a wire with the LOC on the IO net.

Devices affected: MachXO5 (LFMXO5)

Reference number: DNG-30603

Synplify Optimization Can Cause Undesired Shift Register Output in Post Synthesis Simulation.

In some Ethernet based designs targeting Avant devices, Synplify can over optimize shift register logic that implements a delay element. When the array in the shift register is optimized, the post synthesis simulation shows undesired output on the shift register logic output, even though timing analysis passes and LSE does not exhibit the issue.

Workaround: Use NOCLIP, SYN_PRESERVE, or SYN_KEEP attributes to prevent optimizing the array.

Devices affected: Lattice Avant (LAV-AT)

Reference number: DNG-25076

Reveal Debug Insertion Can Cause Invalid EN_CIL And HSEL Parameter Values in DPHY CORE.

When Reveal is inserted into a design that instantiates DPHY CORE, Synplify can generate incorrect EN_CIL and HSEL parameter values for a secured DPHY instance.

Devices affected: CrossLink-NX (LIFCL)

Reference number: DNG-30353

ECO Editor Updates to EBR-based ROM Initialization May Result in INITVAL Contents That Differ from Ip-generated ROM Initialization for the Same Data Pattern.

When using the ECO flow to modify the initialization contents of EBR based ROMs, the resulting gate level memory initialization (INITVAL_xx) may not match the initialization produced by the IP Foundation (FIP) flow for the same intended data pattern. This can cause simulation and hardware behavior of ECO updated ROM contents to differ from the original FIP generated design, leading to potential functional mismatches.

Workaround: Avoid using the ECO editor to modify EBR ROM contents. Instead, update the ROM hex file and regenerate the ROM using the IP Foundation (FIP) flow, then rerun the full implementation flow (synthesis followed by place and route) so that the final gate level netlist uses consistent INITVAL_xx contents based on the updated hex file.

Devices affected: All devices

Reference number: DNG-30489

Unique ID Field is Not Editable in Device Constraint Editor.

For MachXO4 devices, the Unique ID (formerly TraceID) field in the sysCONFIG settings of the Device Constraint Editor is not editable and is locked to the default value of "0000". You cannot configure a custom Unique ID value through the DCE GUI. This is a software limitation in the current release.

Devices affected: MachXO4 (LFMXO4)

Reference number: DNG-29265

When the Width of ROM Data in a Memory Initialization File is Wider Than the Defined ROM Width, Radiant Issues Warnings and Ignores the Extra Bits.

The synthesis engine treats these extra bits as don't-care values and ROM module may be optimized away during synthesis.

In contrast, Diamond enforces strict consistency between the ROM width and the initialization file width, resulting in an error instead of continuing.

Workaround:

- Ensure that the memory initialization file width matches the ROM width defined in your design.
- Treat Radiant warnings (e.g., CG1194, CG532, MO156) as critical and correct the file before synthesis.
- If strict error handling is required, add a manual check in your design flow to validate memory file widths.

Devices affected: MachXO4 (LFMXO4)

Reference number: DNG-29440

CONFIG_LMMI Writes to Enable Multiboot May Fail in Hardware on Crosslink-NX When Using Higher LMMICLK Frequencies.

In Multiboot Reference Designs targeting CrossLink-NX, LMMI writes to CONFIG_LMMI can fail at LMMICLK frequencies above ~40 MHz, even though timing reports are clean. This may prevent the SPIM bit from being set in Control Register 0 and cause the multiboot sequence to fail.

Workaround: Constrain and operate LMMICLK at or below ~10–12 MHz when performing LMMI writes (e.g., when enabling multiboot).

Devices affected: CrossLink-NX (LIFCL)

Reference number: DNG-30992

The DCC and DCM Resource Utility in PAR Report are Missing.

You can still view the usage in the clock report area of the PAR report.

Devices affected: MachXO4 (LFMXO4)

Reference number: DNG-29345

Changing VCC in DCE and Standalone Timing Analyzer Does Not Affect Hold Analysis. Hold Analysis Always Uses VCC Max for Analysis.

Workaround: Manually select voltage during hold analysis. Holding uncertainty can be used to tighten constraints during placer or router.

Devices affected: All devices

Reference number: DNG-29957

LSE Synthesis May Fail When Crc_register Attribute is Used with an Error:” Cdc_register Chain Cannot Be Fully Determined for Register...”.

Devices affected: All devices

Reference number: DNG-29431

Using Distributed RAM (DPRAM) for a Shift-register Path That Feeds a Delay Element Can Cause the Delay Element Output to Behave Incorrectly.

With syn_keep or syn_preserve applied to the shift array, simulation shows glitches, and Reveal capture shows unintended or corrupted data. The problem is observed in both pre-synthesis and post-synthesis Reveal.

Workaround:

- Avoid DPRAM for the shift chain feeding the Delay Element. Use EBR or PFU registers for the shift register resource.
 - In IP configuration, select EBR or Registers as the resource.

- For inferred RTL, guide synthesis to map to block RAM or registers (e.g., set ramstyle to block RAM or registers in your synthesis attributes).
- If you must use DPRAM:
 - Keep the shift depth ≤ 32 where practical to reduce risk.
 - Remove syn_keep and syn_preserve on the internal shift array when not strictly required or apply them at module boundaries instead of the array element level.
- Reverify with simulation and Reveal after changing the resource selection. Designs using EBR or PFU registers do not show the issue.

Devices affected: Lattice Avant (LAV-AT-E70)

Reference number: DNG-29618

Gate-level Timing Simulation May Show an Unexpected Jitter for PLL.

This only affects the gate level timing simulation, and HW behavior is unaffected.

Devices affected: Lattice Avant (LAV-AT-E70)

Reference number: DNG-29299

LSE Synthesis May Fail Without Providing a Clear Error Message If the Design Includes Module Instantiations That Do Not Have Instance Names.

The same design may be compiled successfully with Synplify Pro but later fail during PAR.

Workaround:

- Always provide instance names for all module instantiations in your design.
- If the design fails without an error message, review the RTL for unnamed instances and update them accordingly.

Devices affected: Certus-NX (LFD2NX)

Reference number: DNG-29029

LSE Synthesis May Fail with an Error If the Project Path Length is Too Long. This Occurs Because the Synthesis Engine Has a Limit on the Maximum Path Length It Can Handle for Project Files and Directories.

Workaround:

- Shorten the project path by:

- o Moving the project to a directory closer to the root (e.g., C:\RadiantProjects\).
- o Reducing folder name lengths.
- Avoid using excessively long directory structures for project files.

Devices affected: All devices

Reference number: DNG-28606

Designs Using Nested VMs Fail During Post-Synthesis.

Workaround: Do not use nested VMs. Instantiate VMs separately.

Devices affected: Lattice Avant (LAV-AT)

Reference number: DNG-27317

When Using Synplify Pro, User-Defined Create_Generated_Clock Constraints in the SDC File for PLL Clock Outputs May Be Overwritten by Auto-generated PLL Clock Constraints if a Reveal Core is Added to the Design.

Without Reveal, user-defined constraints propagate correctly through synthesis and implementation. With Reveal present, the constraints are accepted during Constraint Propagation Engine (CPE) but fail to persist after synthesis.

Workaround:

- Define PLL clock constraints in the PDC file instead of SDC. PDC constraints are preserved even when Reveal is added.
- If SDC-based constraints are required, use post-synthesis Reveal debug flow.

Devices affected: CrossLink-NX (LIFCL)

Reference number: DNG-26270

Programming May Fail When Using Compressed Bitstreams.

Workaround: Use plain or uncompressed bitstream formats.

Devices affected: Lattice Avant (LAV-AT)

Reference number: DNG-26097

Radiant Timing Analysis for Designs Using LMMI_CLK / LMMI_CLKO May Show:

- **A missing timing arc from OSCA to CONFIG_CLKRST_CORE on the LMMI clock path (this is a bug).**
- **A 0 ns net delay from CONFIG_CLKRST_CORE to CONFIG_LMMI (this is expected behavior per the current timing model).**

As a result, the report may present a direct path from the OSC IP to CONFIG_LMMI without explicitly reflecting the expected clock path delay from LMMI_CLK to LMMI_CLKO (i.e., OSCA → CONFIG_CLKRST_CORE).

Devices affected: CertusPro-NX (LFCPNX)

Reference number: DNG-27889

Standalone Timing Analyzer Results May Differ from Runsta Results Even When Using the Same Pdc File.

The results from RunSTA are correct.

Workaround: Avoid using Standalone Timing Analyzer and use RunSTA for debug.

Devices affected: Certus-NX (LFD2NX)

Reference number: DNG-27523

The Location for a Secured Component (Hard DPHY) Cannot Be Changed.

Devices affected: CrossLink-NX (LIFCL)

Reference number: DNG-24746

In PLL Simulation, the Phase Stops Moving When It Goes Over 360 Degrees.

In a Phase-Locked Loop (PLL) simulation, the phase should not stop moving but only reset to stay within a specific range (such as 0°–360).

Devices affected: CrossLink-NX (LIFCL)

Reference number: DNG-23458

RTL Simulation of CONFIG_LMMIE And CONFIG_LMMIB Primitives May Fail or Produce Incorrect Results.

When using CONFIG_LMMIE or CONFIG_LMMIB primitives in RTL simulation, the simulation may produce incorrect results or fail entirely. This is a simulation model issue and does not affect hardware behavior.

Devices affected: MachXO5-NX (LFMXO5)

Reference number: DNG-22187

Clocks Using Pclk Routing and Driving Only Fabric Registers May Have Reduced Minimum Pulse Width at Higher Speed Grades.

Devices affected: CertusPro-NX (LFCPNX)

Reference number: DNG-21315

Synplify Pro Synthesis May Fail If The .Sdc File Contains a User-defined Constraint Referencing a Hierarchical Object That Includes a Dot (.). Example: Top.Inst/Out.

Workaround:

- Create the constraint in the .pdc file instead of .sdc file.
- Use LSE for synthesis.

Devices affected: CrossLink-NX (LIFCL)

Reference number: DNG-20134

Inserting a Reveal Core May Cause Undesired Toggling of the FIFO Empty Flag in Pmi_fifo Designs Synthesized with Synplify Pro.

Workaround: Use Post-Synthesis Reveal Debug flow.

Devices affected: CertusPro-NX (LFCPNX)

Reference number: DNG-24358

In Certus-NX LRAM IP Simulation, When DPS is Asserted High, LRAM_Ready May Remain High Instead of Going Low.

This does not affect HW functionality and only affects simulation.

Expected behavior: Driving DPS high powers down LRAM, so lram_ready should be low.

Devices affected: Certus-NX (LFD2NX)

Reference number: DNG-27555

Avant Bitstream Generation May Consume Significantly More Host Memory Than Reported.

During bitstream generation for Avant devices, the Bitgen process may consume significantly more system memory than the reported peak memory usage. This can result in unexpected host memory pressure and, in some cases, out-of-memory failures.

Workaround:

- Run Bitgen on hosts with additional available RAM.
- Do not rely on the reported peak memory usage values.
- Prefer machines with larger memory capacity or Linux hosts for improved stability.

Devices affected: Avant (LAV-AT)

Reference number: DNG-29447

PCIe Configuration Issue (x4 and x8 Lane Configurations).

An issue has been identified in PCIe configurations involving x4 and x8 lane modes. When the lsc_misc_lock bit is asserted in the 03B device, access to the user INIT register space is blocked. This restriction prevents proper programming of lane 2.

Workaround: The affected registers can be overwritten through the LMMI interface.

Devices affected: Lattice Avant (LAV-AT) -- All LAV-AT devices utilizing MPPHYx4 or MPPCIEx4 in their design are impacted.

Reference number: DNG-31227

Physical Designer GUI Does Not Display or Highlight All Instances Within a Hierarchy.

In the Physical Designer GUI, not all instances are displayed in the netlist instance tree when expanding a hierarchy node. In addition, instances that are not shown in the tree are also not highlighted when using the highlight selection feature.

Devices affected: All devices

Reference number: DNG-31731

FIFO32K Simulation Model Output Data Latency Is Longer Than Expected with OUTREG Parameter.

Simulation Model for the FIFO32K primitive produces output data (DO) with an additional read clock cycle of latency than expected, both when the output register is bypassed (OUTREG = "BYPASSED") and when it is enabled (OUTREG = "USED"), causing simulation results to not be cycle-accurate.

Devices affected: Lattice Avant (LAV-AT), Certus-N2 (LN2-CT)

Reference number: DNG-32149

Inserting Reveal During Pre-Synthesis Causes Change in the Hierarchy Names When OSC IP Is Used. It Results in Timing Constraints That Use Hierarchical Objects to be Dropped.

Workaround: Use Post-Synthesis Reveal debug flow.

Devices affected: All devices

Reference number: DNG-29637

Synthesis Fails When Migrating pmi_ram_dp_true from MachXO3L to MachXO4

A design originally targeting MachXO3L in Diamond (using SynplifyPro) synthesizes successfully, but after migration to Radiant for MachXO4 (using the official migration tool), synthesis fails with an error about multiple write clocks in the RAM instance.

The same synthesis tool (SynplifyPro) is used in both flows, but only Radiant reports an error.

Devices affected: MachXO4 (LFMXO4)

Reference number: DNG-31065

FIFO Empty Signal May Be Incorrect If the Clear Signal is Asserted During the First Clock Cycle on Avant Devices.

On Avant devices, if the FIFO clear signal is asserted during the first clock cycle after reset, the FIFO empty signal may not match the synthesized or Place and Route (PAR) netlist behavior. This can result in incorrect FIFO status reporting immediately after reset.

Workaround:

- Do not assert the clear signal during the first clock cycle.
- Apply the clear signal after at least one valid clock cycle has elapsed to ensure proper alignment of the FIFO empty signal.
- Verify FIFO behavior in simulation and hardware after applying this change.

Devices affected: Avant (LAV-AT)

Reference number: DNG-24704

Radiant Programmer Batch Mode May Generate an Incorrect XCF File for AS2 Boards.

When running Radiant Programmer in batch mode for AS2 boards, the generated .xcf file may be incorrect. The same project, when programmed using the GUI mode, produces the correct XCF file. This issue is specific to AS2 board configurations. Batch mode functions correctly for ES1 boards.

Workaround: Use GUI mode to generate the XCF file for AS2 boards. For automated flows, compare batch and GUI outputs and manually correct as needed.

Devices affected: Lattice Avant (LAV-AT)

Reference number: DNG-29314

LSE Resource Sharing Can Cause Mismatches Between RTL Simulation and Synthesized Behavior on Certus-NX Devices.

When using LSE synthesis with resource sharing enabled on Certus NX devices, RTL simulation may pass, but post synthesis simulation and hardware behavior may not match the RTL. This mismatch is not observed when LSE resource sharing is disabled or when using Synplify Pro for synthesis.

Workaround: Disable LSE resource sharing (set Resource Sharing to FALSE in the LSE strategy) or use Synplify Pro for synthesis.

Devices affected: Certus-NX (LFD2NX)

Reference number: DNG-30896

Place and Route Crashes During Placer Phase when DDRDLL Placement Conflicts Exist.

In Place and Route, the placer crashes without a meaningful error message during placement when IO location constraints cause multiple DDRDLL instances to be assigned to the same HPIO bank site, instead of reporting a clear constraint conflict error.

Devices affected: Lattice Avant (LAV-AT)

Reference number: DNG-33026

Internal Pin Functions Displayed in Device Constraint Editor Spreadsheet View.

In the Device Constraint Editor (DCE), internal test and manufacturing pin function names (such as MFGOUT, ATB, and scan data signals) are visible in the Dual Function column of the DCE pin spreadsheet view, exposing internal-only information that is not relevant to design use.

Workaround: Ignore the internal function names shown in the DCE GUI spreadsheet view; the exported pinout file correctly filters internal pin functions.

Devices affected: All devices

Reference number: DNG-28674