Lattice Radiant 2026.1 Software Release Notes

Welcome to Lattice Radiant® software, the complete design environment for Lattice Semiconductor Field Programmable Gate Arrays (FPGAs).

What's New in Radiant 2026.1 Software

- **Device Support**
  - Lattice Avant™ (LAV-AT)
    - G50 (-1/-2/-3) 0.82V (COM/IND) – FBG644
    - G70 (-1/-2/-3) 0.82V (COM/IND) – FBG644
    - X50 (-1/-2/-3) 0.82V (COM/IND) – FBG644
    - X70 (-1/-2/-3) 0.82V (COM/IND) – FBG644

- **Tool and Other Enhancements**

  - **EBR Timing Update for Nexus Devices –** This release introduces updated timing characterization for Embedded Block RAM (EBR) paths that may affect designs using asynchronous clocks in Dual-Port or FIFO modes without output register (non-OREG). Designs with independent read and write clocks or tight timing margins may observe changes in reported timing, including reduced slack or new timing violations in STA. Designs using synchronous clocking or OREG-enabled configurations are not impacted. Customers are recommended to re-run timing analysis with this release and, if needed, improve margin by enabling OREG or refining clock constraints for non-OREG EBR paths.

  - **Power Calculator** – Introduces the IP Summary page as part of the new IP Wizard feature. The IP Summary provides a centralized, non-editable overview of instantiated DDR-related IP blocks (DDR PHY / DDFI), allowing users to view all IP instances within a design and track associated resources and power consumption per IP. This feature is available in Estimation mode and supports DDR-related IP for Avant devices only.

  - **Programmer** – Support has been added for generating STAPL files for multiple MachXO5D devices in a JTAG daisy chain. The Deployment Tool now generates a single archive containing per-device STAPL files. This feature was first introduced in Radiant 2025.2.1.

- **Reveal**

  - The Pipeline Depth option has been added for users to configure pipelining for trigger and trace signal paths. This feature improves timing closure and enables higher sampling performance.

  - In multiple trigger capture mode, the incremental display of captured data was introduced so that users can begin analysis immediately after each trigger event. Additional trigger data continues to be captured in the background, with controls available to view subsequent trigger frames as needed.

  - When using CrossLinkU-NX (LIFCL-33U) device, access to USB23 hard IP control and status registers through the LMMI interface is now supported. This uses the same workflow as accessing and controlling other hard IP blocks in the Reveal environment.

- **Synplify Pro**

  - Synplify Pro introduces enhanced checking for register initialization on flops with asynchronous set/reset. Designs with incorrect initial values on these flops now generate a downgradable error -
    Register <reg> with asynchronous set has an initial value of 0 or
    Register <reg> with asynchronous reset has an initial value of 1

    This enhancement improves detection of reset-related issues that may not be visible in simulation but can lead to functional issues on hardware. As a result, some designs that previously passed may now report errors.

  - To address this:

    - Update the RTL to ensure correct initialization values for flops with asynchronous set/reset, or

    - Override the message in the project .prj file using: Message override -warning <error_ID>

- **Timing Analysis** – Introduces a unified Timing Analysis solution at the Tcl level, consolidating capabilities previously spread across the Post-PAR Timing Report, Timing Analyzer, Standalone Timing Analyzer, and Radiantc.
  A single set of Tcl commands now provides consistent timing constraint creation, querying, and reporting across all supported FPGA families, with improved coverage for complex SDC/PDC constraint combinations.

- **Timing Analyzer GUI** – Optimized for a more responsive interface.

- **Tcl Interface** – Runtime optimization to reduce Tcl+ compilation overhead.

Updating Projects from an Earlier Version

If you want to work on a design project created with an earlier version of Radiant software, it may be necessary to re-create some IP, per the procedures described in the following table.

These procedures adapt the project for the changes in Radiant software.

Versions	IP Regeneration Procedures				
	Avant (LAV-AT)	**MachXO4 (LFMXO4)**	**CrossLink-NX (LIFCL), Certus-N2 (LN2-CT-ES), Certus-NX (LFD2NX), Certus-NX-RT (UT24C), CertusPro-NX (LFCPNX), and CertusPro-NX-RT (UT24CP), MachXO5-NX (LFMXO5)**	**iCE40UP**	**Description**
2026.1	1D_Filter	FIFO_DC	Complex_Mult	Complex_Mult	These IP used in designs created in Radiant 2025.2.1 or earlier must be re-generated in Radiant 2026.1.
	Adder Tree	RAM_DP	FFT_Butterfly	FFT_Butterfly	
	Voltage Temperature Monitor	RAM_DP_True	FIFO	FIFO	
	CREA	RAM_DQ	FIFO_DC	FIFO_DC	
	DDRPHY	ROM	Mult_Accumulate	Mult_Accumulate	
	MIPI_DPHY	Complex_Mult	Mult_Add_Sub	Mult_Add_Sub	
	MPPHY	FFT_Butterfly	Mult_Add_Sub_Sum	Mult_Add_Sub_Sum	
	SEDC Controller	Mult_Accumulate	Multiplier	Multiplier	
	Complex_Mult	Mult_Add_Sub			
	FFT_Butterfly	Mult_Add_Sub_Sum			
	FIFO	Multiplier			
	FIFO_DC				
	Mult_Accumulate				
	Mult_Add_Sub				
	Mult_Add_Sub_Sum				
	Multiplier				

Supported Devices

Lattice Radiant software can be used with either a free license or a subscription license. The two licenses provide access to different device families.

Device Family	Free License	Subscription License
iCE40 UltraPlus (iCE40UP)	◀	◀
Lattice Avant (LAV-AT)[1]		◀

Device Family	Free License	Subscription License
CertusPro™-NX (LFCPNX)	Evaluation Mode[2]	◄
Certus-NX (LFD2NX)	◄	◄
Certus-N2 (LN2-CT-ES)		◄
MachXO4 (LFMXO4)	◄	◄
MachXO5-NX (LFMXO5-15D)[1]		◄
MachXO5-NX (LFMXO5-20TD)[1]		◄
MachXO5-NX (LFMXO5-20TDQ)[1]		◄
MachXO5-NX (LFMXO5-25)	◄	◄
MachXO5-NX (LFMXO5-100T)	Evaluation Mode[2]	◄
MachXO5-NX (LFMXO5-30TD)[1]		◄
MachXO5-NX (LFMXO5-30TDQ)[1]		◄
MachXO5-NX (LFMXO5-35)	◄	◄
MachXO5-NX (LFMXO5-35T)	Evaluation Mode[2]	◄
MachXO5-NX (LFMXO5-55T)	Evaluation Mode[2]	◄
MachXO5-NX (LFMXO5-55TD)[1]		◄
MachXO5-NX (LFMXO5-55TDQ)[1]		◄
MachXO5-NX (LFMXO5-65)	◄	◄
MachXO5-NX (LFMXO5-65T)	Evaluation Mode[2]	◄

Device Family	Free License	Subscription License
CrossLink-NX (LIFCL)	◀	◀
CrossLink-NX (LIFCL-33U)	Evaluation Mode[2]	◀
Certus-NX-RT (UT24C)	Evaluation Mode[2]	◀
CertusPro-NX-RT (UT24CP)	Evaluation Mode[2]	◀

1. To enable this device, please submit a support ticket.

2. Evaluation mode includes time-limited bitstream capability.

Support for Third-Party Synthesis and Simulator Tools

The Synopsys Synplify Pro® for Lattice synthesis and the Siemens QuestaSim® Lattice Edition simulator tools are included in the Radiant software.

- **Synopsys Synplify Pro FPGA synthesis software version X-2025.09LR-SP1**
  - Release Notes for Synplify Pro are located in ..\<*install_directory*>\radiant\2026.1\synpbase\doc\pdf. The file name is fpga_rn.pdf.
  - A full set of documents for Synplify Pro are also located in \<*install_directory*>\radiant\2026.1\synpbase\doc\pdf.

- **Siemens QuestaSim Lattice Edition 2025.2**
  - Release Notes for QuestaSim Lattice Edition are located in <install_directory>\radiant\2026.1\questasim\. The file names are RELEASE_NOTES.html or RELEASE_NOTES.txt.
  - A full set of documents for QuestaSim Lattice Edition are located in <install_directory>\radiant\2026.1\questasim\docs\pdfdocs.

- **Siemens Questa® 2022.3**
- **Cadence Xcelium® 24.03.003**

- **Synopsys VCS® U-2023.03-SP2**

Help Resources

- Online Help updated with CertusPro-NX (LFCPNX), Certus-NX (LFD2NX), MachXO4 (LFMXO4), MachXO5-NX (LFMXO5), CrossLink-NX (LIFCL), Certus-NX-RT (UT24C), CertusPro-NX-RT (UT24CP), and Lattice Avant (LAV-AT) content.
- To view the Online Help, start the Lattice Radiant software and select the 

"Getting Started" icon under Information Center.

  Note: The Firefox Snap install is not supported if you are using Ubuntu 20.04 or 18.04 to access the Radiant Help. This is a result of the snap install's inability to open local HTML pages. You may reinstall the latest version of Firefox using Apt install. For installation instructions, please refer to this guide.

System Requirements

The following shows the basic system requirements for Radiant software:

- Intel x86 64-bit or 64-bit-compatible PC
- OS Support:

64-bit OS	Radiant	Synplify Pro	QuestaSim
Windows 11	✓	✓*	✓
Red Hat Enterprise Linux 8.10	✓	✓	✓
Red Hat Enterprise Linux 9.6	✓	✓	✓
Ubuntu version 24.04 LTS	✓	✓*	✓*
Ubuntu version 22.04 LTS	✓	✓*	✓*

***Note**: The third-party tools have been tested by Lattice on the listed platforms, but the vendors do not officially support them.

- Approximately 50GB free disk space
- Computer Memory Requirement:
  - Nexus – 16GB
  - LAV-AT– 32GB Recommended for running a single project. If running multiple projects, the memory requirement will be higher.

- 1024 X 768 graphics display
- Network adapter for license and network connectivity
- A Web browser with JavaScript capability
- Acrobat Reader

Issues Fixed in this Release

The following known issues are fixed in this release. Their workarounds are no longer needed.

Missing SERDES power rails in Power Calculator for CertusNX devices in CSFBGA121 and CABGA196 packages.

Devices affected: Certus-NX (LFD2NX-28, LFD2NX-40)

Reference number: DNG-32273

The Power Calculator does not display the PCIe/SERDES power supply rails for CertusNX devices in CSFBGA121 and CABGA196 packages, resulting in understated total power estimates when PCIe lanes are used.

Radiant may crash during implementation when DCE is open.

Devices affected: Certus-NX (LFD2NX-35, LFD2NX-65)

Reference number: DNG-28678

DDR3L and LPDDR4 differential clock may not be complementary on the LFCPNX device.

When using LFCPNX devices, DDR3L and LPDDR4 memory interfaces that use a differential clock (for example CK and CK#) may show non ideal differential behavior on the clock pair. The P and N pins of the DDR clock can overlap or appear non complementary on an oscilloscope, which can cause memory interface calibration or training to fail on hardware.

Devices affected: CertusPro-NX (LFCPNX)

Reference number: DNG-29849

Installer displays version as “2025.2” instead of “2025.2.1”.

Devices affected: All devices

Reference number: DNG-31794, DNG-31796, DNG-31798

Some Avant clock powers are not calculated when using Radiant 2025.2.

The dynamic power for certain clock tree routing arcs is not properly accounted for in the Avant devices; you may notice reduced dynamic power for the clock in some of their designs.

Devices affected: Lattice Avant (LAV-AT)

Reference number: DNG-31638

The des_report_flow_status command may show incomplete status after restoring a milestone with prj_open_milestone, because it relies on session history rather than the design database.

Devices affected: All devices

Reference number: DNG-29723

DSP reset configuration in asynchronous mode can cause functional failure.

In Nexus DSP blocks, configuring the PREADD9 RESET attribute for asynchronous reset and tying the reset port to static 0 can leave the DSP multiplier output stuck at zero, causing functional failure even though timing and simulation may appear correct.

Devices affected: CrossLink-NX (LIFCL)

Reference number: DNG-30673

There is a higher latency in ODDR primitives when running with XPROP enabled.

Enabling XPROP in simulation causes higher D to Q latency through the ODDRX4DQS primitive. With XPROP enabled, the DQS output starts toggling about two memory clock cycles (about 3.75 ns at 533.33 MHz) later than expected, leading to DDR violations such as DDR_NO_DQS_TRANSITION_DURING_WR.

Devices affected: CrossLink-NX (LIFCL)

Reference number: DNG-29397

LFMXO4 FIP common user testbench uses GSR_N and fails simulation.

Customer testbenches in the common FIP folder use the GSR instance with port GSR_N. For LFMXO4 devices, the FIP expects GSRB with port GSR instead. When these common testbenches are used with LFMXO4 FIPs, simulation errors occur.

Devices affected: MachXO4 (LFMXO4)

Reference number: DNG-29490

Power Calculator report Effective Theta JA value does not match Power Calculator tool.

In this release, when User Entered Tj is used, the power calculator report shows a numeric Effective Theta JA value while the Power Calculator tool correctly shows N/A.

Devices affected: All devices

Reference number: DNG-30703

FIFO testbench instantiates wrong GSR primitive for LN2-CT devices.

For LN2-CT FIFO Foundation IP, the generated testbench instantiates GSR instead of GSRA. Depending on the compiled simulation library for the selected device, simulation may fail with a module not found error.

Devices affected: Certus-N2 (LN2-CT-ES)

Reference number: DNG-26245

MAP ignores some user IO constraints in post synthesis constraints.

When IO settings for the same port are split across multiple ldc_set_port commands, MAP constraint clean up can treat the last constraint as a duplicate and drop it. As a result, some IO settings such as PULLMODE from the top level constraint file or IP constraints are not applied, and the implemented IO configuration does not match the user constraints.

Devices affected: CrossLink-NX (LIFCL)

Reference number: DNG-31001

IO mode options are not available in Physical Designer for LFMXO4.

For LFMXO4 designs in Radiant 2025.2, IO mode options are missing in Physical Designer. IO related settings cannot be configured from Physical Designer and must be applied using constraints instead.

Devices affected: MachXO4 (LFMXO4)

Reference number: DNG-29150

Timing report critical path does not show DSP location in Device View.

In some designs, the critical path in the timing report does not highlight the DSP block in Device View because the DSP site location is not reported, so the path view cannot display the DSP instance.

Devices affected: All devices

Reference number: DNG-28388

When using Structural Verilog (.vm) in the design flow, information about the synthesis attribute black_box_pad_pin “port_list” is not available in the online help.

Devices affected: All devices

Reference number: DNG-30152

pmi_rom implementation for LFMXO4 may fail PAR with Synplify Pro.

Some LFMXO4 pmi_rom designs with large memory size or wide data width can fail place and route when synthesized with Synplify Pro, due to very high LUT4 usage instead of using EBRs.

Devices affected: MachXO4 (LFMXO4)

Reference number: DNG-29659

Power Calculator IO termination requires users to manually enter the external Rth and Vth values.

When using IO termination in Power Calculator, you must manually enter the external Rth and Vth values used in your design to ensure that power estimates are accurate.

Devices affected: Lattice Avant (LAV-AT)

Reference number: DNG-31409

When using Avant PLL IP configured with an LMMI interface, synthesis fails in Synplify Pro with an error. The issue occurs during synthesis and prevents successful compilation of the design.

Devices affected: Lattice Avant (LAV-AT)

Reference number: DNG-27611

Router report shows more “signals not completely routed” than unrouted connections.

In the IDF flow, the router summary report is inconsistent when routing fails.

Devices affected: Lattice Avant (LAV-AT)

Reference number: DNG-29810

Avant MIPI D-PHY RX: Generated SCLK clock constraint missing in STA

In Avant designs that use the MIPI D-PHY RX soft IP, the automatically generated CREATE_GENERATED_CLOCK constraint for the byte clock SCLK (ECLKDIV output) may be missing its target frequency in the Static Timing Analysis (STA) report. In the Timing Wizard/Report (TWR/SDC section), this generated-clock constraint can also appear as ignored.

Devices affected: Lattice Avant (LAV-AT)

Reference number: DNG-28873

RISCV-based initialization of the DPHY IP fails when a Reveal Controller is present in the design

Designs that include a Reveal Controller do not support RISC-V–based initialization of the DPHY IP. The DPHY initialization fails when both are present in the design.

Devices affected: CertusPro-NX (LFCPNX)

Reference number: DNG-31268

In Radiant 2025.2, the SHAREDEBRINIT=Disable setting for MachXO4 devices does not match Diamond’s behavior for MachXO3 devices.

When disabled:

- Radiant writes EBR initialization data only once in the JEDEC file.
- Diamond writes the same EBR initialization data N times where N is the number of EBRs used for initialization.

There is no functional impact on device operation because both approaches correctly initialize EBR contents.

Devices affected: MachXO4 (LFMXO4)

Reference number: DNG-30070

ECO memory initialization is not supported for LFMXO4 device.

The ECO Editor does not support memory initialization for LFMXO4 (MachXO4) devices. This feature, which is available for other device families, has not yet been implemented for MachXO4. The ECO_MEM information is not present in the post-synthesis UDB for this device family.

Devices affected: MachXO4 (LFMXO4)

Reference number: DNG-29952

IOs are missing in the Physical Designer Placement Mode.

Devices affected: MachXO4 (LFMXO4)

Reference number: DNG-29369

Radiant may crash in very rare cases during implementation when Pre-synthesis Constraints Editor is open.

Devices affected: Lattice Avant (LAV-AT)

Reference number: DNG-29819

Timing analysis and the Tcl command “sta_get_slack -worst” may return different worst slack values.

The command may return a slack value, but it might not be the worst-case slack. The returned slack is valid, but it corresponds to a path that does not represent the worst slack.

In addition, the detailed timing report may contain some arrival values that are incorrect. However, the path of the report, the delays of the connections and arcs along the path, the required value, the arrival value used for slack computation, and the slack of the path are all correct.

Device affected: All devices

Reference number: DNG-27408

LRAM_DP_TRUE simulations may fail on Certus NX devices when “Invoke qrun” is enabled.

For Certus NX devices, enabling Invoke qrun during LRAM_DP_TRUE simulation may result in incorrect read data, error detection becoming stuck, or inconsistent memory initialization behavior.

Devices affected: Certus-NX (LFD2NX)

Reference number: DNG-31309

LFMXO5-55TDQ device missing from primitive templates

The LFMXO5-55TDQ device is not listed in the Primitive Templates (Verilog/VHDL), preventing users from selecting it when generating primitive examples. This affects only the template-generation UI; the device can still be used normally when set in project settings.

Devices affected: MachXO5-NX (LFMXO5-55TDQ)

Reference number: DNG-27155

The BLTS indicator in Reveal Analyzer may be misleading for DDR frequencies at or below 800 MHz.

In the Reveal Analyzer, the BLTS (Built-in Logic Training Sequence) radio button is enabled only for DDR frequencies at or above 933 MHz. For DDR frequencies of 800 MHz and below, the BLTS radio button remains red, which may incorrectly suggest a training failure. In addition, the Calibration Margin Report displays a value of 0 for these lower frequencies, which can be confusing.

Devices affected: Avant (LAV-AT)

Reference number: DNG-26340

Netlist Viewer may display incorrect or disconnected timing paths when cross probing from Timing Analysis.

In Radiant 2025.2, when viewing timing paths in the Netlist Viewer by cross-probing from the Timing Analysis report, the displayed paths may be incorrect or appear disconnected. This affects the visual representation of timing paths in the Netlist Viewer only.

Devices affected: All devices

Reference number: DNG-29138

You may encounter intermittent LSE timing analysis failure for some designs.

Some designs targeting LFD2NX can fail intermittently during LSE timing analysis with Done error code 1. The failure is observed in approximately half of synthesis runs while resource usage and results appear identical between passing and failing runs.

Devices affected: Certus-NX (LFD2NX)

Reference number: DNG-31070

Synthesis fails with CPE segmentation violation when SentinelOne AV is active.

Synthesis may fail for both LSE and Synplify Pro with a CPE segmentation violation or synthesis.exe crash. The issue occurs only on machines where SentinelOne antivirus is active; the same designs complete synthesis successfully on systems without SentinelOne.

Devices affected: All devices

Reference number: DNG-31178

Timing Analyzer ignores the Maximum Slack limit set by the user and displays all slacks. The display also has a mismatch in the units between Timing option setting and General information in the GUI.

This is a GUI issue and not a functional issue

Devices affected: All devices

Reference number: DNG-29930

Timing violations may be reported when the sync_clk_i of the GDDR 7:1 Foundation IP is driven by the PLL IP clock.

The affected path is used only for clock synchronization reset and not for data transfer. The transition occurs only during the initialization sequence and does not occur during normal TX operation.

Devices affected: CertusPro-NX (LFCPNX)

Reference number: DNG-31095

PROGRAMN pin cannot be used as GPIO on LIFCL-33U.

On the LIFCL-33U device, the sysConfig setting PROGRAMN_PORT = DISABLE is not supported. The PROGRAMN pin is always enabled via OTP and cannot be repurposed as a general-purpose I/O. Designs that attempt to set PROGRAMN_PORT = DISABLE will fail DRC.

Devices affected: CrossLink-NX (LIFCL-33U)

Reference number: DNG-28738

Internal device name is visible in DCE device part view.

Devices affected: MachXO4 (LFMXO4-015HE, LFMXO4-015HC, LFMXO4-050HC and LFMXO4-050HE) with specific packages (BFG256, BBG256 and BBG400)

Reference number: DNG-29144

Hold time violations may be observed on EtherCAT IP paths in Radiant, blocking timing closure.

A design originally targeting MachXO3L and synthesizing successfully in Diamond using Synplify Pro may exhibit hold time violations when migrated to Radiant and implemented on CertusPro-NX devices using an EtherCAT IP. Hold violations are observed on EtherCAT IP paths even after following recommended constraint migration steps, including copying PDC constraints to SDC and verifying hierarchical paths. Resource utilization is comparable to reference designs, but the hold violations persist and prevent timing closure.

Devices affected: CertusPro-NX (LFCPNX)

Reference number: DNG-31302

The sta_get_paths command reports a bad flag error when using the -endpoints or -summary options.

Using the sta_get_paths command with the -endpoints or -summary options, for example sta_get_paths -summary or sta_get_paths -pins -endpoints, results in a bad flag error instead of valid output.

Devices affected: CrossLink-NX (LIFCL)

Reference number: DNG-31049

Known Issues for Radiant 2026.1

To view the complete list of known issues, refer to the Lattice Radiant Software Known Issues document. For further assistance, please contact Lattice Technical Support.