



# Watchdog Timer IP

IP Version: v1.6.1

## Release Notes

FPGA-RN-02024-1.0

June 2026

## Disclaimers

Lattice makes no warranty, representation, or guarantee regarding the accuracy of information contained in this document or the suitability of its products for any particular purpose. All information herein is provided AS IS, with all faults, and all associated risk is the responsibility entirely of the Buyer. The information provided herein is for informational purposes only and may contain technical inaccuracies or omissions, and may be otherwise rendered inaccurate for many reasons, and Lattice assumes no obligation to update or otherwise correct or revise this information. Products sold by Lattice have been subject to limited testing and it is the Buyer's responsibility to independently determine the suitability of any products and to test and verify the same. LATTICE PRODUCTS AND SERVICES ARE NOT DESIGNED, MANUFACTURED, OR TESTED FOR USE IN LIFE OR SAFETY CRITICAL SYSTEMS, HAZARDOUS ENVIRONMENTS, OR ANY OTHER ENVIRONMENTS REQUIRING FAIL-SAFE PERFORMANCE, INCLUDING ANY APPLICATION IN WHICH THE FAILURE OF THE PRODUCT OR SERVICE COULD LEAD TO DEATH, PERSONAL INJURY, SEVERE PROPERTY DAMAGE OR ENVIRONMENTAL HARM (COLLECTIVELY, "HIGH-RISK USES"). FURTHER, BUYER MUST TAKE PRUDENT STEPS TO PROTECT AGAINST PRODUCT AND SERVICE FAILURES, INCLUDING PROVIDING APPROPRIATE REDUNDANCIES, FAIL-SAFE FEATURES, AND/OR SHUT-DOWN MECHANISMS. LATTICE EXPRESSLY DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY OF FITNESS OF THE PRODUCTS OR SERVICES FOR HIGH-RISK USES. The information provided in this document is proprietary to Lattice Semiconductor, and Lattice reserves the right to make any changes to the information in this document or to any products at any time without notice.

## Inclusive Language

This document was created consistent with Lattice Semiconductor's inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice's inclusive language [FAQ 6878](#) for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

# Contents

|  |   |
|--|---|
| Contents .....                           | 3 |
| 1. Introduction .....                    | 4 |
| Watchdog Timer IP v1.6.1 .....           | 4 |
| Watchdog Timer IP Earlier Versions ..... | 4 |
| References .....                         | 5 |
| Technical Support Assistance .....       | 6 |

# 1. Introduction

This document contains the Release Notes for the Watchdog Timer IP. For specific details about the IP, refer to the following:

- [Watchdog Timer IP User Guide \(FPGA-IPUG-02097\)](#)

## Watchdog Timer IP v1.6.1

| Software         | Software Version | Summary of Changes  |
|------------------|------------------|---|
| Lattice Radiant™ | 2026.1           | <ul style="list-style-type: none"> <li>• Updated the testbench GSR instance.</li> <li>• Updated the constraint file to include device-specific clock frequency constraints when operating in Cycle mode.</li> <li>• Aligned <i>memory_map.xml</i> with the latest RTL and documentation updates.</li> </ul> |

## Watchdog Timer IP Earlier Versions

| IP Version | Summary of Changes   |
|------------|--|
| 1.6.0      | <ul style="list-style-type: none"> <li>• Updated registers: <ul style="list-style-type: none"> <li>• Removed the reset register.</li> <li>• Corrected the timer bit width.</li> <li>• Removed the option to disable the non-maskable warm boot reset interrupt (<i>nmi_o</i>).</li> </ul> </li> <li>• Fixed issues related to APB access.</li> </ul> |
| 1.5.1      | Updated the <i>int_o</i> port to operate as a bus when in APB mode.  |
| 1.5.0      | Updated <i>memory_map.xml</i> to fix the Propel SGE generation.  |
| 1.4.0      | Updated the testbench GSR instance. Added an APB interface.  |
| 1.3.0      | Updated the IP to support all devices.   |
| 1.2.0      | Added support for CertusPro™-NX devices.   |
| 1.1.0      | Added support for Certus™-NX devices.  |
| 1.0.0      | Initial release.   |

## References

- [Watchdog Timer IP User Guide \(FPGA-IPUG-02097\)](#)
- [Avant-E web page](#)
- [Avant-G web page](#)
- [Avant-X web page](#)
- [Certus-N2 web page](#)
- [Certus-NX web page](#)
- [CertusPro-NX web page](#)
- [CrossLink-NX web page](#)
- [MachXO5-NX web page](#)
- [Watchdog Timer IP Core web page](#)
- [Lattice Radiant Software web page](#)
- [Lattice Propel Design Environment web page](#)
- [Lattice Solutions IP Cores web page](#)
- [Lattice Solutions Reference Designs web page](#)
- [Lattice Insights web page for Lattice Semiconductor training courses and learning plans](#)

## Technical Support Assistance

Submit a technical support case through [www.latticesemi.com/techsupport](http://www.latticesemi.com/techsupport).

For frequently asked questions, refer to the Lattice Answer Database at [www.latticesemi.com/Support/AnswerDatabase](http://www.latticesemi.com/Support/AnswerDatabase).



[www.latticesemi.com](http://www.latticesemi.com)