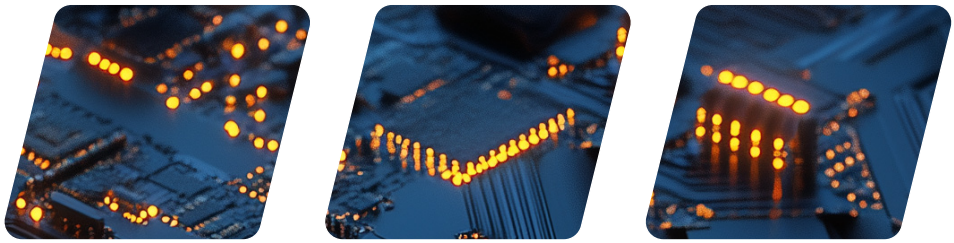
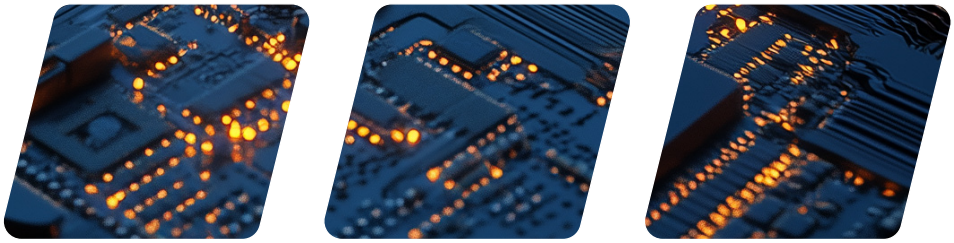


Lattice Nexus™ FPGA Platform: Harnessing FD-SOI Technology for Radiation Tolerance



White Paper

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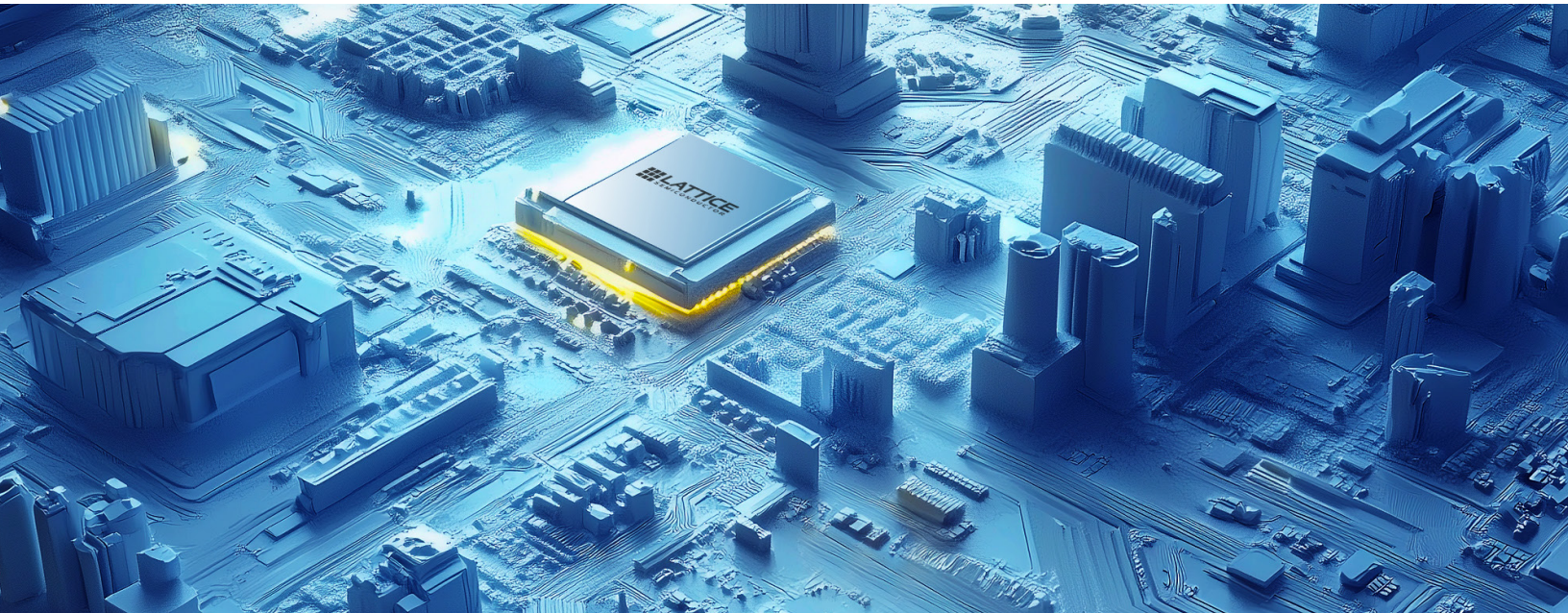
ABSTRACT

As space, aerospace, and medical systems become more intelligent and connected, designers face increasing challenges from radiation-induced failures, rising power constraints, and long product lifecycles in mission-critical environments. Soft errors, single-event effects, and system-level reliability risks can compromise performance and safety, especially in compact, power-limited designs that require autonomous operation and minimal intervention. To address these challenges, this white paper explores how the Lattice Nexus FPGA platform leverages 28 nm fully depleted silicon-on-insulator (FD-SOI) technology to deliver industry-leading radiation tolerance and reliability. FD-SOI inherently reduces radiation-induced charge collection, achieving more than 100X lower soft error rates (SER) than bulk complementary metal-oxide-semiconductor (CMOS) and eliminating single-event latch-up (SEL) by design.



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Introduction

As electronic systems are increasingly deployed in radiation-prone environments such as space, aerospace, and medical applications, designers face a growing set of challenges that extend beyond traditional reliability concerns. Radiation-induced soft errors, single-event effects, and latch-up can compromise system integrity, increase operational risk, and drive costly mitigation strategies at the system level. At the same time, modern designs must meet strict constraints on power consumption, size, weight, and long-term availability, often while operating autonomously for extended periods with minimal opportunity for intervention. These competing demands place significant pressure on conventional FPGA technologies, which struggle to balance radiation tolerance, efficiency, and lifecycle stability in mission-critical applications.

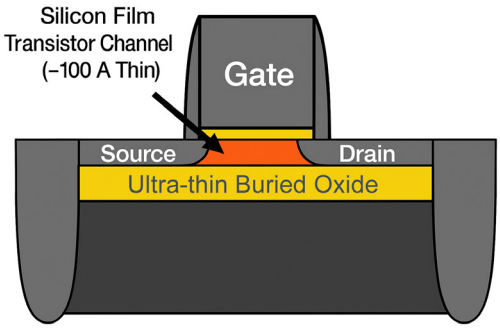
A Balanced FPGA Architecture for Radiation Tolerance, Power Efficiency, and Longevity

The Lattice Nexus FPGA platform addresses these challenges through a purpose-built architecture based on 28 nm FD-SOI technology. FD-SOI inherently reduces radiation-induced charge collection, delivering more than 100X lower soft error rates (SER) than bulk CMOS and eliminating single-event latch-up by design. To further enhance resilience, Nexus FPGAs integrate hardened memory scrubbing, error-correcting code (ECC), and support for triple modular redundancy (TMR), enabling autonomous error correction with minimal system-level intervention. Beyond radiation tolerance, the Nexus platform delivers ultra-low power consumption, compact form factors, high I/O density, advanced security features, and long-term product availability. Together with proven space heritage, these capabilities make Lattice Nexus FPGAs a well-balanced, radiation-tolerant small FPGA solution for modern high-reliability systems.

FD-SOI Advantages in Radiation-Prone Environments

Commercial FD-SOI technology incorporates a thin insulating layer that electrically isolates the transistor channel from the underlying substrate. This isolation significantly reduces sensitivity to substrate noise and radiation-induced charge collection, resulting in more stable and predictable device behavior. As a result, FD-SOI delivers enhanced resilience and reliability in radiation-prone environments, including space, high-altitude, and medical applications. See Figure 1.

Figure 1: FD-SOI Technology with an Ultra-thin Buried Oxide Layer



Demonstrated Radiation Performance

The Lattice Nexus FPGA platform delivers low soft error rates, making it well suited for mission-critical systems. Its FD-SOI technology, combined with robust design practices, enables reliable operation under radiation exposure without sacrificing performance. The FD-SOI substrate significantly reduces charge collection, achieving more than a 100X lower SER compared to bulk CMOS alternatives while preventing latch-up risk altogether.

Single Event Latch-up Immunity

Lattice FPGA-based field-oriented control (FOC) solutions deliver real-time performance with flexible scalability and seamless system integration. These capabilities enable precise motor control, support multiple channels, and simplify connectivity across a wide range of interfaces and protocols. See Table 1.

Table 1: Parameters of the Lattice CertusPro™-NX FPGA Based on the Lattice Nexus Platform

Parameter	Description	Lattice CertusPro-NX (28nm)	Units
SEL	Heavy Ion Single Event Latch-up Immunity	80	MeV-cm²/mg
SEU CRAM	Single Event Upset in Configuration RAM	2.5E-8	Events/bit/day[1]
Neutron SER	High Energy and Thermal Neutron	3.4	Fit/Mb

Single Event Effects Performance

When exposed to heavy ions, the FD-SOI technology in Lattice Nexus reduces the likelihood of single event upsets (SEUs). As a result, single event effects (SEE) occur only at higher radiation levels than in bulk CMOS FPGAs, with no single event functional interrupt (SEFI) observed up to a linear energy transfer (LET) of 80 MeV-cm²/mg.

Built-In Hardened Scrubber, Error Emulation, and TMR Capabilities

Lattice Nexus FPGAs include a hardened memory scrubber that continuously corrects configuration memory upsets and applies error-correcting code across all user memory to maintain data integrity during operation. The platform also supports triple modular redundancy for applications requiring the highest levels of reliability and resilience. Lattice provides utilities to emulate error injection and recovery scenarios. Continuous on-chip scrubbing repairs any flipped configuration bit within 5 ms or less, resulting in fewer than one manual intervention per device-year in geosynchronous orbit (GEO), typically through partial or full reprogramming of the configuration memory.

System-level Implications

Lattice Nexus FPGAs deliver clear system-level benefits that reduce complexity, improve reliability, and optimize size, weight, power, and cost (SWaP-C) for mission-critical designs:

- Longer autonomous uptime: Virtually eliminates most in-orbit scrubbing cycles and reset events
- Simpler designs: No configuration supervisor, SEL clamps, or complex power sequencing required
- Ample radiation margin: Reduces the need for shielding, system-level redundancy, and additional mitigation
- Optimized SWaP-C: Less than 100 mW static power and small package options suit satellites, avionics, and missile platforms

In modern electronic systems, performance depends on more than reliability and radiation tolerance alone. Designers must also balance power consumption, form factor, I/O density, security, and long-term availability to reduce system cost and complexity. Lattice Nexus FPGAs address these requirements with ultra-low power operation, compact packaging, high integration, and robust security features, making them well suited for space-constrained, thermally limited, and mission-critical applications.

Key System-level Efficiency Drivers

Designing efficient systems requires more than raw performance. Power consumption, form factor, security, and long-term availability all play a decisive role in determining system cost, reliability, and scalability. The following system-level efficiency drivers highlight how Lattice Nexus FPGAs address these requirements, enabling designers to reduce complexity, optimize resources, and deliver resilient solutions.

1. Power Consumption

Power is a major cost driver, particularly in thermally constrained environments such as edge devices, aerospace systems, and portable electronics. Higher power consumption increases cooling requirements and drives up operational costs.

- **Lattice Nexus Advantage**
  - Up to 4X lower power compared to competing FPGAs
  - Enables passive cooling and reduced energy costs

2. Form Factor and I/O Density

In compact systems, board space is limited. High I/O density in small packages allows designers to add functionality without increasing system footprint.

- **Lattice Nexus Advantage**
  - Small-footprint packages with high I/O counts
  - On-chip flash integration reduces external components, simplifies design, and lowers BOM cost

3. Security Integration

Security is essential for protecting data and system operation. Hardware-based security features provide a strong foundation for system-level protection.

- **Lattice Nexus Advantage:**
  - Hardware Root of Trust and dual-boot support
  - Support for advanced cryptographic algorithms
  - Faster and more secure boot through optional integrated flash

4. Product Longevity

Frequent product discontinuations can drive costly redesigns, requalification efforts, and supply chain disruptions. Long-term availability is essential for industrial, aerospace, and defense applications that must remain in service for many years.

- **Lattice Nexus Advantage:**
  - Decades-long product availability
  - Strategic lifecycle management that helps avoid premature end-of-life scenarios

Summary

By combining 28 nm fully depleted silicon-on-insulator technology, a hardened SEU detect and correct scrubber, a low-power architecture, and proven TRL-9 space heritage demonstrated through multiple launches in the United States and Europe, Lattice Nexus FPGAs deliver the most balanced radiation-tolerant small FPGA platform available on the market as a commercial off-the-shelf solution.

Reference

Lattice Nexus Platform Webpage https://www.latticesemi.com/en/LatticeNexus

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To learn more about Lattice low power FPGA-based solutions for industrial, automotive, communications, computing, and consumer applications, visit **www.latticesemi.com** or contact us at **www.latticesemi.com/contact** or **www.latticesemi.com/buy**.

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