DC-SCM LTPI IP (New Architecture)

IP Version: v.3.0.0

User Guide

FPGA-IPUG-02312-1.0

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This document was created consistent with Lattice Semiconductor’s inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice’s inclusive language FAQ 6878 for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

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Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviation	Definition
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
AXIL	Advanced eXtensible Interface – Lite
BMC	Board Management Controller
CDC	Clock Domain Crossing
CFG	Configuration
CPLD	Complex Programmable Logic Device
CSR	Control and Status Register
CRC	Cyclic Redundancy Check
CTR	Controller
DC-SCI	Datacenter-ready Secure Control Interface
DC-SCM	Datacenter-ready Secure Control Module
DDR	Dual Data Rate
DUA	Dual Function
EFB	Embedded Function Block
FIFO	First In First Out
FPGA	Field Programmable Gate Array
FSM	Finite State Machine
GDDR	Graphics Dual Data Rate
GPIO	General Purpose Input/Output
HPM	Host Processor Module
I2C	Inter-Integrated Circuit
IP	Intellectual Property
LL	Low Latency
LTPI	LVDS Tunneling Protocol and Interface
LUT	Look-up Table
LVDS	Low Voltage Differential Signaling
MMAP	Memory Map
NL	Normal Latency
OCP	Open Compute Project
OEM	Original Equipment Manufacturer
PLL	Phase-Locked Loop
Rx	Receiver
RWC	Read, Write Clear
SDR	Single Data Rate
SGPIO	Serial General Purpose Input/Output
TDM	Time Division Multiplexing
TGT	Target
Tx	Transmitter
UART	Universal Asynchronous Receiver/Transmitter

1. Introduction

1.1. Overview of the IP

The Lattice Semiconductor DC-SCM LTPI IP Core is a solution compatible with Open Computer Project (OCP) Data Center – Secure Control Module (DC-SCM) Standards in the DC-SCM 2.1 Specification. DC-SCM moves common management, security, and control features from a typical motherboard into a module designed in different form factors, including horizontal and vertical aspects. The basic idea is to enable a common security and management module form and interface that can be used across datacenter platforms. From a data center perspective, DC-SCM enables common management and security to be deployed across a higher percentage of platforms. It also enables the deployment of management and security upgrades on platforms within a generation without redesigning more complex components. From a development perspective, this enables solution providers to remove customer-specific solutions from more complex components, such as motherboards. This enables greater leverage of higher complexity components across platforms. This DC-SCM LTPI IP is OCP Ready™.

LVDS Tunneling Protocol and Interface (LTPI) is a protocol and interface designed for tunneling various low-speed signals between Host Processor Module (HPM) and SCM. The LTPI protocol operates over the Low Voltage Differential Signaling (LVDS) electrical interfaces, which are widely supported by Complex Programmable Logic Devices (CPLDs) and FPGAs. LTPI is the next generation protocol for DC-SCM 2.1, as the replacement for two Serial GPIO (SGPIO) interfaces. The LVDS interface provides higher bandwidth and better scalability than the SGPIO interface. LTPI allows the tunneling of not only GPIOs but also low-speed serial interfaces, such as I2C and UART. It is also extensible with additional proprietary OEM interfaces and provides support for raw data tunneling between HPM CPLD and SCM CPLD. Also, the DC-SCM LTPI IP offers a solution for minimal wire connection between two FPGAs, enabling TDM-based bidirectional communication by aggregating multiple data, including I2C, GPIO, and UART. This adds more flexibility to a customer's system and board design.

Dual-Node LTPI is a new architecture in which one SCM is connected to two HPMs. On the SCM side, there is only one IP that has two sets of channels, each of which connects to one HPM. One combined SCM can save resources by sharing resources.

1.2. Quick Facts

Table 1.1 presents a summary of the DC-SCM LTPI IP.

Table 1.1. DC-SCM LTPI IP Quick Facts

IP Requirements	Supported FPGA Families	MachXO3L™, MachXO3LF™, MachXO3D™, Mach™-NX, and MachXO5™-NX
Resource Utilization	Supported User Interface	GPIO, I2C, UART, OEM, Data to LVDS and vice versa
	Resources	See Table A.1.
Design Tool Support	Lattice Implementation	IP Core Version 3.0.0 – Lattice Diamond™ Software 3.14, Lattice Propel™ Builder Software 2025.2, Lattice Radiant™ Software 2025.2
	Synthesis	Lattice Synthesis Engine
		Synopsys® Synplify Pro® for Lattice
	Simulation	For a list of supported simulators, see the Lattice Diamond software and Lattice Radiant software user guides.

1.3. Features

The key features of the DC-SCM LTPI IP include:

- Compliant with OCP DC-SCM 2.1 LTPI 1.1 Specifications
- Link initialization, discovery, and negotiation
- Supports Multi-Channel Serial Interface.
- Supports up to five channels aggregation or disaggregation, including I2C, UART, GPIO, Data, and OEM.
- Supports GPIO, I2C, UART, OEM, and Data channel aggregation.
- For the I2C interface, each channel can be configured as a controller, a target, or switched dynamically between a controller or target.
- Supports up to 800 Mbps Dual Data Rate (DDR) LVDS data rate for MachXO3L, MachXO3LF, MachXO3D, and Mach-NX devices.
- Supports AMBA 3 APB Protocol v1.0 for register access of the soft IP and data channel.
- Supports OEM frames.
  - Channels quantities are configurable.
  - Channels sequence is configurable.
  - Capability type and content are configurable.

1.4. Licensing and Ordering Information

The DC-SCM LTPI IP is provided at no additional cost with the Lattice Diamond, Lattice Radiant, and Propel Builder software. The IP can be fully evaluated in hardware without requiring an IP license string.

1.5. Naming Conventions

1.5.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.5.2. Signal Names

Signal names that end with:

- _n are active low, asserted when value is logic 0.
- _i are input signals.
- _o are output signals.
- _io are bidirectional signals.

2. Functional Descriptions

2.1. IP Architecture Overview

A high-level block diagram of DC-SCM LTPI IP is shown in Figure 2.1. Data received from external channels are aggregated and transmitted from the SCM side to HPM0 or HPM1 through LVDS. Data received from HPMs is de-aggregated and remapped to external channels.

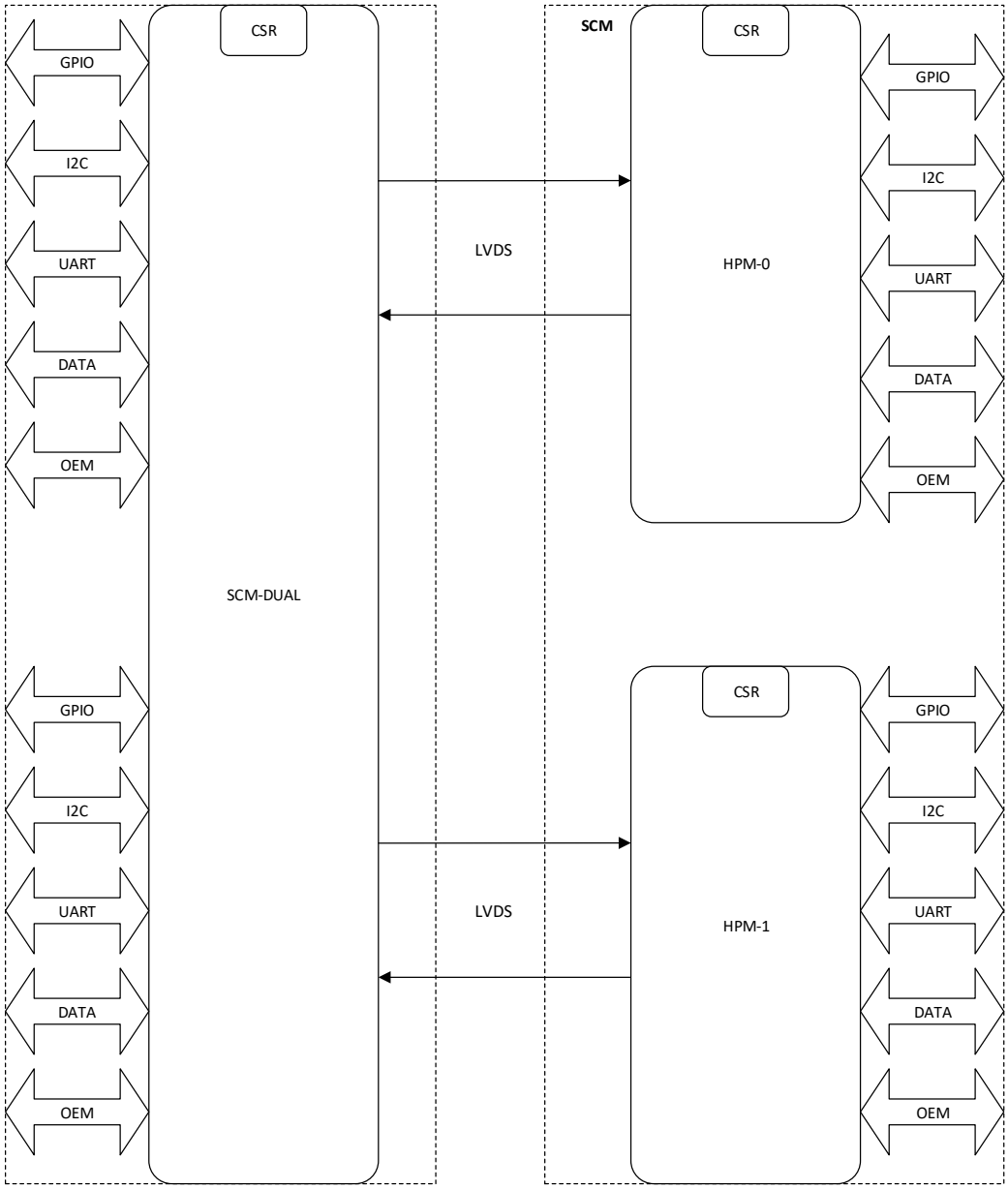

Figure 2.1. High-level Block Diagram of DC-SCM LTPI Connection

The functional block diagram of the DC-SCM LTPI IP set as either SCM or HPM is shown in Figure 2.2.

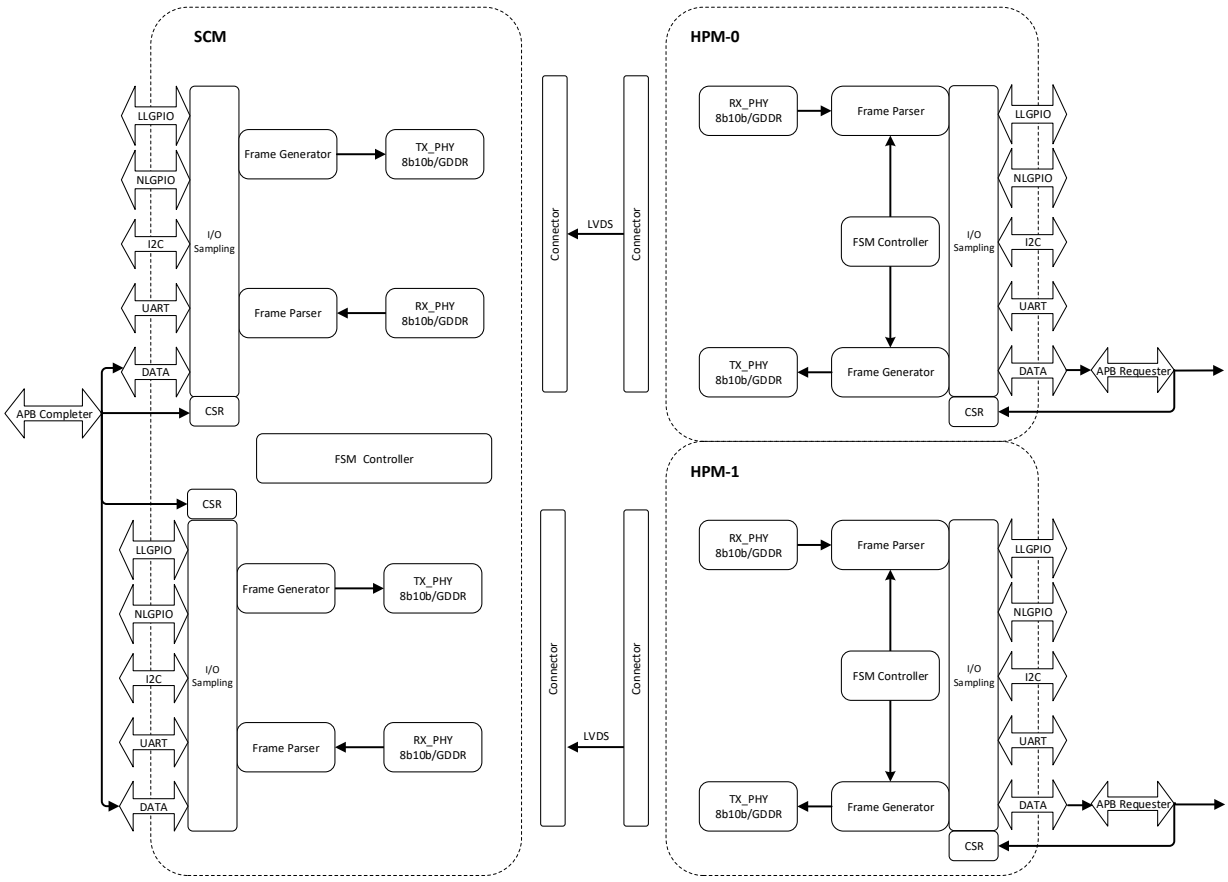

Figure 2.2. Functional Block Diagram of DC-SCM LTPI

DC-SCM LTPI IP consists of I/O sampling, FSM controller, Frame Generator/Parser, 8b/10b Encoder/Decoder, and Graphics Dual Data Rate (GDDR) Transmit and Receive modules. An instance of this IP has both Rx and Tx paths available that can work simultaneously.

Data received from the user side are considered valid data streams for transmission. Payload within frames received is considered valid. Data channel and control and status register (CSR) are memory mapped on the APB completer bus interface on the SCM side, while the data channel is on the APB requestor bus interface on the HPM side. CSR is one target of this bus. Other targets can also be connected to this APB requestor outside the IP. This allows the outside host, such as the CPU on the SCM side, to access the memory mapped peripheral on the HPM side through the data bus.

2.2. Clocking

Below is the list of clocks used by the IP. Figure 2.3 shows the general clock topology.

- A system clock, clk_i, is used to clock the whole core logic. It is kept as a constant value in the system design. This clock is also used to clock the write operation of Tx FIFO and read operation of the Rx FIFO.
- The edge clock, eclk_i, and 90-degree phase shifted edge clock (eclk90_i) are clocks used by the GDDR Tx soft IPs for gear-related processing. These clocks must be source synchronous, with frequency equivalent to the target LVDS PHY frequency. All Clock Domain Crossing (CDC) transfers in the DDR domain are already handled by the hard IPs instantiated to implement the DDR clock tree.
- GDDR Rx generates the core clock sclk based on the received LVDS Rx clock from LTPI. All CDC transfers in the DDR domain are already handled by the hard IPs instantiated to implement the DDR clock tree.
- Both DDR Tx and Rx blocks generate the core clock sclk that is used to clock the read operation of the internal Tx FIFO and write operation of the internal Rx FIFO respectively. Frequency of SCLK is dependent on the LVDS PHY mode and DDR gearing used.

- It is assumed that external channels are operating at much lower frequencies compared to the operating system clock of the IP.

The timing constraint should be added for ECLK0/ECLK90. It is recommended to constrain them to the maximum frequency.

2.2.1. Clocking Overview

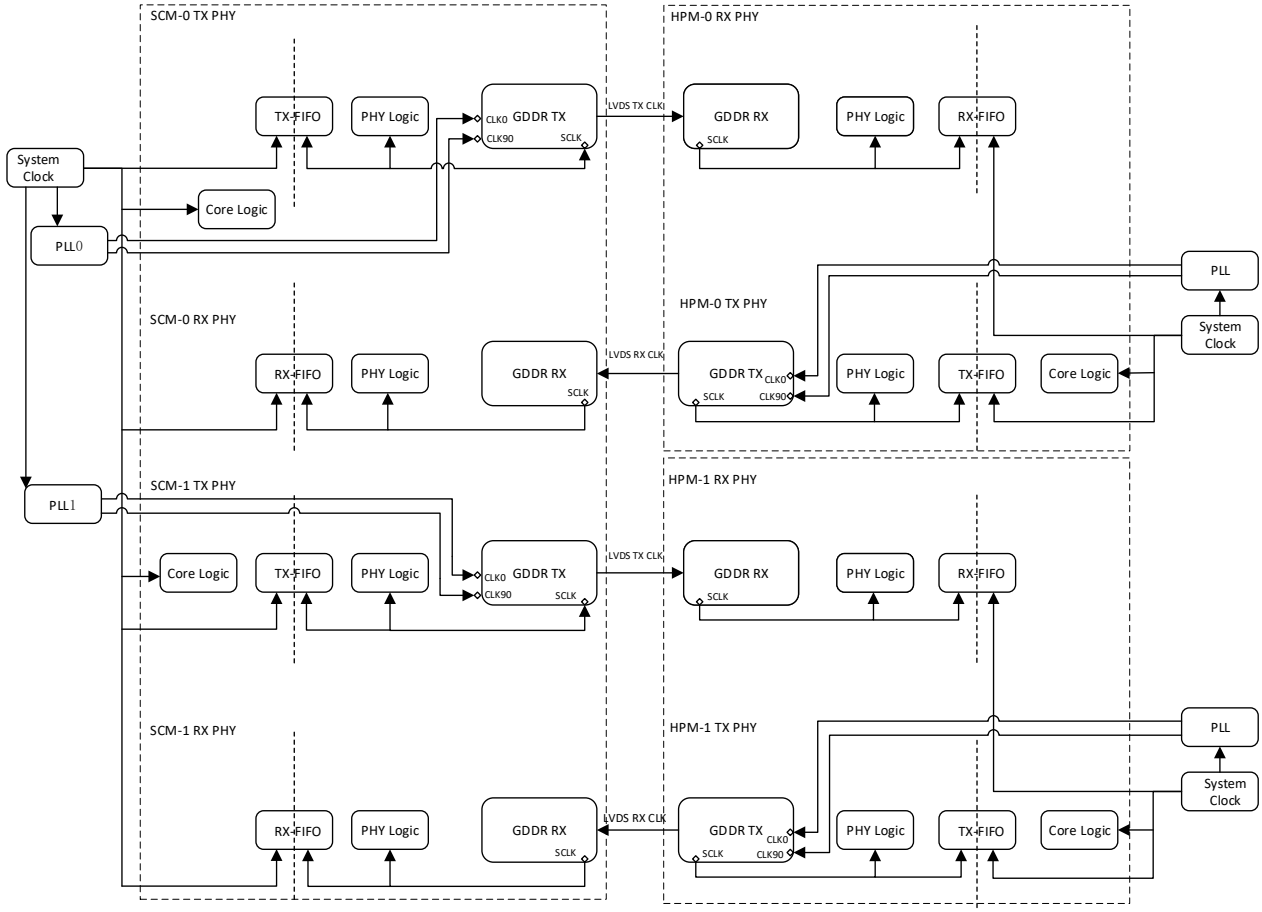

Figure 2.3. System Clock Domain Block Diagram

2.3. Reset

rstn_i , the asynchronous active low reset with synchronous release, is implemented as the system reset of the IP. It is recommended to implement a reset synchronizer circuit in the high-level system design when this IP is used. rstn_i must be synchronized to the input system clock, clk_i.

3. IP Parameter Description

3.1. General

The configurable attributes of the DC-SCM LTPI IP Core are listed and described in Table 3.1. The attributes can be configured through the IP Catalog's Module/IP wizard of the Lattice Propel Builder software or Lattice Radiant software.

Table 3.1. Attributes

Attribute	Selectable Values	Default	Description
General			
Node Number	1, 2	1	Selects the number of LTPI as single node or Dual-Node.
Bus Mode	APB, AXIL	APB	Selects the system bus interface. This version of the IP does not support AXIL yet.
IP Mode	SCM, HPM	SCM	Selects the general function of this IP.
PLL Selection	External, Internal	External	Selects PLL as inside or outside of this IP.
System Frequency	20–100 MHz	50	System frequency for clock signals, such as clk_i and pll_clk_i. System clock frequency and LVDS frequency should be balanced. If not, the GUI shows a warning message: WARNING -- The system frequency and LVDS frequency are not balanced, data frames may be lost. To keep a balance, ensure: System clock frequency >= LVDS frequency*(2 if DDR or 1 if SDR)/(10 if XO5 or 8 if XO3)
LTPI Platform ID	0x[0000–FFFF]	0x4c53 (ASCII:LS)	The initial value of LTPI Platform ID Local in CSR.
OCP LTPI Version	—	Ver1.0 Rev1.2	OCP specification version and revision
Optionality 0/1 (SCM0/1)			
LTPI Frame Type	Default_I/O, OEM_I/O:0, OEM_I/O:1	Default_I/O	Selects the LTPI frame type as default or user-defined.
Auto Move to CFG State	Checked, Unchecked	Checked	Selects whether the control link state machine moves to the configure state automatically or not.
Resource Optimization	Checked, Unchecked	Checked	Selects whether to disable counters in CSR or not to save the LUT resource.
IO Type	LVDS, SubLVDS	LVDS	Only selectable with MachXO5-NX devices. This attribute is to set the I/O standard.
TX ECLK vs DATA	ALIGN, CENTER	CENTER	Selects LVDS phase relation of the TX channel clock and data.
RX ECLK vs DATA	ALIGN, CENTER	CENTER	Selects LVDS phase relation of the RX channel clock and data.
Capabilities			
DDR Mode 0/1			
Dual-Data Rate (DDR)	Checked, Unchecked	Checked	Enables link speed rate DDR when checked, or SDR when unchecked.
Speed Capability 0/1			
X1 (25 MHz)	Checked, Unchecked	Checked	Not editable. Supported by default.
X2 (50 MHz)	Checked, Unchecked	Unchecked	The maximum link speed is 50 MHz.
X3 (75 MHz)	Checked, Unchecked	Unchecked	The maximum link speed is 75 MHz.

Attribute	Selectable Values	Default	Description
X4 (100 MHz)	Checked, Unchecked	Unchecked	The maximum link speed is 100 MHz.
X6 (150 MHz)	Checked, Unchecked	Unchecked	The maximum link speed is 150 MHz.
X8 (200 MHz)	Checked, Unchecked	Unchecked	The maximum link speed is 200 MHz.
X10 (250 MHz)	Checked, Unchecked	Unchecked	The maximum speed is 250 MHz.
X12 (300 MHz)	Checked, Unchecked	Unchecked	The maximum link speed is 300 MHz.
X16 (400 MHz)	Checked, Unchecked	Unchecked	The maximum link speed is 400 MHz.
X24 (600 MHz)	Checked, Unchecked	Unchecked	The maximum link speed is 600 MHz. This speed capability only supports the Lattice Nexus platform.
X32 (800 MHz)	Checked, Unchecked	Unchecked	Not editable. Not supported.
X40 (1000 MHz)	Checked, Unchecked	Unchecked	Not editable. Not supported.
Capability Type 0/1 (SCM0/1)			
Capability Type	8'h[00, 81–FF]	8'h00	Depends on LTPI Frame Type. • The value is 8'h00 if LTPI Frame Type is Default_I/O. • The value is 8'h81 if LTPI Frame Type is OEM_I/O:0. • The value is 8'h[82-FF] if LTPI Frame Type is OEM_I/O:1.
Capability Byte 0: Supported Channels	Depends on channel configuration.	Depends on channel configuration.	LTPI Frame Type = Default_I/O or OEM_I/O:0
Capability Byte 1–2: NL GPIO Number			LTPI Frame Type = Default_I/O or OEM_I/O:0
Capability Byte 3: UART Capabilities			LTPI Frame Type = OEM_I/O:0
Capability Byte 3: I2C Channels On-Off			LTPI Frame Type = Default_I/O
Capability Byte 4: I2C Speed Mode			LTPI Frame Type = Default_I/O
Capability Byte 5: UART Capabilities			LTPI Frame Type = Default_I/O
Capability Byte 6: OEM Capability 0			LTPI Frame Type = Default_I/O
Capability Byte 4–6: I2C Speed Mode			LTPI Frame Type = OEM_I/O:0
Capability Byte 7: OEM Capability 0			LTPI Frame Type = OEM_I/O:0
Capability Byte 7: OEM Capability 1			LTPI Frame Type = Default_I/O
Def IO Capability: Final Capability Value			LTPI Frame Type = Default_I/O
OEM IO 0 Capability: Final Capability Value			LTPI Frame Type = OEM_I/O:0
OEM IO 1 Capability: Final Capability Value			LTPI Frame Type = OEM_I/O:1

Attribute	Selectable Values	Default	Description
Frame Format			
Frame Sequence 0/1 (SCM0/1)			
Frame Byte 0/15	K28.7	K28.7	I/O Frame Comma Symbol
Frame Byte 1/15	8'h00, 8'h10, 8'h11	8'h00	I/O Frame Subtype Symbol • The value is 8'h00 for default I/O frame. • The value is 8'h10 for OEM 0 I/O frame. • The value is 8'h11 for OEM 1 I/O frame.
--content #--	[NL Frame Counter, LL GPIO, NLGPIO, UART, I2C, OEM, NULL]	NL Frame Counter	I/O Frame content. Options depend on whether the channel is enabled or not.
Frame Byte #:#/15	[2–14]:[2–14]	2:2	Occupied bytes numbers depend on the channel quantity. Its value is calculated automatically.
Frame Byte 15/15	CRC	CRC	Cyclic Redundancy Check (CRC) for byte1–14. Its value is calculated automatically.
Configuration 0/1 (SCM0/1)			
Total Bytes in Frame	0–16	12	Total valid bytes in Frame without 0 placeholders. Its value is calculated automatically.
NULL Byte in Frame	0–13	0	Editable when LTPI Frame Type = OEM_I/O:1. The stuff byte, whose value is 0. It is used as a placeholder.
GPIO			
General 0/1 (SCM0/1)			
Enable LL GPIO Channel	Checked, Unchecked	Unchecked	Selects whether to enable the Low Latency GPIO external channel.
Enable NL GPIO Channel	Checked, Unchecked	Unchecked	Selects whether to enable the Normal Latency GPIO external channel.
LL GPIO 0/1 (SCM0/1)			
LL GPIO Width in Total	1–16 or 1–96	16	Editable when Enable LL GPIO channel is checked. Otherwise, its value is 0. If the OEM frame is enabled and data channel is disabled, its width is up to 96.
LL GPIO Initial Value (Hex)	[0, $2^{\text{LL GPIO Width}}$-1]	0	Editable when Enable LL GPIO Channel is checked. Otherwise, its value is 0.
NL GPIO 0/1 (SCM0/1)			
NL GPIO Width in Total	1–1023	16	Editable when Enable NL GPIO Channel is checked. Otherwise, its value is 0.
NL GPIO Width in a Frame	16 or [8, 16, 24, 32,40, 48, 56, 64, 72, 80, 88, 96]	16	Editable when Enable NL GPIO Channel is checked. If the default I/O frame is enabled, its value is fixed to 16. Otherwise, the maximum value depends on NL GPIO Width.
NL GPIO Init Value (Hex)	[0, $2^{\text{NL GPIO Width}}$-1]	0	Editable when Enable NL GPIO Channel is checked. Otherwise, its value is 0.
UART			
General 0/1 (SCM0/1)			
Enable UART Channel	Checked, Unchecked	Unchecked	Selects whether to enable the UART external channel or not.
Number of UART	1–2 or 1–24	2	The external UART number. If the default I/O frame is enabled, the maximum number is 2. Otherwise, the maximum number can be up to 24.
Maximum Baud Rate	9600, 19200, 38400, 57600, 115200, 230400	9600	Supports the maximum UART baud rate, which is related to link speed.

Attribute	Selectable Values	Default	Description
Enable Flow Control	Checked, Unchecked	Unchecked	Selects whether to enable flow control ports of the UART channel.
I2C			
General 0/1 (SCM0/1)			
Enable I2C Channel	Checked, Unchecked	Unchecked	Selects whether to enable the I2C external channel or not.
Enable I2C IO Buffer	Checked, Unchecked	Unchecked	Selects whether to enable the I2C IO buffer or not.
Number of I2C	1–6 or 1–24	6	Specifies the I2C external channel number. If default I/O frame is enabled, the maximum number is 6. Otherwise, the maximum number can be up to 24.
Enable I2C ECHO	Checked, Unchecked	Unchecked	Select whether to enable or disable I2C echo event. To decrease the I2C latency.
I2C Channel # Speed Grade	100K, 400K	100K	Specifies the I2C external channel # speed as 100K or 400K.
I2C Channel # Mode	DUA, CTR, TGT	DUA	Specifies the I2C external channel # mode. • DUA: bidirectional, connected to the I2C controller or target. • CTR: connected to the I2C controller. • TGT: connected to the I2C target.
DATA			
General 0/1 (SCM0/1)			
CSR Port Outside	Checked, Unchecked	Unchecked	Move Inside CSR port to Outside. By this way external host (CPU) can access the CSR standalone.
CSR Port Address Range	0x0000-0x00FF	0x0000-0x00FF	Displayed when CSR Port Outside is enabled. It shows the address range of CSR port.
Data Channel Enable	Checked, Unchecked	Unchecked	Selects whether to enable the data external channel or not. If enabled, the host on the SCM side can access CSR and MMAP target on the HPM side. Refers to Table 5.1 for the address map.
Data Channel Address Base (Hex)	1 GB align	0x40000000(SCM0); 0x80000000(SCM1)	It is the base address for HOST access. 1 GB align. SCM1 = SCM0 + 1 GB
Data Channel Address Size	[0x400, 0x40000000]	0x400	From the memory map target port view, it is the range that HOST can access. On the SCM side, it is 1 GB range if the data channel is enabled. Otherwise, it is 1 KB range that is the CSR space. On the HPM side, it is 1 KB range if the CSR port is enabled.
SEG0: SCM OEM Address	0x0000–0x01FF	0x0000–0x01FF	On the SCM side, the offset is reserved for OEM-defined CPLD or FPGA information, such as CPLD or FPGA image version numbers, device identifiers, and OEM specific information.
SEG1: SCM Side CSR Address	0x0200-0x02FF	0x0200-0x02FF	On the SCM side, the offset is for LTPI Status and Link Training Control Registers. See Table 5.2.
SEG2: SCM Reserved Address	0x0300–0x03FF	0x0300–0x03FF	On the SCM side, the offset is reserved for future use.
SEG3: HPM OEM Address	0x0400–0x5FF	0x0400–0x5FF	On the HPM side, the offset is reserved for OEM-defined CPLD or FPGA information, such as CPLD or FPGA image version numbers, device identifiers, and OEM-specific information.
SEG4: HPM Side CSR Address	0x0600-0x06FF	0x0600-0x06FF	On the HPM side, the offset is for LTPI Status and Link Training Control Registers. See Table 5.2.
SEG5: HPM Reserved Address	0x0700–0x07FF	0x0700–0x07FF	On the HPM side, the offset is reserved for future use.

Attribute	Selectable Values	Default	Description
SEG6: HPM MMAP Address	0x0800–0x3FFFFFFF	0x0800–0x3FFFFFFF	On the HPM side, the offset is the address Space reserved for the memory-mapped channel.
OEM			
General 0/1 (SCM0/1) According to the OCP Default I/O Frame, bytes 11–14 are OEM bytes and tunnelling data of 32 bits oem_io_i/o. Here, the IP reuses part or all these bytes as GPIO, UART, or I2C frames. If using part of them, the remaining bytes are still oem_io_i/o.			
Channel Enable	Checked, Unchecked	Unchecked	Selects whether to enable the OEM external channel or not. The channels' frame is in the Default I/O Frame bytes 11–14.
OEM IO Disable	Checked, Unchecked	Unchecked	Selects whether to disable part or all OEM I/O ports to use as GPIO, UART, or I2C, as described below. If part of the OEM I/O ports is used, the remaining bits are still OEM I/O.
Enable GPIO	Checked, Unchecked	Unchecked	Selects whether to enable GPIO in the OEM frame or not. Its latency is affected by the data channel of the default I/O frame. If the data channel is active, its latency is higher than LL GPIO of Default I/O.
GPIO Width	4, 8, 12, 16, 20, 24, 28, 32	4	GPIO external channel number
GPIO Initial Value	[0, GPIO Width{1}]	0	The initial value of the local GPIO output port when the link is not set up.
Enable I2C Channel	Checked, Unchecked	Unchecked	Selects whether to enable the I2C external channel or not.
Enable I2C IO Buffer	Checked, Unchecked	Unchecked	Selects whether to enable the I2C IO buffer or not.
I2C CH Number	1–8	8	Specifies the I2C external channel number.
Enable I2C ECHO	Checked, Unchecked	Checked	Select whether to enable or disable I2C echo event to decrease the I2C latency.
I2C CH# Speed Grade	100K, 400K	100K	Specifies the I2C external channel # speed as 100K or 400K.
I2C CH# Mode	DUA, CTR, TGT	DUA	Specifies the I2C external channel # mode. • Dual Function (DUA): bidirectional, connected to the I2C controller or target. • Controller (CTR): connected to the I2C controller. • Target (TGT): connected to the I2C target.
Enable UART Channel	Checked, Unchecked	Unchecked	Selects whether to enable the UART external channel or not.
UART Number	1-8	8	External UART number
Maximum Baud Rate	9600, 19200, 38400, 57600, 115200, 230400	9600	Supports maximum UART baud rate, which is related to the link speed.
Enable Flow Control	Checked, Unchecked	Unchecked	Selects whether to enable flow control ports of the UART channel or not.
CH Sort #1	NULL, GPIO, II2C, UART	NULL	Sort the sequence in the default I/O frame byte11–14. Which byte is GPIO, which byte is UART, which byte is I2C and which byte is NULL dummy byte. It is very flexible.
CH Sort #2	NULL, GPIO, II2C, UART	NULL	
CH Sort #3	NULL, GPIO, II2C, UART	NULL	
Channels Sequence	[NULL, GPIO, II2C, UART]: [NULL, GPIO, II2C,	NULL: NULL: NULL	The sequence in the Default I/O Frame bytes 11–14. This is not editable. For example, Channels Sequence is GPIO: II2C: UART, 2 UARTs, 2 I2Cs and 8 GPIOs, then

Attribute	Selectable Values	Default	Description
	UART]: [NULL, GPIO, II2C, UART]		byte 11 is UART, byte 12 is I2C, byte 13 is GPIO, and byte 14 is 0.
Configuration 0/1 (SCM0/1)			
Capability 0	8'h00–8'hFF	—	This is editable when OEM IO Disable is unchecked. When OEM IO Disable is checked, it is I2C enabled or not. Each bit corresponds to each channel. The value is generated according to I2C CH Number automatically. The value is used at the training stage in the advertise frame.
Capability 1	8'h00–8'hFF	—	This is editable when OEM IO Disable is unchecked. When OEM IO Disable is checked, it is the I2C speed mode. Each bit corresponds to each channel. The value is generated according to I2C CH Mode automatically. The value is used at the training stage in the advertise frame. This is not editable.
OEM Width in Total	0-32	32	The remaining oem_io_i/o bits
MISC			
Debug Mode	Checked, Unchecked	Unchecked	Selects whether to enable or disable debug signals displaying on IP ports.

4. Signal Description

Table 4.1. DC-SCM LTPI IP Core Signal Description

Port Name	I/O	Width	Default Value	Description
System				
clk_i	I	1	N/A	System clock
rstn_i	I	1	N/A	Active-low system reset
eclk_i_0	I	1	N/A	GDDR fast sampling clock It has the same frequency as LVDS Clock measured in MHz. It is hidden, if PLL SELECTION = INTERNAL.
eclk90_i_0	I	1	N/A	90-degree shifted for transmit clock generation. It has the same frequency as the LVDS Clock measured in MHz and must be source synchronous with eclk_i. It is hidden, if PLL SELECTION = INTERNAL.
clk_recfg_val_0	O	4	0	PLL re-configure request index value. See LTPI Link Status: LTPI Link Speed in Table 5.2.
clk_recfg_req_0	O	1	0	PLL re-configure request enable. When PLL configuration starts, it de-asserts automatically.
eclk_i_1	I	1	N/A	GDDR fast sampling clock It has the same frequency as LVDS Clock measured in MHz. It is hidden, if PLL SELECTION = INTERNAL.
eclk90_i_1	I	1	N/A	90-degree shifted for transmit clock generation. It has the same frequency as the LVDS Clock measured in MHz and must be source synchronous with eclk_i. It is hidden, if PLL SELECTION = INTERNAL.
clk_recfg_val_1	O	4	0	PLL re-configure request index value. See LTPI Link Status: LTPI Link Speed in Table 5.2.
clk_recfg_req_1	O	1	0	PLL re-configure request enable. When PLL configuration starts, it de-asserts automatically.
PLL				
pll_stable_i_0	I	1	N/A	After pll_rstn_i de-asserts, phase tuning starts. pll_stable_i asserts after phase tunning is done.
pll_stable_i_1	I	1	N/A	After pll_rstn_i de-asserts, phase tuning starts. pll_stable_i asserts after phase tunning is done.
LVDS Interface_0 (SCM0)				
lvds_tx_clk_o_0	O	1	N/A	LVDS TX PHY clock.
lvds_tx_data_o_0	O	1	N/A	LVDS TX PHY data.
lvds_rx_clk_i_0	I	1	N/A	LVDS RX PHY clock.
lvds_rx_data_i_0	I	1	N/A	LVDS RX PHY data.
LVDS Interface_1 (SCM1)				
lvds_tx_clk_o_1	O	1	N/A	LVDS TX PHY clock.
lvds_tx_data_o_1	O	1	N/A	LVDS TX PHY data.
lvds_rx_clk_i_1	I	1	N/A	LVDS RX PHY clock.
lvds_rx_data_i_1	I	1	N/A	LVDS RX PHY data.
Low Latency GPIO Channel Interface_0 (SCM0)				
ll_gpio_i_0	I	16	N/A	Low latency GPIO input pins. It is hidden, if ENABLE LL GPIO CHANNEL = UNCHECKED.
ll_gpio_o_0	O	16	LL GPIO Initial Value	Low latency GPIO output pins. The default value after reset is LL GPIO Initial Value. It is hidden, if ENABLE LL GPIO CHANNEL = UNCHECKED.
Low Latency GPIO Channel Interface_1 (SCM1)				
ll_gpio_i_0	I	16	N/A	Low latency GPIO input pins. It is hidden, if ENABLE LL GPIO CHANNEL = UNCHECKED.

Port Name	I/O	Width	Default Value	Description
ll_gpio_o_0	O	16	LL GPIO Initial Value	Low latency GPIO output pins. The default value after reset is LL GPIO Initial Value. It is hidden, if ENABLE LL GPIO CHANNEL = UNCHECKED.
Normal Latency GPIO Channel Interface_0 (SCM0)				
nl_gpio_i_0	I	NL_GPIO_NUM	N/A	Normal latency GPIO input pins. It is hidden, if ENABLE NL GPIO CHANNEL = UNCHECKED.
nl_gpio_o_0	O	NL_GPIO_NUM	NL_GPIO_INIT	Normal latency GPIO output pins. The default value after reset is NL GPIO Initial Value. It is hidden, if ENABLE NL GPIO CHANNEL = UNCHECKED.
Normal Latency GPIO Channel Interface_1 (SCM1)				
nl_gpio_i_1	I	NL_GPIO_NUM	N/A	Normal latency GPIO input pins. It is hidden, if ENABLE NL GPIO CHANNEL = UNCHECKED.
nl_gpio_o_1	O	NL_GPIO_NUM	NL_GPIO_INIT	Normal latency GPIO output pins. The default value after reset is NL GPIO Initial Value. It is hidden, if ENABLE NL GPIO CHANNEL = UNCHECKED.
I2C Channel Interface_0 (SCM0)				
i2c_scl_io_0	I/O	NUM_OF_I2C	Open Drain	I2C SCL (clock) pin. It is hidden, if ENABLE I2C CHANNEL = UNCHECKED or ENABLE I2C IO BUFFER = UNCHECKED.
i2c_sda_io_0	I/O	NUM_OF_I2C	Open Drain	I2C SDA (data) pin. It is hidden, if ENABLE I2C CHANNEL = UNCHECKED or ENABLE I2C IO BUFFER = UNCHECKED.
i2c_scl_i_0	I	NUM_OF_I2C	N/A	I2C SCL (clock) input pin. It is hidden, if ENABLE I2C CHANNEL = UNCHECKED or ENABLE I2C IO BUFFER = CHECKED.
i2c_scl_en_0	O	NUM_OF_I2C	0	I2C SCL (clock) output enable pin. It is hidden, if ENABLE I2C CHANNEL = UNCHECKED or ENABLE I2C IO BUFFER = CHECKED.
i2c_sda_i_0	I	NUM_OF_I2C	N/A	I2C SDA (data) input pin. It is hidden, if ENABLE I2C CHANNEL = UNCHECKED or ENABLE I2C IO BUFFER = CHECKED.
i2c_sda_en_0	O	NUM_OF_I2C	0	I2C SDA (data) output enable pin. It is hidden, if ENABLE I2C CHANNEL = UNCHECKED or ENABLE I2C IO BUFFER = CHECKED.
I2C Channel Interface_1 (SCM1)				
i2c_scl_io_1	I/O	NUM_OF_I2C	Open Drain	I2C SCL (clock) pin. It is hidden, if ENABLE I2C CHANNEL = UNCHECKED or ENABLE I2C IO BUFFER = UNCHECKED.
i2c_sda_io_1	I/O	NUM_OF_I2C	Open Drain	I2C SDA (data) pin. It is hidden, if ENABLE I2C CHANNEL = UNCHECKED or ENABLE I2C IO BUFFER = UNCHECKED.
i2c_scl_i_1	I	NUM_OF_I2C	N/A	I2C SCL (clock) input pin. It is hidden, if ENABLE I2C CHANNEL = UNCHECKED or ENABLE I2C IO BUFFER = CHECKED.
i2c_scl_en_1	O	NUM_OF_I2C	0	I2C SCL (clock) output enable pin. It is hidden, if ENABLE I2C CHANNEL = UNCHECKED or ENABLE I2C IO BUFFER = CHECKED.
i2c_sda_i_1	I	NUM_OF_I2C	N/A	I2C SDA (data) input pin. It is hidden, if ENABLE I2C CHANNEL = UNCHECKED or ENABLE I2C IO BUFFER = CHECKED.
i2c_sda_en_1	O	NUM_OF_I2C	0	I2C SDA (data) output enable pin. It is hidden, if ENABLE I2C CHANNEL = UNCHECKED or ENABLE I2C IO BUFFER = CHECKED.
UART Channel Interface_0 (SCM0)				
uart_tx_o_0	O	NUM_OF_UART	All 1	UART channel output pin. It is hidden, if ENABLE UART CHANNEL = UNCHECKED.
uart_rx_i_0	I	NUM_OF_UART	N/A	UART channel input pin. It is hidden, if ENABLE UART CHANNEL = UNCHECKED.

Port Name	I/O	Width	Default Value	Description
uart_rts_o_0	O	NUM_OF_UART	All 0	UART miscellaneous pin can be connected to the CTS/RTS pin. Depends on the direction. It is hidden, if ENABLE UART CHANNEL = UNCHECKED.
uart_cts_i_0	I	NUM_OF_UART	N/A	
UART Channel Interface_1 (SCM1)				
uart_tx_o_1	O	NUM_OF_UART	All 1	UART Channel output pin. It is hidden, if ENABLE UART CHANNEL = UNCHECKED.
uart_rx_i_1	I	NUM_OF_UART	N/A	UART Channel input pin. It is hidden, if ENABLE UART CHANNEL = UNCHECKED.
uart_rts_o_1	O	NUM_OF_UART	All 0	UART miscellaneous pin can be connected to the CTS/RTS pin. Depends on the direction. It is hidden, if ENABLE UART CHANNEL = UNCHECKED.
uart_cts_i_1	I	NUM_OF_UART	N/A	
Data Channel Interface-APB Target Interface				
s_apb_psel_i	I	1	N/A	Select signal. Indicates that the target device is selected and a data transfer is required.
s_apb_paddr_i	I	32	N/A	Address signal
s_apb_pwdata_i	I	32	N/A	Write data signal
s_apb_pwrite_i	I	1	N/A	Direction signal. Write = 1, Read = 0.
s_apb_penable_i	I	1	N/A	Enable signal. Indicates the second and subsequent cycles of an APB transfer.
s_apb_pready_o	O	1	1'b0	Ready signal. Indicates transfer completion. The target uses this signal to extend an APB transfer.
s_apb_prdata_o	O	32	32'h0	Read data signal.
s_apb_pslverr_o	O	1	1'b0	APB error signal.
data_tag_in_0	I	8	N/A	Tag field in SCM data frame that can be used by the user of the Data Channel, such as other CPLD or FPGA Logic, BMC FW and so on to identify responses if multiple outstanding Data Request are sent to LTPI. Currently the IP does not support outstanding Data Request yet. It is recommended to set it as a constant value.
data_tag_out_0	O	8	8'h0	
Data Channel Interface-APB Controller Interface				
m0_apb_psel_o	I	1	1'b0	Select signal. selected the target device and a data transfer is required.
m0_apb_paddr_o	I	32	32'h0	Address signal
m0_apb_pwdata_o	I	32	32'h0	Write data signal
m0_apb_pwrite_o	I	1	1'b0	Direction signal. Write = 1, Read = 0.
m0_apb_penable_o	I	1	1'b0	Enable signal. Indicates the second and subsequent cycles of an APB transfer.
m0_apb_pready_i	O	1	N/A	Ready signal. Indicates transfer completion. The target uses this signal to extend an APB transfer.
m0_apb_prdata_i	O	32	N/A	Read data signal.
m0_apb_pslverr_i	O	1	N/A	APB error signal.
OEM Channel Interface_0 (SCM0) According to the OCP Default I/O Frame, bytes 11–14 are OEM bytes and tunnelling data of 32 bits oem_io_i/o. Here, the IP reuses part or all these bytes as GPIO, UART, or I2C frames. If using part of them, the remaining bytes are still oem_io_i/o.				
oem_io_i_0	I	[1-32]	N/A	OEM I/O input port. The width depends on how many bits are reused as GPIO, UART, I2C, or any combination of these.
oem_io_o_0	O	[1-32]	0	OEM I/O output port. The width depends on how many bits are reused as GPIO, UART, I2C, or any combination of these.

Port Name	I/O	Width	Default Value	Description
def_oem_gpio_i_0	I	GPIO Width (OEM)	N/A	OEM Low latency GPIO input pins Its latency is affected by the data channel. It is hidden, if CHANNEL ENABLE = UNCHECKED or OEM IO DISABLE = UNCHECKED or OEM Enable GPIO = UNCHECKED.
def_oem_gpio_o_0	O	GPIO Width (OEM)	GPIO INITIAL VALUE (OEM)	OEM Low latency GPIO output pins The default value after reset is GPIO INITIAL VALUE (OEM). Its latency is affected by the data channel. It is hidden, if CHANNEL ENABLE = UNCHECKED or OEM IO DISABLE = UNCHECKED or OEM Enable GPIO = UNCHECKED.
def_oem_i2c_scl_0	I/O	I2C CH Number (OEM)	Open Drain	OEM I2C SCL (clock) pin It is hidden, if CHANNEL ENABLE = UNCHECKED or OEM IO DISABLE = UNCHECKED or OEM ENABLE I2C CHANNEL = UNCHECKED or OEM ENABLE I2C IO BUFFER = UNCHECKED.
def_oem_i2c_sda_0	I/O	I2C CH Number (OEM)	Open Drain	OEM I2C SDA (data) pin It is hidden, if CHANNEL ENABLE = UNCHECKED or OEM IO DISABLE = UNCHECKED or OEM ENABLE I2C CHANNEL = UNCHECKED or OEM ENABLE I2C IO BUFFER = UNCHECKED.
def_oem_i2c_scl_i_0	I	I2C CH Number (OEM)	N/A	OEM I2C SCL (clock) input pin It is hidden, if CHANNEL ENABLE = UNCHECKED or OEM IO DISABLE = UNCHECKED or OEM ENABLE I2C CHANNEL = UNCHECKED or OEM ENABLE I2C IO BUFFER = CHECKED.
def_oem_i2c_scl_en_0	O	I2C CH Number (OEM)	0	OEM I2C SCL (clock) output enable pin It is hidden, if CHANNEL ENABLE = UNCHECKED or OEM IO DISABLE = UNCHECKED or DOEM_ENABLE I2C CHANNEL = UNCHECKED or OEM ENABLE I2C IO BUFFER = CHECKED.
def_oem_i2c_sda_i_0	I	I2C CH Number (OEM)	N/A	OEM I2C SDA (data) input pin It is hidden, if CHANNEL ENABLE = UNCHECKED or OEM IO DISABLE = UNCHECKED or DOEM_ENABLE I2C CHANNEL = UNCHECKED or OEM ENABLE I2C IO BUFFER = CHECKED.
def_oem_i2c_sda_en_0	O	I2C CH Number (OEM)	0	OEM I2C SDA (data) output enable pin It is hidden, if CHANNEL ENABLE = UNCHECKED or OEM IO DISABLE = UNCHECKED or DOEM_ENABLE I2C CHANNEL = UNCHECKED or OEM ENABLE I2C IO BUFFER = CHECKED.
def_oem_uart_txd_0	O	UART Number (OEM)	All 1	OEM UART Channel output pin It is hidden, if CHANNEL ENABLE = UNCHECKED or OEM IO DISABLE = UNCHECKED or Enable UART Channel = Unchecked.
def_oem_uart_rxd_0	I	UART Number (OEM)	N/A	OEM UART Channel input pin It is hidden, if CHANNEL ENABLE = UNCHECKED or OEM IO DISABLE = UNCHECKED or Enable UART Channel = Unchecked.
def_oem_uart_rts_0	O	UART Number (OEM)	All 0	OEM UART miscellaneous pin can be connected to the RTS pin, depending on the direction. It is hidden, if CHANNEL ENABLE = UNCHECKED or OEM IO DISABLE = UNCHECKED or Enable UART Channel = Unchecked.
def_oem_uart_cts_0	I	UART Number (OEM)	N/A	OEM UART miscellaneous pin can be connected to the CTS pin, depending on the direction. It is hidden, if CHANNEL ENABLE = UNCHECKED or OEM IO DISABLE = UNCHECKED or Enable UART Channel = Unchecked.
OEM Channel Interface_1 (SCM1)				
oem_io_i_1	I	[1-32]	N/A	The OEM I/O input port. The width depends on how many bits are reused as GPIO/UART/I2C.
oem_io_o_1	O	[1-32]	1	The OEM I/O output port. The width depends on how many bits are reused as GPIO/UART/I2C.

Port Name	I/O	Width	Default Value	Description
def_oem_gpio_i_1	I	GPIO Width (OEM)	N/A	OEM Low latency GPIO input pins Its latency is affected by the data channel. It is hidden, if CHANNEL ENABLE = UNCHECKED or OEM IO DISABLE = UNCHECKED or OEM Enable GPIO = UNCHECKED .
def_oem_gpio_o_1	O	GPIO Width (OEM)	GPIO INITIAL VALUE (OEM)	OEM Low latency GPIO output pins The default value after reset is GPIO INITIAL VALUE (OEM). Its latency is affected by the data channel. It is hidden, if CHANNEL ENABLE = UNCHECKED or OEM IO DISABLE = UNCHECKED or OEM Enable GPIO = UNCHECKED.
def_oem_i2c_scl_1	I/O	I2C CH Number (OEM)	Open Drain	OEM I2C SCL (clock) pin It is hidden, if CHANNEL ENABLE = UNCHECKED or OEM IO DISABLE = UNCHECKED or DOEM_I2C_CH_EN = 0 or OEM ENABLE I2C IO BUFFER = UNCHECKED or OEM ENABLE I2C IO BUFFER = UNCHECKED.
def_oem_i2c_sda_1	I/O	I2C CH Number (OEM)	Open Drain	OEM I2C SDA (data) pin It is hidden, if CHANNEL ENABLE = UNCHECKED or OEM IO DISABLE = UNCHECKED or DOEM_I2C_CH_EN = 0 or OEM ENABLE I2C IO BUFFER = UNCHECKED or OEM ENABLE I2C IO BUFFER = UNCHECKED.
def_oem_i2c_scl_i_1	I	I2C CH Number (OEM)	N/A	OEM I2C SCL (clock) input pin It is hidden, if CHANNEL ENABLE = UNCHECKED or OEM IO DISABLE = UNCHECKED or OEM ENABLE I2C CHANNEL = UNCHECKED or OEM ENABLE I2C IO BUFFER = CHECKED.
def_oem_i2c_scl_en_1	O	I2C CH Number (OEM)	0	OEM I2C SCL (clock) output enable pin It is hidden, if CHANNEL ENABLE = UNCHECKED or OEM IO DISABLE = UNCHECKED or OEM ENABLE I2C CHANNEL = UNCHECKED or OEM ENABLE I2C IO BUFFER = CHECKED.
def_oem_i2c_sda_i_1	I	I2C CH Number (OEM)	N/A	OEM I2C SDA (data) input pin It is hidden, if CHANNEL ENABLE = UNCHECKED or OEM IO DISABLE = UNCHECKED or OEM ENABLE I2C CHANNEL = UNCHECKED or OEM ENABLE I2C IO BUFFER = CHECKED.
def_oem_i2c_sda_en_1	O	I2C CH Number (OEM)	0	OEM I2C SDA (data) output enable pin It is hidden, if CHANNEL ENABLE = UNCHECKED or OEM IO DISABLE = UNCHECKED or OEM ENABLE I2C CHANNEL = UNCHECKED or OEM ENABLE I2C IO BUFFER = CHECKED.
def_oem_uart_txd_1	O	UART Number (OEM)	All 1	OEM UART Channel output pin It is hidden, if CHANNEL ENABLE = UNCHECKED or OEM IO DISABLE = UNCHECKED or Enable UART Channel = Unchecked.
def_oem_uart_rxd_1	I	UART Number (OEM)	N/A	OEM UART Channel input pin It is hidden, if CHANNEL ENABLE = UNCHECKED or OEM IO DISABLE = UNCHECKED or Enable UART Channel = Unchecked.
def_oem_uart_rts_1	O	UART Number (OEM)	All 1	OEM UART miscellaneous pin can be connected to the CTS/RTS pin, depending on the direction. It is hidden, if CHANNEL ENABLE = UNCHECKED or OEM IO DISABLE = UNCHECKED or Enable UART Channel = Unchecked.
def_oem_uart_cts_1	I	UART Number (OEM)	N/A	OEM UART miscellaneous pin can be connected to the CTS/RTS pin, depending on the direction. It is hidden, if CHANNEL ENABLE = UNCHECKED or OEM IO DISABLE = UNCHECKED or Enable UART Channel = Unchecked.
Protocol Information_0/1 (SCM0/1)				
link_up_0	O	1	1	The LTPI link is set up on both side.
link_up_1	O	1	1	The LTPI link is set up on both side.

Port Name	I/O	Width	Default Value	Description
Debug_Signals_0/1 (SCM0/1): Display when DEBUG_EN is checked				
rx_frame_aligned_0/1	O	1	0	The received LTPI frame is aligned. The header is found.
rx_frame_crc_error_0/1	O	1	0	The received LTPI frame has CRC errors. It is a pulse.
rx_frame_crc_error_counts_0/1	O	16	0	Counts the received LTPI frame CRC errors from the last system reset. The values are clear either by a system reset or writing 1 to the address 0x34.
last_nl_gpio_update_0/1	O	1	0	Asserts when sequence_nl_gpio_update_0/1 counts to the ceil value.
sequence_nl_gpio_update_0/1	O	8	0	Counts the sequence of NL GPIO per frame. It is continuous and gets back to 0 when it counts to the ceil value.
rx_frame_unknown_comma_symbol_0/1	O	1	0	The received LTPI frames are unknown, that is, they are not I/O or DATA frames.
link_speed_timeout_0/1	O	1	0	Link Speed stage is time out. It is a pulse.
link_config_accept_timeout_0/1	O	1	0	Link Configure (SCM) or Accept (HPM) stage is timeout. It is a pulse.
local_link_state_0/1	O	4	0	Displays the Link status of local SCM or HPM. It varies with the link stage. The values are 0, 1, 2, 3, 4, which meet the OCP specification.
remote_link_state_0/1	O	4	0	Displays the Link status of remote SCM or HPM. It varies with the link stage. The values are 0, 1, 2, 3, 4, which meet OCP specification.

5. Register Description

The LTPI interface provides Configuration Space Registers. The configuration registers are primarily defined for the Board Management Controller (BMC) to have control over LTPI operations. The basic usage of LTPI CSR is to allow BMC to access:

- LTPI Link Status Information
- LTPI Link Capabilities Information
- LTPI Link Configuration Control
- LTPI Channel Operational Telemetry Information
- LTPI Link/Channel Reset Capabilities

The general register map with predefined offsets is shown in Table 5.1, following the OCP LTPI specification. Both SCM and HPM sides have CSR, which can be accessed by the HOST (BMC) on the SCM side, as shown in Figure 2.2.

Table 5.1. General Control and Status Register Map

Offset	Name	Description
0x000–0x1FF	CPLD/FPGA Information	The offset is reserved for OEM-defined CPLD or FPGA information, such as CPLD or FPGA image version numbers, device identifiers, and OEM-specific information.
0x200–0x2FF	LTPI Control and Status	LTPI Status and Link Training Control Registers. See Table 5.2.
0x300–0x3FF	Reserved	Reserved for future use.
0x400–0xFFFFFFFF	LTPI Memory Mapped Channel	Address Space reserved for memory-mapped channel

Table 5.2. LTPI Control and Status Registers

Offset	Name	Bit Field	Type	Bit Field Definition
0x00	LTPI Link Status[1]	31:20	—	Reserved
		19:16	RO	Local LTPI Link State (SCM) State / Encoding: Link Detect / 0x0 Link Speed / 0x1 Advertise / 0x2 Configuration / 0x3 Operational / 0x4 Reserved / 0x5–0xF
		15:12	RO	Local LTPI Link State (HPM) State / Encoding: Link Detect / 0x0 Link Speed / 0x1 Advertise / 0x2 Configuration / 0x3 Operational / 0x4 Reserved / 0x5–0xF

<table>
<tr><th>Offset</th><th>Name</th><th>Bit Field</th><th>Type</th><th>Bit Field Definition</th></tr>
<tr><td rowspan="10"></td><td rowspan="10"></td><td>11:8</td><td>RO</td><td>LTPI Link Speed
<table><tr><th>Link Speed</th><th>Encoding</th></tr><tr><td>Base Freq x1</td><td>0x0</td></tr><tr><td>Base Freq x2</td><td>0x1</td></tr><tr><td>Base Freq x3</td><td>0x2</td></tr><tr><td>Base Freq x4</td><td>0x3</td></tr><tr><td>Base Freq x6</td><td>0x4</td></tr><tr><td>Base Freq x8</td><td>0x5</td></tr><tr><td>Base Freq x10</td><td>0x6</td></tr><tr><td>Base Freq x12</td><td>0x7</td></tr><tr><td>Base Freq x16</td><td>0x8</td></tr><tr><td>Base Freq x24</td><td>0x9</td></tr><tr><td>Base Freq x32</td><td>0xA</td></tr><tr><td>Base Freq x40</td><td>0xB</td></tr><tr><td>Reserved</td><td>0xC–0xF</td></tr></table></td></tr>
<tr><td>7</td><td>RO</td><td>DDR Mode: 0: SDR Mode 1: DDR Mode</td></tr>
<tr><td>6</td><td>—</td><td>Reserved</td></tr>
<tr><td>5</td><td>RWC</td><td>Link Configure/Accept Timeout Error</td></tr>
<tr><td>4</td><td>RWC</td><td>Link Speed Timeout Error</td></tr>
<tr><td>3</td><td>RWC</td><td>Unknown Comma Symbol Error</td></tr>
<tr><td>2</td><td>RWC</td><td>Frame CRC Error</td></tr>
<tr><td>1</td><td>RWC</td><td>LTPI Link Lost Error</td></tr>
<tr><td>0</td><td>RWC</td><td>LTPI Link Aligned 0: Link not Aligned 1: Link Aligned</td></tr>
<tr><td rowspan="4">0x04</td><td rowspan="4">LTPI Detect Capabilities Local</td><td>31:24</td><td>—</td><td>Reserved</td></tr>
<tr><td>23:8</td><td>RW</td><td>Link Speed Capabilities, as in Table 5.3.</td></tr>
<tr><td>7:4</td><td>RO</td><td>Local LTPI Major Version</td></tr>
<tr><td>3:0</td><td>RO</td><td>Local LTPI Minor Version</td></tr>
<tr><td rowspan="4">0x08</td><td rowspan="4">LTPI Detect Capabilities Remote</td><td>31:24</td><td>—</td><td>Reserved</td></tr>
<tr><td>23:8</td><td>RO</td><td>Link Speed Capabilities, as in Table 5.3.</td></tr>
<tr><td>7:4</td><td>RO</td><td>Remote LTPI Major Version</td></tr>
<tr><td>3:0</td><td>RO</td><td>Remote LTPI Minor Version</td></tr>
<tr><td rowspan="2">0x0C</td><td rowspan="2">LTPI Platform ID Local</td><td>31:16</td><td>—</td><td>Reserved</td></tr>
<tr><td>15:0</td><td>RO</td><td>Local LTPI Platform ID</td></tr>
<tr><td rowspan="2">0x10</td><td rowspan="2">LTPI Platform ID Remote</td><td>31:16</td><td>—</td><td>Reserved</td></tr>
<tr><td>15:0</td><td>RO</td><td>Remote LTPI Platform ID</td></tr>
<tr><td>0x14</td><td>LTPI Advertise Capabilities Local Low[2]</td><td>31:0</td><td>RW</td><td>Local LTPI Capabilities Low – Bytes 3:0</td></tr>
<tr><td>0x18</td><td>LTPI Advertise Capabilities Local High[2]</td><td>31:0</td><td>RW</td><td>Local LTPI Capabilities High – Bytes 7:4</td></tr>
<tr><td>0x1C</td><td>LTPI Advertise Capabilities Remote Low</td><td>31:0</td><td>RO</td><td>Remote LTPI Capabilities Low – Bytes 3:0</td></tr>
<tr><td>0x20</td><td>LTPI Advertise Capabilities Remote High</td><td>31:0</td><td>RO</td><td>Remote LTPI Capabilities High – Bytes 7:4</td></tr>
<tr><td>0x24</td><td>LTPI Default Configuration Low[3]</td><td>31:0</td><td>RO</td><td>LTPI Default Configuration Low – Bytes 3:0</td></tr>
<tr><td>0x28</td><td>LTPI Default Configuration High[3]</td><td>31:0</td><td>RO</td><td>LTPI Default Configuration Low – Bytes 7:4</td></tr>
<tr><td>0x2C</td><td>LTPI Link Alignment Error Counter[4]</td><td>31:0</td><td>RWC</td><td>LTPI Link Alignment Error Counter</td></tr>
<tr><td>0x30</td><td>LTPI Link Lost Error Counter[4]</td><td>31:0</td><td>RWC</td><td>LTPI Link Lost Error Counter</td></tr>
<tr><td>0x34</td><td>LTPI CRC Error Counter[4]</td><td>31:0</td><td>RWC</td><td>LTPI CRC Error Counter</td></tr>
<tr><td>0x38</td><td>LTPI Unknown Comma Error Counter[4]</td><td>31:0</td><td>RWC</td><td>LTPI Unknown Comma Error Counter</td></tr>
<tr><td>0x3C</td><td>LTPI Link Speed Timeout Error Counter[4]</td><td>31:0</td><td>RWC</td><td>LTPI Link Speed Timeout Error Counter</td></tr>
</table>

Offset	Name	Bit Field	Type	Bit Field Definition
0x40	LTPI Link Configure/Accept Timeout Error Counter[4]	31:0	RWC	LTPI Link Configure/Accept Timeout Error Counter
0x44	Link Training RX Frames Counter Low[4]	31:24	RWC	Link Configure/Accept Frames Received Counter
		23:16		Link Speed Frames Received Counter
		15:0		Link Detect Frames Received Counter
0x48	Link Training RX Frames Counter High[4]	31:0	RWC	Link Advertise Frames Received Counter
0x4C	Link Training TX Frames Counter Low[4]	31:24	RWC	Link Configure/Accept Frames Sent Counter
		23:16		Link Speed Frames Sent Counter
		15:0		Link Detect Frames Sent Counter
0x50	Link Training TX Frames Counter High[4]	31:0	RWC	Link Advertise Frames Sent Counter
0x54	Operational RX Frames Counter[4]	31:0	RWC	Operational Frames Received
0x58	Operational TX Frames Counter[4]	31:0	RWC	Operational Frames Transmitted
0x5C-0x7F	Reserved	—	—	—
0x80	LTPI Link Control	31:12	—	Reserved
		11	RW	Trigger Configuration State
		10	RW	Automatically Move to Configuration State
		9	RW	Data Channel Reset
		8:2	RW	LTPI I2C Channel Reset Write I2C Channel Link Number
		1	RW	LTPI Link Retraining Request
		0	RW	LTPI Link Software Reset
0x84	NL GPIO counter index	7:0	RO	Indicate the real-time NL GPIO counter index
0x88-0xFF	Reserved	—	—	—

Notes:

1. For an RWC register, the write operations may affect the new value update.
2. The value vary upon the Capability Type 0/1 value shown in Table 3.1. Thus, if LTPI Frame Type changes, this value also changes.
3. If IP Mode is HPM, the value is updated when HPM is configured by SCM. If IP Mode is SCM, the value is updated according to the common Advertise Capabilities values of SCM and HPM during training. Refer to the OCP DC-SCM 2 LTPI Specification (Revision 1.2, Version 1.0), section 4.1.2.3 Link Configuration Example.
4. Disabled if Resource Optimization is checked.

Table 5.3. Speed Capabilities Encoding

Byte	Bit Fields Encoding							
	7	6	5	4	3	2	1	1
0	Base Freq. x12 300 MHz	Base Freq. x10 250 MHz	Base Freq. x8 200 MHz	Base Freq. x6 150 MHz	Base Freq. x4 100 MHz	Base Freq. x3 75 MHz	Base Freq. x2 50 MHz	Base Freq. x1 25 MHz
1	Dual Data Rate 0: SDR 1: DDR	Reserved	Reserved	Reserved	Base Freq. x40 1 GHz	Base Freq. x32 800 MHz	Base Freq. x24 600 MHz	Base Freq. x16 400 MHz

6. Program Flow

Because the Link Speed is changed dynamically during the training process, you should configure the PLL accordingly. The PLL of MachXO3L, MachXO3LF, and MachXO3D devices and the Lattice nexus platform devices are different. So, different drivers are needed. The values in the CSR of both the SCM and HPM sides can be modified dynamically. Also, the host on the SCM side can access peripherals on the HPM side through the data channel after linking up. This chapter is from an SoC design view, not from the perspective of a standalone IP.

6.1. PLL Configuration

The LTPI has two output signals to request a link speed change, clk_recfg_val_0/1 and clk_recfg_req_0/1. The recommended program flow is shown in Figure 6.1. During the initial process, the interrupt service function is registered, and the interrupt enable should be set. Then, wait until IRQ asserts. According to the requested values, PLL is configured with desired frequency and phase shift. During frequency configuration, the PLL is reset. However, during phase shift tuning, the PLL reset is de-asserted, and PLL is not stable yet. So, another signal pll_stable_i_0/1 should output to the LTPI IP after phase shift tunning is done. Wait for the PLL lock signal to assert before starting phase tuning. Another thing to note is that a delay should be added on the SCM side before starting to configure the PLL when IRQ asserts. This time is used to synchronize HPM's state machine. The delay time depends on the system clock frequency of both sides and the FIFO depth of the HPM side.

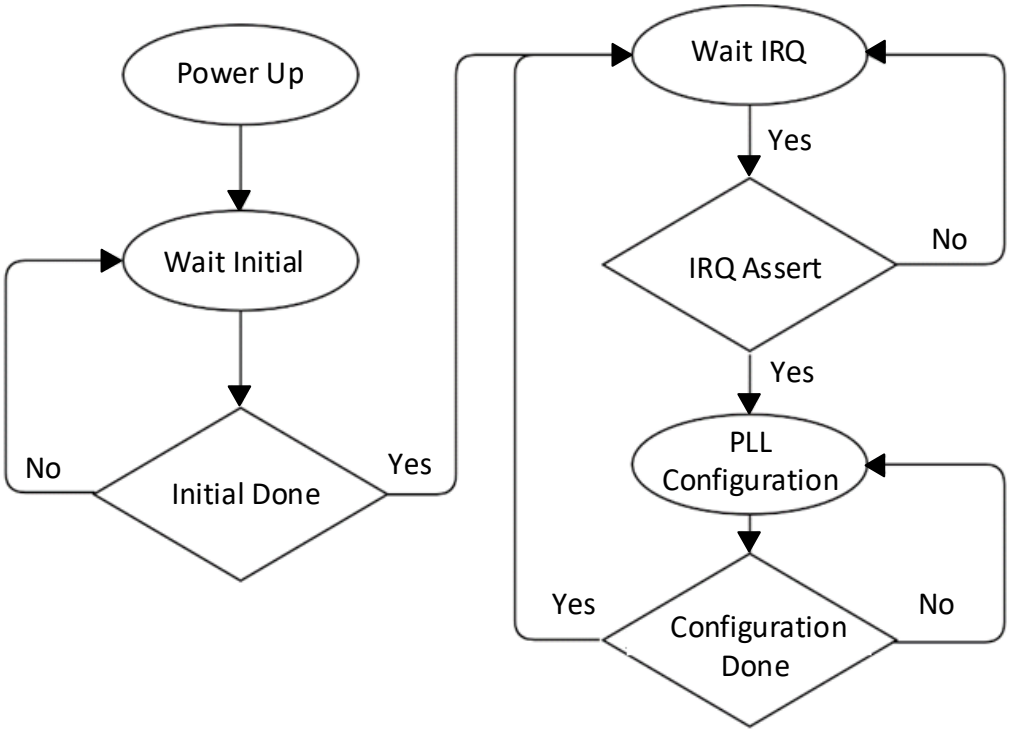

Figure 6.1. PLL Re-configure Program Flow

6.1.1. MachXO3L, MachXO3LF, and MachXO3D Devices PLL Configuration

The PLL operating parameters of MachXO3L, MachXO3LF, and MachXO3D devices can be changed dynamically through the WISHBONE bus of the Embedded Function Block (EFB). You must instantiate the EFB block in your design to use this feature. The user logic's WISHBONE bus is then connected to the EFB block. A hard-wired PLL data bus is used to communicate between the EFB and the PLL. See Using Hardened Control Functions in MachXO3D Devices (FPGA-TN-02117) for more information about using EFB in a design. Also refer to MachXO3D sysClock PLL Usage Guide (FPGA-TN-02070) for more information.

7. Designing with the IP

This section provides information on how to generate the DC-SCM IP Core using the Lattice Propel Builder software. It also introduces how to run simulation and synthesis. Refer to the Lattice Propel Builder 2025.2 User Guide (FPGA-UG-02212) for more details.

7.1. Generating and Instantiating the IP

You can use the Lattice Radiant software to generate IP modules and integrate them into the device's architecture. The steps below describe how to generate the DC-SCM LTPI IP in the Lattice Radiant software.

To generate the DC-SCM LTPI IP:

1. Create a new Lattice Radiant software project or open an existing project.
2. In the **IP Catalog** tab, double-click **server_ltpi** under **IP, Connectivity** category. The **Module/IP Block Wizard** window opens, as shown in Figure 7.1. Enter values in the **Component name** and the **Create in** fields and click **Next**.

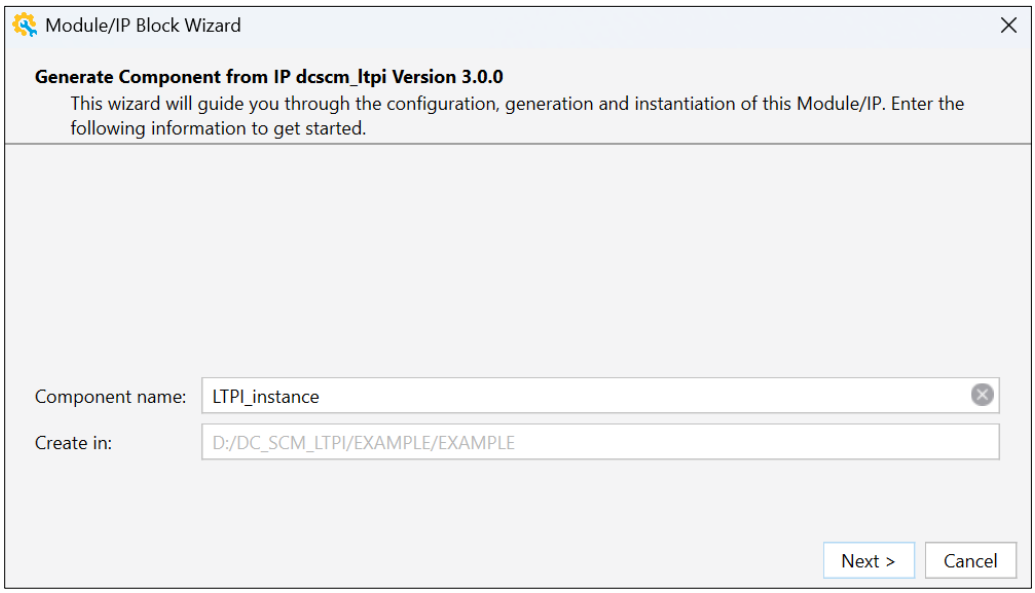

Figure 7.1. Module/IP Block Wizard

3. In the **Module/IP Block Wizard** window, customize the selected DC-SCM LTPI IP using drop-down menus and check boxes. Figure 7.2 shows an example configuration of the IP. For details on the configuration options, refer to the IP Parameter Description section.

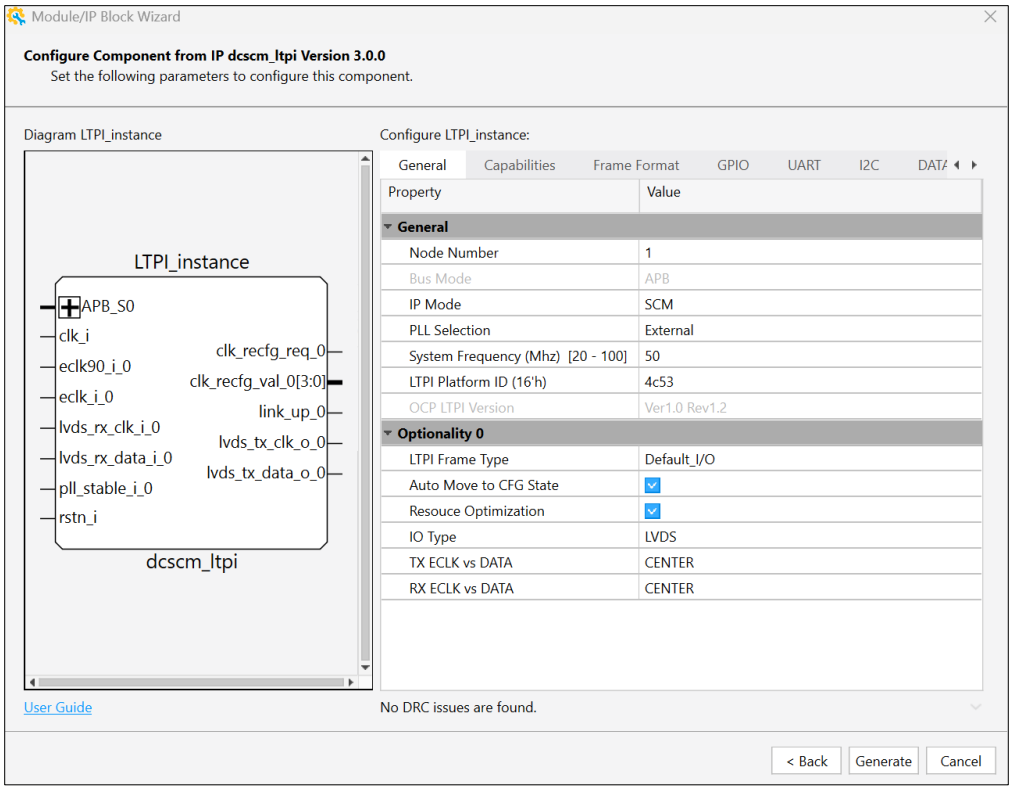

Figure 7.2. IP Configuration

4. Click **Generate**. The **Check Generating Result** dialog box opens, showing design block messages and results, as shown in Figure 7.3.

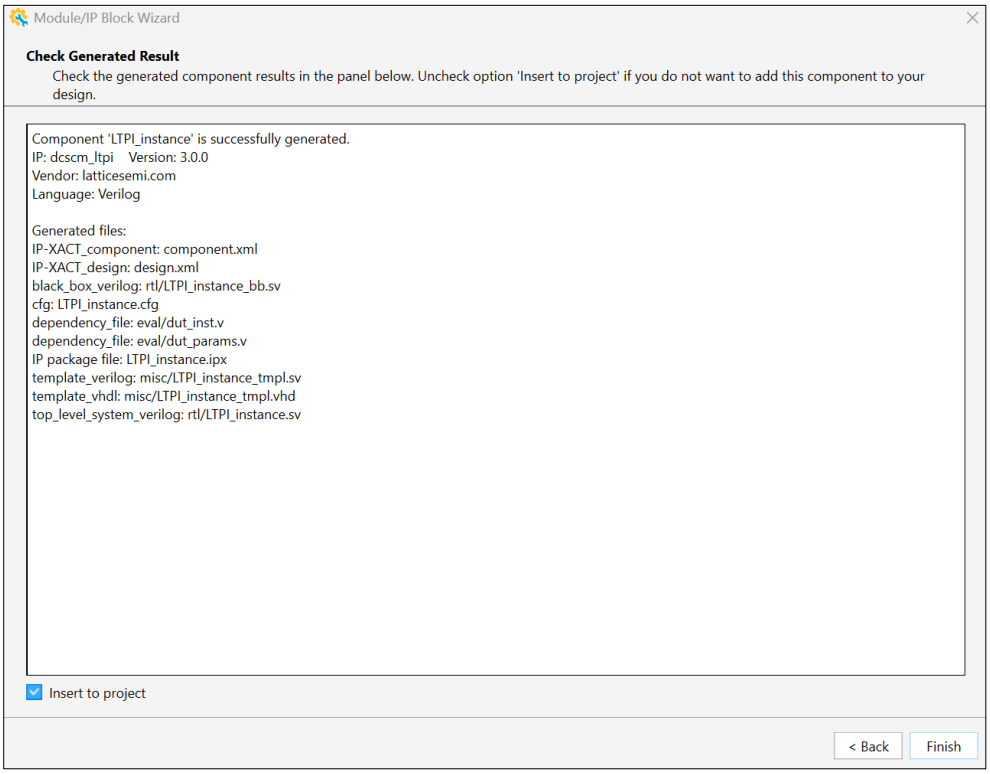

Figure 7.3. Check Generated Result

5. Click **Finish**. All the generated files are placed under the directory paths in the **Create in** and the **Component name** fields.

7.1.1. Generated Files and File Structure

The generated DC-SCM LTPI IP module package includes the black box (<Component name>_bb.v) and instance templates (<Component name>_tmpl.v/vhd) that can be used to instantiate the core in a top-level design. An example RTL top-level reference source file (<Component name>.v) that can be used as an instantiation template for the module is also provided. You may use this top-level reference as the starting template for the top-level complete design. The generated files are listed in Table 7.1.

Table 7.1. Generated File List

Attribute	Description
<Component name>.ipx	This file contains the information on the files associated to the generated IP.
<Component name>.cfg	This file contains the parameter values used in IP configuration.
component.xml	Contains the ipxact:component information of the IP.
design.xml	Documents the configuration parameters of the IP in IP-XACT 2014 format.
rtl/<Component name>.v	This file provides an example RTL top file that instantiates the module.
rtl/<Component name>_bb.v	This file provides the synthesis black box.
driver/ ltpi_nexus_pll.c driver/ ltpi_nexus_pll.h driver/ ltpi_xo3_pll.c driver/ ltpi_xo3_pll.h driver/ ltpi.c driver/ ltpi.h	pll.c/h files are used to configure PLL frequency and phase dynamically. ltpi.c/h files are used to access CSR and data channel.
misc/<Component name>_tmpl.v misc /<Component name>_tmpl.vhd	These files provide instance templates for the module.

7.1.2. Design Implementation

To complete your design, additional steps are needed including to specify analog properties, pin assignments, and timing constraints. You can also add .lpf logic preference files in the Lattice Diamond software.

7.1.2.1. Spreadsheet View

Refer to the Lattice Diamond software User Guide for more information on how to use the device constraint editor.

7.1.2.2. Manual LPF File Creation

Add the logic preference .lpf file in the Lattice Diamond software and define the I/O pins according to the schematic design for ports defined in your design. You can define different types of constraints such as pins, clocks, and other timing paths.

7.1.3. Timing Constraints

The timing constraints are based on the clock frequency used. The timing constraints for the IP are defined in relevant constraint files. The examples below show the IP timing constraints generated for the DC-SCM LTPI IP.

```
FREQUENCY NET "top_scm_inst/sys_clk_w" 50.000000 MHz ;
FREQUENCY NET "top_scm_inst/eclk_w" 400.000000 MHz ;
FREQUENCY NET "top_scm_inst/eclk90_w" 400.000000 MHz ;
FREQUENCY NET "top_scm_inst/ltpi_inst/lscc_dcscm_ltpi_inst/lscc_tx_path_inst/xo3_tx_PHY.lscc_phy_tx_xo3_inst/tx_sclk_o" 100.000000 MHz ;
FREQUENCY NET "top_scm_inst/ltpi_inst/lscc_dcscm_ltpi_inst/lscc_rx_path_inst/xo3_rx_PHY.lscc_phy_rx_xo3_inst/ddrrx_sclk_w" 100.000000 MHz ;
```

Figure 7.4. Timing Constraint File Extracted from the .lpf File for the DC-SCM LTPI IP

Appendix A. Resource Utilization

Table A.1 shows resource utilization of the DC-SCM LTPI IP default configuration for the LCMXO3D devices using Synplify Pro.

Table A.1. Resource Utilization

Configuration	Registers	Slice	LUTs	EBRs
Device: LCMXO3D-9400HC-6BG256C LL GPIO: 16 NL GPIO: 16 I2C: 6 w/ MCTP UART: 2 DATA CH: enable	—	—	—	2

Appendix B. Limitation

I2C tunneling support is limited to Standard (100 kHz) and Fast (400 kHz) modes only.

References

- MachXO3 Family Devices web page
- MachXO3D Family Devices web page
- MachXO5-NX Family Devices web page
- Mach-NX Family Devices web page
- Lattice Diamond Software web page
- Lattice Radiant Software web page
- Lattice Propel Design Environment web page
- Open Compute Project web page
- Using Hardened Control Functions in MachXO3D Devices (FPGA-TN-12117)
- MachXO3D sysClock PLL Usage Guide (FPGA-TN-12171)
- sysCLOCK PLL Design and User Guide for Nexus Platform (FPGA-TN-12195)
- Lattice Propel Builder 2025.2 User Guide (FPGA-UG-02212)
- DC-SCM LTPI IP Release Notes (FPGA-RN-02021)
- DC-SCM 2.1 LVDS Tunneling Protocol & Interface Specification (LTPI)
- Lattice Insights for Lattice Semiconductor Training Series and Learning Plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 1.0, IP v3.0.0, March 2026

Section	Change Summary
All	Initial release.

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