Voltage Temperature Monitor IP

IP Version: v1.2.0

User Guide

FPGA-IPUG-02322-1.0

June 2026

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This document was created consistent with Lattice Semiconductor's inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice's inclusive language FAQ 6878 for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

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Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviation	Definition
ASIC	Application-Specific Integrated Circuit
CPU	Central Processing Unit
EBR	Embedded Block RAM
FIFO	First In First Out
FPGA	Field Programmable Gate Array
HDL	Hardware Description Language
IP	Intellectual Property
LUT	Look-Up Table
PDC	Physical Design Constraint
RAM	Random Access Memory
RTL	Register Transfer Level
VTM	Voltage Temperature Monitor

1. Introduction

This document provides technical information about the Voltage Temperature Monitor (VTM) IP that is supported in Lattice Avant™ and Certus™-N2 FPGA devices. The document aims to provide information essential for IP and system developers, regarding verification, software for integration, testing, and validation. The document covers design specification from Register Transfer Level (RTL) up to IP packaging, IP generation, and integration with the Lattice Radiant™ software.

1.1. Overview of the IP

The Lattice Semiconductor VTM IP is designed to monitor on-die temperatures and voltages.

1.2. Quick Facts

Table 1.1. Summary of the Voltage Temperature Monitor IP

IP Requirements	Supported Devices	Lattice Avant-AT-E, Avant-AT-G, Avant-AT-X, Certus-N2 (except LN2-CT-20ES)
	IP Changes[1]	Refer to the Voltage Temperature Monitor IP Release Notes (FPGA-RN-02114).
Resource Utilization	Supported User Interface	N/A
	Resources	Refer to Appendix A. Resource Utilization.
Design Tool Support	Lattice Implementation	IP v1.2.0 – Lattice Radiant Software 2026.1, Lattice Propel™ Builder 2026.1
	Synthesis	Synopsys® Synplify Pro®
	Simulation	QuestaSim

Note:

1. In some instances, the IP may be updated without changes to the user guide. This user guide may reflect an earlier IP version but remains fully compatible with the later IP version. Refer to the IP Release Notes for the latest updates.

1.3. IP Support Summary

Table 1.2. VTM IP Support Readiness

Device Family	IP	Radiant Timing Model
Lattice Avant-AT-E, Avant-AT-G, Avant-AT-X	VTM	Preliminary
Certus-N2 (except LN2-CT-20ES)	VTM	Preliminary

1.4. Features

Key features of the VTM IP include:

- Up to six on-die temperature sensors
- Two on-die voltage sensors for power-supply voltages
- Static enable or disable of each individual sensor
- Sensor updates at fixed sample rates
- Temperature and voltage alarms
  Each sensor supports configurable upper and lower threshold values with hysteresis.

1.5. Licensing and Ordering Information

The VTM IP is provided at no additional cost with the Lattice Radiant software.

1.6. Naming Conventions

1.6.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.6.2. Signal Names

- _*n* are active low signals, asserted when the value is logic 0.
- _*i* are input signals.
- _*o* are output signals.
- _*io* are bi-directional input/output signals.

2. Functional Description

2.1. IP Architecture Overview

The VTM IP contains separate interfaces for monitoring current sensor values and detecting and clearing alarms.

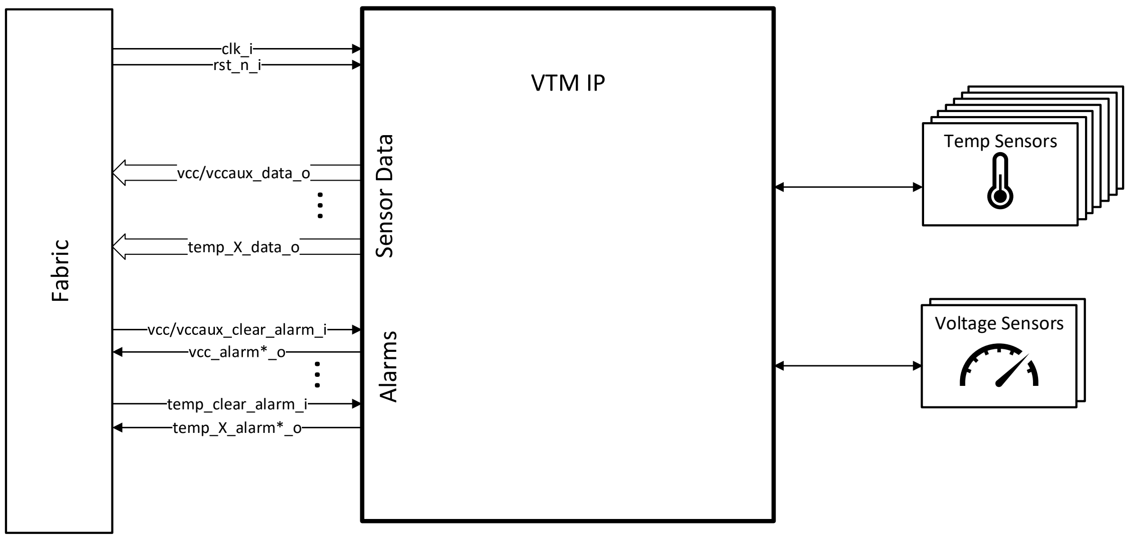

Figure 2.1. VTM IP Block Diagram

2.2. Clocking

2.2.1. Clocking Overview

The VTM IP uses a single clock domain (clk_i). The frequency of this clock is provided by the corresponding parameter to the IP for sensor update frequency calculations.

2.3. Reset

2.3.1. Reset Overview

The VTM IP uses a single reset domain. rst_n_i is used as the system asynchronous reset, which is active low. Reset handling should be done on the system level outside of this IP.

2.4. Sensor Data

The VTM IP sensors are available to you through the sensor data ports. The update rate of the sensor is consistent to allow fixed-time filters on the sensor values. The sensor data is a fixed-point binary value as described below.

If a sensor is disabled in the IP parameters, its output ports are removed from the RTL module interface.

Each sensor has a set of output ports, such as xxx_valid_o, xxx_update_o, and xxx_data_o[11:0]. When the FPGA is configured, each sensor's xxx_valid_o signal is deasserted for an initialization period and then asserted while the output data is valid. If an internal fault is detected, then xxx_valid_o deasserts. After the initialization period, each sensor's output data is updated periodically and the xxx_update_o signal pulses for one clock cycle when the data is updated. This can be used to write the data into a FIFO or trigger an interrupt in a soft CPU for example.

Sensor xxx_data_o[11:0] output data is two's complement fixed-point binary. The upper bit is a sign bit, followed by integer bits, followed by fractional bits. For example, the VCC output value uses Q2.9 format, which means 1 sign, 2 integer bits, and 9 fractional bits. In this format, the binary value `001001100000` represents 1.1875 V, and breaks down like this:

`0 01 001100000 ->` `0` sign, `01` int, `001100000` fraction.

The `0` sign bit means positive, `01` int is 2^0 which equals 1, and `001100000` fraction is $2^{-3} + 2^{-4}$, or 0.1875.

A negative value example is `111110010000`, which represents –0.21875 V.

Negate (2's complement) `111110010000` to get positive number `= (1)00001110000`

`(1)00001110000 ->` 1 sign bit means negative, `00` int, `001110000` fraction = $2^{-3} + 2^{-4} + 2^{-5}$ = 0.21875.

The formats and resolution of each sensor output type is shown in Figure 2.2.

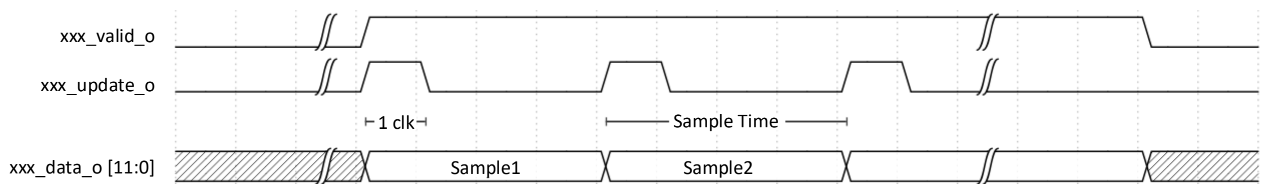

Figure 2.2. Sensor Signals

Table 2.1. Sensor Data Sample Rates and Format

Sensor	Sample Time	Sample Frequency	Output Format
VCC	333 µs	3 kHz	Q2.9: 1 sign, 2 integer, 9 fractional bits
VCCAUX	333 µs	3 kHz	Q2.9: 1 sign, 2 integer, 9 fractional bits
TEMP_X	10 ms	100 Hz	Q8.3: 1 sign, 8 integer, 3 fractional bits

The accuracy of the voltage and temperature sensors is determined by the hardware's capabilities. Some of this accuracy is compromised during the conversion between data formats. To minimize this loss, higher sampling and output resolutions are used. See Table 2.2.

Table 2.2. Sensor Accuracy and Resolution

Sensor	Sensor Accuracy	Sample Resolution	Output Resolution
VCC	14 mV	6 mV	2 mV
VCCAUX	28 mV	12 mV	4 mV
TEMP_X	3.0 °C	0.9 °C	0.125 °C

2.5. Alarms

Alarm outputs are asserted when an alarm triggers and stay asserted until you pulse the xxx_clear_alarm_i port for one clock cycle (Figure 2.3).

Alarms are set by crossing the threshold specified by xxx_ALARM_HIGH/LOW parameters. The xxx_ALARM_HIGH parameter specifies the upper-level voltage or temperature at which an alarm signals. The xxx_ALARM_LOW parameter specifies the lower-level voltage or temperature at which an alarm signals.

The alarms also include a hysteresis parameter to determine when the alarm can be triggered again. If a HIGH alarm is triggered, it is not retriggered until the level drops below the alarm level by the amount given by the HIGH hysteresis value. If the LOW alarm is triggered, it is not retriggered until the level rises above the alarm level by the amount given by the LOW hysteresis value. For example, if VCC_ALARM_HIGH is 1.0 V and VCC_HYSTERESIS_HIGH is 0.1 V, then the alarm triggers when VCC rises above 1.0 V and does not trigger again until the VCC level drops below 0.9 V and then up above 1.0 V later. Note that the output xxx_alarm_high_o is only cleared due to xxx_clear_alarm_i, and not due to values of the sensor level.

By default, the hysteresis value is ±0.1 V offset from the ALARM level for voltages and ±6 °C offset from the ALARM level for temperature. This default can be overridden by xxx_HYSTERESIS_HIGH or xxx_HYSTERESIS_LOW parameters.

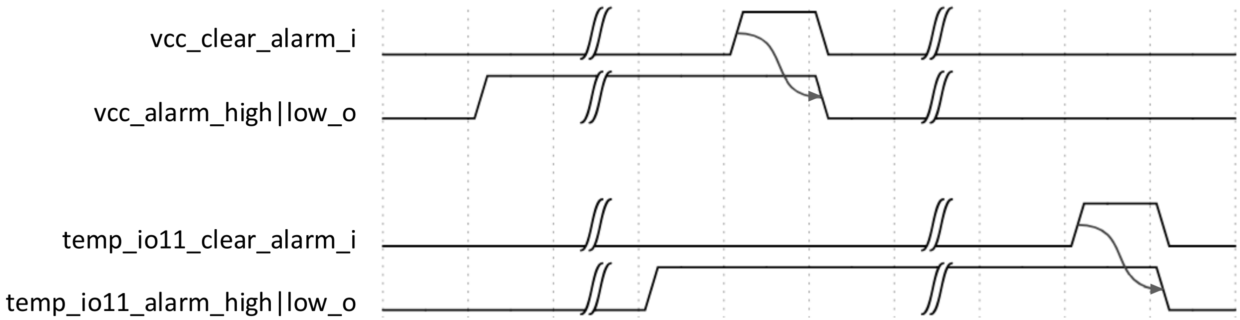

Figure 2.3. Alarm Signals

3. IP Parameter Description

The IP attributes shown in Table 3.1 are available to configure the IP for your use case.

Table 3.1. General Attributes

Attribute	Value	Note
ALARM_SUPPORT	Enabled, Disabled	Disabling this attribute removes the alarm port.
CLK_FREQUENCY	50–200 MHz	This attribute is used to calculate the timing of sensor samples.
MONITOR_VCC	Enabled, Disabled	Disabling this attribute removes the related sensor port.
MONITOR_VCCAUX	Enabled, Disabled	Disabling this attribute removes the related sensor port.
MONITOR_TEMP_SYSCONFIG	Enabled, Disabled	Disabling this attribute removes the related sensor port.
MONITOR_TEMP_IO3	Enabled, Disabled	Disabling this attribute removes the related sensor port.
MONITOR_TEMP_IO8	Enabled, Disabled	Disabling this attribute removes the related sensor port.
MONITOR_TEMP_IO9	Enabled, Disabled	Disabling this attribute removes the related sensor port.
MONITOR_TEMP_IO10	Enabled, Disabled	Disabling this attribute removes the related sensor port.
MONITOR_TEMP_IO11	Enabled, Disabled	Disabling this attribute removes the related sensor port.
VCC_HYSTERESIS_LOW	0.05 V, 0.1 V, 0.2 V, 0.5 V	Hysteresis for VCC low alarm. The attribute value is defaulted to 0.1 V.
VCC_HYSTERESIS_HIGH	0.05 V, 0.1 V, 0.2 V, 0.5 V	Hysteresis for VCC high alarm. The attribute value is defaulted to 0.1 V.
VCCAUX_HYSTERESIS_HIGH	0.05 V, 0.1 V, 0.2 V, 0.5 V	Hysteresis for VCCAUX high alarm. The attribute value is defaulted to 0.2 V.
VCCAUX_HYSTERESIS_LOW	0.05 V, 0.1 V, 0.2 V, 0.5 V	Hysteresis for VCCAUX low alarm. The attribute value is defaulted to 0.2 V.
TEMP_HYSTERESIS_HIGH	2 °C, 4 °C, 6 °C, 10 °C	Hysteresis for Temperature high alarms. The attribute value is defaulted to 6 °C.
TEMP_HYSTERESIS_LOW	2 °C, 4 °C, 6 °C, 10 °C	Hysteresis for Temperature low alarms. The attribute value is defaulted to 6 °C.
VCC_ALARM_HIGH	–0.486 to 2.385 V	Unused if ALARM_SUPPORT is disabled.
VCC_ALARM_LOW	–0.486 to 2.385 V	Unused if ALARM_SUPPORT is disabled.
VCCAUX_ALARM_HIGH	–0.243 to 1.192 V	Unused if ALARM_SUPPORT is disabled.
VCCAUX_ALARM_LOW	–0.243 to 1.192 V	Unused if ALARM_SUPPORT is disabled.
TEMP_SYSCONFIG_ALARM_HIGH	–60.6 to 158.6 °C	Unused if ALARM_SUPPORT is disabled.
TEMP_SYSCONFIG_ALARM_LOW	–60.6 to 158.6 °C	Unused if ALARM_SUPPORT is disabled.
TEMP_IO3_ALARM_HIGH	–60.6 to 158.6 °C	Unused if ALARM_SUPPORT is disabled.
TEMP_IO3_ALARM_LOW	–60.6 to 158.6 °C	Unused if ALARM_SUPPORT is disabled.
TEMP_IO8_ALARM_HIGH	–60.6 to 158.6 °C	Unused if ALARM_SUPPORT is disabled.
TEMP_IO8_ALARM_LOW	–60.6 to 158.6 °C	Unused if ALARM_SUPPORT is disabled.
TEMP_IO9_ALARM_HIGH	–60.6 to 158.6 °C	Unused if ALARM_SUPPORT is disabled.
TEMP_IO9_ALARM_LOW	–60.6 to 158.6 °C	Unused if ALARM_SUPPORT is disabled.
TEMP_IO10_ALARM_HIGH	–60.6 to 158.6 °C	Unused if ALARM_SUPPORT is disabled.
TEMP_IO10_ALARM_LOW	–60.6 to 158.6 °C	Unused if ALARM_SUPPORT is disabled.
TEMP_IO11_ALARM_HIGH	–60.6 to 158.6 °C	Unused if ALARM_SUPPORT is disabled.
TEMP_IO11_ALARM_LOW	–60.6 to 158.6 °C	Unused if ALARM_SUPPORT is disabled.

4. Signal Description

This section describes the VTM IP ports.

Table 4.1. I/O Port List

Port	Width	Direction	Description
Clock and Reset			
clk_i	1	input	System clock, 50 to 200 MHz
rst_n_i	1	input	System asynchronous reset, active low
Sensor Data			
vcc_valid_o	1	output	VCC sensor data valid
vcc_update_o	1	output	VCC sensor data updated
vcc_data_o	12	output	VCC sensor data
vccaux_valid_o	1	output	VCCAUX sensor data valid
vccaux_update_o	1	output	VCCAUX sensor data updated
vccaux_data_o	12	output	VCCAUX sensor data
temp_sysconfig_valid_o	1	output	TEMP_SYSCONFIG sensor data valid
temp_sysconfig_update_o	1	output	TEMP_SYSCONFIG sensor data updated
temp_sysconfig_data_o	12	output	TEMP_SYSCONFIG sensor data
temp_io3_valid_o	1	output	TEMP_IO3 sensor data valid
temp_io3_update_o	1	output	TEMP_IO3 sensor data updated
temp_io3_data_o	12	output	TEMP_IO3 sensor data
temp_io8_valid_o	1	output	TEMP_IO8 sensor data valid
temp_io8_update_o	1	output	TEMP_IO8 sensor data updated
temp_io8_data_o	12	output	TEMP_IO8 sensor data
temp_io9_valid_o	1	output	TEMP_IO9 sensor data valid
temp_io9_update_o	1	output	TEMP_IO9 sensor data updated
temp_io9_data_o	12	output	TEMP_IO9 sensor data
temp_io10_valid_o	1	output	TEMP_IO10 sensor data valid
temp_io10_update_o	1	output	TEMP_IO10 sensor data updated
temp_io10_data_o	12	output	TEMP_IO10 sensor data
temp_io11_valid_o	1	output	TEMP_IO11 sensor data valid
temp_io11_update_o	1	output	TEMP_IO11 sensor data updated
temp_io11_data_o	12	output	TEMP_IO11 sensor data
Alarms (the ports are removed if ALARM_SUPPORT == DISABLED)			
vcc_clear_alarm_i	1	input	Clear VCC alarm
vcc_alarm_high_o	1	output	VCC high alarm
vcc_alarm_low_o	1	output	VCC low alarm
vccaux_clear_alarm_i	1	input	Clear VCCAUX alarm
vccaux_alarm_high_o	1	output	VCCAUX high alarm
vccaux_alarm_low_o	1	output	VCCAUX low alarm
temp_sysconfig_clear_alarm_i	1	input	Clear TEMP_SYSCONFIG alarm
temp_sysconfig_alarm_high_o	1	output	TEMP_SYSCONFIG high alarm
temp_sysconfig_alarm_low_o	1	output	TEMP_SYSCONFIG low alarm
temp_io3_clear_alarm_i	1	input	Clear TEMP_IO3 alarm
temp_io3_alarm_high_o	1	output	TEMP_IO3 high alarm
temp_io3_alarm_low_o	1	output	TEMP_IO3 low alarm
temp_io8_clear_alarm_i	1	input	Clear TEMP_IO8 alarm
temp_io8_alarm_high_o	1	output	TEMP_IO8 high alarm
temp_io8_alarm_low_o	1	output	TEMP_IO8 low alarm

Port	Width	Direction	Description
temp_io9_clear_alarm_i	1	input	Clear TEMP_IO9 alarm
temp_io9_alarm_high_o	1	output	TEMP_IO9 high alarm
temp_io9_alarm_low_o	1	output	TEMP_IO9 low alarm
temp_io10_clear_alarm_i	1	input	Clear TEMP_IO10 alarm
temp_io10_alarm_high_o	1	output	TEMP_IO10 high alarm
temp_io10_alarm_low_o	1	output	TEMP_IO10 low alarm
temp_io11_clear_alarm_i	1	input	Clear TEMP_IO11 alarm
temp_io11_alarm_high_o	1	output	TEMP_IO11 high alarm
temp_io11_alarm_low_o	1	output	TEMP_IO11 low alarm

5. Designing with the IP

This section provides information on how to generate the IP using the Lattice Radiant software and how to run simulation and synthesis. For more details on the Lattice Radiant software, refer to the Lattice Radiant Software User Guide.

5.1. Generating and Instantiating the IP

You can use the Lattice Radiant software to generate IP modules and integrate them into a device architecture. The steps below describe how to generate the VTM IP in the Lattice Radiant software.

To generate the VTM IP:

1. Create a new Lattice Radiant software project or open an existing project.
2. In the **IP Catalog** tab, double-click **Voltage Temperature Monitor** under the **Architecture_Modules** category. The **Module/IP Block Wizard** opens, as shown in Figure 5.1. Enter values in the **Component name** and the **Create in** fields and click **Next**.

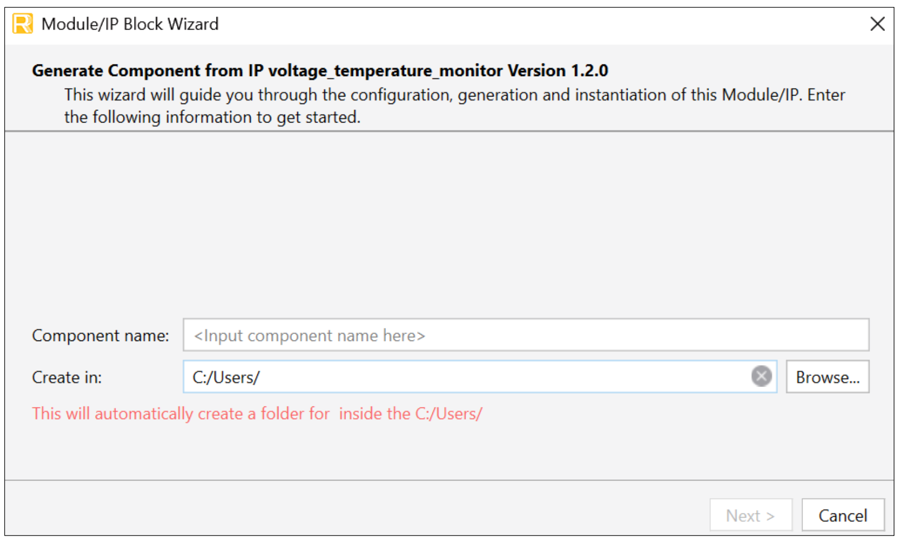

Figure 5.1. Module/IP Block Wizard

3. In the next **Module/IP Block Wizard** window, customize the selected VTM IP using drop-down lists and check boxes. Figure 5.2 shows an example configuration of the VTM IP. For details on the configuration options, refer to the IP Parameter Description section.

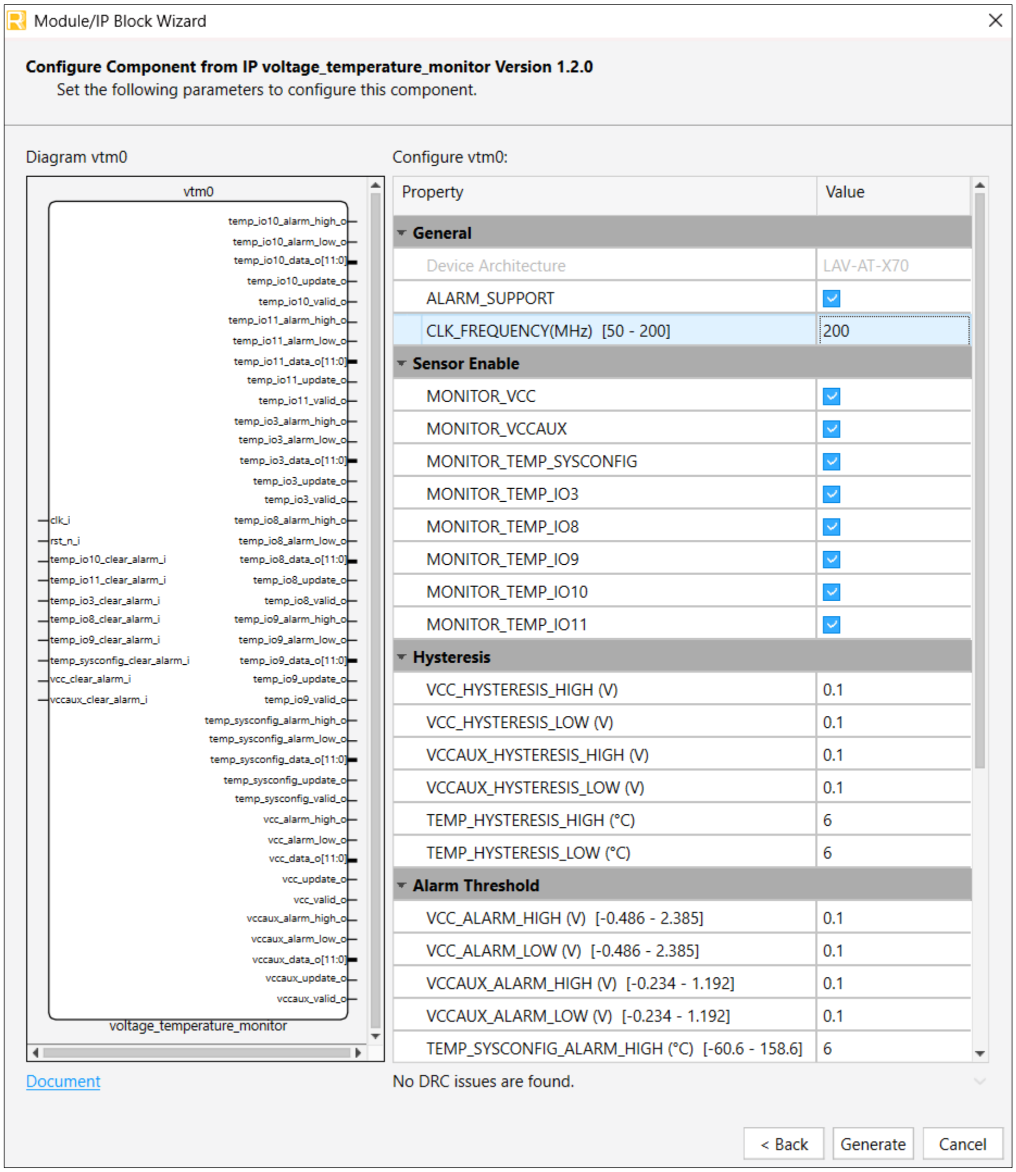

Figure 5.2. IP Configuration

4. Click **Generate**. The **Check Generated Result** dialog box opens, showing design block messages and results (Figure 5.3).

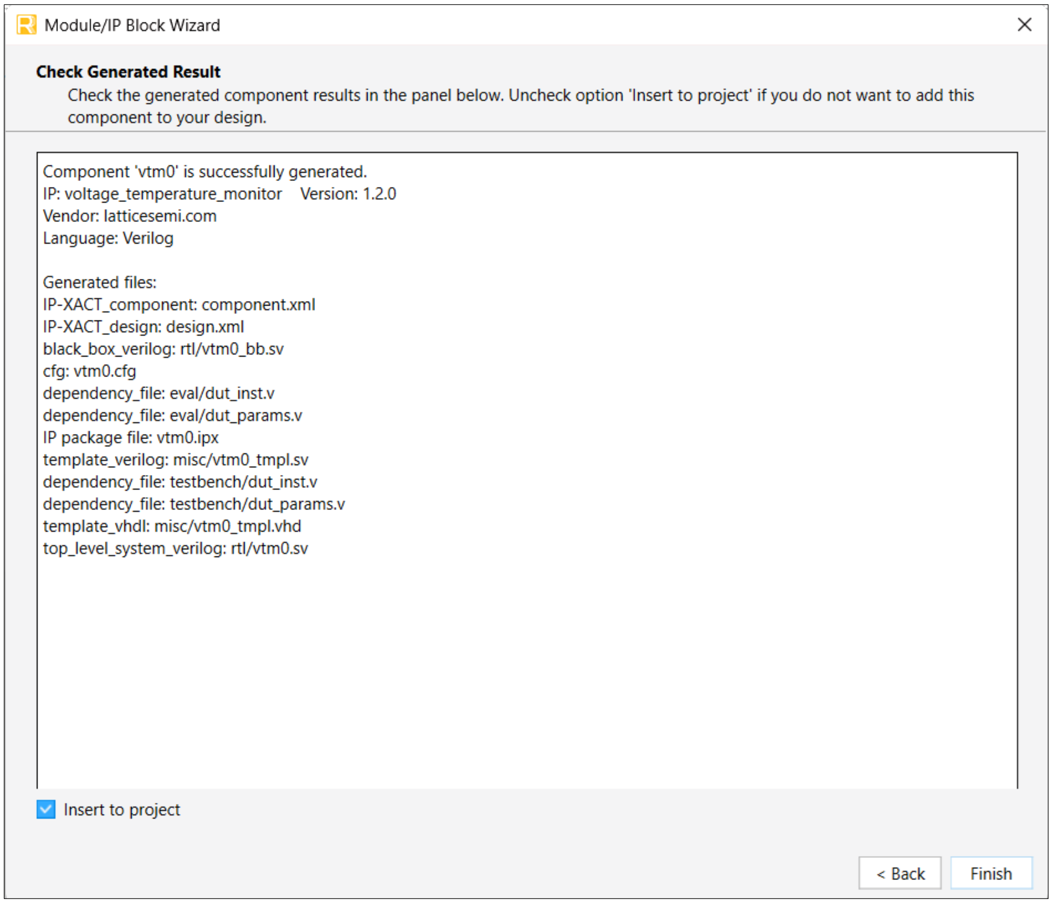

Figure 5.3. Check Generated Result

5. Click **Finish**. All the generated files are placed under the directory paths in the **Create in** and the **Component name** fields shown in Figure 5.1.

5.1.1. Generated Files and File Structure

The generated VTM IP package includes the closed-box (<Component name>_bb.v) and instance templates (<Component name>_tmpl.v/vhd) that can be used to instantiate the core in a top-level design. An example RTL top-level reference source file (<Component name>.v) that can be used as an instantiation template for the module is also provided. You may also use this top-level reference as the starting template for the top-level of your complete design. The generated files are listed in Table 5.1.

Table 5.1. Generated File List

Attribute	Description
<Component name>.ipx	This file contains the information on the files associated to the generated IP.
<Component name>.cfg	This file contains the parameter values used in IP configuration.
component.xml	Contains the ipxact: component information of the IP.
design.xml	Documents the configuration parameters of the IP in the IP-XACT 2014 format.
rtl/<Component name>.v	This file provides an example RTL top file that instantiates the module.
rtl/<Component name>_bb.v	This file provides the synthesis closed-box.
misc/<Component name>_tmpl.v misc /<Component name>_tmpl.vhd	These files provide instance templates for the module.

5.2. Design Implementation

Completing your design includes additional steps to specify analog properties, pin assignments, and timing and physical constraints. You can add and edit the constraints using the Device Constraint Editor or by manually creating a Physical Design Constraint (PDC) file.

Post-Synthesis constraint files (.pdc) include both timing and non-timing constraint .pdc source files for storing logical timing or physical constraints. Constraints that are added using the Device Constraint Editor are saved to the active .pdc file. The active post-synthesis design constraint file is then used as input for post-synthesis processes.

Refer to the relevant sections in the Lattice Radiant Software User Guide for more information on how to create or edit constraints and how to use the Device Constraint Editor.

5.3. Timing and Physical Constraint

The following line is the minimum constraint requirement of the IP to be added in the .pdc file to generate a 100 MHz clock source for the IP:

```
create_clock -name {clk_i} -period 10 [get_ports clk_i]
```

Appendix A. Resource Utilization

Table A.1 shows a sample resource utilization of the VTM IP on a LAV-AT-X70-1LFG676C device.

Table A.1. Resource Utilization

IP Configuration	LUTs	Registers	EBR	ASIC Component	Target Device	Synthesis Tool
Default	2385	1857	10	1	LAV-AT-X70-1LFG676C	Synplify Pro

References

- Lattice Avant-E Family Devices web page
- Lattice Avant-G Family Devices web page
- Lattice Avant-X Family Devices web page
- Lattice Certus-N2 Family Devices web page
- Voltage Temperature Monitor IP Release Notes (FPGA-RN-02114)
- Lattice Radiant FPGA design software
- Lattice Propel Design Environment web page
- Lattice Radiant Timing Constraints Methodology (FPGA-AN-02059)
- Lattice Insights for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, please refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Note: In some instances, the IP may be updated without changes to the user guide. The user guide may reflect an earlier IP version but remains fully compatible with the later IP version. Refer to the IP Release Notes for the latest updates.

Revision 1.0, IP v1.2.0, June 2026

Section	Change Summary
All	Initial release.

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