Lattice Radiant 2025.2.1 Software Release Notes

Welcome to Lattice Radiant® software, the complete design environment for Lattice Semiconductor Field Programmable Gate Arrays (FPGAs).

What's New in Radiant 2025.2.1 Software

- **Device Support:**
  - Certus-NX™ (LFD2NX)
    - 35 (-7/-8/-9) 1.0V (COM/IND) – CABGA256
    - 65 (-7/-8/-9) 1.0V (COM/IND) – CABGA256
  - MachXO4™ (LFMXO4)
    - The –6 speed grade has been removed for the following devices:
      - 015HE (-5) 1.2V (COM/IND) – UUG36
      - 025HE (-5) 1.2V (COM/IND) – UUG49
      - 050HE (-5) 1.2V (COM/IND) – UUG81
    - The following device, previously supported in Radiant 2025.2, has been removed in this release:
      - 050HE (-5/-6) 1.2V (COM/IND) – TSG144

- **Tool and Other Enhancements**
  - **Radiant software –** Radiant 2025.2.1 is a full standalone release and can be installed directly without Radiant 2025.2.
  - **Installation**
    - After downloading and extracting the 2025.2.1.321.0_Radiant folder, launch the installation by double-clicking **2025.2.1.321.0_Radiant.exe**.
    - Radiant 2025.2.1 includes enhanced installer validation to prevent incomplete or corrupted installations caused by certain antivirus software.
    - The installer has been enhanced to display an error message when DLL loading fails due to potential antivirus interference, directing you to verify

the antivirus configuration (for example, by whitelisting the affected Radiant DLLs).

- **Bitstream** – USERCODE has been added to the bitstream options to enable support for server designs.
- **Programmer** – Warm reboot option has been added to the ESFB operations in Radiant Programmer for LFMXO5-15D, LFMXO5-55TD, and LFMXO5-55TDQ devices.
- **Power Calculator** – The power model used for Avant-EGX HPIO I/Os, including DDRPHY and I/O termination, has been updated to reflect the latest silicon-correlated data. This improves the accuracy of power estimates for Avant-EGX designs.

Updating Projects from an Earlier Version

If you want to work on a design project created with an earlier version of Radiant software, it may be necessary to re-create some IP, per the procedures described in the following table.

These procedures adapt the project for the changes in Radiant software.

Versions	IP Regeneration Procedures			
	Avant (LAV-AT)	**MachXO4 (LFMXO4)**	**CrossLink-NX (LIFCL), Certus-N2 (LN2-CT-ES), Certus-NX (LFD2NX), Certus-NX-RT (UT24C), CertusPro-NX (LFCPNX), and CertusPro-NX-RT (UT24CP), MachXO5-NX (LFMXO5)**	**Description**
2025.2.1	SEDC Controller	FIFO_DC RAM_DP_True	N/A	These IP used in designs created in Radiant 2025.2 or earlier must be re-generated in Radiant 2025.2.1.

Supported Devices

Lattice Radiant software can be used with either a free license or a subscription license. The two licenses provide access to different device families.

Device Family	Free License	Subscription License
iCE40 UltraPlus (iCE40UP)	◀	◀
Lattice Avant (LAV-AT)		◀
CertusPro™-NX (LFCPNX)	Evaluation Mode	◀
Certus-NX (LFD2NX)	◀	◀
Certus-N2 (LN2-CT-ES)		◀
MachXO4 (LFMXO4)	◀	◀
MachXO5-NX (LFMXO5-15D)[1]		◀
MachXO5-NX (LFMXO5-20TD)[1]		◀
MachXO5-NX (LFMXO5-20TDQ)[1]		◀
MachXO5-NX (LFMXO5-25)	◀	◀
MachXO5-NX (LFMXO5-100T)	Evaluation Mode	◀
MachXO5-NX (LFMXO5-30TD)[1]		◀
MachXO5-NX (LFMXO5-30TDQ)[1]		◀
MachXO5-NX (LFMXO5-35)	◀	◀
MachXO5-NX (LFMXO5-35T)	Evaluation Mode	◀
MachXO5-NX (LFMXO5-55T)	Evaluation Mode	◀

Device Family	Free License	Subscription License
MachXO5-NX (LFMXO5-55TD)[1]		◄
MachXO5-NX (LFMXO5-55TDQ)[1]		◄
MachXO5-NX (LFMXO5-65)	◄	◄
MachXO5-NX (LFMXO5-65T)	Evaluation Mode	◄
CrossLink-NX (LIFCL)	◄	◄
CrossLink-NX (LIFCL-33U)	Evaluation Mode	◄
Certus-NX-RT (UT24C)	Evaluation Mode	◄
CertusPro-NX-RT (UT24CP)	Evaluation Mode	◄

1. To enable this device, please submit a support ticket.

Support for Third-Party Synthesis and Simulator Tools

The Synopsys Synplify Pro® for Lattice synthesis tool and the Siemens QuestaSim® Lattice Edition simulator tools are included in the Radiant software.

- **Synopsys Synplify Pro FPGA synthesis software version W-2025.03LR-SP1**
  - Release Notes for Synplify Pro are located in ..\<*install_directory*>\radiant\2025.2.1\synpbase\doc\. The file name is release_notes.pdf.
  - A full set of documents for Synplify Pro are also located in \<*install_directory*>\radiant\2025.2.1\synpbase\doc\.
- **Siemens QuestaSim Lattice Edition 2025.2**
  - Release Notes for QuestaSim Lattice Edition are located in <install_directory>\radiant\2025.2.1\questasim\. The file names are RELEASE_NOTES.html or RELEASE_NOTES.txt.

  - A full set of documents for QuestaSim Lattice Edition are located in <install_directory>\radiant\2025.2.1\questasim\docs\pdfdocs.
- **Siemens Questa® 2022.3**
- **Cadence Xcelium® 24.03.003**
- **Synopsys VCS® U-2023.03-SP2**

Help Resources

- Online Help updated with CertusPro-NX (LFCPNX), Certus-NX (LFD2NX), MachXO4 (LFMXO4), MachXO5-NX (LFMXO5), CrossLink-NX (LIFCL), Certus-NX-RT (UT24C), CertusPro-NX-RT (UT24CP), and Lattice Avant (LAV-AT) content.
- To view the Online Help, start the Lattice Radiant software and select the 

"Getting Started" icon under Information Center.

  Note: The Firefox Snap install is not supported if you are using Ubuntu 20.04 or 18.04 to access the Radiant Help. This is a result of the snap install's inability to open local HTML pages. You may reinstall the latest version of Firefox using Apt install. For installation instructions, please refer to this guide.

System Requirements

The following shows the basic system requirements for Radiant software:

- Intel x86 64-bit or 64-bit-compatible PC
- OS Support:

64-bit OS	Radiant	Synplify Pro	QuestaSim
Windows 10	✓	✓	✓
Windows 11	✓	✓*	✓
Red Hat Enterprise Linux 8.10	✓	✓	✓
Ubuntu version 24.04 LTS	✓	✓*	✓*
Ubuntu version 22.04 LTS	✓	✓*	✓*

***Note**: The third-party tools have been tested by Lattice on the listed platforms, but the vendors do not officially support them.

- Approximately 50GB free disk space

- Computer Memory Requirement:
  - Nexus – 16GB
  - LAV-AT– 32GB Recommended for running a single project. If running multiple projects, the memory requirement will be higher.
- 1024 X 768 graphics display
- Network adapter for license and network connectivity
- A Web browser with JavaScript capability
- Acrobat Reader

Issues Fixed in this Release

The following known issues are fixed in this release. Their workarounds are no longer needed.

When using Radiantc for ECO flows, the eco_config_memory command requires the design database to be initialized first. If des_read_udb is not executed before eco_config_memory, memory configuration will fail.

Devices affected: Certus-NX (LFD2NX)

Bug number: DNG-27493

Internal PLL of MIPI D-PHY does not lock when clocked by an external PLL with fractional clocks.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-24807

Huge IOLOGIC hold-time increase when switching from –8 to –M speed grade causes contradictory hold-timing results.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-27259

Programmer fails to launch when a non-Lattice FTDI programming cable is connected.

Devices affected: All devices

Bug number: DNG-31044

MAP error blocking ldc_set_location constraints on MPPHY refclk pins.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-30953

In some LAV-AT designs with heavily cascaded DSP chains, Place and Route may fail with no error message.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-30749

When using the MachXO4 device in Power Calculator, the reported dynamic LUT power is significantly higher than expected.

Devices affected: MachXO4 (LFMXO4)

Bug number: DNG-30671

CREB model: no post-synthesis simulation file generated due to unencrypted licensed module

Devices affected: MachXO4 (LFMXO4)

Bug number: DNG-30634

Incremental synthesis fails with compile points but passes with hard type for JRC design.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-29944

Post-synthesis TCE does not infer the correct clock frequency from PLL.

Devices affected: MachXO4 (LFMXO4)

Bug number: DNG-29970

Standalone Physical Designer application fails to launch in Linux.

Devices affected: All devices

Bug number: DNG-29701

Incorrect Dual Boot Behaviour with Specific sysCONFIG Settings.

Devices affected: MachXO4 (LFMXO4)

Bug number: DNG-29393

SEI Editor generates incorrect SEI information.

Devices affected: MachXO4 (LFMXO4)

Bug number: DNG-29364

Bitstream generation may error out when specifying custom idcode (MY_ASSP=ON).

Devices affected: MachXO4 (LFMXO4)

Bug number: DNG-29152

Password may still show up even though the Hide/Show Password is checked/unchecked in the bitstream security settings GUI.

Devices affected: All devices

Bug number: DNG-29999

During LSE synthesis in Radiant 2025.2, the expected critical warning CRITICAL <35001747> – Bit(s) of a register stuck at '0' may not appear even when the condition exists.

This warning is intended to alert users about registers that are stuck at zero.

Devices affected: All devices

Bug number: DNG-29724

Simulation Wizard GUI may issue a false error message “Simulation top parsing failed” when LPDDR4 IP is used. This does not affect the simulation.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-29676

Cannot constrain MIPI HSRXEN pin of soft DPHY in both Avant and Nexus devices.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-29657

When an IP’s constraints.sdc file contains a set_false_path, the constraint is silently dropped during synthesis.

Devices affected: Lattice Avant (LAV-AT-E70), CrossLink-NX (LIFCL)

Bug number: DNG-29653

Pre-Synthesis Constraint Editor may experience a segmentation fault when adding set_max_delay/set_min_delay constraint into the project without any constraint file set in the original project through Pre-Synthesis Timing Constraint Editor.

Devices affected: All devices

Bug number: DNG-29570

The bitstream hardware data status of LFD2NX-35/65 is missing.

The bitstream hardware data status is Preliminary.

Devices affected: Certus-NX (LFD2NX-35, LFD2NX-65)

Bug number: DNG-28463

The power file revision is shown as advanced in LFMXO5-35/35T/65/65T devices.

The power file revision should be Preliminary.

Devices affected: MachXO5-NX (LFMXO5-35, LFMXO5-35T, LFMXO5-65, LFMXO5-65T)

Bug number: DNG-26755

MachXO4 internal flash: .sed and .sea file generation error.

Devices affected: MachXO4 (LFMXO4)

Bug number: DNG-30450

IBIS hardware data status is not available in the IBIS reports for all LFMXO4-080HE packages.

Devices affected: MachXO4 (LFMXO4)

Bug number: DNG-29994

When simulating certain IP cores (PCIe IP, MPCS IP, 10G MAC IP, SLVS-EC IP) using QuestaSim Lattice Edition, repeated warnings appear indicating that non-differential clock signals are being used.

The message typically states that the input signals (e.g., CLKP and CLKN) are not differential. This warning can be ignored if the functionality is correct.

Devices affected: Certus-NX (LFD2NX)

Bug number: DNG-30104

In Radiant 2025.2, the Place and Route (PAR) Design process completes successfully even though the PAR Utilization Summary reports more than 100% SLICE for LFD2NX-28.

Devices affected: Certus-NX (LFD2NX-28)

Bug number: DNG-30080

In Radiant 2025.2, the Programmer utility does not display the bitstream checksum value.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-30013

The VHDL testbench template utility in Radiant may fail to generate a testbench and flags errors. These errors are not caused by the user's design and should be ignored.

This only affects VHDL testbench generation. Verilog designs have no issues in generating testbenches.

Devices affected: All devices

Bug number: DNG-29978

When a .fdc constraints file is used for synthesis, Synplify Pro issues an error message "Input file <file>.fdc does not end with .ldc. Please provide a valid file type"

Devices affected: All devices

Bug number: DNG-29306

When opening the Place & Route Timing Analysis report in Radiant, the displayed content may appear truncated, preventing users from viewing the full report details. This is a display issue in the report viewer.

Devices affected: All devices

Bug number: DNG- 29808

When opening or double-clicking an .ipx file, the Module/IP Block Wizard window may appear too small, making its contents difficult to read or navigate. This is a GUI scaling issue and does not affect the functionality of the IP configuration.

Devices affected: All devices

Bug number: DNG-29827

Post synthesis simulation may fail when top-level module is not specified in the project, and the design is compiled from the command-line using LSE synthesis engine in Linux OS.

Devices affected: MachXO5 (LFMXO5)

Bug number: DNG-29792

Known Issues for Radiant 2025.2.1

The following are known issues for Radiant Software 2025.2.1. For assistance with these issues, please contact Lattice Technical Support.

Installer displays version as “2025.2” instead of “2025.2.1”.

Workaround:

1. At the Start Menu shortcut prompt, enter the following path: Lattice Radiant Software 2025.2.1.
2. After installation is complete, rename the desktop icon to “Radiant Software 2025.2.1”.

Devices affected: All devices

Bug number: DNG-31794, DNG-31796, DNG-31798

Some Avant clock powers are not calculated when using Radiant 2025.2.

The dynamic power for certain clock tree routing arcs is not properly accounted for in the Avant devices; you may notice reduced dynamic power for the clock in some of their designs.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-31638

DELAYE used on a clock path can cause the delayed output to be stuck low in hardware.

For Avant devices, a design that routes a clock through a DELAYE element to drive a delayed output can result in the delayed output pin being stuck low in hardware, even though post-map and post-PAR simulation waveforms appear correct. The issue is related to an incorrect DELAYMUX selection for the DELAYE path in the generated bitstream.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-31260

Timing report shows infinite slack on output paths when set_max_delay uses datapath_only.

In some designs that use a generated clock on an output port, applying a set_max_delay constraint with the datapath_only option on output paths can cause the timing report to show INF (infinite) slack for those paths. The affected paths are not reported as violating even when they should, because the tool initializes timing at the generated clock output with a default clock phase that does not match the generated clock definition.

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-29538

The des_report_flow_status command may show incomplete status after restoring a milestone with prj_open_milestone, because it relies on session history rather than the design database.

Devices affected: All devices

Bug number: DNG-29723

You may encounter intermittent LSE timing analysis failure for some designs.

Some designs targeting LFD2NX can fail intermittently during LSE timing analysis with Done error code 1. The failure is observed in approximately half of synthesis runs while resource usage and results appear identical between passing and failing runs.

Workaround: Use Synplify instead of LSE to synthesize the design to avoid the intermittent LSE and timing analysis failure.

Devices affected: Certus-NX (LFD2NX)

Bug number: DNG-31070

DSP reset configuration in asynchronous mode can cause functional failure.

In Nexus DSP blocks, configuring the PREADD9 RESET attribute for asynchronous reset and tying the reset port to static 0 can leave the DSP multiplier output stuck at zero, causing functional failure even though timing and simulation may appear correct.

Workaround: Use dynamic reset or configure the DSP to use synchronous reset mode instead of tying an asynchronous reset port to static 0.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-30673

GDDR aligned mode capture clock phase not configured for Avant device.

When GDDR RX in Avant devices is configured to Aligned mode, the capture clock lacks the expected phase shift or delay, which can cause timing analysis failures.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-31269

There is a higher latency in ODDR primitives when running with XPROP enabled.

Enabling XPROP in simulation causes higher D to Q latency through the ODDRX4DQS primitive. With XPROP enabled, the DQS output starts toggling about two memory clock cycles (about 3.75 ns at 533.33 MHz) later than expected, leading to DDR violations such as DDR_NO_DQS_TRANSITION_DURING_WR.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-29397

PCIe primitive parameter overrides do not take effect.

PCIe primitive parameters set in the PCIE.v module are not correctly applied to the PCIe core registers in hardware or simulation. As a result, the PCIe link may fail to train or link up.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-28201

LFMXO4 FIP common user testbench uses GSR_N and fails simulation.

Customer testbenches in the common FIP folder use the GSR instance with port GSR_N. For LFMXO4 devices, the FIP expects GSRB with port GSR instead. When these common testbenches are used with LFMXO4 FIPs, simulation errors occur.

Devices affected: MachXO4 (LFMXO4)

Bug number: DNG-29490

You may encounter a Large RAM DP True synthesis error when Port B byte enable is used.

The Large RAM DP True (LRAM_DP_TRUE) IP can fail synthesis when Port B byte enable is enabled with 16 bit data width and output registers on both ports. The generated RTL creates an invalid ben_b_w part select, leading to errors such as index out of range and multiple non tristate drivers on ben_b_i[1].

Workaround: Do not use LRAM_DP_TRUE with byte enable enabled on both ports and output registers enabled on both ports. If the design allows, temporarily disable byte enable or the output register on one or both ports.

If you must use this configuration, a temporary RTL edit can be used: locate the generated RTL file for the instance, find the assign statement that defines the overflow padding for ben_b_w, and modify it to remove the extra +1 and match the ben_a_w form, for example:

assign ben_b_w[(BWID_B - 1):(BYTE_WIDTH_B - (BWID_B * i1))] = {(BYTE_WIDTH_B - (BWID_B * i1)){1'b1}} ;

Then rebuild the project using the edited RTL.

Devices affected: Certus-NX (LFD2NX)

Bug number: DNG-31307

Power Calculator report Effective Theta JA value does not match Power Calculator tool.

In this release, when User Entered Tj is used, the power calculator report shows a numeric Effective Theta JA value while the Power Calculator tool correctly shows N/A.

Devices affected: All devices

Bug number: DNG-30703

DQSBUF delay values in Timing Analyzer does not match with post PAR simulation.

For LFCPNX designs, DQSBUF shifted clock delays (DQSI2DQSR_DEL, S2DQSW_DEL) reported in Static Timing Analysis can differ significantly from post PAR simulation values. The STA reports about 0.5 ns larger delay than post PAR for arcs such as DQSI to DQSR90 and ECLKIN to DQSW270, which can cause confusion when correlating STA and simulation results.

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-30385

DDR3L and LPDDR4 differential clock may not be complementary on the LFCPNX device.

When using LFCPNX devices, DDR3L and LPDDR4 memory interfaces that use a differential clock (for example CK and CK#) may show non ideal differential behavior on the clock pair. The P and N pins of the DDR clock can overlap or appear non complementary on an oscilloscope, which can cause memory interface calibration or training to fail on hardware.

Workaround: Implement the DDR clock P and N pins as separate single ended pins instead of as a differential clock pair.

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-29849

FIFO testbench instantiates wrong GSR primitive for LN2-CT devices.

For LN2-CT FIFO Foundation IP, the generated testbench instantiates GSR instead of GSRA. Depending on the compiled simulation library for the selected device, simulation may fail with a module not found error.

Workaround: In the generated FIFO Foundation IP testbench, rename the GSR instance to use the GSRA primitive, for example change GSR to GSRA in the module instantiation.

Devices affected: Certus-N2 (LN2-CT-ES)

Bug number: DNG-26245

Synthesis fails with CPE segmentation violation when SentinelOne AV is active.

Synthesis may fail for both LSE and Synplify Pro with a CPE segmentation violation or synthesis.exe crash. The issue occurs only on machines where SentinelOne antivirus is active; the same designs complete synthesis successfully on systems without SentinelOne.

Devices affected: All devices

Bug number: DNG-31178

MAP ignores some user IO constraints in post synthesis constraints.

When IO settings for the same port are split across multiple ldc_set_port commands, MAP constraint clean up can treat the last constraint as a duplicate and drop it. As a result, some IO settings such as PULLMODE from the top level constraint file or IP constraints are not applied, and the implemented IO configuration does not match the user constraints.

Workaround: In the post synthesis constraint file, do not split IO settings across multiple ldc_set_port lines for the same port. For io_sda_z, specify the full IO configuration in a single line (matching the io_scl_z style), for example:

ldc_set_port -iobuf {PULLMODE=UP CLAMP=ON DIFFRESISTOR=OFF DRIVE=8 IO_TYPE=LVCMOS33} [get_ports io_sda_z]

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-31001

There are missing AXI4 Lite constraints when using encrypted IP for Avant devices.

For encrypted AXI4 Lite IP used with Avant devices in Radiant 2025.2, some dpram related false path constraints are not applied, causing hold timing violations. The same constraints are applied correctly, and timing violations do not occur when using the unencrypted IP with the same configuration.

Workaround: Update the AXI4 Lite constraints to replace the encrypted portion of the instance path (for example gen_pmi.gen_async.u_fifo) with a wildcard (/*/) so the constraints match the renamed instances in the encrypted IP. Use this with care to avoid unintentionally setting false paths on other parts of the design.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-29853

LRAM initialization from ECO Editor sets only 8 bits out of 32.

When initializing a 65536x8 LRAM from ECO Editor (all 1s or from a .mem file), only the first 8 bits of every 32 bit word are initialized correctly and the remaining 24 bits are left as 0 in the bitstream.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-29226

IO mode options are not available in Physical Designer for LFMXO4.

For LFMXO4 designs in Radiant 2025.2, IO mode options are missing in Physical Designer. IO related settings cannot be configured from Physical Designer and must be applied using constraints instead.

Workaround: Use Device Constraint Editor to create and modify IO related constraints, since IO mode cannot be set through Physical Designer for LFMXO4.

Devices affected: MachXO4 (LFMXO4)

Bug number: DNG-29150

Timing report critical path does not show DSP location in Device View.

In some designs, the critical path in the timing report does not highlight the DSP block in Device View because the DSP site location is not reported, so the path view cannot display the DSP instance.

Devices affected: All devices

Bug number: DNG-28388

Bounding Box Selected Instance Resource Count does not report register usage correctly.

In the Bounding Box user interface, Selected Instance Resource Count can show zero usage for selected registers or flops because the count is taken from the MAP resource usage report, which does not include these instances for the affected designs.

Devices affected: MachXO5-NX (LFMXO5)

Bug number: DNG-26318

There is an IBIS Model mismatch for Pull Mode and Series Resistance when using the LFMXO4 device.

In the LFMXO4 device family, pull mode and series resistance are not loaded correctly during IBIS report generation, which prevents the system from finding a matching IBIS model. When this issue occurs, you will see warning 1191010, and the affected input pins will not have IBIS information listed in the IBIS report.

Devices affected: MachXO4 (LFMXO4)

Bug number: DNG-31303

When using Structural Verilog (.vm) in the design flow, information about the synthesis attribute black_box_pad_pin “port_list” is not available in the online help.

Devices affected: All devices

Bug number: DNG-30152

In Radiant 2025.2, PAR ignores user location constraints for instantiated DCC and performs automatic placements of the instantiated DCCs.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-30001

Timing Analyzer ignores the Maximum Slack limit set by the user and displays all slacks. The display also has a mismatch in the units between Timing option setting and General information in the GUI.

This is a GUI issue and not a functional issue

Devices affected: All devices

Bug number: DNG-29930

Power Calculator DDRPHY tab activity inputs use AF and EF instead of RX/TX/IDLE.

In the Power Calculator DDRPHY tab, the AF and EF fields are still displayed instead of the RX percent, TX percent, IDLE percent, and data_H/data_L percentages. The RX, TX, and IDLE percentages must sum to 100%.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-31469

pmi_rom implementation for LFMXO4 may fail PAR with Synplify Pro.

Some LFMXO4 pmi_rom designs with large memory size or wide data width can fail place and route when synthesized with Synplify Pro, due to very high LUT4 usage instead of using EBRs.

Devices affected: MachXO4 (LFMXO4)

Bug number: DNG-29659

Timing violations may be reported when the sync_clk_i of the GDDR 7:1 Foundation IP is driven by the PLL IP clock.

The affected path is used only for clock synchronization reset and not for data transfer. The transition occurs only during the initialization sequence and does not occur during normal TX operation.

Workaround: Manually add the set_false_path constraint between eclk and sync_clk_i in the design PDC file or set the sync_clk_i to 25MHz.

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-31095

Maximum Slack Limit option in Timing Analyzer has no effect on reported paths.

In the Timing Analyzer, the Maximum Slack Limit setting is currently non-functional. Paths are reported regardless of the configured slack limit.

Devices affected: All devices

Bug number: DNG-30518

Power Calculator IO termination requires users to manually enter the external Rth and Vth values.

When using IO termination in Power Calculator, you must manually enter the external Rth and Vth values used in your design to ensure that power estimates are accurate.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-31409

LOC attribute may be ignored for output ports declared as reg when using Synplify Pro.

In Synplify Pro, a LOC attribute attached to an output port declared as a reg and driving a flip flop can be ignored. As a result, PAR may place the output on a different package pin than specified by the LOC. The issue is not seen with LSE or when the output is declared as a wire with the LOC on the IO net.

Devices affected: MachXO5 (LFMXO5)

Bug number: DNG-30603

Synplify optimization can cause undesired shift register output in post synthesis simulation.

In some Ethernet based designs targeting Avant devices, Synplify can over optimize shift register logic that implements a delay element. When the array in the shift register is optimized, the post synthesis simulation shows undesired output on the shift register logic output, even though timing analysis passes and LSE does not exhibit the issue.

Workaround: Use NOCLIP, SYN_PRESERVE, or SYN_KEEP attributes to prevent optimizing the array.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-25076

Reveal debug insertion can cause invalid EN_CIL and HSEL parameter values in DPHY CORE.

When Reveal is inserted into a design that instantiates DPHY CORE, Synplify can generate incorrect EN_CIL and HSEL parameter values for a secured DPHY instance.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-30353

ECO Editor updates to EBR-based ROM initialization may result in INITVAL contents that differ from IP-generated ROM initialization for the same data pattern.

When using the ECO flow to modify the initialization contents of EBR based ROMs, the resulting gate level memory initialization (INITVAL_xx) may not match the initialization produced by the IP Foundation (FIP) flow for the same intended data pattern. This can cause simulation and hardware behavior of ECO updated ROM contents to differ from the original FIP generated design, leading to potential functional mismatches.

Workaround: Avoid using the ECO editor to modify EBR ROM contents. Instead, update the ROM hex file and regenerate the ROM using the IP Foundation (FIP) flow, then rerun the full implementation flow (synthesis followed by place and route) so that the final gate level netlist uses consistent INITVAL_xx contents based on the updated hex file.

Devices affected: All devices

Bug number: DNG-30489

Unique ID field is not editable in Device Constraint Editor.

For MachXO4 devices, the Unique ID (formerly TraceID) field in the sysCONFIG settings of the Device Constraint Editor is not editable and is locked to the default value of "0000". You cannot configure a custom Unique ID value through the DCE GUI. This is a software limitation in the current release.

Workaround: None. This will be addressed in a future release.

Devices affected: MachXO4 (LFMXO4)

Bug number: DNG-29265

PROGRAMN pin cannot be used as GPIO on LIFCL-33U.

On the LIFCL-33U device, the sysConfig setting PROGRAMN_PORT = DISABLE is not supported. The PROGRAMN pin is always enabled via OTP and cannot be repurposed as a general-purpose I/O. Designs that attempt to set PROGRAMN_PORT = DISABLE will fail DRC.

Workaround: None. Do not use the PROGRAMN pin as GPIO on LIFCL-33U devices.

Devices affected: CrossLink-NX (LIFCL-33U)

Bug number: DNG-28738

When using Avant PLL IP configured with an LMMI interface, synthesis fails in Synplify Pro with an error. The issue occurs during synthesis and prevents successful compilation of the design.

Workaround:

- Use the PLL IP without the LMMI interface if possible.
- If LMMI functionality is required, consider alternative design approaches or contact Lattice support for guidance until a fix is available.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-27611

Router report shows more “signals not completely routed” than unrouted connections for JRC IDF design

For the JRC customer design in the IDF flow, the router summary report is inconsistent when routing fails.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-29810

When the width of ROM data in a memory initialization file is wider than the defined ROM width, Radiant issues warnings and ignores the extra bits.

The synthesis engine treats these extra bits as don’t-care values and ROM module may be optimized away during synthesis.
In contrast, Diamond enforces strict consistency between the ROM width and the initialization file width, resulting in an error instead of continuing.

Workaround:

- Ensure that the memory initialization file width matches the ROM width defined in your design.
- Treat Radiant warnings (e.g., CG1194, CG532, MO156) as critical and correct the file before synthesis.
- If strict error handling is required, add a manual check in your design flow to validate memory file widths.

Devices affected: MachXO4 (LFMXO4)

Bug number: DNG-29440

Avant MIPI D-PHY RX: Generated SCLK clock constraint missing in STA

In Avant designs that use the MIPI D-PHY RX soft IP, the automatically generated CREATE_GENERATED_CLOCK constraint for the byte clock SCLK (ECLKDIV output) may be missing its target frequency in the Static Timing Analysis (STA) report. In the Timing Wizard/Report (TWR/SDC section), this generated-clock constraint can also appear as ignored.

Workaround: Manually add an ECLK/SCLK clock constraint in your PDC/SDC file for the MIPI D-PHY clock pin so that Radiant can correctly derive and report the SCLK generated clock for Avant.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-28873

CONFIG_LMMI writes to enable multiboot may fail in hardware on CrossLink NX when using higher LMMICLK frequencies.

In Multiboot Reference Designs targeting CrossLink-NX, LMMI writes to CONFIG_LMMI can fail at LMMICLK frequencies above ~40 MHz, even though timing reports are clean. This may prevent the SPIM bit from being set in Control Register 0 and cause the multiboot sequence to fail.

Workaround: Constrain and operate LMMICLK at or below ~10–12 MHz when performing LMMI writes (e.g., when enabling multiboot).

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-30992

RISCV-based initialization of the DPHY IP fails when a Reveal Controller is present in the design

Designs that include a Reveal Controller do not support RISC-V–based initialization of the DPHY IP. The DPHY initialization fails when both are present in the design.

Workaround: Do not use Reveal Controller in designs that require DPHY initialization via RISC-V. Remove Reveal Controller to allow DPHY initialization to complete.

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-31268

In Radiant 2025.2, the SHAREDEBRINIT=Disable setting for MachXO4 devices does not match Diamond's behavior for MachXO3 devices.

When disabled:

- Radiant writes EBR initialization data only once in the JEDEC file.
- Diamond writes the same EBR initialization data N times where N is the number of EBRs used for initialization.

There is no functional impact on device operation because both approaches correctly initialize EBR contents.

Devices affected: MachXO4 (LFMXO4)

Bug number: DNG-30070

ECO memory initialization is not supported for LFMXO4 device.

The ECO Editor does not support memory initialization for LFMXO4 (MachXO4) devices. This feature, which is available for other device families, has not yet been implemented for MachXO4. The ECO_MEM information is not present in the post-synthesis UDB for this device family.

Devices affected: MachXO4 (LFMXO4)

Bug number: DNG-29952

IOs are missing in the Physical Designer Placement Mode.

Devices affected: MachXO4 (LFMXO4)

Bug number: DNG-29369

The DCC and DCM resource utility in PAR report are missing.

You can still view the usage in the clock report area of the PAR report.

Devices affected: MachXO4 (LFMXO4)

Bug number: DNG-29345

Internal device name is visible in DCE device part view.

Devices affected: MachXO4 (LFMXO4-015HE, LFMXO4-015HC, LFMXO4-050HC and LFMXO4-050HE) with specific packages (BFG256, BBG256 and BBG400)

Bug number: DNG-29144

Changing VCC in DCE and Standalone Timing Analyzer does not affect hold analysis. Hold Analysis always uses VCC Max for analysis.

Workaround: Manually select voltage during hold analysis. Holding uncertainty can be used to tighten constraints during placer or router.

Devices affected: All devices

Bug number: DNG-29957

LSE Synthesis may fail when CRC_Register attribute is used with an error:" CDC_Register chain cannot be fully determined for register…".

Devices affected: All devices

Bug number: DNG-29431

Radiant may crash in very rare cases during implementation when Pre-synthesis Constraints Editor is open.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-29819

Using Distributed RAM (DPRAM) for a shift-register path that feeds a Delay Element can cause the Delay Element output to behave incorrectly.

With syn_keep or syn_preserve applied to the shift array, simulation shows glitches, and Reveal capture shows unintended or corrupted data. The problem is observed in both pre-synthesis and post-synthesis Reveal.
Workaround:

- Avoid DPRAM for the shift chain feeding the Delay Element. Use EBR or PFU registers for the shift register resource.
    - In IP configuration, select EBR or Registers as the resource.
    - For inferred RTL, guide synthesis to map to block RAM or registers (e.g., set ramstyle to block RAM or registers in your synthesis attributes).
- If you must use DPRAM:
    - Keep the shift depth ≤ 32 where practical to reduce risk.
    - Remove syn_keep and syn_preserve on the internal shift array when not strictly required or apply them at module boundaries instead of the array element level.
- Reverify with simulation and Reveal after changing the resource selection. Designs using EBR or PFU registers do not show the issue.

Devices affected: Lattice Avant (LAV-AT-E70)

Bug number: DNG-29618

Gate-level timing simulation may show an unexpected jitter for PLL.

This only affects the gate level timing simulation and HW behavior is unaffected.

Devices affected: Lattice Avant (LAV-AT-E70)

Bug number: DNG-29299

LSE synthesis may fail without providing a clear error message if the design includes module instantiations that do not have instance names.

The same design may be compiled successfully with Synplify Pro but later fail during PAR.
Workaround:

- Always provide instance names for all module instantiations in your design.
- If the design fails without an error message, review the RTL for unnamed instances and update them accordingly.

Devices affected: Certus-NX (LFD2NX)

Bug number: DNG-29029

Radiant may crash during implementation when DCE is open.

Workaround: Close DCE and run implementation.

Devices affected: Certus-NX (LFD2NX-35, LFD2NX-65)

Bug number: DNG-28678

LSE synthesis may fail with an error if the project path length is too long. This occurs because the synthesis engine has a limit on the maximum path length it can handle for project files and directories.

Workaround:

- Shorten the project path by:
  - Moving the project to a directory closer to the root (e.g., C:\RadiantProjects\).
  - Reducing folder name lengths.
- Avoid using excessively long directory structures for project files.

Devices affected: All devices

Bug number: DNG-28606

Designs using nested VMs fail during post-synthesis.

Workaround: Do not use nested VMs. Instantiate VMs separately.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-27317

When using Synplify Pro, user-defined create_generated_clock constraints in the SDC file for PLL clock outputs may be overwritten by auto-generated PLL clock constraints if a Reveal Core is added to the design.

Without Reveal, user-defined constraints propagate correctly through synthesis and implementation. With Reveal present, the constraints are accepted during Constraint Propagation Engine (CPE) but fail to persist after synthesis.

Workaround:

- Define PLL clock constraints in the PDC file instead of SDC. PDC constraints are preserved even when Reveal is added.
- If SDC-based constraints are required, use post-synthesis Reveal debug flow.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-26270

Programming may fail when using compressed bitstreams.

Workaround: Use plain or uncompressed bitstream formats.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-26097

Radiant timing analysis for designs using LMMI_CLK / LMMI_CLKO may show:

- **A missing timing arc from OSCA to CONFIG_CLKRST_CORE on the LMMI clock path (this is a bug).**
- **A 0 ns net delay from CONFIG_CLKRST_CORE to CONFIG_LMMI (this is expected behavior per the current timing model).**

As a result, the report may present a direct path from the OSC IP to CONFIG_LMMI without explicitly reflecting the expected clock path delay from LMMI_CLK to LMMI_CLKO (i.e., OSCA → CONFIG_CLKRST_CORE).

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-27889

Standalone Timing Analyzer results may differ from RunSTA results even when using the same pdc file.

The results from RunSTA are correct.

Workaround: Avoid using Standalone Timing Analyzer and use RunSTA for debug.

Devices affected: Certus-NX (LFD2NX)

Bug number: DNG-27523

Timing analysis and the Tcl command “sta_get_slack -worst” may return different worst slack values.

The command may return a slack value, but it might not be the worst-case slack. The returned slack is valid, but it corresponds to a path that does not represent the worst slack.

In addition, the detailed timing report may contain some arrival values that are incorrect. However, the path of the report, the delays of the connections and arcs along the path, the required value, the arrival value used for slack computation, and the slack of the path are all correct.

Device affected: All devices

Bug number: DNG-27408

The location for a secured component (Hard DPHY) cannot be changed.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-24746

In PLL simulation, the phase stops moving when it goes over 360 degrees.

In a Phase-Locked Loop (PLL) simulation, the phase should not stop moving but only reset to stay within a specific range (such as 0°–360).

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-23458

RTL simulation of CONFIG_LMMIE and CONFIG_LMMIB primitives may fail or produce incorrect results.

When using CONFIG_LMMIE or CONFIG_LMMIB primitives in RTL simulation, the simulation may produce incorrect results or fail entirely. This is a simulation model issue and does not affect hardware behavior.

Devices affected: MachXO5-NX (LFMXO5)

Bug number: DNG-22187

Clocks using pclk routing and driving only fabric registers may have reduced minimum pulse width at higher speed grades.

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-21315

Synplify Pro synthesis may fail if the .sdc file contains a user-defined constraint referencing a hierarchical object that includes a dot (.). Example: top.inst/out.

Workaround:

- Create the constraint in the .pdc file instead of .sdc file.
- Use LSE for synthesis.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-20134

Inserting a Reveal Core may cause undesired toggling of the FIFO empty flag in pmi_fifo designs synthesized with Synplify Pro.

Workaround: Use Post-Synthesis Reveal Debug flow.

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-24358

In Certus-NX LRAM IP simulation, when DPS is asserted high, lram_ready may remain high instead of going low.

This does not affect HW functionality and only affects simulation.
Expected behavior: Driving DPS high powers down LRAM, so lram_ready should be low.

Devices affected: Certus-NX (LFD2NX)

Bug number: DNG-27555

Avant bitstream generation may consume significantly more host memory than reported.

During bitstream generation for Avant devices, the Bitgen process may consume significantly more system memory than the reported peak memory usage. This can result in unexpected host memory pressure and, in some cases, out-of-memory failures.

Workaround:

- Run Bitgen on hosts with additional available RAM.
- Do not rely on the reported peak memory usage values.
- Prefer machines with larger memory capacity or Linux hosts for improved stability.

Devices affected: Avant (LAV-AT)

Bug number: DNG-29447

Inserting Reveal during pre-synthesis causes change in the hierarchy names when OSC IP is used. It results in timing constraints that use hierarchical objects to be dropped.

Workaround: Use Post-Synthesis Reveal debug flow.

Devices affected: All devices

Bug number: DNG-29637

LRAM_DP_TRUE simulations may fail on Certus NX devices when “Invoke qrun” is enabled.

For Certus NX devices, enabling Invoke qrun during LRAM_DP_TRUE simulation may result in incorrect read data, error detection becoming stuck, or inconsistent memory initialization behavior.

Workaround:

- Disable "Invoke qrun" (recommended).
- If qrun is required, regenerate/update the testbench and restart from a clean state.

Devices affected: Certus-NX (LFD2NX)

Bug number: DNG-31309

LFMXO5-55TDQ device missing from primitive templates

The LFMXO5-55TDQ device is not listed in the Primitive Templates (Verilog/VHDL), preventing users from selecting it when generating primitive examples. This affects only the template-generation UI; the device can still be used normally when set in project settings.

Workaround:

- Select a similar LFMXO5 device in the Primitive Templates tool to generate reference examples.
- Manually adapt the template code as needed.
- Ensure the project device is correctly set to LFMXO5-55TDQ.

Devices affected: MachXO5-NX (LFMXO5-55TDQ)

Bug number: DNG-27155

Synthesis Fails when migrating pmi_ram_dp_true from MachXO3L to MachXO4

A design originally targeting MachXO3L in Diamond (using SynplifyPro) synthesizes successfully, but after migration to Radiant for MachXO4 (using the official migration tool), synthesis fails with an error about multiple write clocks in the RAM instance.

The same synthesis tool (SynplifyPro) is used in both flows, but only Radiant reports an error:

Devices affected: MachXO4 (LFMXO4)

Bug number: DNG-31065

Hold time violations may be observed on EtherCAT IP paths in Radiant, blocking timing closure.

A design originally targeting MachXO3L and synthesizing successfully in Diamond using Synplify Pro may exhibit hold time violations when migrated to Radiant and implemented on CertusPro-NX devices using an EtherCAT IP. Hold violations are observed on EtherCAT IP paths even after following recommended constraint migration steps, including copying PDC constraints to SDC and verifying hierarchical paths.

Resource utilization is comparable to reference designs, but the hold violations persist and prevent timing closure.

Workaround:

- Review and adjust timing constraints, ensuring all hierarchical paths are correct.
- Experiment with different Radiant tool settings or seeds.

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-31302

The BLTS indicator in Reveal Analyzer may be misleading for DDR frequencies at or below 800 MHz.

In the Reveal Analyzer, the BLTS (Built-in Logic Training Sequence) radio button is enabled only for DDR frequencies at or above 933 MHz. For DDR frequencies of 800 MHz and below, the BLTS radio button remains red, which may incorrectly suggest a training failure. In addition, the Calibration Margin Report displays a value of 0 for these lower frequencies, which can be confusing.

Workaround:

- Ignore the BLTS radio button and Calibration Margin Report for DDR frequencies ≤800MHz; these indicators are not valid for lower frequencies.
- Refer to other training and calibration results for status.

Devices affected: Avant (LAV-AT)

Bug number: DNG-26340

FIFO empty signal may be incorrect if the clear signal is asserted during the first clock cycle on Avant devices.

On Avant devices, if the FIFO clear signal is asserted during the first clock cycle after reset, the FIFO empty signal may not match the synthesized or Place and Route (PAR) netlist behavior. This can result in incorrect FIFO status reporting immediately after reset.

Workaround:

- Do not assert the clear signal during the first clock cycle.
- Apply the clear signal after at least one valid clock cycle has elapsed to ensure proper alignment of the FIFO empty signal.
- Verify FIFO behavior in simulation and hardware after applying this change.

Devices affected: Avant (LAV-AT)

Bug number: DNG-24704

Netlist Viewer may display incorrect or disconnected timing paths when cross probing from Timing Analysis.

In Radiant 2025.2, when viewing timing paths in the Netlist Viewer by cross-probing from the Timing Analysis report, the displayed paths may be incorrect or appear disconnected. This affects the visual representation of timing paths in the Netlist Viewer only.

Workaround: Use the Timing Analysis report as the source of truth for timing paths and slack values.

Devices affected: All devices

Bug number: DNG-29138

Radiant Programmer batch mode may generate an incorrect XCF file for AS2 boards.

When running Radiant Programmer in batch mode for AS2 boards, the generated .xcf file may be incorrect. The same project, when programmed using the GUI mode, produces the correct XCF file. This issue is specific to AS2 board configurations. Batch mode functions correctly for ES1 boards.

Workaround: Use GUI mode to generate the XCF file for AS2 boards. For automated flows, compare batch and GUI outputs and manually correct as needed.

Devices affected: Avant (LAV-AT)

Bug number: DNG-29314

The sta_get_paths command reports a bad flag error when using the -endpoints or -summary options.

Using the sta_get_paths command with the -endpoints or -summary options, for example sta_get_paths -summary or sta_get_paths -pins -endpoints, results in a bad flag error instead of valid output.

Workaround: Avoid using the -endpoints or -summary options with sta_get_paths. Use other supported options to obtain timing paths.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-31049

LSE resource sharing can cause mismatches between RTL simulation and synthesized behavior on Certus-NX devices.

When using LSE synthesis with resource sharing enabled on Certus NX devices, RTL simulation may pass, but post synthesis simulation and hardware behavior may not match the RTL. This mismatch is not observed when LSE resource sharing is disabled or when using Synplify Pro for synthesis.

Workaround: Disable LSE resource sharing (set Resource Sharing to FALSE in the LSE strategy) or use Synplify Pro for synthesis.

Devices affected: Certus-NX (LFD2NX)

Bug number: DNG-30896