



Certus-NX-65 Development Board

Evaluation Board User Guide

FPGA-EB-02075-1.0

January 2026

Disclaimers

Lattice makes no warranty, representation, or guarantee regarding the accuracy of information contained in this document or the suitability of its products for any particular purpose. All information herein is provided AS IS, with all faults, and all associated risk is the responsibility entirely of the Buyer. The information provided herein is for informational purposes only and may contain technical inaccuracies or omissions, and may be otherwise rendered inaccurate for many reasons, and Lattice assumes no obligation to update or otherwise correct or revise this information. Products sold by Lattice have been subject to limited testing and it is the Buyer's responsibility to independently determine the suitability of any products and to test and verify the same. LATTICE PRODUCTS AND SERVICES ARE NOT DESIGNED, MANUFACTURED, OR TESTED FOR USE IN LIFE OR SAFETY CRITICAL SYSTEMS, HAZARDOUS ENVIRONMENTS, OR ANY OTHER ENVIRONMENTS REQUIRING FAIL-SAFE PERFORMANCE, INCLUDING ANY APPLICATION IN WHICH THE FAILURE OF THE PRODUCT OR SERVICE COULD LEAD TO DEATH, PERSONAL INJURY, SEVERE PROPERTY DAMAGE OR ENVIRONMENTAL HARM (COLLECTIVELY, "HIGH-RISK USES"). FURTHER, BUYER MUST TAKE PRUDENT STEPS TO PROTECT AGAINST PRODUCT AND SERVICE FAILURES, INCLUDING PROVIDING APPROPRIATE REDUNDANCIES, FAIL-SAFE FEATURES, AND/OR SHUT-DOWN MECHANISMS. LATTICE EXPRESSLY DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY OF FITNESS OF THE PRODUCTS OR SERVICES FOR HIGH-RISK USES. The information provided in this document is proprietary to Lattice Semiconductor, and Lattice reserves the right to make any changes to the information in this document or to any products at any time without notice.

Inclusive Language

This document was created consistent with Lattice Semiconductor's inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice's inclusive language [FAQ 6878](#) for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

Contents

Abbreviations in This Document.....	6
1. Introduction.....	7
1.1. Certus-NX-65 Development Board.....	7
1.2. Features.....	8
1.3. LFD2NX-65 Device.....	9
2. Jumper Definition.....	10
3. Applying Power to the Board.....	11
4. Programming.....	13
4.1. Hard JTAG Download Interface.....	13
4.2. Programming Certus-NX LFD2NX-65 SRAM.....	14
4.3. Hard I2C Download Interface.....	15
5. SPI Flash Module Programing.....	17
6. Soft JTAG/UART User Interface.....	20
6.1. Soft JTAG User Interface.....	20
6.2. Soft UART User Interface.....	21
7. LFD2NX-65 Clock Sources.....	22
8. RGMII Ethernet Connections.....	23
9. HyperRAM.....	25
10. PCIe Gold Finger.....	26
11. Headers and Test Connections.....	27
11.1. Versa Headers.....	27
11.2. Arduino Board GPIO Headers (DNI).....	29
11.3. FPC Headers.....	30
11.4. Aardvark Header (DNI).....	31
11.5. Raspberry Pi Board GPIO Header (DNI).....	31
11.6. PMOD Headers.....	32
11.7. User I2C Interface.....	33
11.8. ADC and Potentiometer.....	33
12. LEDs and Switches.....	35
12.1. DIP Switches.....	35
12.2. General Purpose Push Buttons.....	36
12.3. General Purpose LEDs.....	36
13. Software Requirements.....	37
14. Storage and Handling.....	37
15. Ordering Information.....	37
Technical Support Assistance.....	38
Appendix A. Certus-NX-65 Development Board Schematics.....	39
Appendix B. Certus-NX-65 Development Board Bill of Materials.....	55
Appendix C. User Defined Preference File.....	66
References.....	71
Revision History.....	72

Figures

Figure 1.1. Top View of Certus-NX-65 Development Board	7
Figure 1.2. Bottom View of Certus-NX-65 Development Board	8
Figure 3.1. Board Power Supply.....	11
Figure 4.1. JTAG/I2C Programming Architecture.....	13
Figure 4.2. JTAG Test Header	13
Figure 4.3. Open Radiant Programmer.....	14
Figure 4.4. Radiant Programmer – Device Properties	15
Figure 4.5. I2C Programming Mode.....	16
Figure 5.1. MASTER_SPI_PORT Setting.....	17
Figure 5.2. Connection of SPI Flash Module and Certus-NX-65 Development Board	17
Figure 5.3. Radiant Programmer – Scan Device.....	18
Figure 5.4. LFD2NX-65 Device Detected.....	18
Figure 5.5. SPI Flash Operation Dialog.....	19
Figure 6.1. JTAG/UART User Interfacing.....	20
Figure 7.1. On-board Clock Resources.....	22
Figure 10.1. Top Side of PCIe Edge Connector.....	26
Figure 11.1. Circuit Design for ADC0.....	34
Figure 11.2. Circuit Design for ADC1.....	34
Figure 11.3. Trimmer Wiper Description	34
Figure 12.1. Two-Position and Four-Position DIP Switch Circuits.....	35
Figure 12.2. Two-Position and Four-position DIP Switches	35
Figure A.1. Title Page	39
Figure A.2. Block Diagram.....	40
Figure A.3. Raspberry Pi and Prototype (BANK0 and BANK3)	41
Figure A.4. LEDs and Flash PMOD3 (BANK1)	42
Figure A.5. FTDI to Hard JTAG I/F and PMOD2 (BANK2).....	43
Figure A.6. HyperRAM and PCIe (BANK5 and BANK80)	44
Figure A.7. SGMII & RGMII PHY, FPC, and PMOD1 (BANK6 and BANK4).....	45
Figure A.8. Versa Connector and Segment LED (BANK7 and BANK8).....	46
Figure A.9. Arduino and Aardvark Headers (BANK9).....	47
Figure A.10. FTDI to Soft JTAG I/F and PMOD0 (BANK 11)	48
Figure A.11. Power Rails and Monitors (1)	49
Figure A.12. Power Rails and Monitors (2)	50
Figure A.13. USB Power	51
Figure A.14. Power Regulators	52
Figure A.15. Power Tree	53
Figure A.16. Revision History.....	54

Tables

Table 2.1. Jumper Definition.....	10
Table 3.1. On-board Major Power Rails.....	12
Table 3.2. LFD2NX-65 I/O Bank Power Rails Stuff.....	12
Table 3.3. LFD2NX-65 Major Power Rails Stuff.....	12
Table 4.1. Config JTAG Connections	14
Table 4.2. Other Config JTAG Control Signals	14
Table 4.3. Download I2C Connections	16
Table 6.1. Soft JTAG Connections	20
Table 6.2. Soft UART Connections	21
Table 7.1. Input Clock Options.....	22
Table 8.1. SGMII Ethernet PHY Interfacing	23
Table 9.1. HyperRAM Controller Interconnections	25
Table 10.1. Gold Finger Pin Connections	26
Table 11.1. Versa J27 Header Pin Connections.....	27
Table 11.2. Versa J28 Header Pin Connections.....	28
Table 11.3. Arduino J21 Pin Connections	29
Table 11.4. Arduino J22 Pin Connections	29
Table 11.5. Arduino J23 Pin Connections	30
Table 11.6. Arduino J24 Pin Connections	30
Table 11.7. FPC Header Pin Connections.....	30
Table 11.8. Aardvark J26 Header Pin Connections	31
Table 11.9. Raspberry Pi J5 Header Pin Connections	31
Table 11.10. J9 Header Pin Connections	32
Table 11.11. J34 Header (DNI) Pin Connections	32
Table 11.12. J53 Header (DNI) Pin Connections	33
Table 11.13. I2C Connections	33
Table 12.1. Two-Position DIP Switch Signals	35
Table 12.2. Four-Position DIP Switch Signals.....	35
Table 12.3. Push Button Switch Signals	36
Table 12.4. LED Signals	36
Table 15.1. Ordering Information	37

Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviation	Definition
ASC	Analog Sense and Control
CMOS	Complementary Metal-Oxide Semiconductor
DNI	Do Not Install
FTDI	Future Technology Devices International
FPC	Flexible Printed Circuit
GPIO	General Purpose Input/Output
I2C	Inter-Integrated Circuit
LDO	Low Dropout
LVDS	Low Voltage Differential Signaling
PCIe	Peripheral Component Interconnect Express
SLVS	Scalable Low Voltage Signaling
SPI	Serial Peripheral Interface
TPI	Twisted Pair Interface

1. Introduction

The Lattice Semiconductor Certus-NX-65 Development Board allows you to investigate and experiment with the features of the LFD2NX-65 FPGA. The features of the Certus-NX-65 Development Board can assist you with the rapid prototyping and testing of your specific designs.

The Certus-NX-65 Development Board is part of the Certus-NX-65 Development Kit, which includes the following:

- SPI Flash Module
- 12 V AC/DC Power Adapter
- Mini USB Cable
- PCIe Standard Add-in Card I/O Bracket
- Quick Start Guide

The contents of this user guide include top-level functional descriptions of the various portions of the development board, descriptions of the on-board headers, diodes and switches, and a complete set of schematics.

1.1. Certus-NX-65 Development Board

The Certus-NX-65 Development Board features the Certus-NX-65 FPGA in the BBG484 package. The board can expand the usability of the Certus-NX-65 FPGA with PMOD, and Raspberry PI connectors. Easy-to-use board resources of the jumpers, LED indicators, push buttons, and switches are available for various user-defined applications with Arduino, Raspberry, PCIe, RJ45, Versa, and Aardvark headers.

Figure 1.1 shows the top view of the Certus-NX-65 Development Board. Figure 1.2 shows the bottom view of this board.

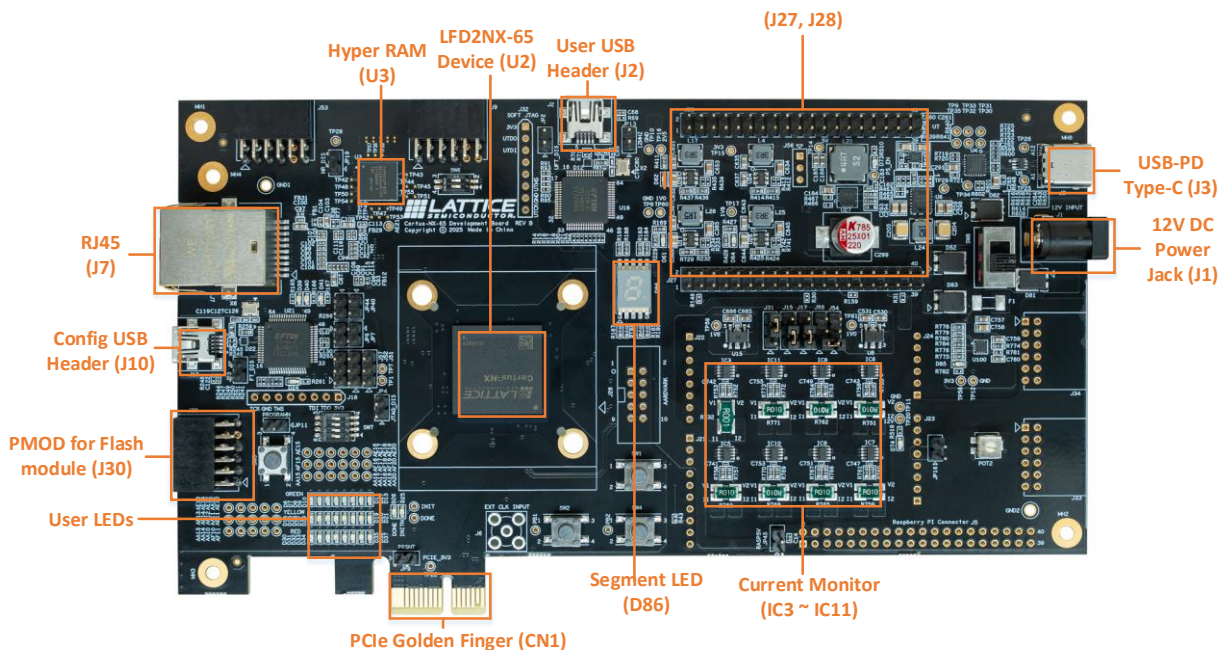


Figure 1.1. Top View of Certus-NX-65 Development Board

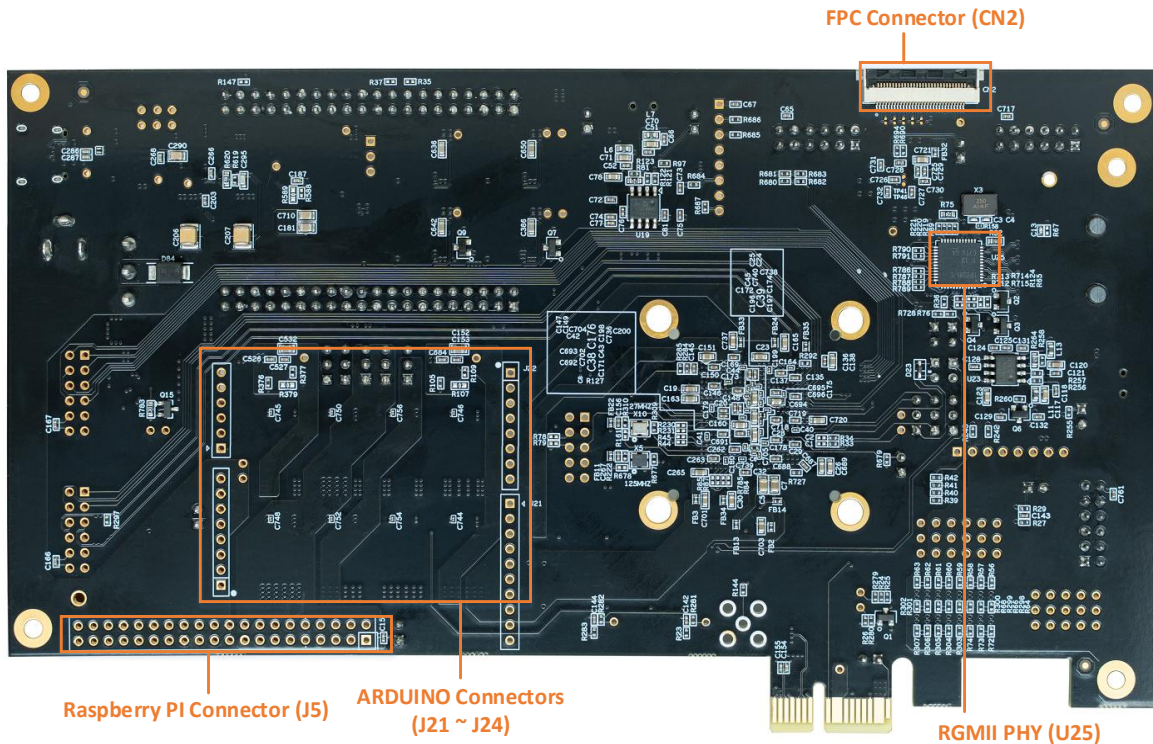


Figure 1.2. Bottom View of Certus-NX-65 Development Board

1.2. Features

- On-board LFD2NX-65 device
- One Gbe PHY RJ45 connectors, with RGMII PHY support
- HyperRAM™ up to 800 MBps
- PCIe Gen2 x1 Edge Connector
- Versa Headers bridge with Lattice ASC Demo Board to support L-ASC10
- General Purpose Input/Output (GPIO) interface with PMOD, Arduino and Raspberry Pi boards
- USB-B connection for device programming with JTAG and Inter-Integrated Circuit (I2C) utility
- Additional mini-USB connection for users with Soft JTAG and UART utility
- Four-position DIP-Switch and two-position DIP-Switch, three push buttons, eight red LEDs, eight yellow LEDs and eight green LEDs for demo purposes
- ADC interface with 10K POT
- One FPC header with six pairs of LVDS
- Multiple reference clock sources
- Optional Aardvark header
- Support FPGA Power Evaluation
- Lattice Radiant™ programming support

Note: DNI stands for *Do Not Install* parts and DI stands for *Do Install* parts for assembly.

Caution: The Certus-NX-65 Development Board contains ESD-sensitive components. ESD safe practices should be followed while handling and using the development board.

1.3. LFD2NX-65 Device

The Certus-NX-65 Development Board features the LFD2NX-65 device in a 484-ball caBGA package. This device offers a variety of features and programmability. Its cryptographic engine supports user-mode security features. Along with the cryptographic engine, numerous system functions are included, such as two PLLs and 2,304 kbits of embedded RAM plus hardened implementations of I2C and SPI. Certus-NX FPGAs feature one hard PCIe link layer IP block which supports PCIe Gen1 and Gen2 with one ×1 configuration. The devices also have flexible and high performance I/O that support numerous single-ended and differential standards, including controller and SLVS. For more information on the capabilities of the LFD2NX-65 device, see [Certus-NX Family Data Sheet \(FPGA-DS-02078\)](#).

2. Jumper Definition

Table 2.1. Jumper Definition

Part	Description	Setting	Default
JP19	HyperRAM U3 ResetN	<ul style="list-style-type: none"> Open: U3 is active. Closed: Holds HyperRAM in RESET. 	Open
JP2	FTDI U18 Reset	<ul style="list-style-type: none"> Open: U18 is active. Closed: Holds U18 in RESET. 	Open
JP3	FTDI U21 Reset	<ul style="list-style-type: none"> Open: U21 is active. Closed: Holds U21 in RESET. 	Open
JP4	JTAG Disable	<ul style="list-style-type: none"> Open: FPGA JTAG is active. Closed: FPGA JTAG is disabled. 	Open
JP11	ProgramN	—	Open
JP13	12 MHz to FPGA	<ul style="list-style-type: none"> Open: 12 MHz is not connected to the FPGA. Closed: Input 12 MHz to FPGA. 	Open
JP16	+5.0 V from Arduino Connectors	<ul style="list-style-type: none"> Open: Arduino Connectors are self-powered. Closed: A 5 V supply is provided to Arduino Connectors. 	Open
JP45	Raspberry PI Connector (J5) Power	<ul style="list-style-type: none"> Open: Raspberry PI is self-powered. Closed: A 5 V supply is provided to the Raspberry PI connector. 	Open
JP7, J51, J52	FTDI dedicated I2C	<ul style="list-style-type: none"> JP7 closed, J51 1–2 short, J52 1–2 short: I2C bus is connected. JP7 open, J51 2–3 short, J52 2–3 short: UART is connected. 	JP7 open J51 2–3 short J52 2–3 short
JP6, J57	User I2C	<ul style="list-style-type: none"> JP6 closed, J57 1–2 short: User I2C bus is connected to FTDI I2C. JP6 open, J57 open: User I2C bus is disconnected. 	JP6 open J57 open
JP9	PCIe reset	—	Open
JP40	RGMII PHY ResetN	<ul style="list-style-type: none"> Open: U3 is active. Closed: Holds HyperRAM in RESET. 	Open
JP44	RGMII PHY INTN/PWDN	<ul style="list-style-type: none"> Open: U3 is active. Closed: Holds HyperRAM in POWER DOWN. 	Open
J15	Bank 0 Power Select	<ul style="list-style-type: none"> 1–2 short: VCCIO0 is powered from the on-board +3.3V. 2–3 short: VCCIO0 is from Raspberry PI connector +3.3V_RASP. 	Open
J17	Bank 9 Power Select	<ul style="list-style-type: none"> 1–2 short: VCCIO9 is powered from the on-board +3.3V. 2–3 short: VCCIO9 is from ARDUINO Connectors +3.3V_AR. 	Open

3. Applying Power to the Board

As shown in [Figure 3.1](#), the Certus-NX LFD2NX-65 Development Board can be powered up from three external power sources: 12 V through the DC power input jack J1; 15 V through the Type-C USB connector J3, converted to 12 V through an on-board DC-DC converter; or 12 V through the PCIe edge connector CN1. And the switch SW8 is used to switch the power supply between J1 and J3: UP for J1, DOWN for J3. All power inputs are protected by eFuse, which protects against overcurrent and reverse polarity, and supports adjustable overcurrent thresholds (0.5 A–6 A) and configurable overvoltage settings.

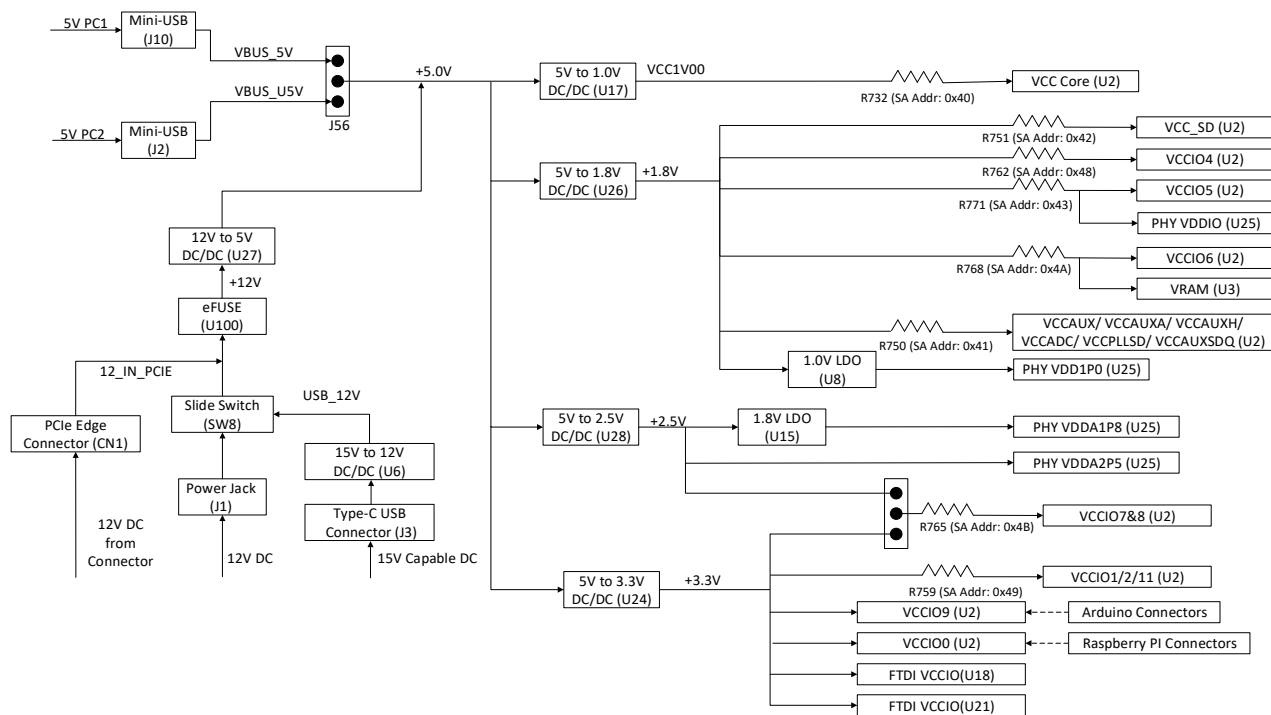


Figure 3.1. Board Power Supply

For the board extension, 5 V DC power can also supply Raspberry Pi and Arduino boards through the jumpers and on-board headers, to consolidate AC/DC adapters for stack boards system. Conversely, 5 V DC power for Certus-NX-65 Development Board can be supplied either from mated Raspberry Pi or Arduino Boards, if they are powered up by external AC/DC adapters already. You need to ensure 5 V power from a single source when adding JP45 or JP16 jumpers. However, maintaining 5 V DC supplier is the basic requirement to power on board. You can verify proper operation by checking the power good yellow LED D73.

[Table 3.1](#) summarizes on-board major power rails and their test points.

Table 3.1. On-board Major Power Rails

Power Net Name	Primary Source	Test Point
USB_VBUS	Type-C USB Connector	—
VBUS_12V	DC/DC Regulator (U6)	—
+12V	DC Power Jack (J1), PCIe Edge Connector (CN1) or VBUS_12V, Selected by Slide switch (SW8)	TP20
VBUS_5V	Mini-USB Header (J10)	J56
VBUS_U5V	Mini-USB Header (J2)	J56
+5.0V	DC/DC Regulator (U27)	TP14
+3.3V	DC/DC Regulator (U24)	TP15
+2.5V	DC/DC Regulator (U28)	TP16
+1.8V	DC/DC Regulator (U26)	TP17
VCC1V00	DC/DC Regulator (U17)	TP60
VCCA_1V8	LDO (U15)	TP59
VCCA_1V0	LDO (U8)	TP61
+3.3V_RASP	Raspberry Pi Header (J5)	—
+3.3V_AR	Arduino Header (J23)	—

As shown in [Figure 3.1](#), this board provides multiple power options for I/O bank voltage flexibility. [Table 3.2](#) summarizes the V_{CCIO} support matrix on this board. For power consumption evaluation, this board facilitates some $0.01\ \Omega$ sense resistors and current monitor IC with I2C compatible interface to measure the voltage drop on each power rail.

Table 3.2. LFD2NX-65 I/O Bank Power Rails Stuff

LFD2NX-65 Power (U2)	Jumpers	3.3 V	2.5 V	1.8 V	1.2 V	1.1 V	External 3.3 V	Power Monitor	
								I2C Address	Sense Resistor
V_{CCIO0}	J15	Pin 1–2	—	—	—	—	Pin 2–3	NA	NA
V_{CCIO1} & V_{CCIO2} & V_{CCIO11}	—	Fixed	—	—	—	—	—	0X49	R759
V_{CCIO3}	J54 & J55	J54 Pin1 – J55 Pin1	J54 Pin2 – J55 Pin2	J54 Pin3 – J55 Pin3	—	—	—	NA	NA
V_{CCIO4}	—	—	—	Fixed	—	—	—	0X48	R762
V_{CCIO5}	—	—	—	Fixed	—	—	—	0x43	R771
V_{CCIO6}	—	—	—	Fixed	—	—	—	0X4A	R768
V_{CCIO7} & V_{CCIO8}	J31	Pin 1–2	Pin 2–3	—	—	—	—	0X4B	R153
V_{CCIO9}	J17	Pin 1–2	—	—	—	—	Pin 2–3	NA	NA

Other than the power rail for each I/O Bank, this board also provides some test points to evaluate the major power consumptions for the LFD2NX-65 device, as listed in [Table 3.3](#).

Table 3.3. LFD2NX-65 Major Power Rails Stuff

LFD2NX-65 Power (U3)	Sense Resistor	Resistance	I2C Address
V_{CC_CORE}	R732	$0.001\ \Omega$	0X40
V_{CCSD}	R751	$0.01\ \Omega$	0X42
$V_{CC_AUX}/V_{CC_AUXH}/V_{CCAUXA}/V_{CCAUXSDQ}/V_{CCPLLSD}/V_{CC_ADC}$	R750	$0.01\ \Omega$	0X41

4. Programming

The hardened JTAG/I2C programming architecture of the Certus-NX-65 Development Board is shown in [Figure 4.1](#). The board has a built-in download controller for programming the LFD2NX-65 device. It uses an FT2232H Future Technology Devices International (FTDI) part U21 to convert USB to JTAG from port A, or convert USB to I2C from port B. Using the Detect Cable function with the Lattice Radiant programming software installed, you can detect dual ports after powering up the board and connect the mini-USB to USB-A cable from J10 to your PC, ensuring the FTDI reset control jumper JP3 is not populated as default. The software select option FTUSB-0 is dedicated for hard JTAG and FTUSB-1 is dedicated for hard I2C or UART. The two options match with port A and port B, respectively, from the hardware perspective.

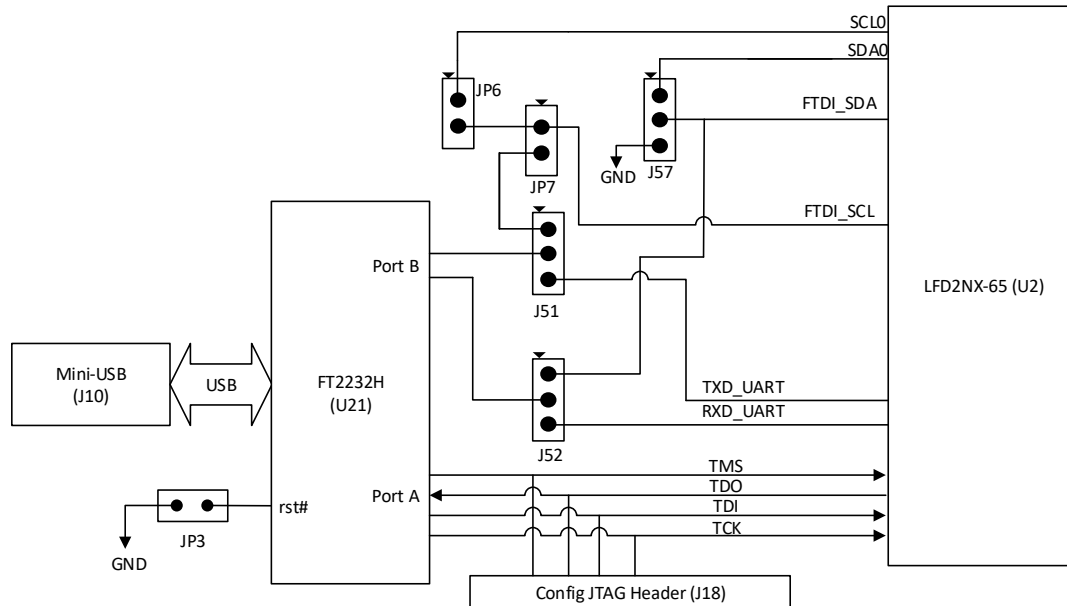


Figure 4.1. JTAG/I2C Programming Architecture

4.1. Hard JTAG Download Interface

An eight-pin header J18 (DNI) ([Figure 4.2](#)) allows you to probe the JTAG signals to access the LFD2NX-65 JTAG port from the external JTAG host, such as the external Lattice HW-USBN-2B Programming Cable available separately or to access the SSPI port from the external SPI host. The JTAG connections between J18 and the LFD2NX-65 device are listed in [Table 4.1](#).

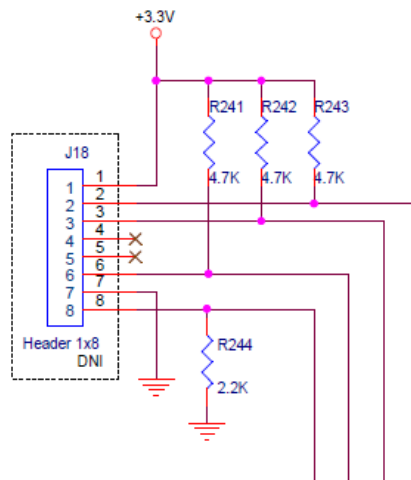


Figure 4.2. JTAG Test Header

Table 4.1. Config JTAG Connections

J18 Pin Number	JTAG Net Name	LFD2NX-65 Ball Location for JTAG	Optional SSPI Function
1	+3.3V	—	—
2	TDO	G13	SSI
3	TDI	F16	SSO
4	—	—	—
5	—	—	—
6	TMS	F11	SCSN
7	GND	—	—
8	TCK	H17	SCLK

The Certus-NX-65 Development Board also provides test points for other dedicated JTAG configuration pins, as shown in [Table 4.2](#).

Table 4.2. Other Config JTAG Control Signals

Net Name	LFD2NX-65 Ball Location	LED Indicator	Test Point
JTAGEN	F15	—	Pin 2 of JP4
PROGRAMN	D16	—	—
INITN	D17	D25	TP INIT
DONE	C20	D26	TP DONE

4.2. Programming Certus-NX LFD2NX-65 SRAM

The Radiant Programmer software can be used to program the .bit file to the LFD2NX-65 SRAM. The Radiant Programmer is integrated into the Lattice Radiant software and it is also available as a stand-alone version.

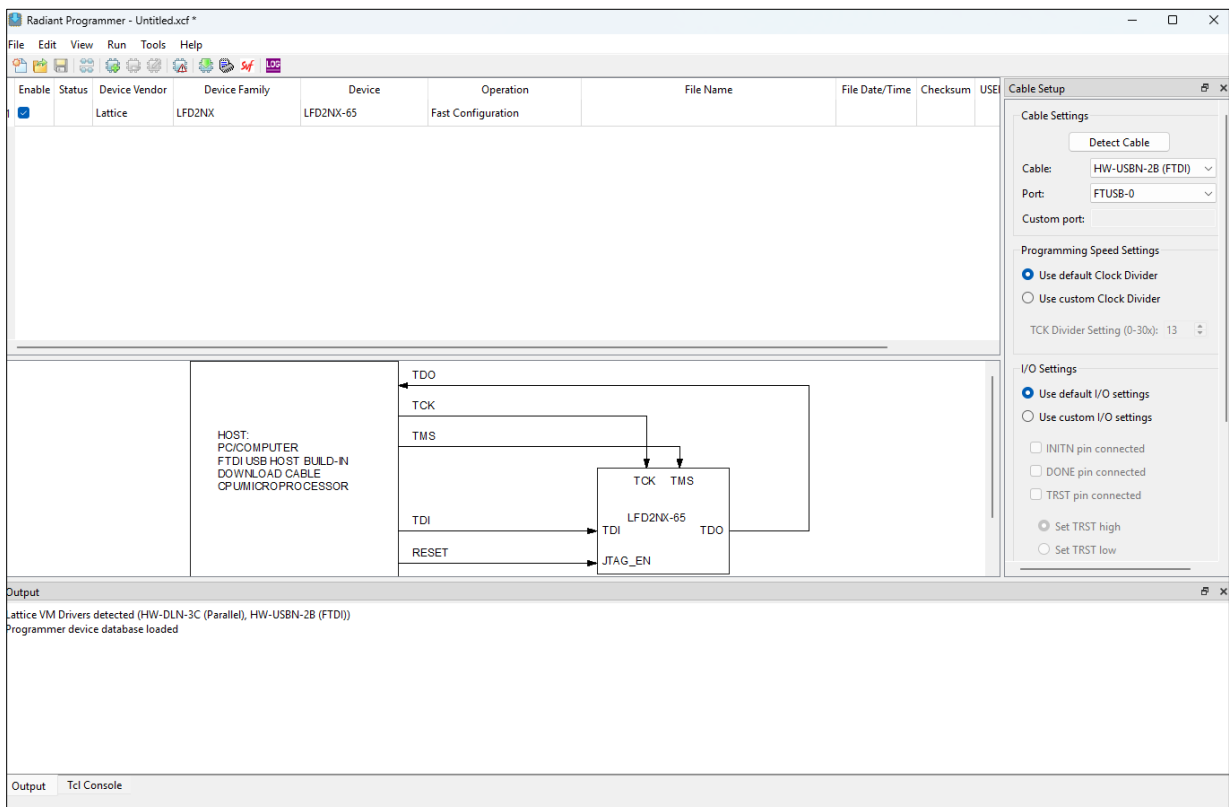


Figure 4.3. Open Radiant Programmer

To program the LFD2NX-65 SRAM:

1. Connect the PC and the header J10 of the Certus-NX-65 Development Board using the USB cable.
2. In the Lattice Radiant software, click **Tools > Programmer**. Or, in Windows, go to **Start > Lattice Radiant Software 2025.2 > Radiant Programmer**.
3. The Radiant Programmer interface opens, as shown in [Figure 4.3](#). Select FTUSB-0 for **Port** in the **Cable Setup** filed.
4. Double-click the **Operation** field.
5. The **Device Properties** dialog box opens, as shown in [Figure 4.4](#). Select the following options:
 - Target Memory – Compressed Random Access Memory (CRAM)
 - Port Interface – JTAG
 - Access Mode – Direct Programming
 - Operation – Fast Configuration
 - Programming file – Select the .bit file to be programmed.

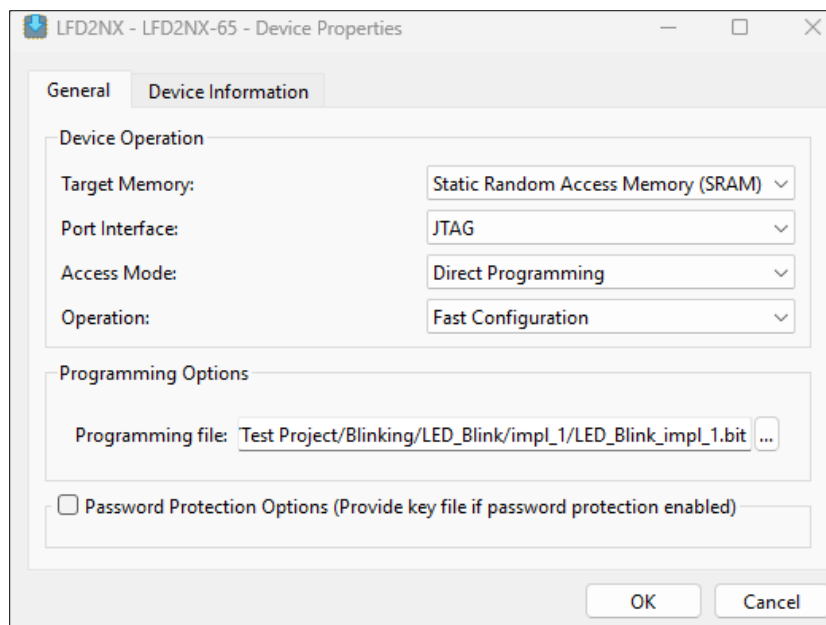


Figure 4.4. Radiant Programmer – Device Properties

6. Click **OK**.

To program the .bit file, click the Program button in the Radiant Programmer or select **Run > Program Device**. If successful, the Status column shows PASS. The Output pane also shows INFO – Operation: successful.

4.3. Hard I2C Download Interface

The USB hub on the PC can also detect the addition of the USB function on Config FTDI Port B. You can select the port FTUSB-1 on the programmer interface for accessing from Config FTDI Port B to the LFD2NX-65 device dedicated I2C download port named FTDI_SDA/FTDI_SCL, with 2.2 kΩ pull-up resistor each. The Diode D23 is inserted to support I2C clock stretching mode with JP7 added to drive FTDI_SCL from FTDI. [Figure 4.5](#) details the design of Config FTDI Port B for dedicated I2C download interface. [Table 4.3](#) summarizes the interconnection with the LFD2NX-65 device and its supported circuits. JP12 and JP13 are used to connect the dedicated I2C download port of the LFD2NX-65 device with the bridge I2C bus SDA0/SCL0 cross the whole board, in case you need to access the I2C download port from on-board headers other than the Config FTDI part. For the detailed connection from other headers to bridge the I2C bus SDA0/SCL0, refer to the [User I2C Interface](#) section.

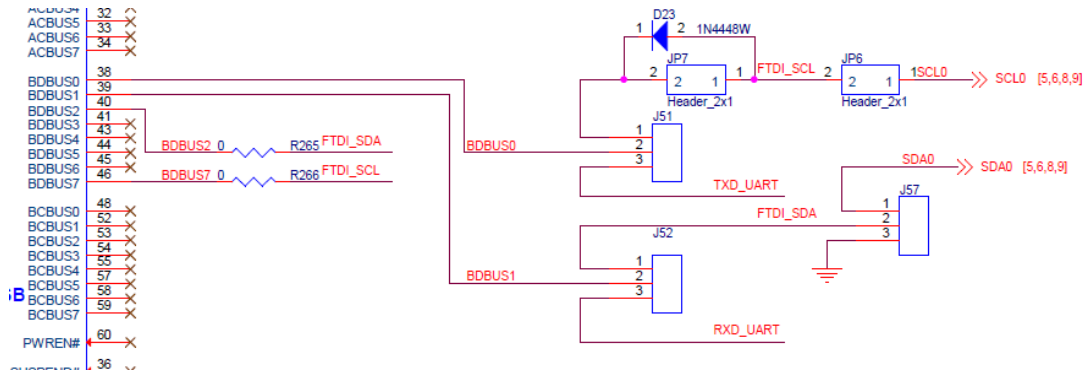


Figure 4.5. I2C Programming Mode

Table 4.3. Download I2C Connections

Download I2C Net Name	LFD2NX-65 Ball Location for JTAG	2.2 kΩ Pull-up Resistor	Bridge I2C Net Name	Bridge Jumper
FTDI_SCL	A19	R34	SCL0	JP6 close
FTDI_SDA	A18	R33	SDA0	J57 1–2 close

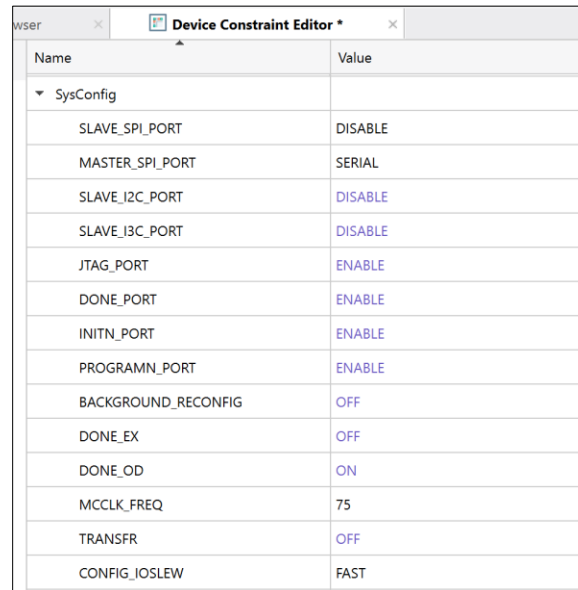
For more information on LFD2NX-65 JTAG/ I2C programming, refer to [Common Programming and Configuration FAQs with Supplementary Concepts for CrossLink-NX, Certus-NX, and CertusPro-NX \(FPGA-AN-02048\)](#).

5. SPI Flash Module Programming

The Certus-NX-65 Development Board kits include a SPI flash module, which uses the IS25LP064D flash chip.

Note:

Ensure the previous bitstream has MASTER_SPI_PORT enabled. The default setting for this attribute is DISABLE. Select any value other than DISABLE from the drop-down menu. Note that the maximum supported frequency for programming this module is 75 MHz, and MCCLK_FREQ must not exceed this limit. This frequency limit is due to the physical distance between the SPI flash and the Certus-NX FPGA. These settings can be set in Device Constraint Editor (Figure 5.1).



Name	Value
▼ SysConfig	
SLAVE_SPI_PORT	DISABLE
MASTER_SPI_PORT	SERIAL
SLAVE_I2C_PORT	DISABLE
SLAVE_I3C_PORT	DISABLE
JTAG_PORT	ENABLE
DONE_PORT	ENABLE
INITN_PORT	ENABLE
PROGRAMN_PORT	ENABLE
BACKGROUND_RECONFIG	OFF
DONE_EX	OFF
DONE_OD	ON
MCCLK_FREQ	75
TRANSFR	OFF
CONFIG_IOSLEW	FAST

Figure 5.1. MASTER_SPI_PORT Setting

Follow steps below to program the flash device.

1. Connect the SPI Flash module and J30 of the Certus-NX-65 Development Board J30, as shown in Figure 5.2.

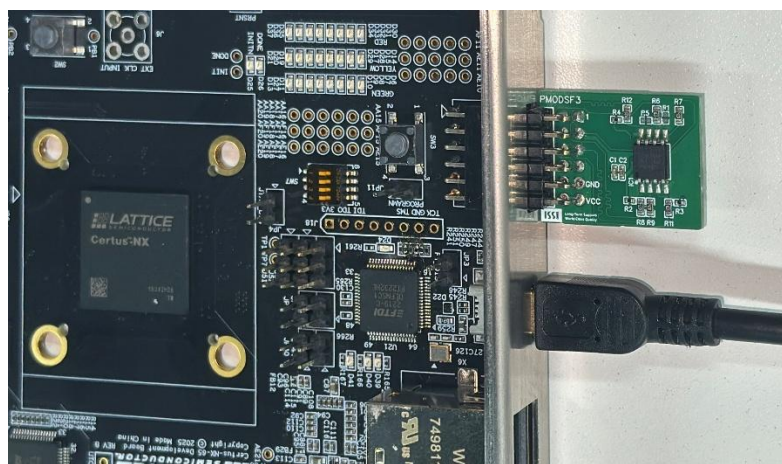


Figure 5.2. Connection of SPI Flash Module and Certus-NX-65 Development Board

2. Connect the PC and J10 of the Certus-NX-65 Development Board header using the USB cable.
3. In the Lattice Radiant software, click **Tools > Programmer**. Or, in Windows, go to **Start > Lattice Radiant Software 2025.2 > Radiant Programmer**.

- Click **Run > Scan Device** to check the board through the FTUSB-0 Port of the embedded HW-USBN-2B(FTDI) cable, as shown in [Figure 5.3](#). The Certus-NX-65 device named LFD2NX-65 should be detected on the JTAG chain, as shown in [Figure 5.4](#).

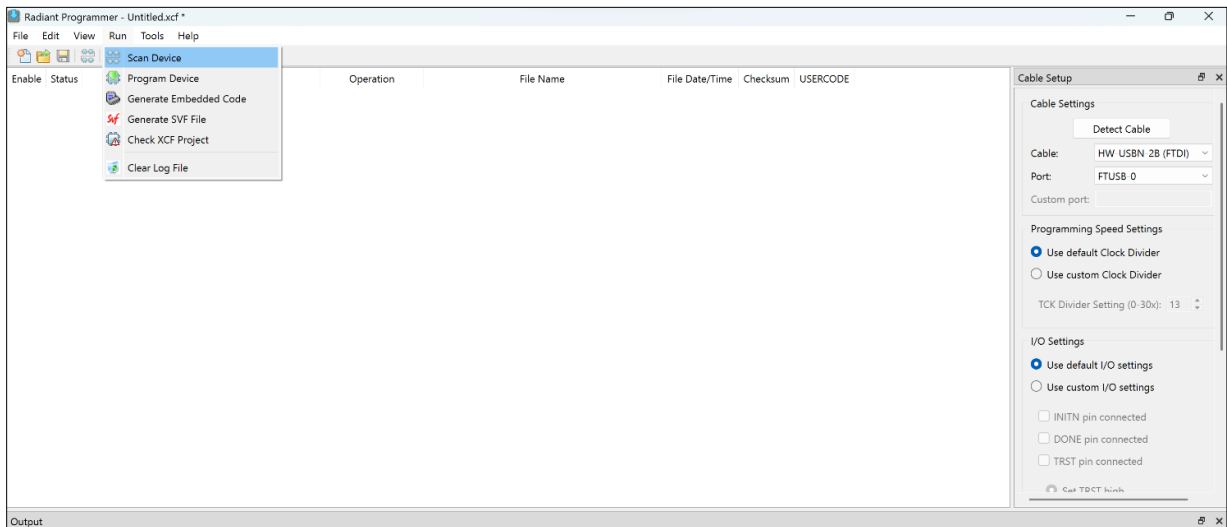


Figure 5.3. Radiant Programmer – Scan Device

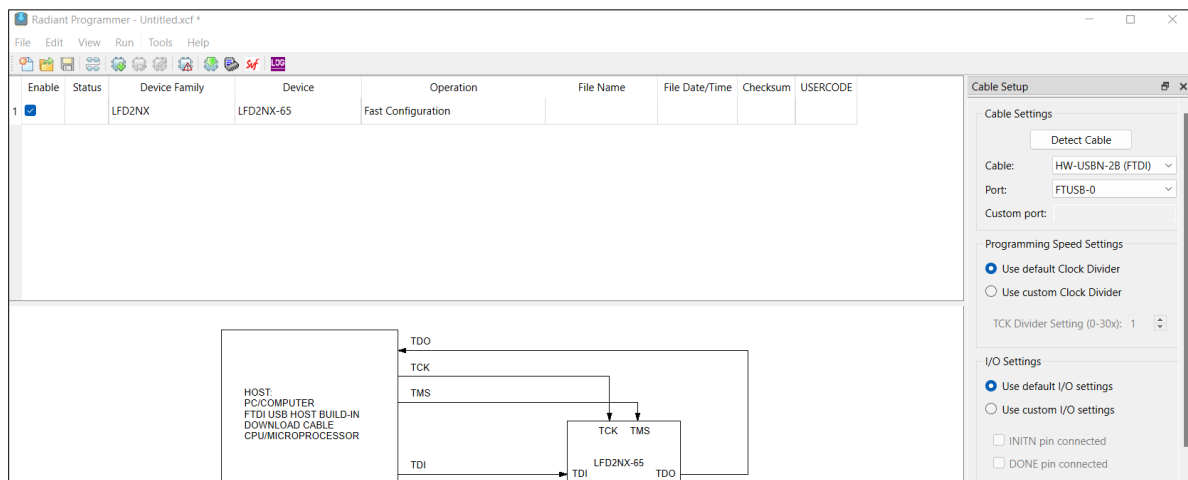


Figure 5.4. LFD2NX-65 Device Detected

- Open the **Device Properties** dialog box by double clicking the **Operation** column. Select **External SPI Flash Memory** from the **Target Memory** drop-down list in the **Device Operation** area. You can then see the **Device Properties** dialog showing the Flash memory details ([Figure 5.5](#)).

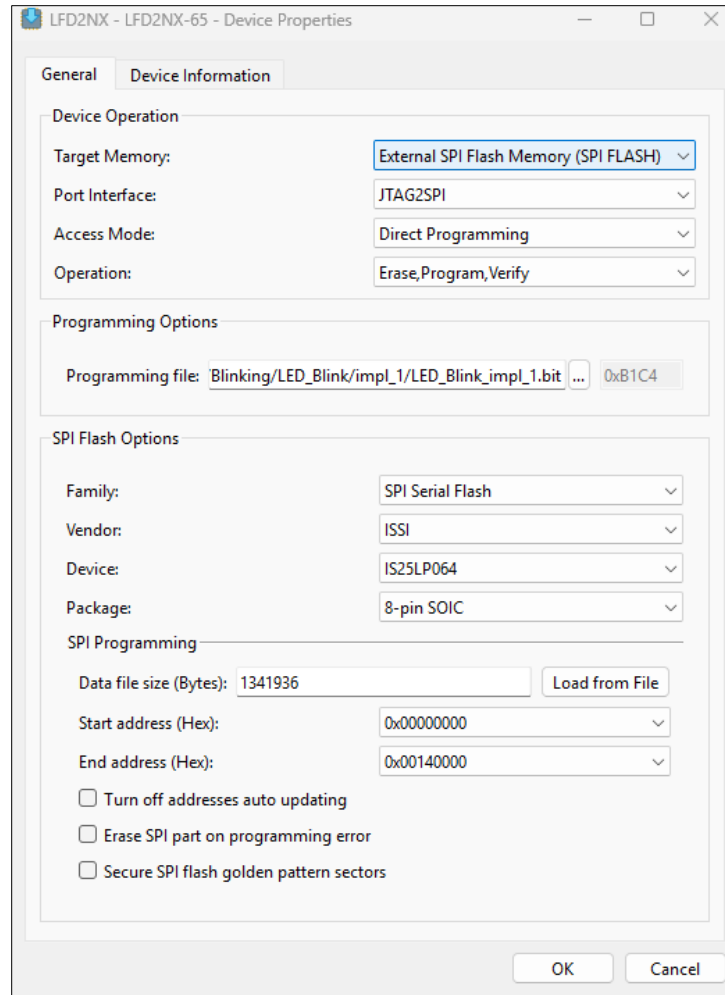



Figure 5.5. SPI Flash Operation Dialog

6. Confirm the Device Operation options as follows:
 - **Target Memory** is External SPI Flash Memory;
 - **Port Interface** is JTAG2SPI;
 - **Access Mode** is Direct Programming;
 - **Operation** is Erase, Program, Verify.
7. Confirm the SPI Flash options as follows:
 - **Family** is SPI Serial Flash;
 - **Vendor** is ISSI;
 - **Device** is IS25LP064;
 - **Package** is 8-pin SOIC.
8. For the programming file, click ... to select the .bit file.
9. Click **OK**.
10. Click the Program Device button  in Radiant Programmer.

6. Soft JTAG/UART User Interface

The soft JTAG/UART user interface for the Certus-NX-65 Development Board is shown in Figure 6.1. It also uses an FT2232H FTDI part U18 to convert USB to user JTAG from Port A, or convert USB to UART from Port B. Use the Detect Cable function with the Lattice Radiant programming software installed and ensure the FTDI reset control jumper JP8 is not populated by default. You can detect other dual ports after powering up the board. You can then connect the mini-USB to the USB-A cable from J19 to your PC. The software select option FTUSB-0 is targeted for user JTAG, and FTUSB-1 is targeted for UART. The two options are mapped with Port A and Port B, respectively, from the hardware perspective.

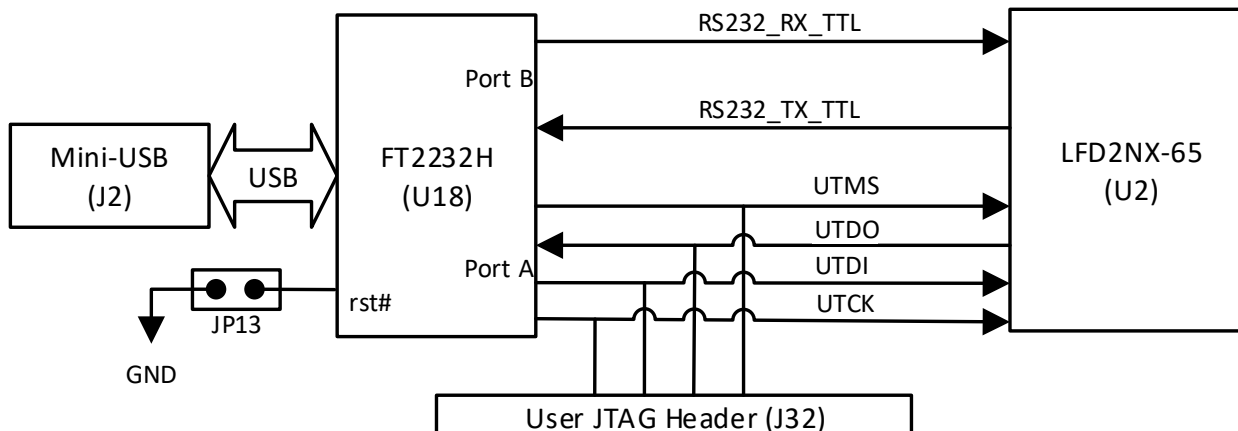


Figure 6.1. JTAG/UART User Interfacing

6.1. Soft JTAG User Interface

User FTDI Port A is connected with GPIOs in Bank 11 directly. You need to allocate GPIOs for adaption with JTAG signals by programmable logic, which is defined by FTDI Port A when converting USB to JTAG through FTUSB-0. J18 is an eight-pin standalone JTAG header that is used with an external Lattice download cable available separately, when the FTDI part is disabled from the JTAG chain after setting JP13. J32 can also be used as a test point when USB to JTAG is working.

Table 6.1. Soft JTAG Connections

J18 Pin Number	FTDI Signal	JTAG Net Name	LFD2NX-65 Ball Location
1	—	VCCIO1	—
2	UADBUS2	UTDO	AB5
3	UADBUS1	UTDI	AB2
4	—	—	—
5	—	—	—
6	UADBUS3	UTMS	AB4
7	—	GND	—
8	UADBUS0	UTCK	AB3

6.2. Soft UART User Interface

User FTDI Port B is also connected with GPIOs in Bank 11 directly. You need to allocate GPIOs for adaptation with UART signals by the programmable logic, which is defined by FTDI Port B when converting USB to UART through FTUSB-1.

Table 6.2. Soft UART Connections

FTDI Signal	UART Net Name	LFD2NX-65 Ball Location for Port A
UBDBUS0	RS232_RX_TTL	AA6
UBDBUS1	RS232_TX_TTL	AA5
UBDBUS2	RTSn	AA2
UBDBUS3	CTSn	AA1
UBDBUS4	DTRn	AB7
UBDBUS5	DSRn	AB8
UBDBUS6	DCDn	AB6
UBDBUS7	RI	AA7

7. LFD2NX-65 Clock Sources

The Certus-NX-65 Development Board has multiple external clock options for the LFD2NX-65 applications, as shown in Figure 7.1.

- 12 MHz from U18 (FTDI)
- 27 MHz from X10 (OSC MEM)
- External clock source from J6 (SMA)
- Differential 125 MHz from X5

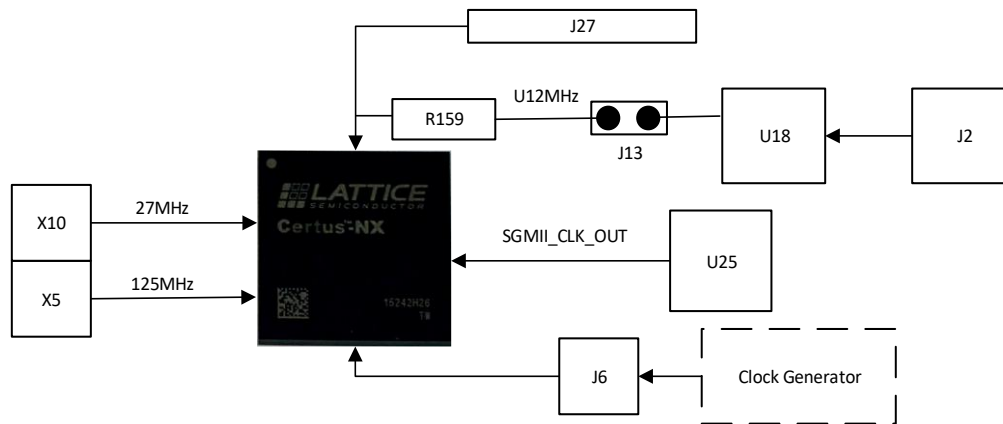


Figure 7.1. On-board Clock Resources

You need to take care that only 27 MHz and 125 MHz clocks are active in default after the board is powered up. Both 12 MHz clocks from the FT2232H FTDI U18 device are not always on without some hardware configuration. The 25 MHz of RGMII and the external clock need a source from other devices.

Table 7.1. Input Clock Options

Clock Frequency	Net Name	LFD2NX-65 Ball Location	Clock Source	I/O Type	Enable Conditions
12 MHz	EXPCON_OSC	P5	U18	LVCMS033	Needs to add R159 and JP13. USB header J2 is powered on and connected.
27 MHz	27M_OSC	F4	X10	LVCMS033	Always on. Add R161 to use FPGA to disable or control the clock output.
Customer	OSC_IN	A6	J6	LVCMS033	Needs to add J6 SMA. Connected to an external clock generator through the SMA cable.
125 MHz	125M_OSC	F17	X5	LVCMS033	Always on. Add R678 to use FPGA to disable or control the clock output.
25 MHz	SGMII_CLK_OUT	R14	U25	LVCMS018	Power on J1. U7 is enabled.

8. RGMII Ethernet Connections

The Certus-NX-65 Development Board can support independent Ethernet connections through on-board RGMII PHY devices. The part number of the RGMII PHY is DP83867ERGZT. Table 8.1 lists the signals from the FPGA interfacing with RGMII PHY devices.

Table 8.1. SGMII Ethernet PHY Interfacing

U25 Pin Number	U25 Signal Name	Net Name	Certus-NX-65 Ball Location	Application Note
1	TD_P_A	SGMII_MD0_P	—	To RJ45
2	TD_M_A	SGMII_MD0_N	—	To RJ45
3	VDDA2P5		—	2.5 V Power
4	TD_P_B	SGMII_MD1_P	—	To RJ45
5	TD_M_B	SGMII_MD1_N	—	To RJ45
6	VDD1P0		—	1.0 V Power
7	TD_P_C	SGMII_MD2_P	—	To RJ45
8	TD_M_C	SGMII_MD2_N	—	To RJ45
9	VDDA2P5	SGMII_VDDA2P5	—	2.5 V Power
10	TD_P_D	SGMII_MD3_P	—	To RJ45
11	TD_M_D	SGMII_MD3_N	—	To RJ45
12	RBIAS	—	—	—
13	VDDA1P8	SGMII_VDDA1P8	—	1.8 V Power
14	XO	PHY_XO	—	25 MHz Crystal Output
15	XI	PHY_XI	—	25 MHz Crystal Input
16	MDC	MDIO_CLK	U15	Optional pull up to VDDIO
17	MDIO	MDIO_DATA	U14	Pull up to VDDIO
18	CLK_OUT	SGMII_CLK_OUT	R14	With 22 Ω debounce resistor
19	VDDIO	SGMII_VDDIO	—	VCCIO6
20	JTAG_CLK	—	—	Pull down to GND
21	JTAG_TDO	—	—	Pull up to VDDIO
22	JTAG_TMS	—	—	Pull up to VDDIO
23	JTAG_TDI	—	—	Pull up to VDDIO
24	VDD1P0	VCCA_1V_PHY	—	1.0 V Power
25	TX_D3	RGMII_TXD3	—	RGMII Data
26	TX_D2	RGMII_TXD2	—	RGMII Data
27	TX_D1/SGMII_SIP	RGMII_TXD1/SGMII_SIP	AB9	RGMII Data
28	TX_D0/SGMII_SIN	RGMII_TXD0/SGMII_SIN	AB10	RGMII Data
29	GTX_CLK	RGMII_TXCLK	V10	RGMII transmit clock
30	VDDIO	SGMII_VDDIO	—	I/O Power
31	VDD1P0	VCCA_1V_PHY	—	1.0 V Power
32	RX_CLK	RGMII_RXCLK	W10	RGMII receive clock
33	RX_D0/SGMII_COP	RGMII_RXD0/SGMII_COP	W12	RGMII Data
34	RX_D1/SGMII_CON	RGMII_RXD1/SGMII_CON	V12	RGMII Data
35	RX_D2/SGMII_SOP	RGMII_RXD2/SGMII_SOP	AB11	RGMII Data
36	RX_D3/SGMII_SON	RGMII_RXD3/SGMII_SON	AA11	RGMII Data
37	TX_CTRL	RGMII_TX_CTRL	W13	RGMII transmit control
38	RX_CTRL	RGMII_RX_CTRL	Y13	RGMII receive control
39	GPIO_0	—	—	Pull down to GND
40	GPIO_1	—	—	Pull down to GND

U25 Pin Number	U25 Signal Name	Net Name	Certus-NX-65 Ball Location	Application Note
41	VDDIO	SGMII_VDDIO	—	I/O Power
42	VDD1P0	VCCA_1V_PHY	—	1.0 V Power
43	RESETN	PHY_RSTN	U16	Default pull down
44	INT/PWDN	PHY_INT	V16	Pulled up by default. Shunt JP3 to pull down.
45	LED_2	SGMII_LED2	—	Drive Red LED D41
46	LED_1	SGMII_LED1	—	Drive Red LED D40
47	LED_0	SGMII_LED0	—	Drive Red LED D39
48	VDDA1P8	SGMII_VDDA1P8	—	1.8 V Power

9. HyperRAM

This section describes the LFD2NX-65 device interconnection HyperRAM on the Certus-NX LFD2NX-65 Development Board (Table 9.1).

Table 9.1. HyperRAM Controller Interconnections

HyperRAM in 49-Ball FBGA		Net Name	
Symbol Name	Ball Location	Net Name	LFD2NX-65 Ball Location
CS#	A4	HR_CSN	Y20
CK	B3	HR_CK	AB16
CK#	B2	HR_CKN	AA16
DQ0	D4	HR_DQ0	W17
DQ1	D3	HR_DQ1	AA22
DQ2	C5	HR_DQ2	V15
DQ3	D5	HR_DQ3	W16
DQ4	D6	HR_DQ4	V17
DQ5	E4	HR_DQ5	Y18
DQ6	E3	HR_DQ6	W18
DQ7	E2	HR_DQ7	W22
DQ8	F5	HR_DQ8	Y19
DQ9	F1	HR_DQ9	V19
DQ10	F7	HR_DQ10	AB15
DQ11	F2	HR_DQ11	V20
DQ12	G5	HR_DQ12	AA21
DQ13	G1	HR_DQ13	V18
DQ14	G7	HR_DQ14	AA15
DQ15	G2	HR_DQ15	V22
RWDS0	C4	HR_RW0	Y21
RWDS1	F4	HR_RW1	W21
RESET#	A5	HR_RSTN	AA20

10. PCIe Gold Finger

Certus-NX LFD2NX-65 Development Board supports x1 PCIe Gen2, as shown in [Figure 10.1](#). The signal connections are listed in [Table 10.1](#).



Figure 10.1. Top Side of PCIe Edge Connector

Table 10.1. Gold Finger Pin Connections

CN1 Pin Number	Net Name	LFD2NX-65 Ball Location
A1	PRSNT1n	—
A2,A3,B1,B2,B3	12_IN_PCIE	—
A4,A12,A15,A18,B4,B7,B13,B16,B18	GND	—
A9,A10,B8	PCIE_3V3	—
A11	PCIE_PERSTn	A19
A13	PCIE_CLKp	B11
A14	PCIE_CLKn	C11
A16	x1_PERp0	A10
A17	x1_PERn0	A9
B14	x1_PETp0	A13
B15	x1_PETn0	A12
B17	PRSNT2n	—
—	R0_ext	E11
—	RETO_ref	E12

11. Headers and Test Connections

This section describes the Certus-NX-65 Development Board headers and test connections.

11.1. Versa Headers

The board provides two headers, J27 and J28, for expansion purposes.

Table 11.1. Versa J27 Header Pin Connections

J27 Pin Number	Net Name	LFD2NX-65 Ball Location
1	GND	—
2	NC	—
3	EXPCON_2V5 ¹	—
4	EXPCON_IO29	P1
5	EXPCON_IO30	P3
6	EXPCON_IO31	P2
7	EXPCON_IO32	M1
8	EXPCON_IO33	P4
9	EXPCON_IO34	M2
10	EXPCON_IO35	M4
11	EXPCON_IO36	L2
12	EXPCON_IO37	R3
13	EXPCON_IO38	W8
14	EXPCON_IO39	W9
15	EXPCON_IO40	L3
16	EXPCON_IO41	P6
17	EXPCON_IO42	L4
18	EXPCON_IO43	R5
19	EXPCON_IO44	L6
20	EXPCON_IO45	R6
21	5VIN ¹	—
22	GND	—
23	EXPCON_2V5 ¹	—
24	GND	—
25	+3.3V	—
26	GND	—
27	+3.3V	—
28	GND	—
29	EXPCON_OSC	P5
30	GND	—
31	EXPCON_CLKIN	U6
32	GND	—
33	EXPCON_CLKOUT	L5
34	GND	—
35	EXPCON_3V3 ²	—
36	GND	—
37	EXPCON_3V3 ²	—

J27 Pin Number	Net Name	LFD2NX-65 Ball Location
38	GND	—
39	EXPCON_3V3 ¹	—
40	GND	—

Notes:

1. The net is optionally connected to the power source through a resistor DNI.
2. The net is optionally connected to the power source through a resistor DI.

Table 11.2. Versa J28 Header Pin Connections

J28 Pin Number	Net Name	LFD2NX-65 Ball Location
1	HPE_RESOUT#	N6
2	GND	—
3	EXPCON_IO0	N5
4	EXPCON_IO1	N4
5	EXPCON_IO2	W6
6	EXPCON_IO3	V8
7	EXPCON_IO4	V9
8	EXPCON_IO5	W7
9	EXPCON_IO6	U8
10	EXPCON_IO7	W4
11	EXPCON_IO8	V5
12	EXPCON_IO9	W3
13	EXPCON_IO10	V4
14	EXPCON_IO11	V3
15	EXPCON_IO12	U5
16	EXPCON_IO13	W2
17	EXPCON_IO14	T5
18	EXPCON_IO15	W1
19	GND	—
20	EXPCON_3V3 ¹	—
21	EXPCON_IO16	T4
22	GND	—
23	EXPCON_IO17	T1
24	GND	—
25	EXPCON_IO18	T2
26	GND	—
27	EXPCON_IO19	T3
28	EXPCON_IO20	W5
29	EXPCON_IO21	V1
30	GND	—
31	EXPCON_IO22	U2
32	EXPCON_IO23	V2
33	EXPCON_IO24	N2
34	GND	—
35	EXPCON_IO25	R1
36	EXPCON_IO26	R4
37	EXPCON_IO27	U1
38	HPE_CARSEL#	R2

J28 Pin Number	Net Name	LFD2NX-65 Ball Location
39	EXPCON_IO28	N1
40	GND	—

Notes:

- The net is optionally connected to the power source through a resistor DI.

11.2. Arduino Board GPIO Headers (DNI)

The board provides four headers, J21, J22, J23, and J24, for the Arduino Zero Board adaptation.

Table 11.3. Arduino J21 Pin Connections

J21 Pin Number	Net Name	Arduino ZERO Board Signal	LFD2NX-65 Ball Location	Comments
1	AR_IO8	~D8/PA06	G5	—
2	AR_IO9	~D9/PA07	F6	—
3	AR_SS_IO10	~D10/PA18/SS	F7	Defaults to the SS function on the Arduino ZERO Board.
4	AR_MOSI_IO11	~D11/PA16/COPI	J7	Defaults to the COPI function on the Arduino ZERO Board.
5	AR_MISO_IO12	~D12/PA19/CIPO	K7	Defaults to the CIPO function on the Arduino ZERO Board.
6	AR_SCK_IO13	~D13/PA17/SCK	J5	Defaults to the SCK function on the Arduino ZERO Board.
7	GND	GND	—	—
8	AR_AREF	AREF/PA03	J2	AR_AREF connection to AREF through R43.
9	AR_SDA	D20/PA22/SDA	F3	Defaults to the SDA function on the Arduino ZERO Board. It is optionally connected to SDA0 through R44 (DNI).
10	AR_SCL	D21/PA23/SCL	G3	Defaults to the SCL function on the Arduino ZERO Board. It is optionally connected to SCL0 through R45 (DNI).

Table 11.4. Arduino J22 Pin Connections

J22 Pin Number	Net Name	Arduino ZERO Board Signal	LFD2NX-65 Ball Location	Comments
1	AR_IO0	D0/RX/PA11	J4	—
2	AR_IO1	D1//TX/PA10	G6	—
3	AR_IO2	D2/PA14	K5	—
4	AR_IO3	~D3/PA09	G7	—
5	AR_IO4	~D4/PA08	J3	—
6	AR_IO5	~D5/PA15	J1	—
7	AR_IO6	~D6/PA20	H1	—
8	AR_IO7	D7/PA21	G4	—

Table 11.5. Arduino J23 Pin Connections

J23 Pin Number	Net Name	Arduino ZERO Board Signal	LFD2NX-65 Ball Location	Comments
1	AR_IO14	ATN	K4	—
2	NC	IOREF	—	—
3	AR_RESET	RESET	J8	Pin J8 should be set high by default. Avoid making the Arduino ZERO Board in the Reset status when connected.
4	+3.3V_AR	+3V3	—	3.3 V power supply from the Arduino ZERO Board.
5	AR_5V	+5V	—	Jump to 5 V on-board power rail through JP16.
6	GND	GND	—	—
7	GND	GND	—	—
8	+12V	VIN	—	Share with +12 V on-board power rail.

Note:

If JP6 is installed, a 5 V power can be supplied from either the Arduino Board or the Certus-NX-65 Development Board. With JP6 removed, both boards need their own 5 V power.

Table 11.6. Arduino J24 Pin Connections

J24 Pin Number	Net Name	Arduino ZERO Board Signal	LFD2NX-65 Ball Location	Comments
1	AR_AD0	D14/ADC0/PA02	F1	Defaults to ADC0 on Arduino ZERO Board.
2	AR_AD1	D15/ADC1/PB08	F2	Defaults to ADC1 on Arduino ZERO Board.
3	AR_AD2	D16/ADC2/PB09	H3	Defaults to ADC2 on Arduino ZERO Board.
4	AR_AD3	D17/ADC3/PA04	H4	Defaults to ADC3 on Arduino ZERO Board.
5	AR_AD4	D18/ADC4/PA05	G1	Defaults to ADC4 on Arduino ZERO Board.
6	AR_AD5	D19/ADC5/PB02	H7	Defaults to ADC5 on Arduino ZERO Board.

11.3. FPC Headers

The board provides one 30-Pin FPC headers CN2, for board signal extension. It gets six pairs of LVDS or SLVS signals for high-speed data transmitter or receiver.

Table 11.7. FPC Header Pin Connections

CN2 at the Top Side		
Pin Number	Net Name	Ball Location
1	NC	—
2	DATA0_N	Y10
3	DATA0_P	Y9
4	GND	—
5	DATA1_N	U10
6	DATA1_P	T10
7	GND	—
8	DATA2_N	AA12
9	DATA2_P	Y12
10	GND	—
11	DATA3_N	AB12
12	DATA3_P	AB13
13	GND	—
14	DATA4_N	U13
15	DATA4_P	V13

CN2 at the Top Side		
Pin Number	Net Name	Ball Location
16	GND	—
17	DATA5_N	V14
18	DATA5_P	W15
19	GND	—
20	NC	—
21	NC	—
22	GND	—
23	NC	—
24	NC	—
25	GND	—
26	NC	—
27	NC	—
28	TP28	—
29	TP28	—
30	NC	—

11.4. Aardvark Header (DNI)

The Aardvark I2C/SPI Host Adapter is a fast and powerful I2C bus and SPI bus host adapter through USB. It allows you to interface a Windows, Linux, or Mac OS X PC through USB to a downstream embedded system environment and transfer serial messages using the I2C and SPI protocols.

The Certus-NX-65 Development Board provides an Aardvark compatible header for customer applications. The I2C bus is optionally connecting to a global I2C bus on the board.

Table 11.8. Aardvark J26 Header Pin Connections

J26 Pin Number	Net Name	LFD2NX-65 Ball Location
1	AK_SCL	K2
2	GND	—
3	AK_SDA	K3
4	+5V_I2C	—
5	AK_MISO	L1
6	+5V_SPI	—
7	AK_SCLK	J6
8	AK_MOSI	L1
9	AK_SS	K1
10	GND	—

11.5. Raspberry Pi Board GPIO Header (DNI)

The Certus-NX-65 Development Board provides a 40-pin receptacle that is compatible with the GPIO header of Raspberry Pi 2/3 serial models.

Table 11.9. Raspberry Pi J5 Header Pin Connections

J5 Pin Number	Net Name	LFD2NX-65 Ball Location	J6 Pin Number	Net Name	LFD2NX-65 Ball Location
1	3.3V_RASP ¹	—	2	RASP_5V ²	—
3	RASP_IO02	D9	4	RASP_5V ²	—

J5 Pin Number	Net Name	LFD2NX-65 Ball Location	J6 Pin Number	Net Name	LFD2NX-65 Ball Location
5	RASP_IO03	D8	6	GND	—
7	RASP_IO04	C8	8	RASP_IO14	G8
9	GND	—	10	RASP_IO15	F8
11	RASP_IO17	B7	12	RASP_IO18	G7
13	RASP_IO27	A5	14	GND	—
15	RASP_IO22	B5	16	RASP_IO23	E4
17	3.3V_RASP ¹	—	18	RASP_IO24	E3
19	RASP_IO10	E4	20	GND	—
21	RASP_IO09	D3	22	RASP_IO25	F3
23	RASP_IO11	D2	24	RASP_IO08	F1
25	GND	—	26	RASP_IO07	G3
27	RASP_ID_SD	E2	28	RASP_ID_SC	E1
29	RASP_IO05	E1	30	GND	—
31	RASP_IO06	A3	32	RASP_IO12	F5
33	RASP_IO13	B3	34	GND	—
35	RASP_IO19	B4	36	RASP_IO16	H5
37	RASP_IO26	A4	38	RASP_IO20	H7
39	GND	—	40	RASP_IO21	H8

Notes:

1. 3.3 V power is supplied from the Raspberry Pi Board.
2. The 5 V power can come from either the Raspberry Pi Board or the Certus-NX-65 Development Board when jumper JP7 is installed. When jumper JP7 is not installed, both boards need their own 5 V power.

11.6. PMOD Headers

The Certus-NX-65 Development Board provides three 12-pin receptacle headers that is compatible with the Digilent PMOD™ interface spec.

Table 11.10. J9 Header Pin Connections

J9 Pin Number	Net Name	LFD2NX-65 Ball Location	J9 Pin Number	Net Name	LFD2NX-65 Ball Location
1	PMOD0_1	Y7	7	PMOD0_5	Y2
2	PMOD0_2	Y4	8	PMOD0_6	Y8
3	PMOD0_3	Y3	9	PMOD0_7	Y6
4	PMOD0_4	Y5	10	PMOD0_8	Y1
5	GND	—	11	GND	—
6	VCCIO2	—	12	VCCIO2	—

Table 11.11. J34 Header (DNI) Pin Connections

J34 Pin Number	Net Name	LFD2NX-65 Ball Location	J34 Pin Number	Net Name	LFD2NX-65 Ball Location
1	PMOD1_1	R21	7	PMOD1_5	P22
2	PMOD1_2	R22	8	PMOD1_6	U17
3	PMOD1_3	T21	9	PMOD1_7	T22
4	PMOD1_4	U18	10	PMOD1_8	P21
5	GND	—	11	GND	—
6	+1.8V	—	12	+1.8V	—

Table 11.12. J53 Header (DNI) Pin Connections

J53 Pin Number	Net Name	LFD2NX-65 Ball Location	J53 Pin Number	Net Name	LFD2NX-65 Ball Location
1	PMOD2_1	E15	7	PMOD2_5	E16
2	PMOD2_2	E14	8	PMOD2_6	F18
3	PMOD2_3	G19	9	PMOD2_7	G18
4	PMOD2_4	E17	10	PMOD2_8	E18
5	GND	—	11	GND	—
6	VCCIO_3V3BANK	—	12	VCCIO_3V3BANK	—

11.7. User I2C Interface

This board provides more options for user I2C access from different LFD2NX-65 Wide Range I/O to multiple on-board headers. They are solidly connected for target applications, but those connections to bridge SCL0/SDA0 are not populated by default. You need to customize the interconnection for I2C applications across the board. For example, if you want to use an Aardvark I2C host to access the ARDUINO Board, you can use the internal fabric logic of LFD2NX-65 to bridge AK_SCL/AK_SDA with AR_SCL/AR_SDA, or add bridge resistors according to [Table 11.13](#) to connect all of them to SCL0/SDA0 for bridge interconnections on board without involving the FPGA. You also need to set up the design with the tri-state mode for output high with pull-up resistors. If there is no pull-up set up on the counterpart boards or internal GPIOs of the FPGA, you can add JP12 and JP13 to leverage FTDI's I2C pull-up R33 and R34 for SCL0/SDA0. Note that the multi-drives should be disabled for FTDI_SCL/FTDI_SDA in this case. You can add JP9 to disable FTDI output and force the FPGA output High-Z from ball location A19/A18.

By adding JP12 and JP13, you can also access the FPGA I2C configure interface from those extension boards with I2C host through SCL0/SDA0, which provides the flexibility to update the bitstream from an extension board in some applications.

Table 11.13. I2C Connections

Extend header	LFD2NX-65 Bank	LFD2NX-65 Ball Location for JTAG	Net Name	Bridge Resistor to SCL0/SDA0
Versa Header (J28)	1	W2	EXPCON_IO13	R35
		T5	EXPCON_IO15	R37
Aardvark Header (J26)	6	K2	AK_SCL	R231 (DNI)
		K3	AK_SDA	R230 (DNI)
Arduino Header (J21)	6	G3	AR_SCL	R45 (DNI)
		F3	AR_SDA	R44 (DNI)
Raspberry Pi Header (J5)	7	D4	RASP_ID_SC	R85 (DNI)
		E2	RASP_ID_SD	R87 (DNI)
Raspberry Pi Header (J5)	7	D8	RASP_IO03	R785 (DNI)
		D9	RASP_IO02	R84 (DNI)

11.8. ADC and Potentiometer

There are two dedicate ADC input pairs for the LFD2NX-65 device. This board provides multiple application options. Positive input of another pair ADC1 is connected to a 10 kΩ Trimmer Potentiometers (POT2) which provides voltage variation from 0 V to selectable VCCIO4, as shown in [Figure 11.2](#). The negative input of ADC1 is grounded through a 1 kΩ resistor.

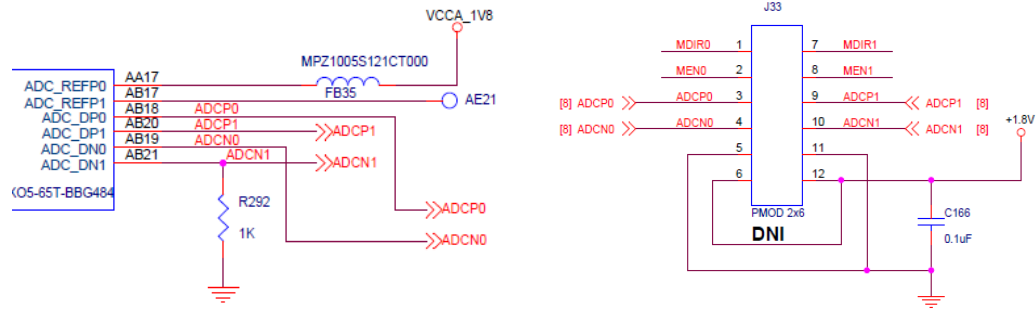


Figure 11.1. Circuit Design for ADC0

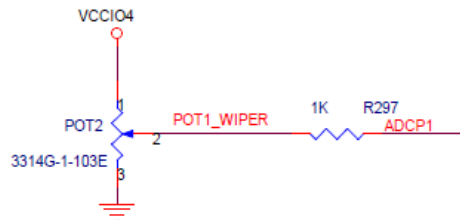


Figure 11.2. Circuit Design for ADC1

Rotate the Trimmer clockwise to decrease the voltage, as shown in Figure 11.3. To increase the voltage to ADCP1, rotate the POT counter-clockwise.

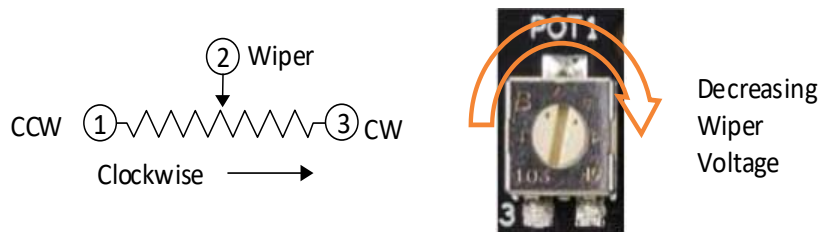


Figure 11.3. Trimmer Wiper Description

12. LEDs and Switches

LEDs and switches of the Certus-NX-65 Development Board that can be used in demonstrations and customer designs are described in this section.

12.1. DIP Switches

Four LFD2NX-65 pins are connected to the two switches of SW6 and the four switches of SW7, as shown in the circuit design in [Figure 12.1](#). The DIP switches are connected to logic level 0 when in the ON position, as shown in [Figure 12.2](#).

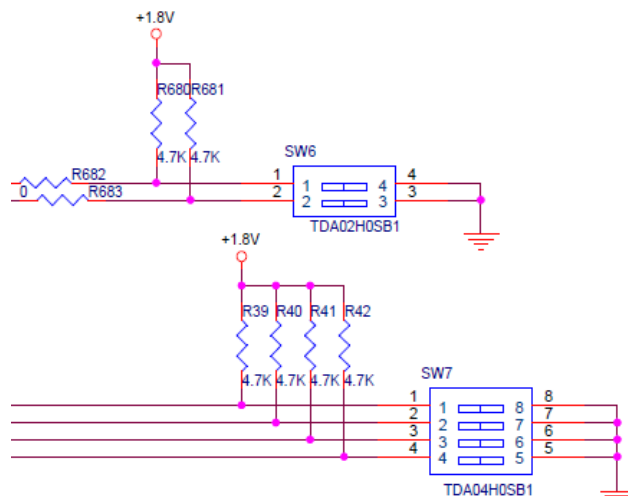


Figure 12.1. Two-Position and Four-Position DIP Switch Circuits

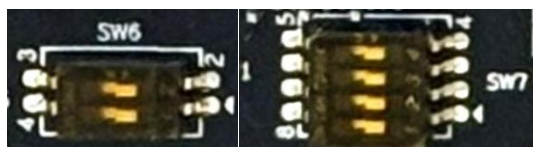


Figure 12.2. Two-Position and Four-position DIP Switches

One side of each switch is connected to GPIOs within the VCIO4 bank and pulled up through 4.7 kΩ resistors. The other side is grounded. The designated pins are connected, as shown in [Table 12.1](#).

Table 12.1. Two-Position DIP Switch Signals

Net Name	LFD2NX-65 Ball Location	SW6 DIP Switch Position	4.7 kΩ Pull-up Resistor	Logic Input Level at ON Position
DIP1	P20	1	R682	0
DIP2	P19	2	R683	0

Table 12.2. Four-Position DIP Switch Signals

Net Name	LFD2NX-65 Ball Location	SW7 DIP Switch Position	4.7 kΩ Pull-up Resistor	Logic Input Level at ON Position
DIP1	T19	1	R39	0
DIP2	T20	2	R40	0
DIP3	R18	3	R41	0
DIP4	T18	4	R42	0

12.2. General Purpose Push Buttons

The Certus-NX-65 Development Board provides four push button switches, SW1, SW2, SW3, and SW4, for demonstrations and user applications. Pressing these buttons drives a logic level 0 to the corresponding I/O pins.

Table 12.3. Push Button Switch Signals

Push Button Number	LFD2NX-65 Ball Location	Function
SW1	W5	ASC Reset
SW2	D6	General-purpose
SW3	D16	PROGRAMN
SW4	C5	General-purpose

SW1 connected with EXPCON_IO20 is used as the ASC global reset push button, which is connected to the MANDATORY_RESET signal when mated with the Lattice ASC Bridge Board. Refer to [ASC Bridge Board Evaluation Board User Guide \(FPGA-EB-02025\)](#) for detailed information with ASC application. SW3 is used as the PROGRAMN push button to trigger the configuration process without power cycle. For detailed information on PROGRAMN, refer to [Common Programming and Configuration FAQs with Supplementary Concepts for CrossLink-NX, Certus-NX, and CertusPro-NX \(FPGA-AN-02048\)](#).

12.3. General Purpose LEDs

The Certus-NX-65 Development Board provides eight red LEDs that are connected to general purpose I/O. The LEDs are lighted when the output is driven LOW. [Table 12.4](#) lists the LEDs and their associated pins.

Table 12.4. LED Signals

LEDs Ref Name	Signal Name	LFD2NX-65 Ball Location	Color
D6	LED_0	E20	Green
D7	LED_1	E21	Green
D8	LED_2	D20	Green
D9	LED_3	D21	Green
D10	LED_4	D19	Green
D11	LED_5	D18	Green
D12	LED_6	B20	Green
D13	LED_7	A21	Green
D14	LED_8	C18	Yellow
D15	LED_9	A20	Yellow
D16	LED_10	B19	Yellow
D17	LED_11	B18	Yellow
D18	LED_12	C17	Yellow
D19	LED_13	A17	Yellow
D20	LED_14	B17	Yellow
D21	LED_15	A16	Yellow
D30	LED_16	B16	Red
D31	LED_17	A15	Red
D32	LED_18	B15	Red
D33	LED_19	B14	Red
D34	LED_20	C14	Red
D35	LED_21	C13	Red
D36	LED_22	D13	Red
D37	LED_23	E13	Red

13. Software Requirements

The following software are required to develop designs for the Certus-NX-65 Development Board:

- Lattice Radiant Software 2025.2 or later
- Radiant Programmer 2025.2 or later


14. Storage and Handling

Static electricity can shorten the life span of electronic components. Observe these tips to prevent damage that can occur from electrostatic discharge:

- Use antistatic precautions such as operating on an antistatic mat and wearing an antistatic wristband.
- Store the Certus-NX-65 Development Board in the provided packaging.
- Touch a metal USB housing to equalize voltage potential between you and the board.

15. Ordering Information

Table 15.1. Ordering Information

Description	Ordering Part Number	China RoHS Environment-Friendly Use Period (EFUP)
Certus-NX-65 Development Board	LFD2NX-65-EVN	

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Appendix A. Certus-NX-65 Development Board Schematics


	5	4	3	2	1																		
	Certus-NX-65 Development Board Rev - B																						
D	<p>01 - Title Page</p> <p>02 - Block Diagram</p> <p>03 - Raspberry Pi and Prototype (BANK0 and BANK3)</p> <p>04 - LEDs and Flash PMOD3 (BANK1)</p> <p>05 - FTDI to Hard JTAG I/F and PMOD2 (BANK2)</p> <p>06 - HyperRAM and PCIe (BANK5 and BANK80)</p> <p>07 - SGMII&RGMII PHY, FPC, and PMOD1 (BANK6 and BANK4)</p> <p>08 - Versa Connector and Segment LED (BANK7 and BANK8)</p> <p>09 - Arduino and Aardvark Headers (BANK9)</p> <p>10 - FTDI to Soft JTAG I/F and PMOD0 (BANK11)</p>																						
C																							
B	<p>11 - Power Rails and Monitors (1)</p> <p>12 - Power Rails and Monitors (2)</p> <p>13 - USB Power</p> <p>14 - Power Regulators</p> <p>15 - Power Tree</p> <p>16 - Revision History</p>																						
A	<div style="text-align: center;">  <p>Lattice Semiconductor Applications Email: techsupport@latticesemi.com Phone (503) 268-8001 -or- (800) LATTICE</p> </div> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td colspan="3" style="text-align: center;">Title Page</td> </tr> <tr> <td style="font-size: small;">Size</td> <td style="font-size: small;">Project</td> <td style="font-size: small;">Schematic Rev</td> </tr> <tr> <td style="text-align: center;">A</td> <td style="text-align: center;">Certus-NX-65 Development Board</td> <td style="text-align: center;">1.0</td> </tr> <tr> <td colspan="2"></td> <td style="font-size: small;">Board Rev</td> </tr> <tr> <td colspan="2"></td> <td style="text-align: center;">B</td> </tr> <tr> <td style="font-size: small;">Date:</td> <td style="font-size: small;">Friday, January 30, 2026</td> <td style="font-size: small;">Sheet 1 of 16</td> </tr> </table>					Title Page			Size	Project	Schematic Rev	A	Certus-NX-65 Development Board	1.0			Board Rev			B	Date:	Friday, January 30, 2026	Sheet 1 of 16
Title Page																							
Size	Project	Schematic Rev																					
A	Certus-NX-65 Development Board	1.0																					
		Board Rev																					
		B																					
Date:	Friday, January 30, 2026	Sheet 1 of 16																					
	5	4	3	2	1																		

Figure A.1. Title Page

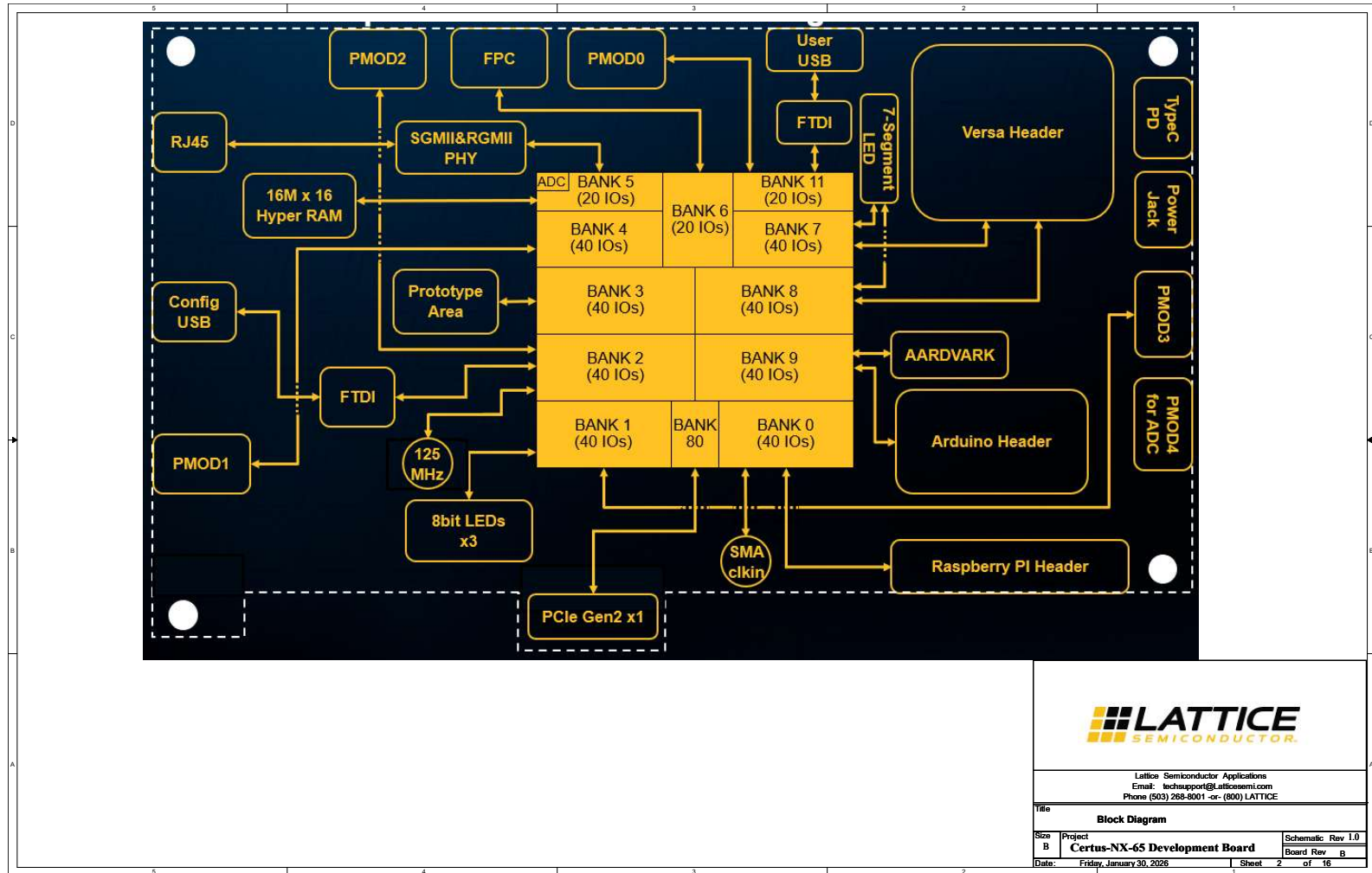


Figure A.2. Block Diagram

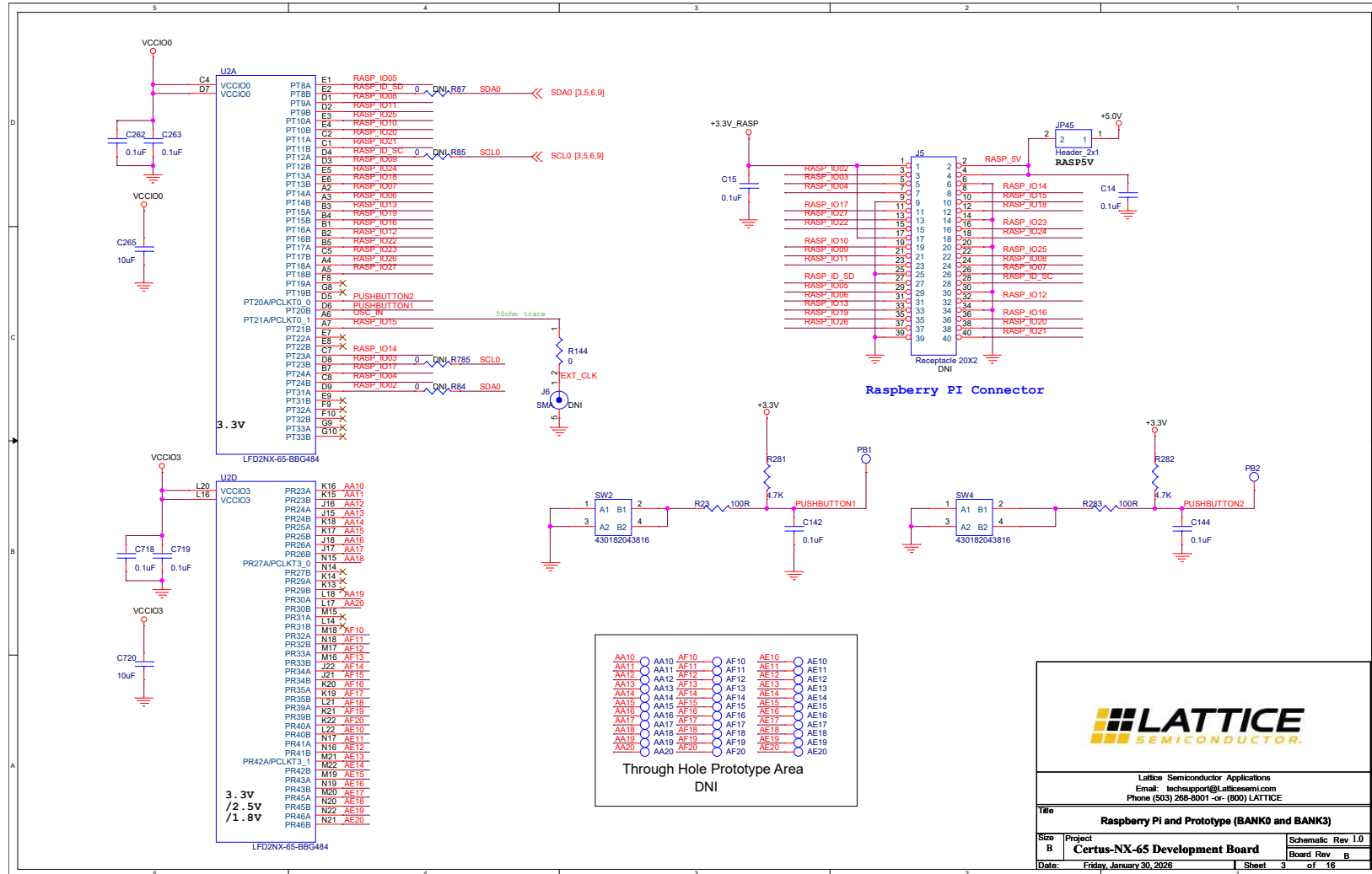


Figure A.3. Raspberry Pi and Prototype (BANK0 and BANK3)

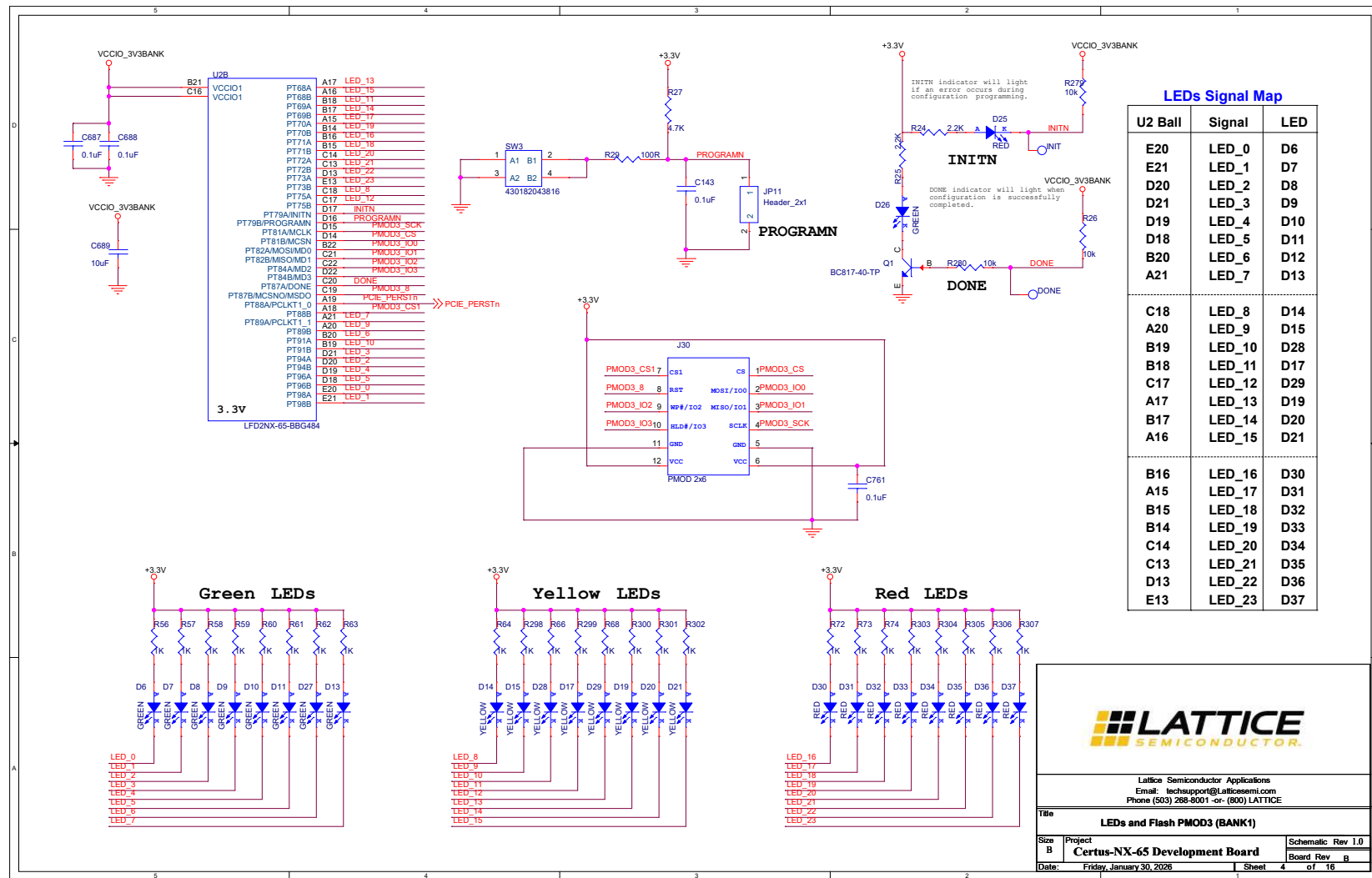


Figure A.4. LEDs and Flash PMOD3 (BANK1)

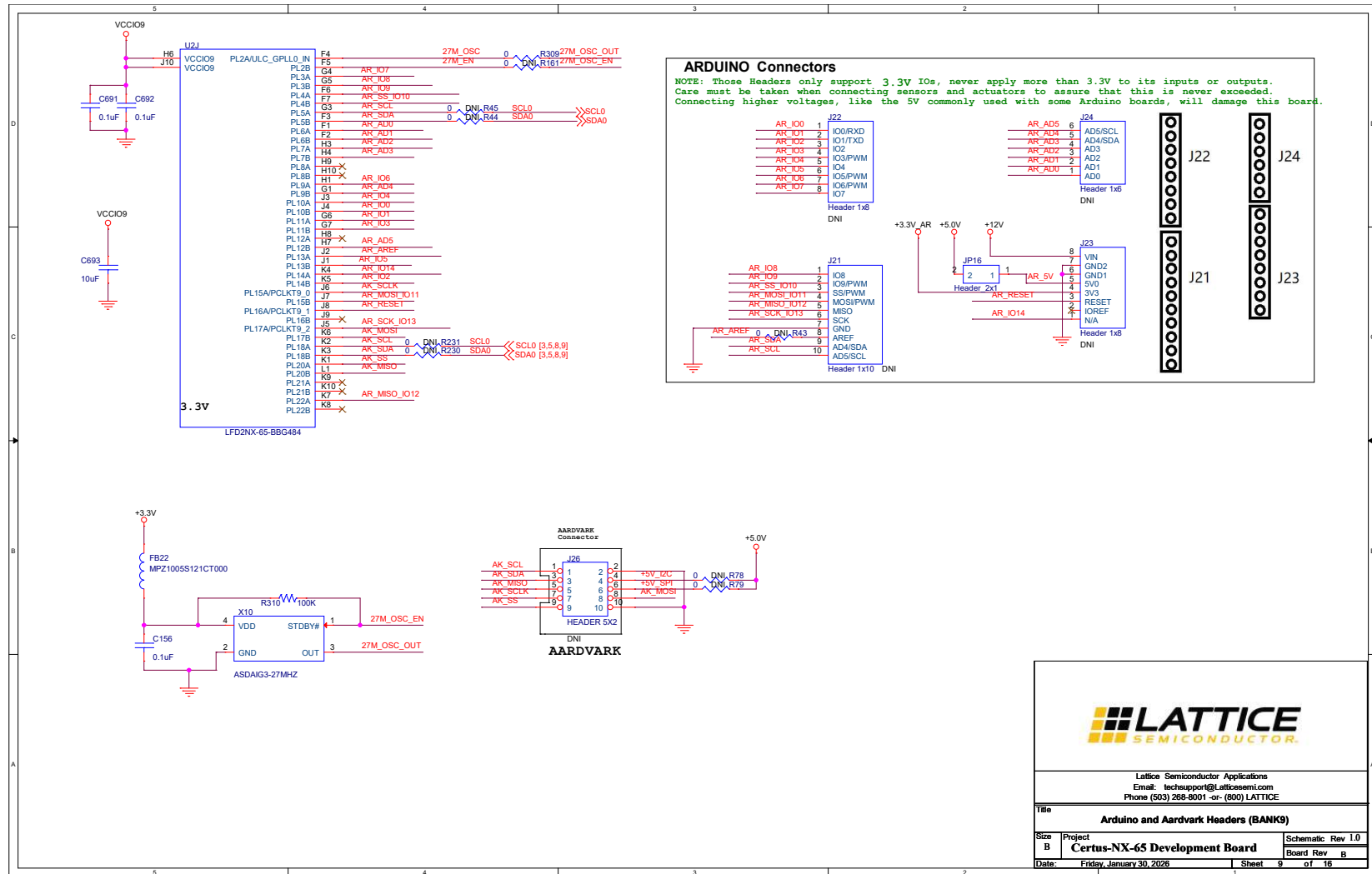


Figure A.9. Arduino and Aardvark Headers (BANK9)

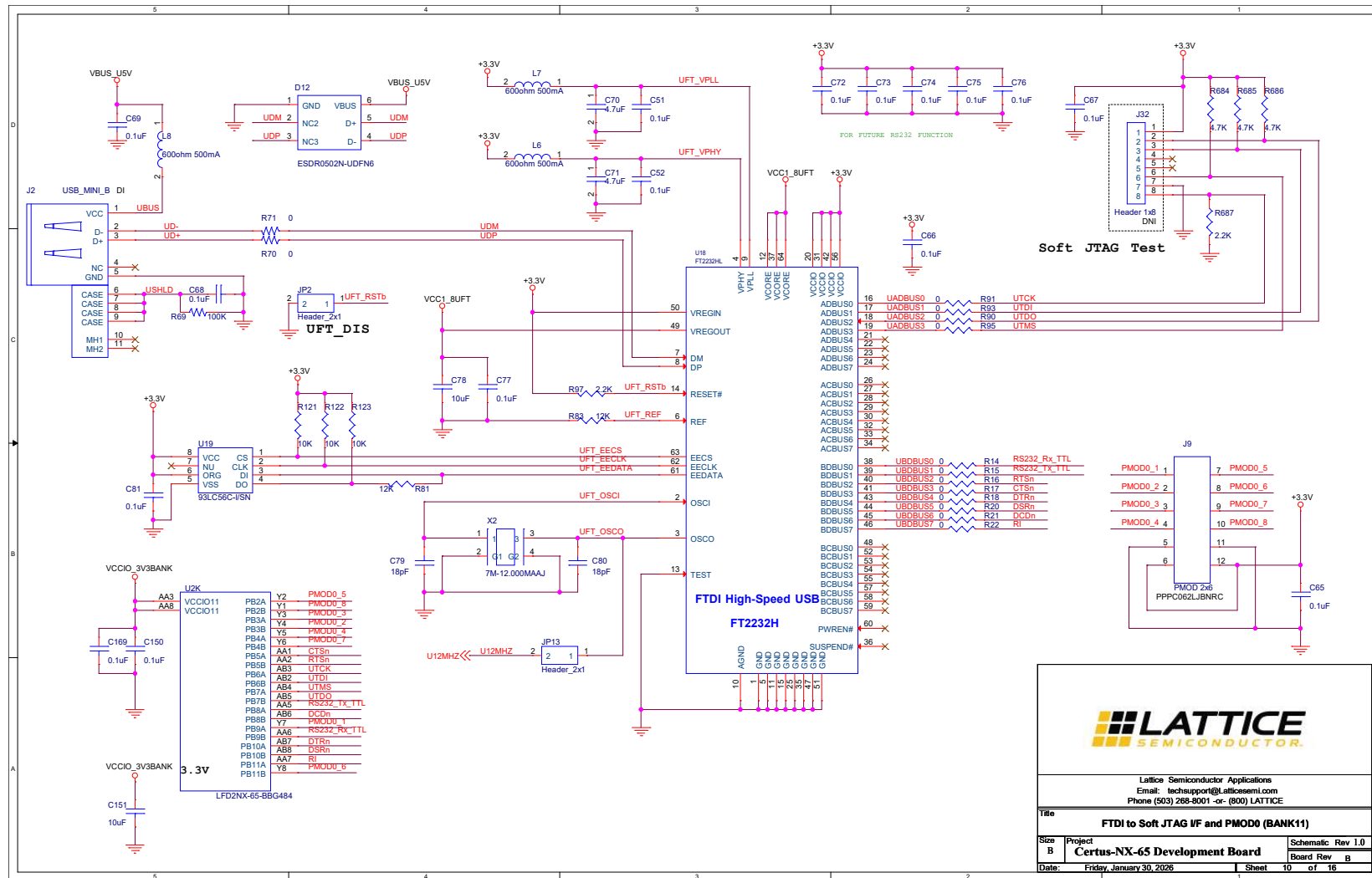


Figure A.10. FTDI to Soft JTAG I/F and PMOD0 (BANK 11)

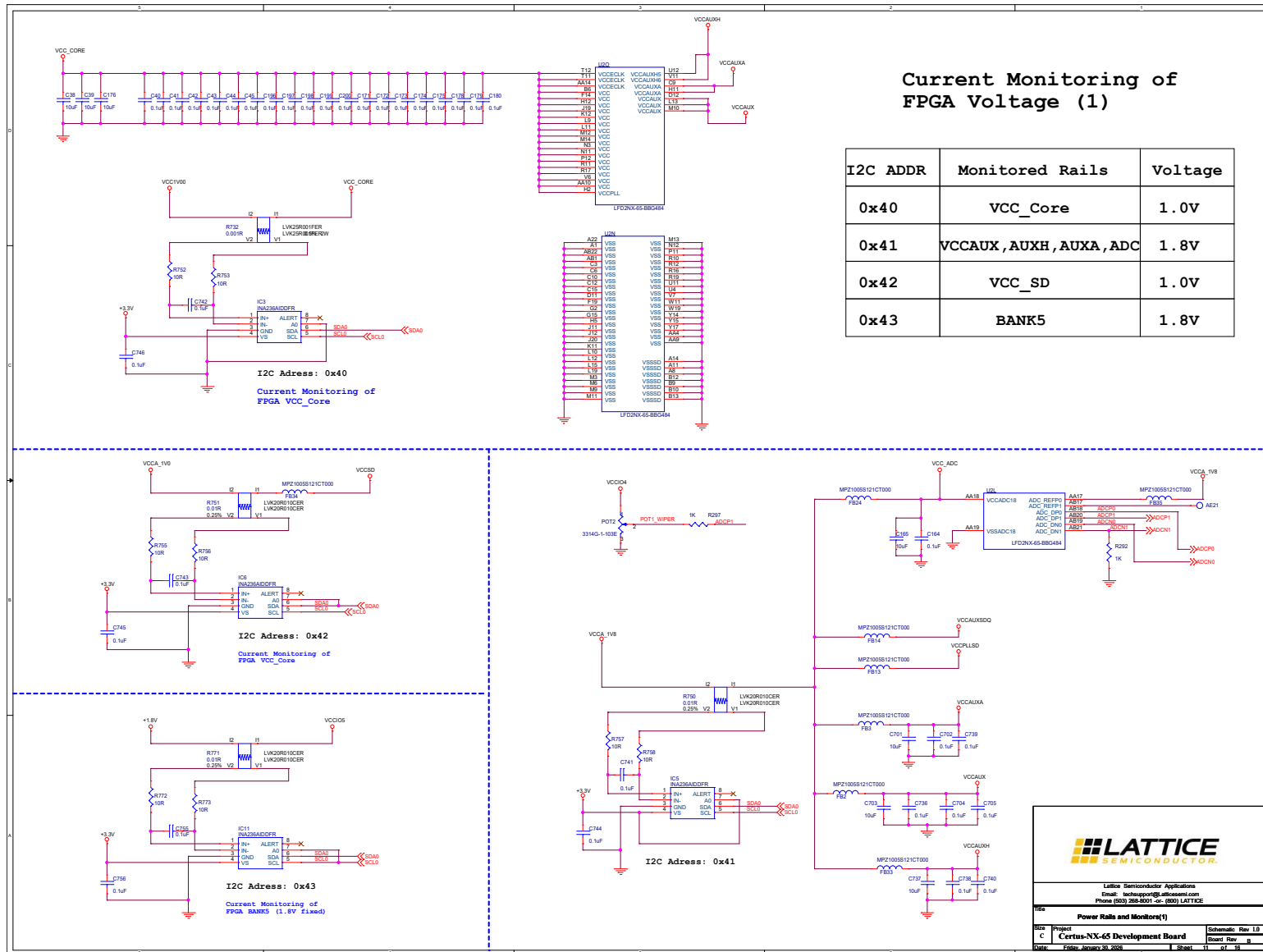


Figure A.11. Power Rails and Monitors (1)

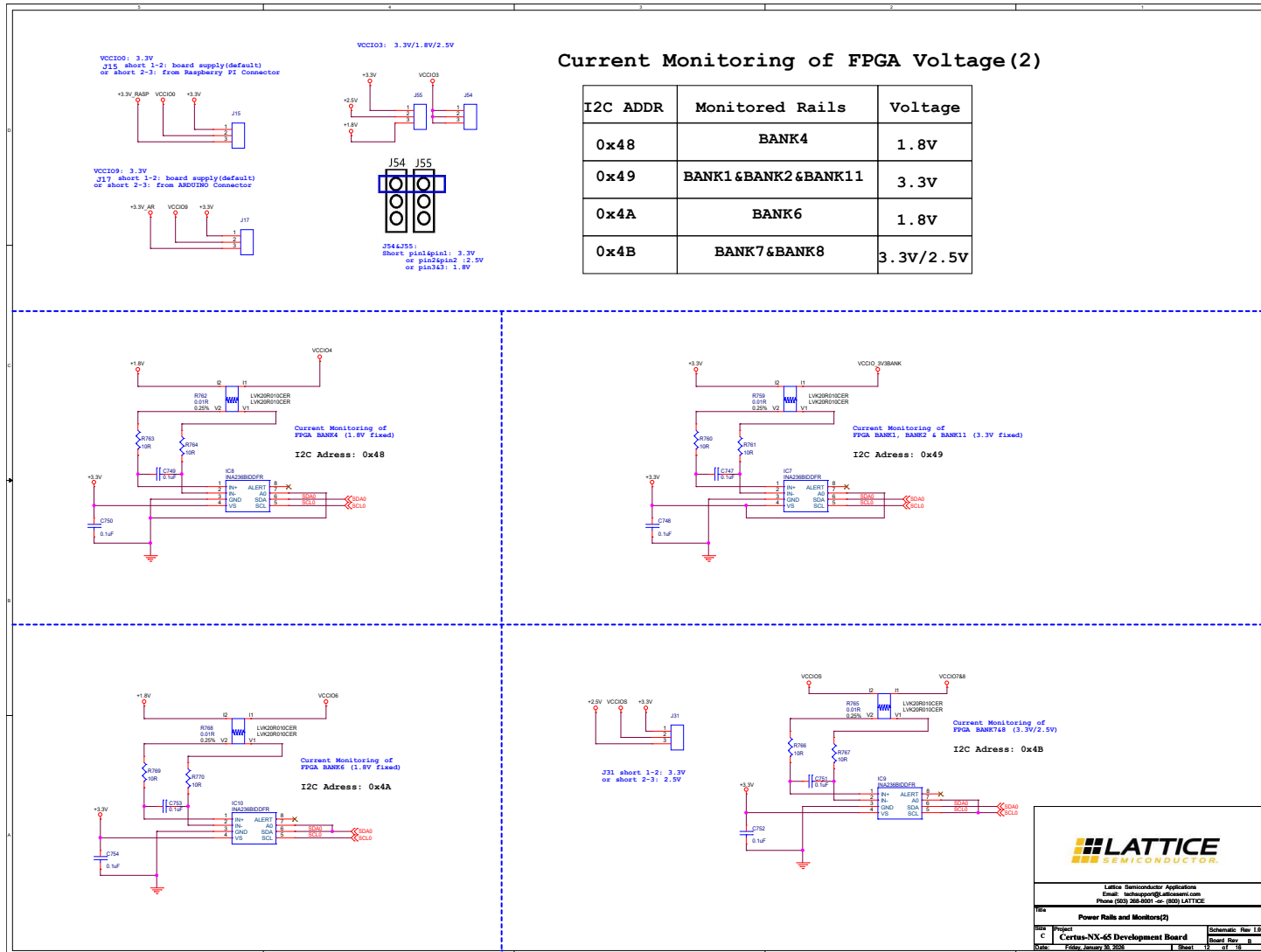


Figure A.12. Power Rails and Monitors (2)

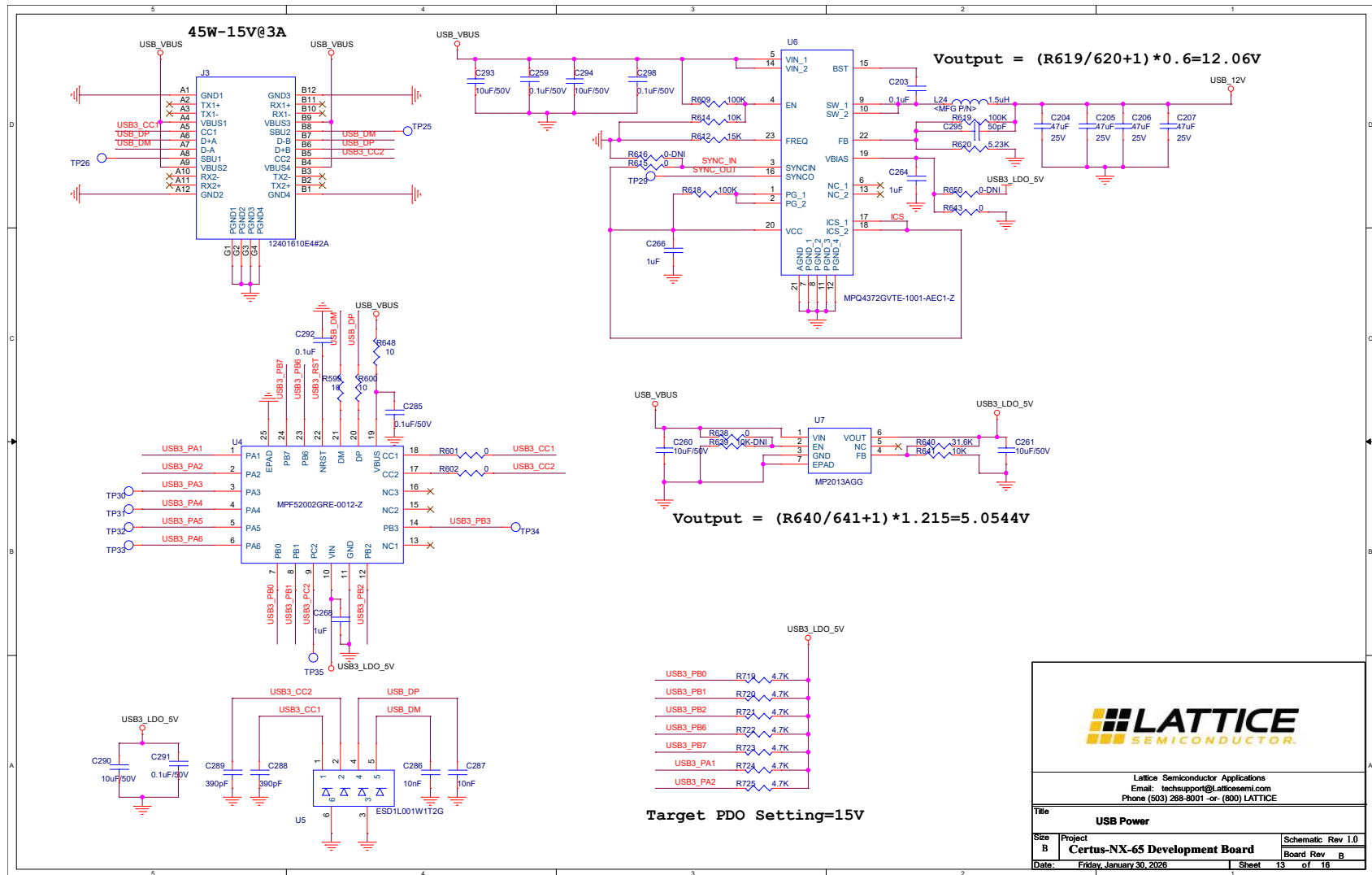


Figure A.13. USB Power

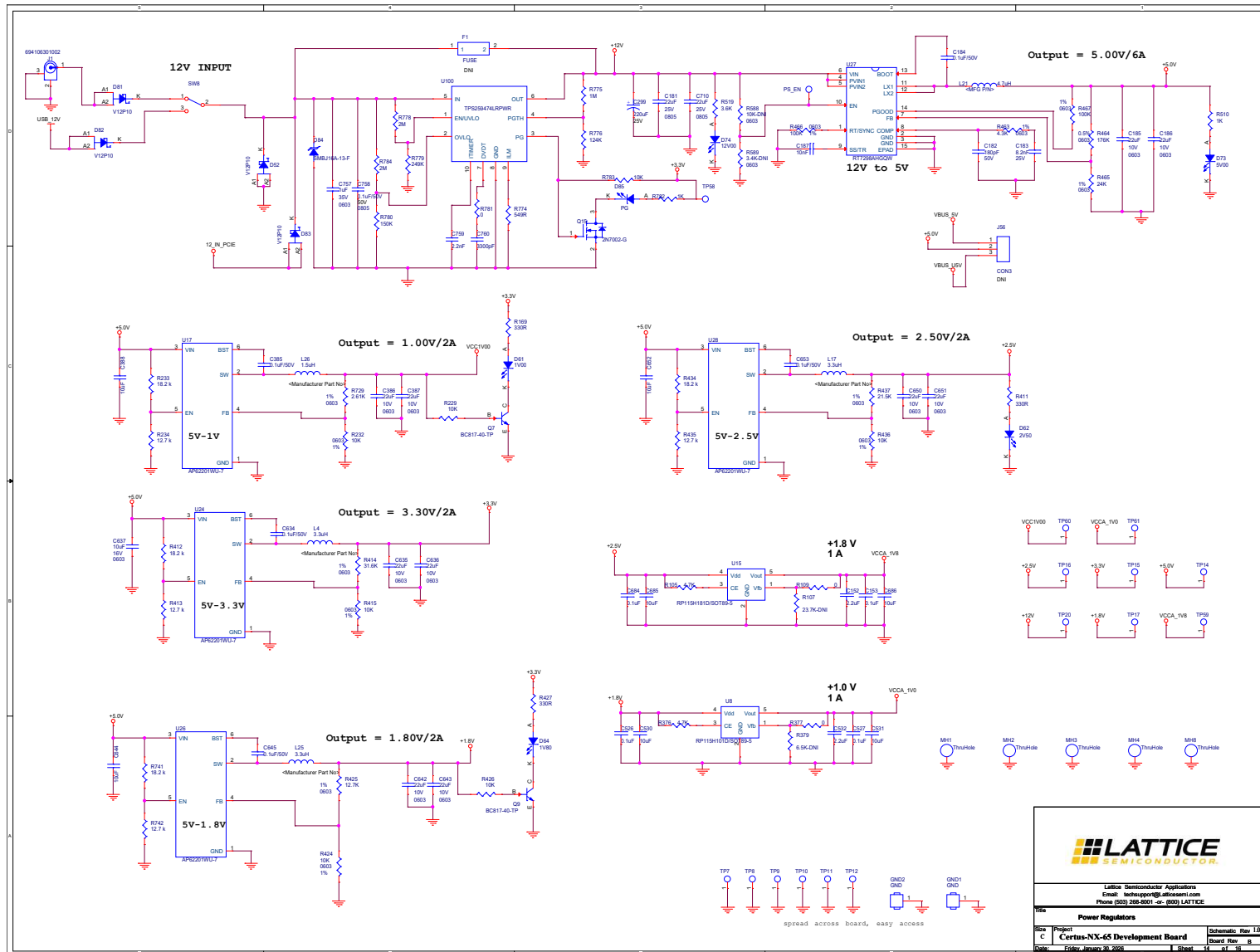


Figure A.14. Power Regulators

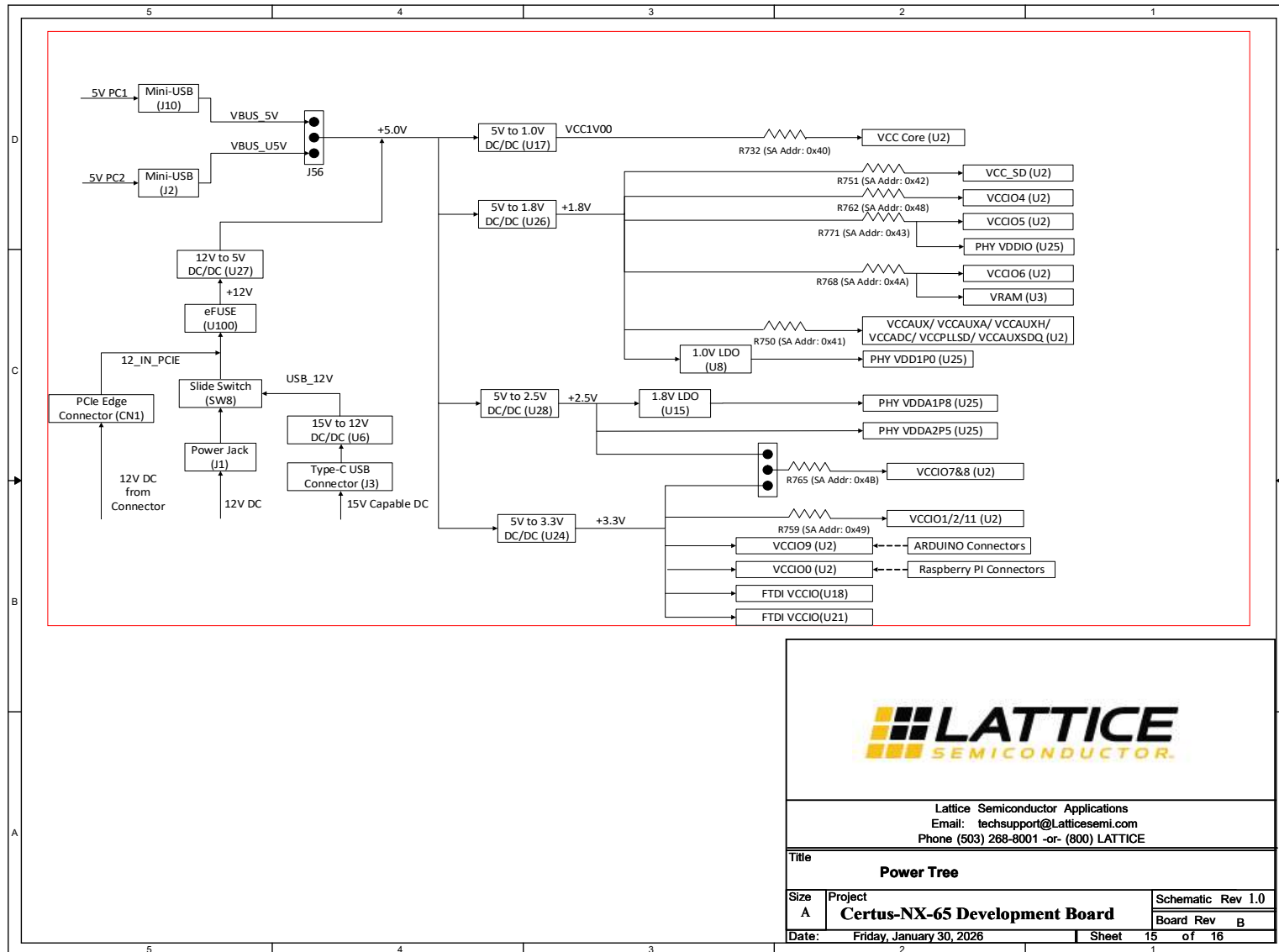


Figure A.15. Power Tree

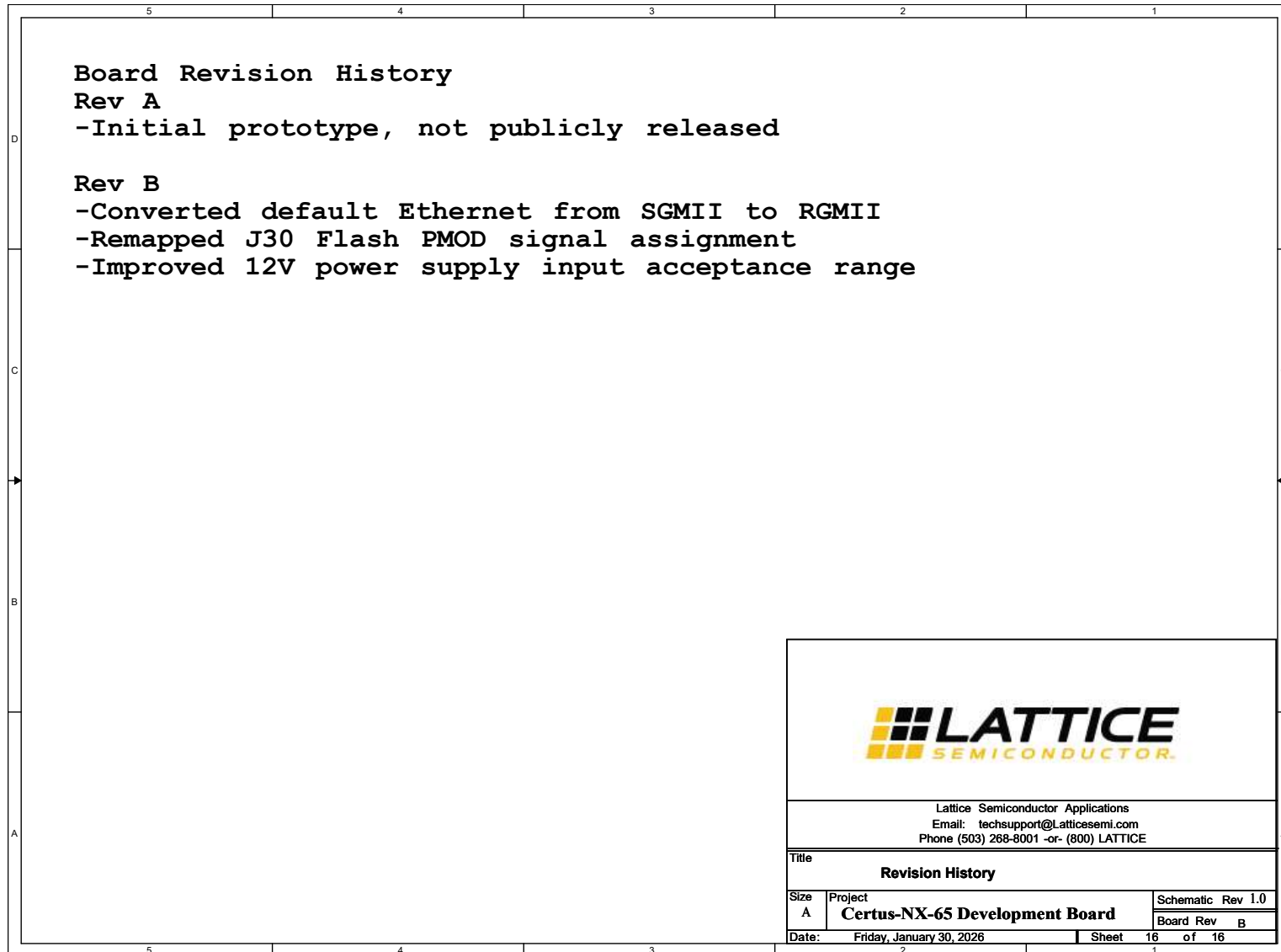


Figure A.16. Revision History

Appendix B. Certus-NX-65 Development Board Bill of Materials

Item	Qty	Reference	Part	PCB Footprint	Part Number	Manufacturer	Description	Comment
1	1	CN1	PCI Express x1 Edge Finger Conn.	PCI-E-X1	—	—	—	DNI
2	1	CN2	0462880 3000084 6+	0462880 3000084 6plus	0462880300 00846+	KYOCERA/AVX	CONN FFC BOTTOM 30POS 0.5MM R/A	—
3	2	C1,C2	150pF	C0402	GCM1555C1 H151JA16J	Murata	CAP CER 150PF 50V COG/NPO 0402	DNI
4	7	C3,C4,C13,C79,C80,C126,C127	18pF	C0402	C0402C180K 3GACTU	Kemet	CAP CER 18PF 25V COG/NPO 0402	—
5	2	C5,C7	47uF	C0805	C2012X5R1A 476M125AC	TDK	CAP CER 47UF 10V X5R 0805	—
6	2	C6,C8	0.47uF	C0201	CL03A474KQ 3NUNC	Samsung	CAP CER 0.47UF 6.3V X5R 0201	—
7	86	C14,C15,C20,C24,C25,C28,C29,C32,C51,C52,C65,C66,C67,C68,C69,C72,C73,C74,C75,C76,C77,C81,C93,C94,C95,C96,C101,C102,C107,C108,C113,C114,C115,C118,C119,C121,C122,C124,C125,C128,C129,C130,C131,C132,C135,C136,C137,C142,C143,C144,C145,C146,C147,C148,C149,C150,C153,C156,C160,C166,C167,C169,C203,C262,C263,C267,C292,C526,C527,C684,C687,C688,C691,C692,C694,C695,C717,C718,C719,C725,C726,C727,C729,C730,C731,C761	0.1uF	C0402	C0402C104K 4RACTU	Kemet	CAP CER 0.1UF 16V X7R 0402	—
8	29	C19,C23,C26,C30,C38,C39,C78,C87,C97,C103,C109,C123,C138,C151,C163,C165,C176,C265,C530,C685,C686,C689,C693,C696,C701,C703,C720,C721,C737	10uF	C0603	LMK107BJ10 6MALTD	Taiyo Yuden	CAP CER 10UF 10V X5R 0603	—
9	27	C40,C41,C42,C43,C44,C45,C164,C171,C172,C173,C174,C175,C178,C179,C180,C196,C197,C198,C199,C200,C702,C704,C705,C736,C738,C739,C740	0.1uF	C0201	GRM033R60 J104KE19D	Murata	CAP CER 0.1UF 6.3V X5R 0201	—

Item	Qty	Reference	Part	PCB Footprint	Part Number	Manufacturer	Description	Comment
10	4	C70,C71,C117,C120	4.7uF	C0603	CL10A475KP8NNNC	Samsung	CAP CER 4.7UF 10V X5R 0603	—
11	7	C88,C100,C105,C111,C187,C286,C287	10nF	C0402	CC0402KRX7R7BB103	Yageo	CAP CER 10000PF 16V X7R 0402	—
12	16	C89,C90,C91,C92,C98,C99,C104,C106,C110,C112,C116,C264,C266,C268,C728,C732	1uF	C0402	GRM155R61E105KA12D	Murata	CAP CER 1UF 25V X5R 0402	—
13	2	C152,C532	2.2uF	C0805	CL21B225KP FNNNE	Samsung	CAP CER 2.2UF 10V X7R 0805	—
14	2	C154,C155	220NF-0402SMT	C0402	CL05B224KO5NNNC	Samsung	CAP CER 0.22UF 16V X7R 0402	—
15	2	C181,C710	22uF	C0805	GRM21BR61E226ME44L	Murata	CAP CER 22UF 25V X5R 0805	—
16	1	C182	180pF	C0402	04025C181KAT2A	KYOCERA AVX	CAP CER 180PF 50V X7R 0402	—
17	1	C183	8.2nF	C0402	GRM155R71E822KA01D	Murata	CAP CER 8200PF 25V X7R 0402	—
18	10	C184,C259,C285,C291,C298,C385,C634,C645,C653,C758	0.1uF/50V	C0805	VJ0805Y104KXAMR	Vishay	CAP CER 0.1UF 50V X7R 0805	—
19	10	C185,C186,C386,C387,C635,C636,C642,C643,C650,C651	22uF	C0603	CL10A226M P8NUNE	Samsung	CAP CER 22UF 10V X5R 0603	—
20	4	C204,C205,C206,C207	47uF	C1210	KGM32LR51E476MU	KYOCERA AVX	CAP CER 47UF 25V X5R 1210	—
21	5	C260,C261,C290,C293,C294	10uF/50V	C0805	GRM21BR61H106KE43L	Taiyo Yuden	CAP CER 10UF 50V X5R 0805	—
22	2	C288,C289	390pF	C0201	0201YC391KAT2A	Murata	CAP CER 390PF 16V X7R 0201	—
23	1	C295	50pF	C0603	06035A500JAT2A	KYOCERA AVX	CAP CER 50PF 50V NPO 0603	—
24	1	C299	220uF	L10r3x10r3	A785KN227M1ELAS029	Kemet	CAP ALUMHYB 220UF 20% 25V SMD	—
25	3	C388,C644,C652	10uF	C0805	C2012X5R1E106M085AC	TDK	CAP CER 10UF 25V X5R 0805	—
26	2	C531,C637	10uF	C0603	EMK107BBJ106MA-T	Taiyo Yuden	CAP CER 10UF 16V X5R 0603	—

Item	Qty	Reference	Part	PCB Footprint	Part Number	Manufacturer	Description	Comment
27	16	C741,C742,C743,C744,C745, C746,C747,C748,C749,C750, C751,C752,C753,C754,C755, C756	0.1uF	C0201	GRM033R61 A104ME15D	Murata	CAP CER 0.1UF 10V X5R 0201	—
28	1	C757	1uF	C0603	C1608X7R1V 105K080AC	TDK	CAP CER 1UF 35V X7R 0603	—
29	1	C759	2.2nF	C0603	C0603C222K 5RACTU	Kemet	CAP CER 2200PF 50V X7R 0603	—
30	1	C760	3300pF	C0603	C0603X332K 5RACTU	Kemet	CAP CER 3300PF 50V X7R 0603	—
31	15	D6,D7,D8,D9,D10,D11,D13, D26,D27,D61,D62,D64,D73, D74,D85	GREEN	APT1608	APT1608CG CK	Kingbright	LED GREEN CLEAR CHIP SMD	—
32	2	D12,D22	ESDR050 2N- UDFN6	UDFN6_ 040	ESDR0502N MUTBG	Onsemi	TVS DIODE 5.5VWM 6UDFN	—
33	8	D14,D15,D17,D19,D20,D21, D28,D29	YELLOW	APT1608	APT1608SYC K	Kingbright	LED YELLOW CLEAR CHIP SMD	—
34	1	D23	1N4448 W	1N4448 W	1N4448WT	Onsemi	DIODE GEN PURP 75V 200MA SOD523F	—
35	13	D24,D25,D30,D31,D32,D33, D34,D35,D36,D37,D39,D40, D41	RED	APT1608	APT1608EC	Kingbright	LED RED CLEAR CHIP SMD	—
36	4	D52,D81,D82,D83	V12P10	TO-277A	V12P10- M3/86A	Vishay	DIODE SCHOTTKY 100V 12A TO277A	—
37	1	D84	SMBJ16A -13-F	D- SMBJ16	SMBJ16A- 13-F	Diodes Incorporated	TVS DIODE 16VWM 26VC SMB	—
38	1	D86	7- SEGMENT	LED10- 057-394- XZFMDK 05A	XZFMDK05A	SUNLED	DISPLAY 7- SEG 0.2" SGL RED 10SMD	—
39	15	FB1,FB2,FB3,FB11,FB12, FB13,FB14,FB22,FB24,FB29, FB31,FB32,FB33,FB34,FB35	MPZ100 5S121CT 000	FB0402	MPZ1005S1 21CT000	TDK	FERRITE BEAD 120 OHM 0402 1LN	—
40	1	F1	FUSE	FU0680L	0680L4000- 05	Bel Fuse Inc.	FUSE BRD MNT 4A 125VAC/VD C 2SMD	DNI

Item	Qty	Reference	Part	PCB Footprint	Part Number	Manufacturer	Description	Comment
41	4	IC3,IC5,IC6,IC11	INA236A IDDFR	SOT23-8- 0r65	INA236AIDD FR	TI	IC CURRENT MON 0.015% TSOT23-8	—
42	4	IC7,IC8,IC9,IC10	INA236BI DDFR	SOT23-8- 0r65	INA236BIDD FR	TI	IC CURRENT MON 0.015% TSOT23-8	—
43	13	JP2,JP3,JP4,JP6,JP7,JP9,JP11, JP13,JP16,JP19,JP40,JP44, JP45	Header_ 2x1	Header_ 2x1	861400021Y O2LF	Amphenol	CONN HEADER VERT 2POS 2.54MM	—
44	1	J1	6941063 01002	6941063 01002	6941063010 02	Würth	CONN PWR JACK 2.1X5.5MM SOLDER	—
45	2	J2,J10	USB_MI NI_B	usb2-0- rec-240- 0001-9	UX60-MB- 5ST	Hirose	UX60-MB- 5ST	—
46	1	J3	1240161 0E4#2A	USB_TYP EC_RA_S MT	12401610E4 #2A	Amphenol	CONN RCP USB3.1 TYPEC 24P SMD RA	—
47	1	J5	Receptac le 20X2	HDR254- 2X20_so cket	PPTC202LFB NRC	Sullins	CONN HDR 40POS 0.1 TIN PCB	DNI
48	1	J6	SMA	bnc5- 100-280t	5-1814832-1	TE	CONN SMA JACK STR 50 OHM PCB	DNI
49	1	J7	7498111 001-RJ45	RJ45- 7498111 001	7498111001	Würth	CONN JACK 1PORT SURFACE MOUNT	—
50	3	J9,J53,J30	PMOD 2x6	PPPC062 LIBN-RC	PPPC062LJB N-RC	Sullins	PPPC062LJ BN-RC	—
51	8	J15,J17,J31,J51,J52,J54,J55, J57	CON3	HDR1X3	PH1-03-UA	Adam Tech	CONN HEADER VERT 3POS 2.54MM	—
52	1	J56	CON3	HDR1X3	PH1-03-UA	Adam Tech	CONN HEADER VERT 3POS 2.54MM	DNI
53	2	J18,J32	Header 1x8	hdr_amp _87220_ 8_1x8_1 00	22284081	Molex	CONN HEADER VERT 8POS 2.54MM	DNI

Item	Qty	Reference	Part	PCB Footprint	Part Number	Manufacturer	Description	Comment
54	1	J21	Header 1x10	CONF1X 10- 254P_26 12X240X 850H_TH	1012937891 0002BLF	Amphenol	CONN HEADER VERT 10POS 2.54MM	DNI
55	2	J22,J23	Header 1x8	CONF1X 8- 254P_21 04X240X 850H_TH	1012937890 8002BLF	Amphenol	CONN HEADER VERT 8POS 2.54MM	DNI
56	1	J24	Header 1x6	CONF1X 6- 254P_15 96X240X 850H_TH	1012937890 6002BLF	Amphenol	CONN HEADER VERT 6POS 2.54MM	DNI
57	1	J26	HEADER 5X2	HDR254- 2X5_SHR OUDED	30310- 6002HB	3M	CONN HEADER VERT 10POS 2.54MM	DNI
58	2	J27,J28	HDR40	HDR- 20x2	PRPC020DFB NRC	Sullins	CONN HEADER VERT 40POS 2.54MM	—
59	2	J33,J34	PMOD 2x6	PPPC062 LIBN-RC	PPPC062LJB N-RC	Sullins	CONN HDR 12POS 0.1 GOLD PCB R/A	DNI
60	3	L4,L17,L25	3.3uH	SRP4020 TA-3R3M	SRP4020TA- 3R3M	Bourns Inc.	FIXED IND 3.3UH 3.5A 76 MOHM SMD	—
61	6	L6,L7,L8,L11,L12,L13	600ohm 500mA	fb0603	BLM18AG60 1SN1D	Murata	FERRITE BEAD 600 OHM 0603 1LN	—
62	1	L21	4.7uH	8mmx8 mm	NR8040T4R7 N	Taiyo Yuden	FIXED IND 4.7UH 4.1A 23.4MOHM SM	—
63	2	L24,L26	1.5uH	SRP4020 TA-1R5M	SRP4020TA- 1R5M	Bourns Inc.	FIXED IND 1.5UH 4.5A 42 MOHM SMD	—
64	1	POT2	3314G-1- 103E	sot23- 3314G-1	3314G-1- 103E	Bourns Inc.	TRIMMER 10K OHM 0.25W GW TOP ADJ	—
65	7	Q1,Q2,Q3,Q4,Q6,Q7,Q9	BC817- 40-TP	SOT23-3	BC817-40-TP	Micro Commercial Co	TRANS NPN 45V 0.8A SOT-23	—

Item	Qty	Reference	Part	PCB Footprint	Part Number	Manufacturer	Description	Comment
66	1	Q15	2N7002-G	SOT23	2N7002-G	Microchip	MOSFET N-CH 60V 115MA SOT23	—
67	44	R14,R15,R16,R17,R18,R20,R21,R22,R31,R35,R37,R70,R71,R90,R91,R93,R95,R109,R144,R245,R246,R247,R249,R250,R251,R265,R266,R309,R377,R601,R602,R615,R638,R643,R677,R682,R683,R781,R786,R787,R788,R789,R790,R791	0	R0402	RC0402JR-070RL	Yageo	RES 0 OHM JUMPER 1/16W 0402	—
68	6	R23,R29,R36,R89,R283,R285	100R	R0402	ERJ-2RKF1000X	Panasonic	RES SMD 100 OHM 1% 1/10W 0402	—
69	14	R24,R25,R33,R34,R76,R77,R97,R219,R220,R221,R244,R255,R687,R728	2.2K	R0402	CRCW04022K20FKED	Vishay	RES SMD 2.2K OHM 1% 1/16W 0402	—
70	11	R26,R121,R122,R123,R256,R257,R258,R279,R280,R614,R641	10K	R0402	RC0402FR-0710KL	Yageo	RES 10K OHM 1% 1/16W 0402	—
71	3	R124,R714,R712	10K	R0402	RC0402FR-0710KL	Yageo	RES 10K OHM 1% 1/16W 0402	DNI
72	29	R27,R39,R40,R41,R42,R105,R241,R242,R243,R260,R281,R282,R284,R376,R680,R681,R684,R685,R686,R690,R694,R719,R720,R721,R722,R723,R724,R725,R727	4.7K	R0402	CRCW04024K70FKED	Vishay	RES SMD 4.7K OHM 1% 1/16W 0402	—
73	20	R30,R35,R37,R43,R44,R45,R67,R78,R79,R84,R85,R87,R146,R147,R159,R161,R230,R231,R678,R785	0	R0402	RC0402JR-070RL	Yageo	RES 0 OHM JUMPER 1/16W 0402	DNI
74	1	R32	11K	R0603	RT0603DRD0711KL	Yageo	RES SMD 11K OHM 0.5% 1/10W 0603	—
75	1	R38	2.2K	R0402	CRCW04022K20FKED	Vishay	CRCW0402 2K20FKED	DNI
76	33	R56,R57,R58,R59,R60,R61,R62,R63,R64,R66,R68,R72,R73,R74,R165,R166,R167,R261,R292,R297,R298,R299,R300,R301,R302,R303,R304,R305,R306,R307,R510,R679,R782	1K	R0402	RC0402FR-071KL	Yageo	RES 1K OHM 1% 1/16W 0402	—

Item	Qty	Reference	Part	PCB Footprint	Part Number	Manufacturer	Description	Comment
77	3	R713,R715,R65	2.49K	R0402	RC0402FR-072K49L	Yageo	RES 2.49K OHM 1% 1/16W 0402	—
78	9	R69,R222,R248,R310,R466,R467,R609,R618,R619	100K	R0402	RC0402FR-07100KL	Yageo	RES 100K OHM 1% 1/16W 0402	—
79	9	R75,R183,R184,R185,R186,R187,R188,R189,R190	22	R0603	RC0603FR-0722RL	Yageo	RES 22 OHM 1% 1/10W 0603	—
80	4	R81,R83,R259,R264	12K	R0603	RC0603FR-0712KL	Yageo	RES 12K OHM 1% 1/10W 0603	—
81	1	R107	23.7K-DNI	R0603	RC0603FR-0723K7L	Yageo	RES 23.7K OHM 1% 1/10W 0603	DNI
82	1	R127	976R	R0402	RP73PF1E976RBT	TE	RES 976 OHM 0.1% 1/10W 0402	—
83	1	R158	1M Ohm	R0201	RC0201JR-071ML	Yageo	RES 1M OHM 5% 1/20W 0201	—
84	3	R169,R411,R427	330R	R0603	ERJ-3EKF3300V	Panasonic	RES SMD 330 OHM 1% 1/10W 0603	—
85	7	R229,R232,R415,R424,R426,R436,R783,	10K	R0603	RC0603FR-0710KL	Yageo	RES 10K OHM 1% 1/10W 0603	—
86	4	R233,R412,R434,R741	18.2 k	R0402	RT0402BRD0718K2L	Yageo	RES SMD 18.2KOHM 0.1% 1/16W 0402	—
87	4	R234,R413,R435,R742	12.7 k	R0402	ERJ-2RKF1272X	Panasonic	RES SMD 12.7K OHM 1% 1/10W 0402	—
88	1	R379	6.5K-DNI	R0603	RC0603DR-076K49L	Yageo	RES 6.49K OHM 0.5% 1/10W 0603	DNI
89	2	R414,R640	31.6K	R0603	RC0603FR-0731K6L	Yageo	RES 31.6K OHM 1% 1/10W 0603	—

Item	Qty	Reference	Part	PCB Footprint	Part Number	Manufacturer	Description	Comment
90	1	R425	12.7K	R0603	RC0603FR-1312K7L	Yageo	RES 12.7K OHM 1% 1/10W 0603	—
91	1	R437	21.5K	R0603	RC0603FR-0721K5L	Yageo	RES 21.5K OHM 1% 1/10W 0603	—
92	1	R463	4.3K	R0603	RC0603FR-074K3L	Yageo	RES 4.3K OHM 1% 1/10W 0603	—
93	1	R464	176K	R0603	RT0603DRE07176KL	Yageo	RES SMD 176K OHM 0.5% 1/10W 0603	—
94	1	R465	24K	R0603	RC0603FR-0724KL	Yageo	RES 24K OHM 1% 1/10W 0603	—
95	1	R519	3.6K	R0402	RC0402JR-073K6L	Yageo	RES 3.6K OHM 5% 1/16W 0402	—
96	2	R588,R639	10K-DNI	R0402	RC0402FR-0710KL	Yageo	RES 10K OHM 1% 1/16W 0402	DNI
97	1	R589	3.4K-DNI	R0603	RC0603FR-073K4L	Yageo	RES 3.4K OHM 1% 1/10W 0603	DNI
98	3	R599,R600,R648	10	R0402	RC0402FR-0710RL	Yageo	RES 10 OHM 1% 1/16W 0402	—
99	1	R612	15K	R0603	RC0603FR-0715KL	Yageo	RES 15K OHM 1% 1/10W 0603	—
100	2	R616,R650	0-DNI	R0402	RC0402JR-070RL	Yageo	RES 0 OHM JUMPER 1/16W 0402	DNI
101	1	R620	5.23K	R0603	RC0603FR-075K23L	Yageo	RES 5.23K OHM 1% 1/10W 0603	—
102	1	R729	2.61K	R0603	RC0603FR-072K61L	Yageo	RES 2.61K OHM 1% 1/10W 0603	—

Item	Qty	Reference	Part	PCB Footprint	Part Number	Manufacturer	Description	Comment
103	1	R732	0.001R	LVK25R0 01FER	LVK25R001F ER	Ohmite	RES 0.001 OHM 2W 2512 WIDE	—
104	7	R750,R751,R759,R762,R765, R768,R771	0.01R	LVK20R0 10CER	LVK20R010C ER	Ohmite	0.75W 0.010 OHM 0.25% LVK(2010)	—
105	16	R752,R753,R755,R756,R757, R758,R760,R761,R763,R764, R766,R767,R769,R770,R772, R773	10R	R0603	RC0603FR- 0710RL	Yageo	RES 10 OHM 1% 1/10W 0603	—
106	1	R774	549R	R0603	RC0603FR- 07549RL	Yageo	RES 549 OHM 1% 1/10W 0603	—
107	1	R775	1M	R0603	RC0603FR- 071ML	Yageo	RES 1M OHM 1% 1/10W 0603	—
108	1	R776	124K	R0603	CRCW06031 24KFKEA	Vishay	RES SMD 124K OHM 1% 1/10W 0603	—
109	2	R778,R784	2M	R0603	RC0603FR- 072ML	Yageo	RES 2M OHM 1% 1/10W 0603	—
110	1	R779	249K	R0603	RC0603FR- 07249KL	Yageo	RES 249K OHM 1% 1/10W 0603	—
111	1	R780	120K	R0603	RC0603FR- 07120KL	Yageo	RES 200K OHM 1% 1/10W 0603	—
112	4	SW1,SW2,SW3,SW4	4301820 43816	4301820 43816	4301820438 16	C&K Components	SWITCH TACTILE SPST-NO 0.05A 12V	—
113	1	SW6	TDA02H OSB1	sw4-050- 228-smd	TDA02H0SB 1	C&K Components	SWITCH SLIDE DIP SPST 0.025A 24V	—
114	1	SW7	TDA04H OSB1	sw8-050- 228-smd	TDA04H0SB 1	C&K Components	SWITCH SLIDE DIP SPST 0.025A 24V	—
115	1	SW8	1101M2 S2CQE2	SWITCH_ 3P-6A	1101M2S2C QE2	C&K Components	SWITCH SLIDE SPDT 6A 120V	—
116	1	U2	LFD2NX- 65- BBG484	BGA484J -080- 19X19- SOCKET		LATTICE		Target device

Item	Qty	Reference	Part	PCB Footprint	Part Number	Manufacturer	Description	Comment
117	1	U3	S80KS25 64GACH	BGA49C 100P7X7 _800X80 0X100	S80KS2564G ACHI040	Infineon Technologies	IC PSRAM 256MBIT HYPERBUS 49FBGA	—
118	1	U4	MPF520 02GRE- 0012-Z	QFN24N 4X4P0_5	MPF52002G RE-0012-Z	MPS	MPS USB PD controller QFN-24	—
119	1	U5	ESD1L00 1W1T2G	SC-88	ESD1L001W 1T2G	Onsemi	TVS 4 CH LOW CAP ESD PROTECT	—
120	1	U6	MPQ437 2GVTE- 1001- AEC1-Z	QFN-23	MPQ4372GV TE-1001- AEC1-Z	MPS	36V, 6A- 11A Low EMI Synchrono us Step- Down Converters	—
121	1	U7	MP2013 AGG	QFN6- MP2013	MP2013AGG -Z	MPS	40V, 150mA, Low- Quiescent Current Linear Regulator	—
122	1	U8	RP115H1 01D/SOT 89-5	SOT89-5	RP115H101 D-T1-FE	Nisshinbo	IC REG LINEAR 1V 1A SOT89-5	—
123	1	U15	RP115H1 81D/SOT 89-5	SOT89-5	RP115H181 D-T1-FE	Nisshinbo	RP115H181 D-T1-FE	—
124	4	U17,U24,U26,U28	AP62201 WU-7	TSOT26_ AP62201 WU-7	AP62201WU -7	Diodes Incorporated	IC REG BUCK ADJ 2A TSOT26	—
125	2	U18,U21	FT2232H L	tqfp64_0 p5_12p2 x12p2_h 1p6	FT2232HL	FTDI	IC USB HS DUAL UART/FIFO 64-LQFP	Use Lattice Inventory
126	2	U19,U23	93LC56C -I/SN	so8_50_ 244	93LC56C- I/SN	Microchip	IC EEPROM 2KBIT MICROWIR E 8SOIC	—
127	1	U25	DP83867 ERGZT	48VQFN _DP8386 7	DP83867ER GZT	TI	IC ETHERNET PHY 48VQFN	—
128	1	U27	RT7298A HGQW	14- WQFN	RT7298AHG QW	Richtek USA Inc.	IC REG BUCK ADJ 6A 14WQFN	—
129	1	U100	TPS2594 74LRPW R	QFN10- 2x2- TPS2594 7	TPS259474L RPWR	TI	IC ELECTRONI C FUSE 10VQFN	—

Item	Qty	Reference	Part	PCB Footprint	Part Number	Manufacturer	Description	Comment
130	2	X2,X6	7M-12.000MAAJ	xtal_4p_7m	7M-12.000MAAJ-T	TXC	CRYSTAL 12.0000MH Z 18PF SMD	—
131	1	X3	ABM3-25	XTAL_AB M3	ABM7-25.000MHZ-D2Y-T	Abracon	CRYSTAL 25.0000MH Z 18PF SMD	—
132	1	X5	ASDMB-125MHZ	x4-2520	ASDMB-125.000MHZ -XY-T	Abracon	MEMS OSC XO 125.0000M HZ LVCMOS	—
133	1	X10	ASDAIG3-27MHZ	x4-2520	ASDAIG3-27.000MHZ-X-K-T	Abracon	OSC XO 27.000MHZ 1.8V CMOS SMD	—
134	1	PCBA	LFD2NX-65-EVN-PCB	LFD2NX-65-EVN-PCB	LFD2NX-65-EVN-PCB	—	—	—
135	1	Add-in Card I/O Bracket	Add-in Card I/O Bracket	Standard , full hight	E012388A	EALHE	PCIe Standard Add-in Card I/O bracket for Lattice LFD2NX-65-EVN, full height	For Kitting,Ship together with PCBA
136	2	screw	screw	M3 x 5mm	E012390A	Shunxinyuan	PM3*5 Pan Head Cross Recess, Nickel Plated	For Kitting,Ship together with PCBA
137	1	screw	screw	#6-32	E012389A	Shunxinyuan	6#-32*6 Hex Head, Nickel Plated	For Kitting,Ship together with PCBA

Appendix C. User Defined Preference File

```
// These names follow the Certus-NX-65 Development Board schematic but,
// they may be defined by the user. Thus, they can be copied into the
// preference file and edited to match a different naming convention if
// needed or used to fill in the Spreadsheet view.
```

```
// LFD2NX-65 LED Connections
ldc_set_location -site {E20} [get_ports {LED_GREEN[0]}]
ldc_set_location -site {E21} [get_ports {LED_GREEN[1]}]
ldc_set_location -site {D20} [get_ports {LED_GREEN[2]}]
ldc_set_location -site {D21} [get_ports {LED_GREEN[3]}]
ldc_set_location -site {D19} [get_ports {LED_GREEN[4]}]
ldc_set_location -site {D18} [get_ports {LED_GREEN[5]}]
ldc_set_location -site {B20} [get_ports {LED_GREEN[6]}]
ldc_set_location -site {A21} [get_ports {LED_GREEN[7]}]
ldc_set_location -site {C18} [get_ports {LED_YELLOW[0]}]
ldc_set_location -site {A20} [get_ports {LED_YELLOW[1]}]
ldc_set_location -site {B19} [get_ports {LED_YELLOW[2]}]
ldc_set_location -site {B18} [get_ports {LED_YELLOW[3]}]
ldc_set_location -site {C17} [get_ports {LED_YELLOW[4]}]
ldc_set_location -site {A17} [get_ports {LED_YELLOW[5]}]
ldc_set_location -site {B17} [get_ports {LED_YELLOW[6]}]
ldc_set_location -site {A16} [get_ports {LED_YELLOW[7]}]
ldc_set_location -site {B16} [get_ports {LED_RED[0]}]
ldc_set_location -site {A15} [get_ports {LED_RED[1]}]
ldc_set_location -site {B15} [get_ports {LED_RED[2]}]
ldc_set_location -site {B14} [get_ports {LED_RED[3]}]
ldc_set_location -site {C14} [get_ports {LED_RED[4]}]
ldc_set_location -site {C13} [get_ports {LED_RED[5]}]
ldc_set_location -site {D13} [get_ports {LED_RED[6]}]
ldc_set_location -site {E13} [get_ports {LED_RED[7]}]

//Segment Display
ldc_set_location -site {P8} [get_ports seg_a]
ldc_set_location -site {U9} [get_ports seg_b]
ldc_set_location -site {T7} [get_ports seg_c]
ldc_set_location -site {T6} [get_ports seg_d]
ldc_set_location -site {R7} [get_ports seg_e]
ldc_set_location -site {R8} [get_ports seg_f]
ldc_set_location -site {P7} [get_ports seg_g]
ldc_set_location -site {N7} [get_ports seg_dp]

//DIP Switch Connections
ldc_set_location -site {P20} [get_ports DIPSW21]
ldc_set_location -site {P19} [get_ports DIPSW22]
ldc_set_location -site {T19} [get_ports DIPSW1]
ldc_set_location -site {T20} [get_ports DIPSW2]
ldc_set_location -site {R18} [get_ports DIPSW3]
ldc_set_location -site {T18} [get_ports DIPSW4]

//Push Button Connections
ldc_set_location -site {D6} [get_ports SW2]
ldc_set_location -site {D5} [get_ports SW4]

//ldc_set_sysconfig {PROGRAMN_PORT=DISABLE}
```

```
//ldc_set_location -site {D16} [get_ports PB4]

//Clock inputs
ldc_set_location -site {F17} [get_ports 125M_OSC]

//HyperRAM
# DQS GROUP 0
ldc_set_location -site {P10} [get_ports {dqs[0]}]
ldc_set_location -site {R13} [get_ports {dq[0]}]
ldc_set_location -site {R14} [get_ports {dq[1]}]
ldc_set_location -site {N12} [get_ports {dq[2]}]
ldc_set_location -site {N11} [get_ports {dq[3]}]
ldc_set_location -site {T14} [get_ports {dq[4]}]
ldc_set_location -site {T15} [get_ports {dq[5]}]
ldc_set_location -site {R16} [get_ports {dq[6]}]
ldc_set_location -site {R15} [get_ports {dq[7]}]
# DQS GROUP 1
ldc_set_location -site {P14} [get_ports {dqs[1]}]
ldc_set_location -site {N13} [get_ports {dq[8]}]
ldc_set_location -site {P15} [get_ports {dq[9]}]
ldc_set_location -site {P16} [get_ports {dq[10]}]
ldc_set_location -site {M14} [get_ports {dq[11]}]
ldc_set_location -site {N14} [get_ports {dq[12]}]
ldc_set_location -site {M12} [get_ports {dq[13]}]
ldc_set_location -site {M11} [get_ports {dq[14]}]
ldc_set_location -site {L11} [get_ports {dq[15]}]

# CK, CKE, CS, CA
ldc_set_location -site {T12} [get_ports clkout_p]
ldc_set_location -site {T11} [get_ports clkout_n]
ldc_set_location -site {P11} [get_ports csn]

//PMOD0 Connections
ldc_set_location -site {Y7} [get_ports PMOD0_1]
ldc_set_location -site {Y4} [get_ports PMOD0_2]
ldc_set_location -site {Y3} [get_ports PMOD0_3]
ldc_set_location -site {Y5} [get_ports PMOD0_4]
ldc_set_location -site {Y2} [get_ports PMOD0_5]
ldc_set_location -site {Y8} [get_ports PMOD0_6]
ldc_set_location -site {Y6} [get_ports PMOD0_7]
ldc_set_location -site {Y1} [get_ports PMOD0_8]

//PMOD1 Connections
ldc_set_location -site {R21} [get_ports PMOD1_1]
ldc_set_location -site {R22} [get_ports PMOD1_2]
ldc_set_location -site {T21} [get_ports PMOD1_3]
ldc_set_location -site {U18} [get_ports PMOD1_4]
ldc_set_location -site {P22} [get_ports PMOD1_5]
ldc_set_location -site {U17} [get_ports PMOD1_6]
ldc_set_location -site {T22} [get_ports PMOD1_7]
ldc_set_location -site {P21} [get_ports PMOD1_8]

//USER JTAG Connections
ldc_set_location -site {AB2} [get_ports UTDI]
ldc_set_location -site {AB5} [get_ports UTDO]
ldc_set_location -site {AB4} [get_ports UTMS]
```

```
ldc_set_location -site {AB3} [get_ports UTCK]
```

```
//USER RS232 Connections
```

```
ldc_set_location -site {AA6} [get_ports RS232_Rx_TTL]
ldc_set_location -site {AA5} [get_ports RS232_Tx_TTL]
ldc_set_location -site {B15} [get_ports RTSn]
ldc_set_location -site {A15} [get_ports CTSn]
ldc_set_location -site {E13} [get_ports DTRn]
ldc_set_location -site {E12} [get_ports DSRn]
ldc_set_location -site {D14} [get_ports DCDn]
ldc_set_location -site {E15} [get_ports RI]
```

```
//RASPBERRY PI Connections
```

```
ldc_set_location -site {E8} [get_ports RASP_I002]
ldc_set_location -site {F6} [get_ports RASP_I003]
ldc_set_location -site {G9} [get_ports RASP_I004]
ldc_set_location -site {G1} [get_ports RASP_I005]
ldc_set_location -site {G2} [get_ports RASP_I006]
ldc_set_location -site {G3} [get_ports RASP_I007]
ldc_set_location -site {F1} [get_ports RASP_I008]
ldc_set_location -site {E2} [get_ports RASP_I009]
ldc_set_location -site {F7} [get_ports RASP_I010]
ldc_set_location -site {F2} [get_ports RASP_I011]
ldc_set_location -site {F5} [get_ports RASP_I012]
ldc_set_location -site {G6} [get_ports RASP_I013]
ldc_set_location -site {G8} [get_ports RASP_I014]
ldc_set_location -site {F8} [get_ports RASP_I015]
ldc_set_location -site {H5} [get_ports RASP_I016]
ldc_set_location -site {E7} [get_ports RASP_I017]
ldc_set_location -site {G7} [get_ports RASP_I018]
ldc_set_location -site {H4} [get_ports RASP_I019]
ldc_set_location -site {H7} [get_ports RASP_I020]
ldc_set_location -site {H8} [get_ports RASP_I021]
ldc_set_location -site {E5} [get_ports RASP_I022]
ldc_set_location -site {E4} [get_ports RASP_I023]
ldc_set_location -site {E3} [get_ports RASP_I024]
ldc_set_location -site {F3} [get_ports RASP_I025]
ldc_set_location -site {H6} [get_ports RASP_I026]
ldc_set_location -site {E6} [get_ports RASP_I027]
ldc_set_location -site {E1} [get_ports RASP_ID_SC]
ldc_set_location -site {D1} [get_ports RASP_ID_SD]
```

```
//VERSA HEADER Connections
```

```
ldc_set_location -site {N5} [get_ports EXPCON_I00]
ldc_set_location -site {N4} [get_ports EXPCON_I01]
ldc_set_location -site {W6} [get_ports EXPCON_I02]
ldc_set_location -site {V8} [get_ports EXPCON_I03]
ldc_set_location -site {V9} [get_ports EXPCON_I04]
ldc_set_location -site {W7} [get_ports EXPCON_I05]
ldc_set_location -site {U8} [get_ports EXPCON_I06]
ldc_set_location -site {W4} [get_ports EXPCON_I07]
ldc_set_location -site {V5} [get_ports EXPCON_I08]
ldc_set_location -site {W3} [get_ports EXPCON_I09]
ldc_set_location -site {V4} [get_ports EXPCON_I010]
ldc_set_location -site {V3} [get_ports EXPCON_I011]
```

```
ldc_set_location -site {U5} [get_ports EXPCON_I012]
ldc_set_location -site {W2} [get_ports EXPCON_I013]
ldc_set_location -site {T5} [get_ports EXPCON_I014]
ldc_set_location -site {W1} [get_ports EXPCON_I015]
ldc_set_location -site {T4} [get_ports EXPCON_I016]
ldc_set_location -site {T1} [get_ports EXPCON_I017]
ldc_set_location -site {T2} [get_ports EXPCON_I018]
ldc_set_location -site {T3} [get_ports EXPCON_I019]
ldc_set_location -site {W5} [get_ports EXPCON_I020]
ldc_set_location -site {V1} [get_ports EXPCON_I021]
ldc_set_location -site {U2} [get_ports EXPCON_I022]
ldc_set_location -site {V2} [get_ports EXPCON_I023]
ldc_set_location -site {N2} [get_ports EXPCON_I024]
ldc_set_location -site {R1} [get_ports EXPCON_I025]
ldc_set_location -site {R4} [get_ports EXPCON_I026]
ldc_set_location -site {U1} [get_ports EXPCON_I027]
ldc_set_location -site {N1} [get_ports EXPCON_I028]
ldc_set_location -site {P1} [get_ports EXPCON_I029]
ldc_set_location -site {P3} [get_ports EXPCON_I030]
ldc_set_location -site {P2} [get_ports EXPCON_I031]
ldc_set_location -site {M1} [get_ports EXPCON_I032]
ldc_set_location -site {P4} [get_ports EXPCON_I033]
ldc_set_location -site {M2} [get_ports EXPCON_I034]
ldc_set_location -site {M4} [get_ports EXPCON_I035]
ldc_set_location -site {L2} [get_ports EXPCON_I036]
ldc_set_location -site {R3} [get_ports EXPCON_I037]
ldc_set_location -site {W8} [get_ports EXPCON_I038]
ldc_set_location -site {W9} [get_ports EXPCON_I039]
ldc_set_location -site {L3} [get_ports EXPCON_I040]
ldc_set_location -site {P6} [get_ports EXPCON_I041]
ldc_set_location -site {L4} [get_ports EXPCON_I042]
ldc_set_location -site {R5} [get_ports EXPCON_I043]
ldc_set_location -site {L6} [get_ports EXPCON_I044]
ldc_set_location -site {R6} [get_ports EXPCON_I045]
ldc_set_location -site {P5} [get_ports EXPCON_OSC]
ldc_set_location -site {U6} [get_ports EXPCON_CLKIN]
ldc_set_location -site {L5} [get_ports EXPCON_CLKOUT]
ldc_set_location -site {N6} [get_ports HPE_RESOUT#]
ldc_set_location -site {R2} [get_ports HPE_CARDSEL#]
```

//Aardvark Header Connections

```
ldc_set_location -site {K2} [get_ports AK_SCL]
ldc_set_location -site {K3} [get_ports AK_SDA]
ldc_set_location -site {L1} [get_ports AK_MISO]
ldc_set_location -site {N2} [get_ports AK_SCLK]
ldc_set_location -site {N3} [get_ports AK_SS]
ldc_set_location -site {N4} [get_ports AK_MOSI]
```

//Arduino Header Connections

```
ldc_set_location -site {J4} [get_ports AR_I00]
ldc_set_location -site {G6} [get_ports AR_I01]
ldc_set_location -site {K5} [get_ports AR_I02]
ldc_set_location -site {G7} [get_ports AR_I03]
ldc_set_location -site {J3} [get_ports AR_I04]
ldc_set_location -site {J1} [get_ports AR_I05]
```

```
ldc_set_location -site {H1} [get_ports AR_I06]
ldc_set_location -site {G4} [get_ports AR_I07]
ldc_set_location -site {G5} [get_ports AR_I08]
ldc_set_location -site {F6} [get_ports AR_I09]
ldc_set_location -site {F7} [get_ports AR_SS_I010]
ldc_set_location -site {J7} [get_ports AR_MOSI_I011]
ldc_set_location -site {K7} [get_ports AR_MISO_I012]
ldc_set_location -site {J5} [get_ports AR_SCK_I013]
ldc_set_location -site {K4} [get_ports AR_I014]
ldc_set_location -site {F3} [get_ports AR_SDA]
ldc_set_location -site {G3} [get_ports AR_SCL]
ldc_set_location -site {J8} [get_ports AR_RESET]
ldc_set_location -site {F1} [get_ports AR_AD0]
ldc_set_location -site {F2} [get_ports AR_AD1]
ldc_set_location -site {H3} [get_ports AR_AD2]
ldc_set_location -site {H4} [get_ports AR_AD3]
ldc_set_location -site {G1} [get_ports AR_AD4]
ldc_set_location -site {H7} [get_ports AR_AD5]
```

References

For more information, refer to:

- [Certus-NX Devices web page](#)
- [Certus-NX Family Data Sheet \(FPGA-DS-02078\)](#)
- [Programming Cable User Guide \(FPGA-UG-02042\)](#)
- [Common Programming and Configuration FAQs with Supplementary Concepts for CrossLink-NX, Certus-NX, and CertusPro-NX \(FPGA-AN-02048\)](#)

Revision History

Revision 1.0, January 2026

Section	Change Summary
Introduction	In the Features section, changed t <i>HyperRAM™ up to 800 MBps, ×16 bits</i> to <i>HyperRAM™ up to 800 MBps</i> .
Jumper Definition	In Table 2.1. Jumper Definition : <ul style="list-style-type: none">corrected the jumper group label from <i>JP7, J51, J57</i> to <i>JP7, J51, J52</i>;for the JP7, J51, J52 group, changed Default from <i>JP7 closed, J51 1–2 short, J52 1–2 short</i> to <i>JP7 open, J51 2–3 short J52 2–3 short</i>.
Programming	In the Hard JTAG Download Interface section, removed the following: <i>JP4 for JTAGEN is used to pull down the JTAGEN to disable JTAG port. Using SW3 push button with PROGRAMN reloads the bitstream from the internal Flash when the PROGRAMN_PORT function is enabled by the software.</i>
Headers and Test Connections	In Table 11.13. I2C Connections , changed <i>R35 (DNI)</i> to <i>R35</i> and changed <i>R37 (DNI)</i> to <i>R37</i> .
Appendix A. Certus-NX-65 Development Board Schematics	Updated this section.

Revision 0.80, December 2025

Section	Change Summary
All	Initial Preliminary release.



www.latticesemi.com