Design Advisory

December 2025 **Lattice Confidential** **#FPGA-DA-251201 Rev 1.0**

Fast Corner Timing Analysis Update for Certus-NX, CertusPro-NX, MachXO5-NX, and CrossLink-NX FPGAs

Description

Radiant 2025.2 introduces an adjustment to **Hold Time (Thold) analysis** for **Certus™-NX, CertusPro™-NX, MachXO5™-NX, and CrossLink™-NX FPGAs**.

What changed:
In previous releases, Thold checks at the fast corner (worst case for Thold) use **Vcc(min)**. Starting with Radiant 2025.2, these checks now use **Vcc(max)** at the fast corner.

Why this matters:
This update provides a more accurate representation of device behavior under worst-case conditions, improving timing closure reliability and overall design robustness.

The following documents provide additional information:

- Change in Thold Timing Analysis with the Fast Corner timing model in Certus-NX, CertusPro-NX, MachXO5-NX, and CrossLink-NX FPGAs Knowledge Database Article
- Lattice Radiant Software v2025.2 Release Notes available on www.latticesemi.com

Please note that there are no changes to silicon or timing models for the affected FPGA families.

Products Affected

This advisory applies to all Certus-NX, CertusPro-NX, MachXO5-NX and CrossLink-NX FPGAs.

Recommended Actions

Customers are advised to refer to the Knowledge Database article linked above to determine if additional action would be appropriate for their designs.

For further information or inquiries, please contact your local Lattice Sales representative or Lattice Technical Support.