The Low Power Programmable Leader

Virtual Partner Summit

November 2025

WELCOME PARTNERS!

LATTICE SEMICONDUCTOR

Logistics

Participants are in “listen-only” mode.

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2. Type your question in the text field.
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Agenda

- Welcome Notes, Events & Newsletter
- Lattice Corporate Update
- Silicon, SW, & IP Roadmap Updates
- Focus Applications
  - Edge AI
  - Video/Vision
  - Connectivity
  - Embedded
  - Security/Servers
- Q&A

Partner Network Team

Kambiz Khalilian
Ecosystem Partnerships

Harvey Caponpon
Partner Network Management

Today's Presenters

Esam Elashmawi
Chief Strategy & Marketing Officer

Joel Coplen
Sr. Dir., Product Planning

Karl Wachswender
Sr. Principal System Architect

Mamta Gupta
AVP, Datacenter, Telcom, Security

2025 Calendar of Events

Quarter	Show	Show Dates	Location
Q1'25	CES	January 7–10	Las Vegas, NV
	Automotive World	January 22–24	Tokyo, Japan
	FPGA Forum	February 5–6	Royal Garden Hotel (Trondheim)
	MWC	March 3–6	Barcelona, Spain
	Embedded World	March 11–13	Nuremberg, Germany
	SEFUW – Space FPGA Users Workshop	March 25–27	ESTEC, Noordwijk, Netherlands
Q2'25	Intel Client Ecosystem Symposium	April 23–24	Taipei, Taiwan
	New Tech	May 20–21	Tel Aviv, Israel
	Embedded Vision Summit	May 20–22	Santa Clara, CA
	Computex	May 20–23	Taipei, Taiwan
	HMI Car Europe	June 16–17	Berlin, Germany
	FAIM (Intl Conf on Flexible Automation & Intelligent Manufacturing)	June 21–24	New York City, NY
Q3'25	FPGA Conference Europe	July 1–3	Munich, Germany
	APAC Technical Summit	July 17	Tokyo, Japan
	FPGA World	Sept. 9	Stockholm, Sweden
	Electronica India	Sept. 17–19	Bengaluru, India
Q4'25	FPGA Horizons	Oct. 7	Pullman London St. Pancras, London, UK
	AutoSens	Oct. 7–9	Barcelona, Spain
	OCP Summit	Oct. 13–16	San Jose, CA
	AutoTech Science Fair Expo	Oct. 16	Silicon Valley, CA

Events Highlights

20 events in 2025 with over 100 Partner Participations (Demos & Presentations)

Upcoming Events '25/ '26

Quarter	Show	Show Dates	Location
Q4'25	Auto Tech China	November 20-22, 2025	Guangzhou, China
	SPS Drives	November 25-27, 2025	Nuremberg, Germany
Q1'26	FPGA Forum	February 11-12, 2026	Trondheim, Norway
	Mobile World Congress	March 2-5, 2026	Barcelona, Spain
	Embedded World	March 10-12, 2026	Nuremberg, Germany
Q2'26	Embedded Vision Summit	May 19-21, 2026	Santa Clara, California
	New Tech Expo	May 26-27, 2026	Tel Aviv, Israel
	Computex	June 2-5, 2026	Taipei, Taiwan
	FPGA Conference Europe	June 30 - July 2, 2026	Munich, Germany

Subject to change

Partner with Lattice at Industry Events
Explore opportunities to collaborate with us at upcoming events.
Contact us at partners@latticesemi.com

Partner Network Newsletter

Lattice Semiconductor Partner Network Updates for Q3'25

Welcome New Program Partners!

What's Inside?

- Early Access Program: Lattice MachXO5™-NX (LFMXO5-55TDQ)
- Partner Solutions Update on Broad Market Calls
- EDA & Embedded Partner Types Now Live on the Lattice Website
- Partner Spotlight: intoPIX Accelerates Automotive Innovation With TicoRAW
- Webinar: Unlock the Power of Edge AI for Human-Machine Interfaces
- Webinar: TPMs and FPGAs: A Powerful Combination for System Security
- Recent & Upcoming Lattice Events

Early Access Program

Lattice MachXO5™-NX TDQ (LFMXO5-55TDQ)

The soon-to-be-announced Lattice MachXO5™-NX TDQ devices, built on Lattice's low power Nexus platform, expand the MachXO5-NX FPGA family's capabilities for secure control applications with root-of-trust features supporting state-of-the art classical cryptography and CNSA 2.0 approved Post-Quantum Cryptography (PQC) to address the increased threat to system security. With full suite of CNSA 2.0 prescribed PQC algorithm support, these devices ensure robust protection against emerging quantum threats, future-proofing your security infrastructure.

Not receiving our Partner Network Quarterly newsletter?
To subscribe, contact us at partners@latticesemi.com

LATTICE CORPORATE UPDATE

Esam Elashmawi
Chief Strategy and Marketing Officer

Q3 2025 Earnings Overview & Highlights

REVENUE

$133.3M

7.6% Growth QoQ

GROSS MARGIN

69.5%*

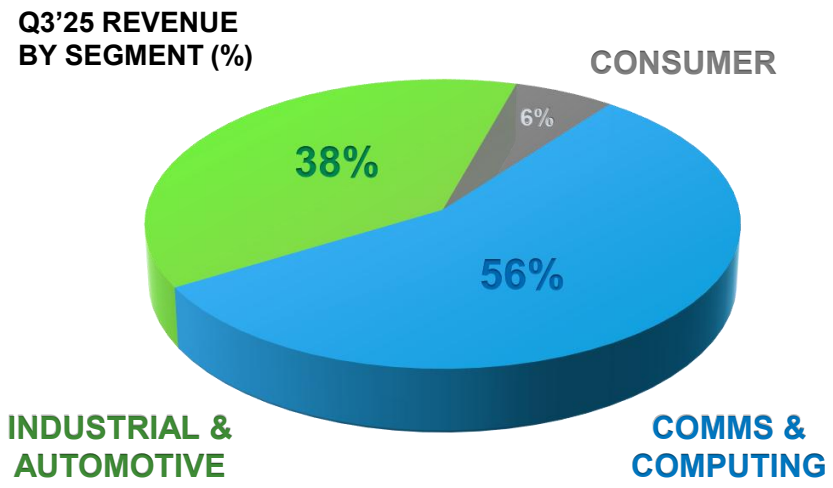
ADJUSTED EBITDA

35.6%*

"We delivered a strong quarter, with broad-based growth across our end markets, and grew non-GAAP earnings 17% quarter over quarter. Our Communications and Computing business achieved record revenue, and we are expecting continued growth into the fourth quarter and beyond. We continue to drive operating leverage and expand profitability, with significant revenue and non-GAAP EPS growth of 13% and 29%, respectively, expected in the second half of 2025."

Ford Tamer, CEO

End Market Overview



Highlights

- Grew Q3'25 revenue, gross margin, and profitability sequentially; Highest sequential revenue growth in more than four years; Guiding both revenue and profitability up in Q4
- Record Communications & Computing segment revenue in Q3, up 21% YoY, with an expanding footprint in general purpose and AI servers
- Percentage of AI usage across products expected to be in the high teens in 2025 and in the mid-20's in 2026
- Launched the Lattice MachXO5™-NX TDQ family, industry's 1st PQC-ready FPGA
- Industrial and Automotive channel inventory normalization remains on track for year-end
- Remain on track to hit goal of high-teens percentage of new product revenue for full year 2025

Non-GAAP based on earnings reported Nov. 3, 2025 | *Adjusted Non-GAAP

Our Mission

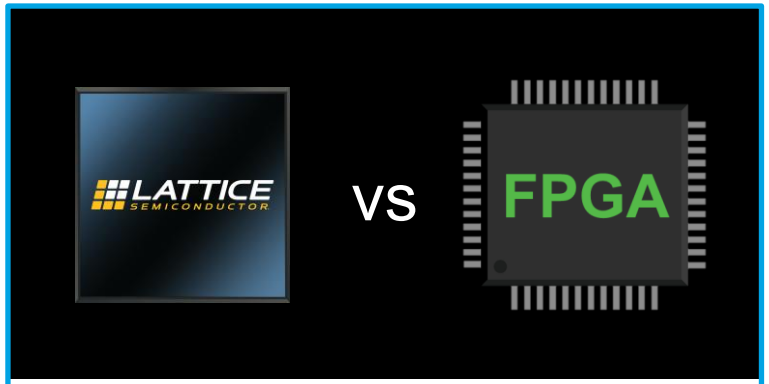
To Be the Low Power Programmable Leader

DIFFERENTIATED
FPGA Platform Optimized for Small and Mid-range

DIVERSIFIED
Across Largest and Fastest Growing Applications

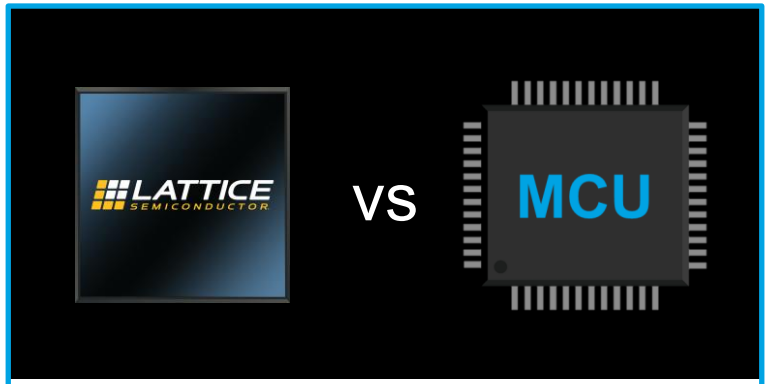
DELIVERING
Faster Than Industry Growth

Differentiated FPGA Platform Optimized for Small and Mid-range



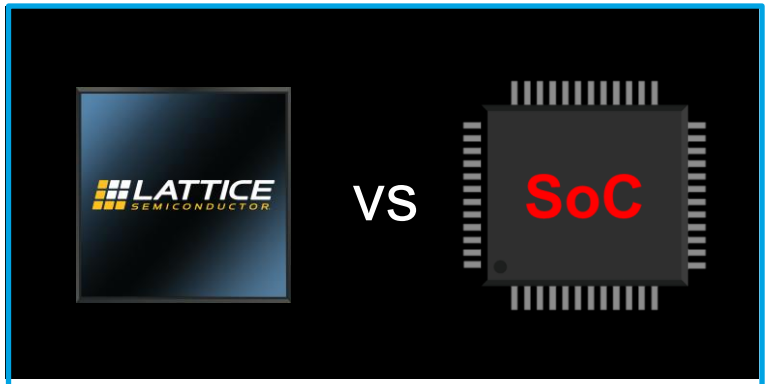
LATTICE BENEFITS

- Lower Power
- Smaller Size
- Better Value
- Faster Boot Time
- Longevity



LATTICE BENEFITS

- Lower Latency
- Deterministic
- Higher Precision
- Faster Performance
- More Connectivity
- Future Proofing



LATTICE BENEFITS

- Partnerships with MPU leaders provide flexible customer solutions
- Marry optimal FPGA with best MPU for application
- Code in C, PyTorch, TensorFlow

Diversified Across Largest and Fastest Growing Applications

COMMS & COMPUTING

Control, Security, and Manageability for AI Platforms

- Multi-generation programmable flexibility for XPU, Switch, NIC, Storage, BMC, ASIC
- Multi-function: boot, security, bridging, I/O expansion, power sequencing, board/rack management

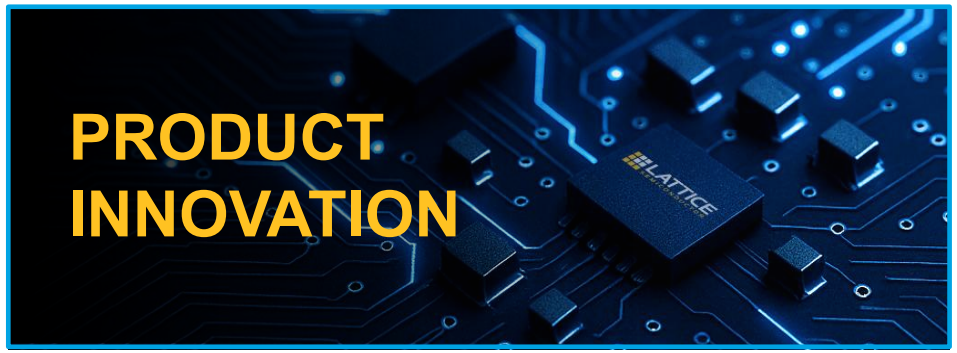
INDUSTRIAL & AUTOMOTIVE

Traditional and Emerging Applications

- Companion chip to vision and motion control, in humanoid, AMR, industrial robots, medical, A&D
- AI “brain” in Far Edge/Physical AI
- Multi-function: HMI, camera/lidar/radar sensor fusion, signal processing, control, communication

Non-GAAP based on earnings reported August 4, 2025 | *Adjusted Non-GAAP

Deliver Faster Than Industry Growth



KEY PRIORITIES

- Expand design wins and production ramps for highest ROI opportunities
- Gain market share in Comms/Compute & Industrial/Auto
- Lead in small FPGA by 2027, and in small/mid FPGA (non-SOC) by 2030
- Deliver faster than industry revenue growth and even faster EPS growth

Value of Our Ecosystem

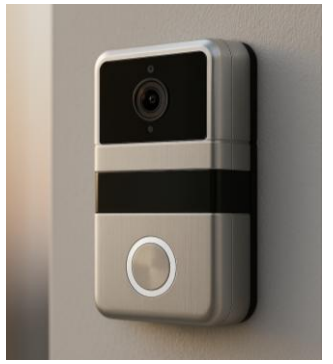
Automotive Lidar

- MIPI CSI-2 aggregation & Bridging
- Data formatting
- Functional safety & control

CITROBITS NewTec CIPHERA

Smart Home Video System

- Complete ISP pipeline for smart home cameras
- Image quality optimization for low-light environments
- NXP i.MX8 H.264 encoding & networking



Helion ENGINEERING VISION NXP OmniVision

5G Integrated Small Cell

- 5G Small Cell PCIe® to JESD204B bridge
- PCIe Gen3x4 Endpoint, JESD204B at 6.144 Gbps x4
- Support interoperability with ADI for JESD204B

ANALOG DEVICES logic fruit Technologies NXP VVDN TECHNOLOGIES

Medical Product

- Converting video from HDMI and DisplayPort sources to USB for high-resolution medical-grade monitors in surgical or diagnostic setups

Parretto SLS System Level Solutions Designing Through Innovation tinyvision.ai

LATTICE SEMICONDUCTOR

THANK YOU, PARTNERS!

Let’s Win Together in 2026 and Beyond!

SILICON, SW, & IP ROADMAP UPDATES

Joel Coplen
Sr. Dir., Product Planning

Lattice Value Proposition

LATTICE SEMICONDUCTOR

The Low Power Programmable Leader

Lattice FPGA Portfolio

PLATFORM	DEVICE FAMILIES

LATTICE AVANT™

Edge-optimized Processing

Cutting-edge General Purpose Processing

Advanced Connectivity

LATTICE NEXUS 2™

LATTICE NEXUS™

Embedded Vision Processing

General Purpose Processing

Next Gen Hardware Security

Advanced General Purpose Processing

Enhanced System Monitor and Control

Advanced System Control

Embedded Vision Processing with USB

Industry 1st PQC-Enabled FPGA

FPGA Platform Leadership

Architected for applications requiring up to 16G SERDES and up to 200k LCs

Architected for applications requiring up to 25G SERDES and up to 500k LCs

LOWER POWER

FASTER PERFORMANCE

SMALLER SIZE

Lattice Nexus Small FPGA Platform

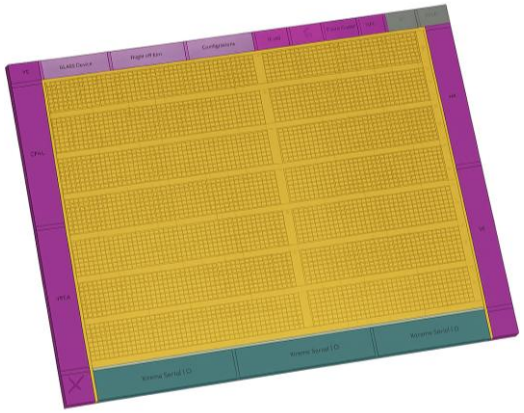
Platform Capabilities

LOWEST POWER
Up to 4X LOWER

HIGHEST PERFORMANCE
Up to 3X FASTER

SMALLEST SIZE
Up to 10X SMALLER

FPGA FABRIC
- Up to 100K LCs
- 20 mS configuration
- SEU Immunity



FAST & FLEXIBLE I/O
- LVCMOS 0.9 to 3.3V
- MIPI D-PHY up to 2.5Gbps
- LVDS up to 1.5Gbps
- DDR 3, LPDDR3/4

SERIAL INTERFACES
- Up to eight 10G SERDES
- 10GbE, PCIe 3.0, DP/eDP
- USB 3.2/2.0

SECURITY AND CONFIGURATION
- Bitstream encryption / authentication
- Hashing algorithms, TRNG, AES

Device Families

Lattice CrossLink™-NX
- Video Connectivity FPGA
- MIPI D-PHY and USB

New Devices Launched in 2025

Lattice Certus™-NX & Lattice CertusPro™-NX
- General Purpose FPGA
- Multi Protocol SERDES

Lattice MachXO5™-NX
- Secure Control FPGA
- Integrated Flash Configuration

Comparisons based on comparable mainstream devices at time of Platform launch
Not all capabilities on all devices

New Lattice Certus™-NX & Lattice MachXO5™-NX Expanded Offering

Lowest Power, Smallest Packages with PCIe & GigE, High I/O Density, 100X Lower SER, and Security

New Devices Released July 2025

- New Lattice MachXO5-NX & Lattice Certus-NX I/O-optimized devices for high-I/O, space constrained applications
- New 0.8mm pitch packages ideal for industrial and comms applications
- Package migration to future-proof designs

Lattice Certus-NX	Product Family		Lattice Certus-NX (Logic Optimized)				Lattice Certus-NX (I/O Optimized)			
	Product Line		LFD2NX-9	LFD2NX-17	LFD2NX-28	LFD2NX-40	LFD2NX-15	LFD2NX-25	LFD2NX-35	LFD2NX-65
	Logic	Logic Cells	9k	17k	28k	39k	15k	25k	35k	65k
	Ball Pitch	Type (Size)	Total (WRIO, HPIO, ADC)/(PCIe Gen2)							
	0.5 mm	121 BGA (6 × 6 mm)	77 (23,48,6)/(0) A	77 (23,48,6)/(0) A	81 (23,58,0)/(1) A	81 (23,58,0)/(1) A				
	0.8 mm	196 BGA (12 × 12 mm)	77 (23,48,6)/(0) A	77 (23,48,6)/(0) A	156 (92,58,6)/(0) A	156 (92,58,6)/(0) A				
		256 BGA (14 × 14 mm)			191 (111,74,6)/(1) A	191 (111,74,6)/(1) A	205 (159,40,6)/(0)	205 (159,40,6)/(0)	181 (145,30,6)/(1)	181 (145,30,6)/(1)
		400 BGA (17 × 17 mm)					311 (257,48,6)/(0)	311 (257,48,6)/(0)	313 (259,48,6)/(0)	313 (259,48,6)/(0)
		484 BGA (19 × 19 mm)							371 (317,48,6)/(1)	371 (317,48,6)/(1)

Lattice MachXO5-NX	Product Family		Lattice MachXO5-NX (I/O Optimized)				Lattice MachXO5-NX (Logic Optimized)		
	Product Line		LFMXO5-15D	LFMXO5-25	LFMXO5-35T	LFMXO5-65TD	LFMXO5-55T	LFMXO5-55TD	LFMXO5-100T
	Logic	Logic Cells	14k	27k	35k	65k	53k	53k	96k
	Ball Pitch	Type (Size)	Total (WRIO, HPIO, ADC)/(PCIe Gen2)						
	0.8 mm	196 BGA (12 × 12 mm)							
		256 BGA (14 × 14 mm)	205 (159,40,6)/(0)	205 (159,40,6)/(0)	195 (159,30,6)/(1)	195 (159,30,6)/(1)			
		400 BGA (17 × 17 mm)	305 (251,48,6)/(0)	305 (251,48,6)/(0)	336 (282,48,6)/(0)	336 (282,48,6)/(0)	297 (159,132,6)/(1+1)	297 (160,132,6)/(1+1)	297 (159,132,6)/(1+1)
		484 BGA (19 × 19 mm)			366 (330,30,6)/(1)	366 (330,30,6)/(1)			

Lattice MachXO5™-NX Secure FPGAs

Root of Trust Control FPGA

Q4 2024

Lattice MachXO5D™-NX

Industry 1st RoT FPGA with Post-Quantum Cryptography

Lattice MachXO5-NX 55 TDQ
(Logic Optimized)

Q4 2025

PQC-enabled FPGA Family Expansion

Lattice MachXO5-NX 20/30 TDQ
(I/O Optimized)

More I/O, Density, Security Feature Options Coming 2026/2027

Empowering Customers to Oversee and Safeguard Computing, Communication, and Industrial Systems

Lattice MachXO5™-NX TD/TDQ – Key Security Enhancements

More I/O, Density, Security Feature Options Coming 2026/2027

Security Features	LFMXO5-25/55T/100T	LFMXO5-15D/20TD/30TD	LFMXO5-55TD	LFMXO5-20/30TDQ	LFMXO5-55TDQ
Config/Program Port Lock	Yes	Yes	Yes	Yes	Yes
Flash Asset Lock	No	Yes	Yes	Yes	Yes
Bitstream Security	Yes	Yes	Yes	Yes	Yes
User Security	Yes	Yes	Yes	Yes	Yes
TRNG	Yes	Yes	Yes	Yes	Yes
AES-256	CBC	CBC	CBC, GCM	CBC	CBC, GCM
HMAC/SHA	256-bit	384-bit	512-bit	384-bit	512-bit
ECC	No	384-bit	521-bit	384-bit	384-bit
RSA	No	No	Up to 4K	No	No
XMSS, LMS	No	No	No	Yes	Yes
ML-DSA, ML-KEM	No	No	No	No	Yes
Golden/backup, Ping-pong	Yes	Yes	Yes	Yes	Yes
Version Rollback Protection	No	Yes	Yes	Yes	Yes
Pub & Priv Key Pair Gen	No	Yes	Yes	Yes	Yes
Key Mgmt & Revocation	No	Yes	Yes	Yes	Yes
Typical Application	Non-RoT Control	RoT Control	RoT Control & PFR	RoT Control	RoT Control & PFR

Lattice Avant™ Mid-Range FPGA Platform

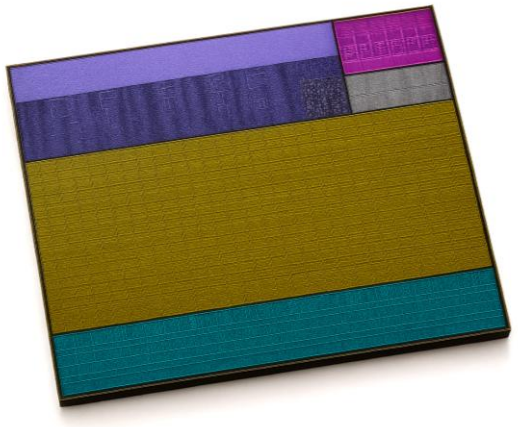
Platform Capabilities

LOWEST POWER
Up to 2.5X
LOWER

HIGHEST PERFORMANCE
Up to 2.5X
FASTER

SMALLEST SIZE
Up to 6X
SMALLER

FPGA FABRIC
- Up to 700K SLCs



FAST & FLEXIBLE I/O
- LVCMOS 0.9 to 3.3V
- MIPI D-PHY up to 1.8Gbps
- LVDS up to 1.5Gbps
- DDR4, LPDDR4, DDR5

SERIAL INTERFACES
- Up to twenty-eight 25G SERDES
- Hardened PCIe 4.0, 25G Ethernet, DP/eDP, JESD204B/C

SECURITY AND CONFIGURATION
- ECC521 authentication & AES-GCM encryption
- SHA3-512 PQC ready
- Anti-tamper and PUF
- User security

Device Families

Launched Dec. 2022

Lattice Avant™-E
- LPDDR4
- Bitstream encryption & authentication

Launched Dec. 2023

Lattice Avant™-G
- Lattice Avant-E plus
- 12.5 Gbps SERDES

Lattice Avant™-X
- Lattice Avant-G Plus
- 25 Gbps SERDES, DDR5 & user security

Rollout Continues

Comparisons based on comparable mainstream devices at time of Platform launch
Not all capabilities on all devices

Lattice Nexus 2 Small FPGA Platform

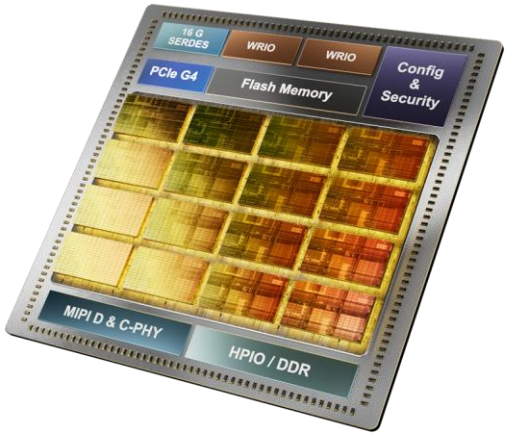
Platform Capabilities

LOWEST POWER
Up to
3X LOWER

HIGHEST PERFORMANCE
Up to
3X FASTER

SMALLEST SIZE
Up to
5X SMALLER

FPGA FABRIC
- Up to 220K SLCs
- 20 mS configuration
- SED / SEC



SERIAL INTERFACES
- Up to eight 16G SERDES
- 10GbE, PCIe 4.0, DP/eDP

SECURITY AND CONFIGURATION
- Bitstream encryption / authentication
- Hashing algorithms, TRNG, AES

FAST & FLEXIBLE I/O
- LVCMOS 0.9 to 3.3V
- MIPI D-PHY up to 2.5Gbps
- LVDS up to 1.5Gbps
- DDR4, LPDDR4
- 4.5Gbps MIPI D-PHY & 7.98Gbps C-PHY

Device Families

Launched Dec. 2024

Lattice Certus™-N2
- General Purpose FPGA
- Multi-protocol SERDES

Under Development

Lattice CrossLink™-N2
- Video Connectivity FPGA
- MIPI D-PHY and USB

Lattice Mach™-N2
- Secure Control FPGA
- Integrated Flash Configuration

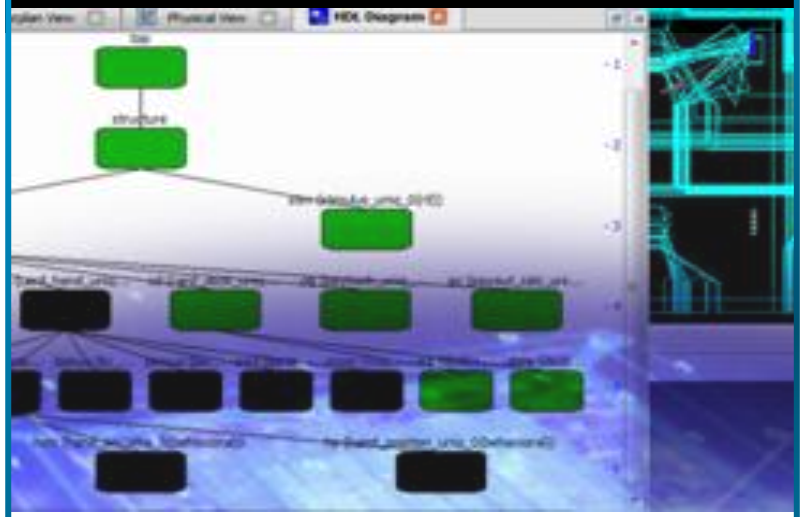
Comparisons based on comparable mainstream devices at time of Platform launch
Not all capabilities on all devices

Lattice MachXO4™: Next Generation of Lattice Mach FPGAs

- Up to 4X lower static power
- Up to 36% more I/O per package area
- Most secure control FPGA in its class
  - On-chip dual-boot
  - Bitstream security (encryption + authentication)
- Resilient supply chain and reliable production support for 20+ years
- Access simplified design with Lattice Radiant® tool and the latest software solution stacks

Easy-to-use Software

LATTICE DIAMOND™ DESIGN SOFTWARE



Powerful FPGA Design & Verification Environment

Easy Design Exploration

Easy to Use Powerful Tools

Optimized for Lattice Devices

Pre-Nexus Tool
1 Release Per Year

LATTICE RADIANT™ DESIGN SOFTWARE

Best-in-class, Easy-to-use Design Software

Simplified Flow for Faster Design

Increase Re-use with IP Tools

Leading Synthesis & Simulation

LATTICE PROPEL™

Complete Toolset for Embedded System Design

IP System Integration Environment

Software Development Kit & Libraries

Build, Compile, Analyze, Debug

Focus Tools
2 Release Per Year

Lattice Tools Roadmap

		2025	2026*	2027*
QoR	**Lattice Avant**	Lattice Avant Design Optimization Guide	LSE QoR improvement +FMAX Improvement Timing Closure Recommendation Tool	+FMAX Improvement Compile Time Improvement
	Lattice Nexus	New Lattice Nexus Analytic Placement Engine +FMAX improvement	+FMAX Improvement Compile Time Improvement	
Debug		SERDES Debug – BERT External Memory Controller Debug Incremental Post-PAR Debug	Reveal Ease of Use Remote Debug	Reveal Ease of Use
IP Flows		Execute Program from External Flash – Flash XIP mode Project Templates for Low-Power and Multi-Processor Designs	Mathworks Custom IP Flow	Mathworks Optimized Libraries Mathworks Hardware in the Loop Simulation Flow Tighter Propel Integration with Radiant
Ease of Use		Report Files Upgrade	Timing Analysis Reporting Radiant Messages Usability Expanded Tcl commands capability	Fully Scripted Interactive Design Flow Advanced Floorplanning
Power		Power Optimization – Dynamic Clock Gating for Nexus & Avant	Power Optimization via Area Reduction for Avant Simplified IP Flow for Estimation Mode (PLL, DDR, I/O)	Simplified

* Roadmap is subject to change

Soft IP Overview

Primary focus on horizontal IP categories

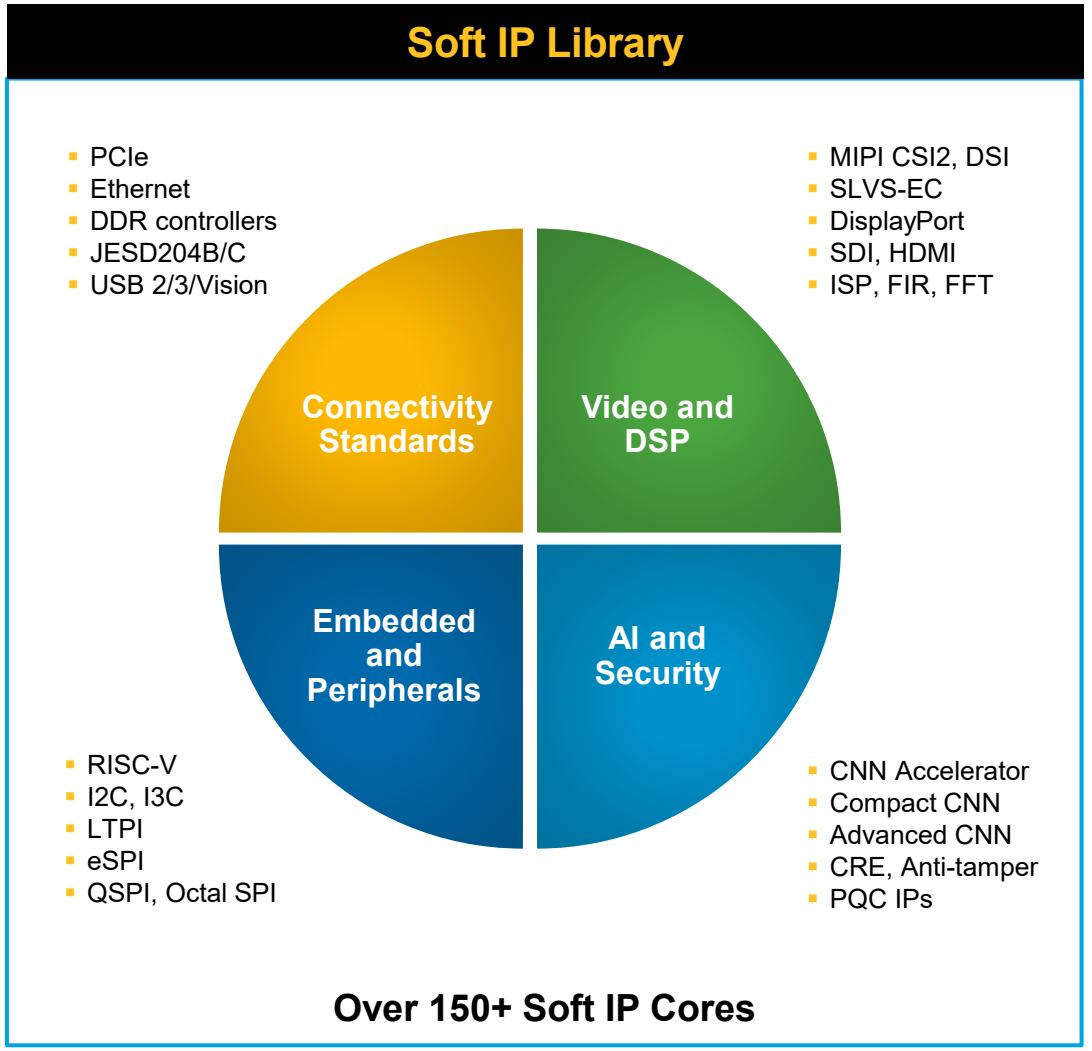
- PCIe, Ethernet, DDR, MIPI, security, peripherals
- Quality, features, drivers, & MPPHY

Reference designs to accelerate TTM

- Modular RDs with seamless IP interconnect
- Soft RISC-V GSRD and connectivity focus

Partner eco-system for application specific IPs

- Video: SLVS-EC, HDMI, SDI, CoaXPress, SMPTE, IPMX, ISP, VIP, CV
- Industrial/Comm: JESD204B/C, MACSEC, PTP/TSN, Aurora, CAN, eCPRI



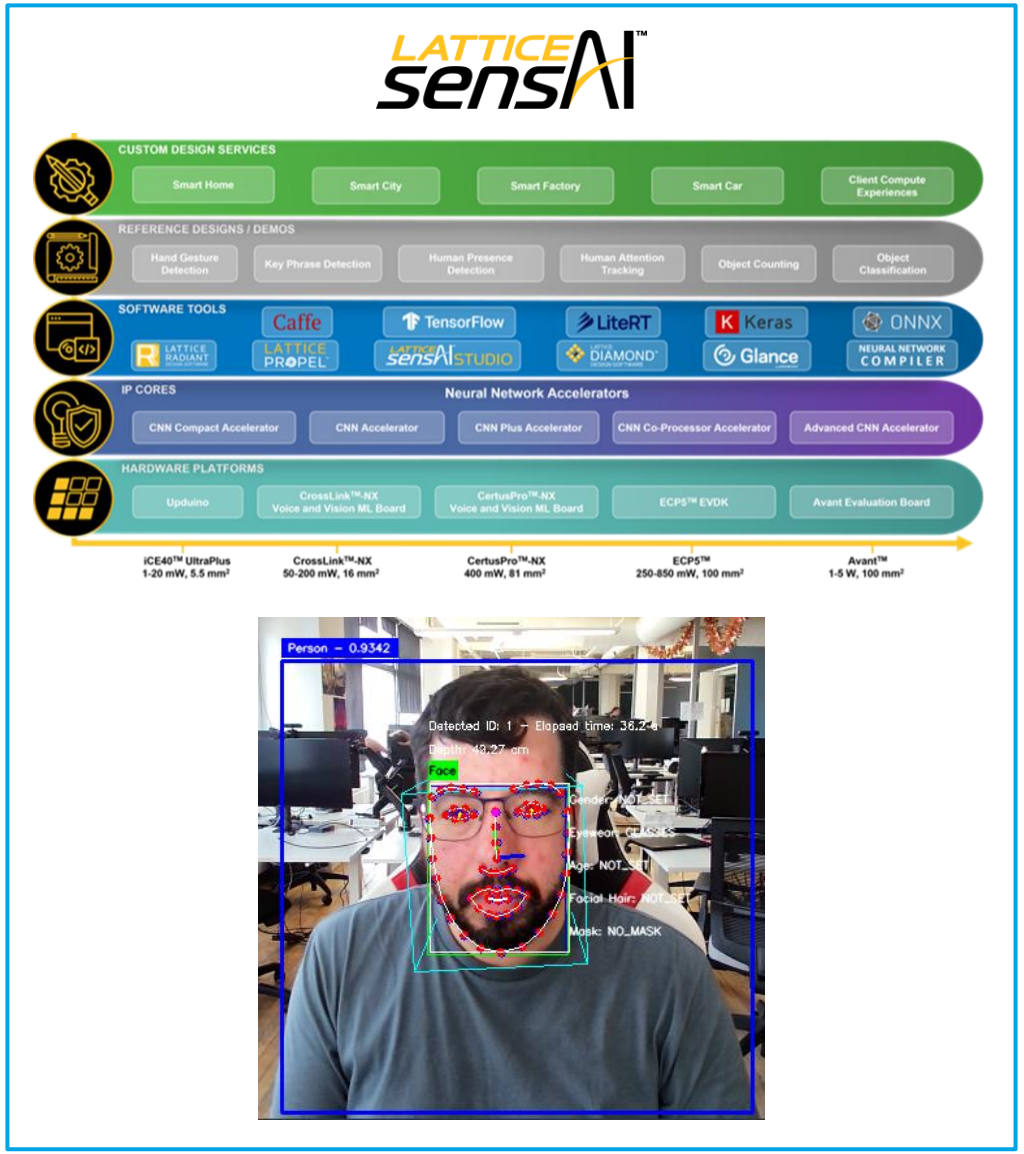
Contact Lattice for joint promotion of partner IPs based on Nexus and Avant

EDGE AI, VIDEO/VISION, CONNECTIVITY & EMBEDDED

Karl Wachswender
Sr. Principal System Architect

Focus Application: Far Edge AI Sensor Processing

- **Edge AI Challenges**
  - Processing at the edge requires low power specialized acceleration
  - Building a POC has become simpler, building production use case is complex
  - Limited AI skill, tool expertise, and inadequate dataset
- **Our Offerings**
  - Lattice FPGAs connect wide range of sensors with on device AI inferencing
  - Pretrained and purpose-built models offering quick time to market
  - Tools for model training and tuning, programable and future-proof acceleration
- **What Sets Us Apart**
  - Optimized and accurate application specific AI Models
  - Millions of units deployed globally in various conditions
  - Low power and deterministic latency FPGAs
- **Example Use cases**
  - Factory Automation: Industrial machine vision, defect detection, and HMI
  - Automotive: Internal and external monitoring, CMS, DMS, EMS, OMS
  - Smart City: Traffic monitoring and analysis



Success Story

BACKGROUND

Application	Industrial HMI
Lattice Device	LFCPNX-100
Socket Function	Operator Compliance HMI Solution
Customer Requirements	Standalone always on vision sensor with USB interface, processing and providing data on operator status

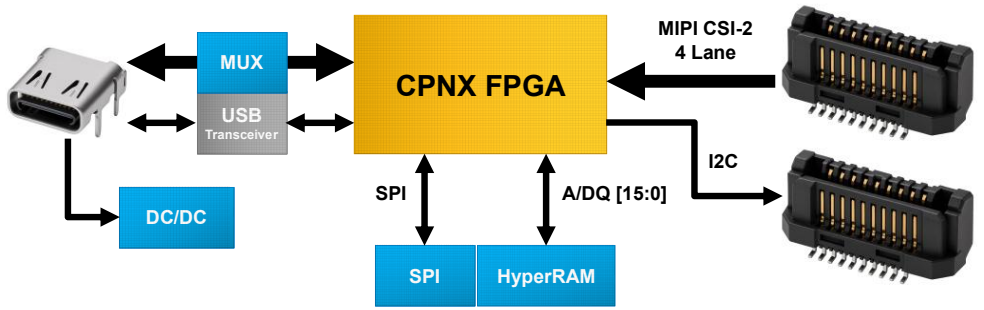
HOW LATTICE WON

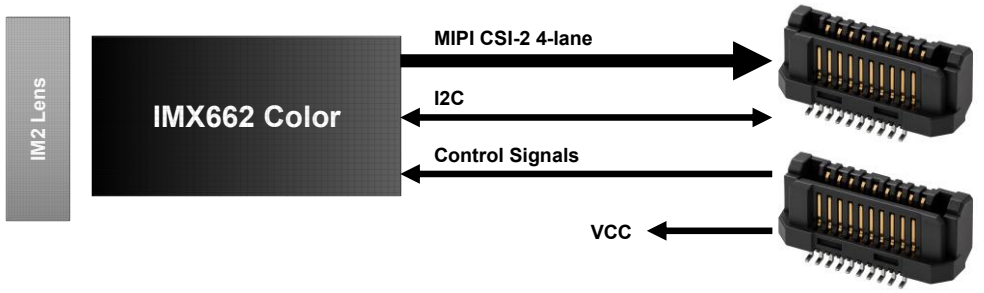
Lattice Advantages	▪ Pretrained models ▪ High accuracy ▪ Off the shelf hardware
Actions Taken to Win	▪ Demonstrated leadership in small models for HMI ▪ Easy to use demo for use case validation ▪ Partner provided camera hardware ▪ Developed additional models for the customer

CALL TO ACTION:

- Build cameras HW for target applications such as industrial machine vision and automotive
- Leverage HMI, multi object and defect detection purpose built and pretrained models
- Port your own models into Lattice FPGAs
- Download Lattice sensAI™ 8.0 (launching in Dec. '25) to build new edge AI use cases

BLOCK DIAGRAM

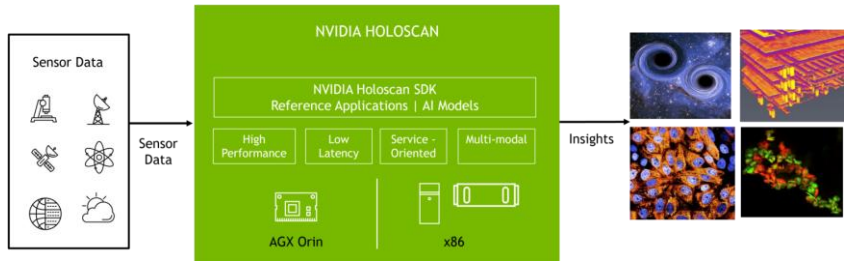




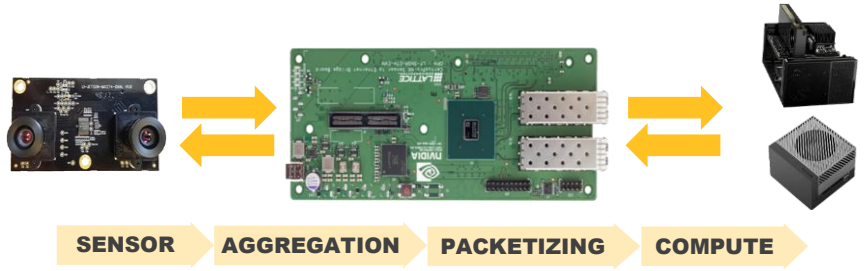
Focus Application Sensor-bridge & Pre-processing

- **Edge AI: NVIDIA Holoscan**
  - Hardware & software platform for creating real-time, AI-powered applications for sensor processing, especially at the edge
  - Designed to handle data streams from sensors like cameras and lidar, using optimized libraries and microservices for low-latency processing
  - Application areas: medical imaging, robotics, media production
- **Lattice FPGA Holoscan Sensor Bridge (HSB)**
  - FPGA based development kit for sensor to Ethernet bridging
    - Sensor aggregation, preprocessing, packetization
  - Low latency, low power, extremely flexible & scalable
  - Starting point : Holoscan Sensor Bridge Reference Design
- **Holoscan Bridge Board Ecosystem**
  - NVIDIA/Lattice ecosystem partners: sensor modules, derivative HSB boards, interface & adapter cards, FPGA IP, Design services
  - Dozens of customers – many need HW/SW design support

NVDIA Holoscan for HPC Workflow



Sensor Bridge Kit



Growing Lattice HSB Ecosystem Partnerships

ADVANTECH · D3 Embedded · e-con Systems (Think Camera. Think e-con.) · LEOPARD IMAGING · LIPS · PhotonLogic · RidgeRun · SENSING 森云智能 · TAURO TECHNOLOGIES · YUAN

Success Story

BACKGROUND

Application	Humanoid Robotics
Lattice Device	▪ LFCPNX-100-9LFG672IAQT ▪ LFCPNX-100-9CBG256IAQT ▪ LIFCL-40-9MG121I
Socket Function	Holoscan Sensor Bridge (HSB)
Customer Requirements	Small, low power, low latency bridge between sensors and NVIDIA Jetson Thor™ via HSB

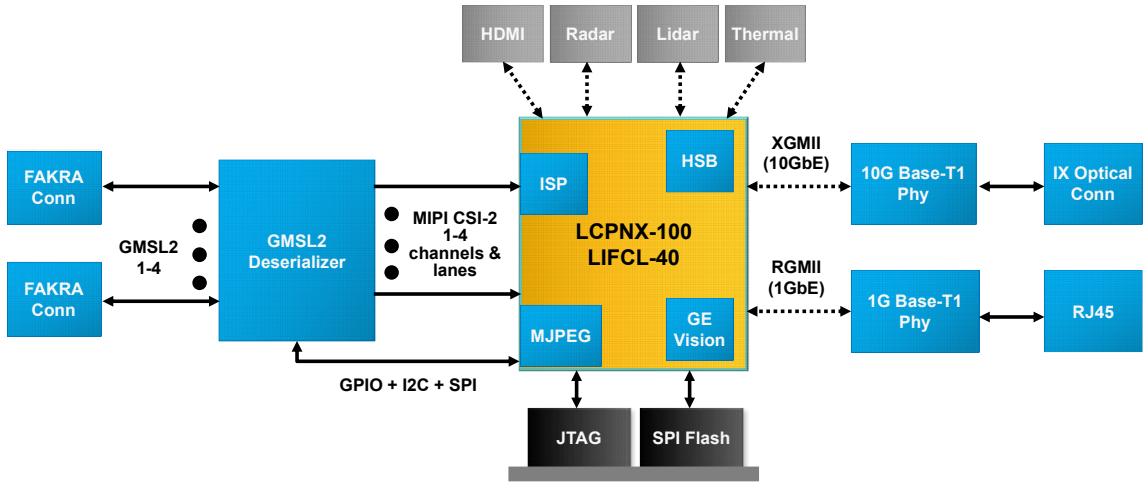
HOW LATTICE WON

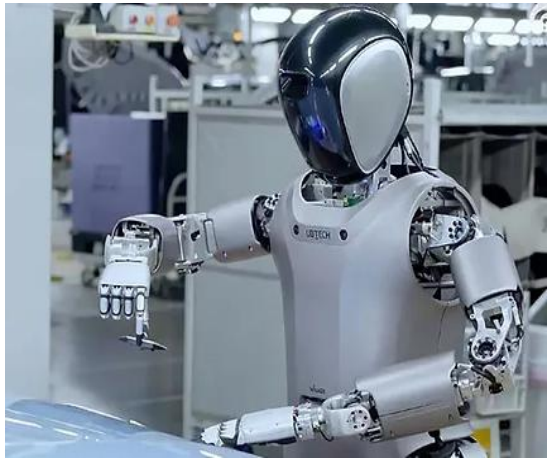
Lattice Advantages	▪ HSB Leader ▪ Low power & small FF leadership ▪ MIPI, HDMI, JPEG, GigE vision, & ISP IP ▪ Outstanding technical, sales and marketing support
Actions Taken to Win	▪ Demonstrate HSB leadership ▪ Close collaboration with NVIDIA, customer, and design service & IP partners ▪ Weekly sync meetings ▪ Engage vertical apps team ▪ Executive alignment

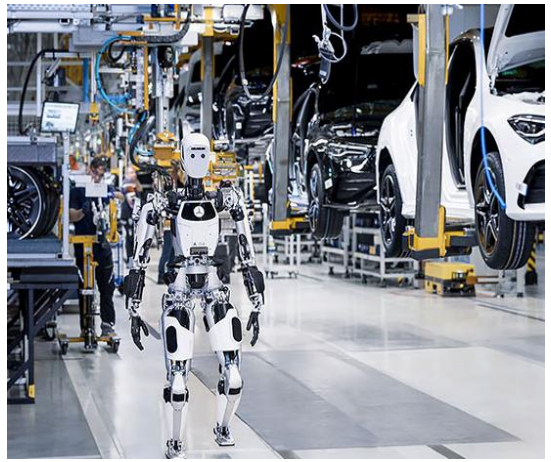
CALL TO ACTION:

- Leverage Lattice Holoscan reference design; explore new business opportunities
- Provide engineering services around Lattice HSB Solution (sensor boards, derivative/custom boards, adapter boards, FPGA IP, …)

BLOCK DIAGRAM





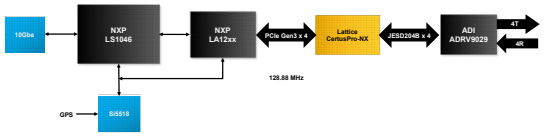


Focus Application Real Time Ethernet

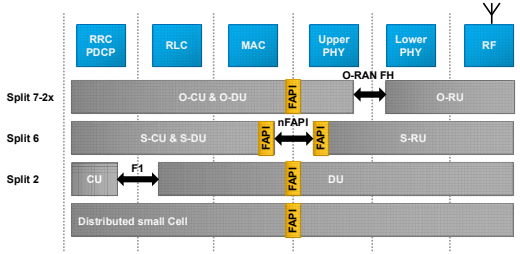
- **Connectivity and Bridging**
  - Support industrial Ethernet protocols with low power up to FPGA families IP
  - Enable analog front end or bridge analog part to standard interfaces like PCIe like JESD204
  - Application areas: motor control, robotic and SDN, T&M
- **Lattice FPGA IP offering**
  - FPGA based EtherCat® IP from Beckhoff
    - Ref design on Analog Device/Arrow/Lattice MCB Q1/2026
  - Low latency, low power, extremely flexible & scalable
  - NXP partnership small cell for PCIe to JESD204
- **Ecosystem**
  - Supplier ecosystem partners: motor control boards, interface & adapter cards, FPGA IP, design services and protocol stack

BLOCK DIAGRAM

Option 2-Based Outdoor Private Network



ORAN Split Design (4T4R NXP/ADI) – All-in-One Box



Ecosystem Partnerships

ANALOG DEVICES · ARROW · EtherCAT · BECKHOFF · NXP · RT-LABS

Success Story

BACKGROUND

Application:	Industrial PLC
Lattice Device:	Lattice MachXO5™-NX 35/65
Socket Function:	EtherCAT Real-Time Networking
Customer Requirements:	Small, low power, low latency, flash-based FPGA

HOW LATTICE WON

Lattice Advantages:	▪ Industrial FLSH-based FPGA Leader ▪ Low power & small FF leadership ▪ Partnership with RT-Labs ▪ Outstanding technical, sales and marketing support
Actions Taken to Win:	▪ Demonstrate EtherCat® ▪ Close collaboration with RT-Labs ▪ Design service in house SSAE team (engage vertical apps team) ▪ Executive alignment

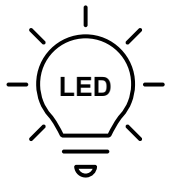
CALL TO ACTION:

- Leverage Lattice EtherCat reference design; explore new business opportunities
- Provide engineering services around industrial Ethernet (partnership with ADI and RT-Labs)

Motor Control – EtherCAT Reference Design ADI-MCB (LFCPNX-100) GSRD Based

EtherCAT®

PoC – Demonstration of Basic Functionality:
1. Basic parameters are hard-coded (LED toggling)
2. Integrated into ADI-MCB GSRD-based system
3. Basic integration Test Suite (TBD) with GSRD



RD – Testable Baseline:
1. Configurable Parameters for Motor Application
2. Functional Test Suite for EtherCAT (TBD) w/GSRD
3. Functional Test Suite for PROFINET (TBD) w/GSRD
4. U-Phy Stack basic operation and setup w/GSRD
5. Motor Control control basic BLDC test w/GSRD

Motor Control
EnDat 2.2
BLDC

Stack – Developmental Baseline:
1. Performance benchmarking data w/GSRD
2. Fully Functional Test Suite (TBD) w/GSRD
3. Fully Functional U-Phy Stack with EtherCAT and PROFINET w/GSRD
4. Integrate Motion Control basic BLDC test w/GSRD
5. Integrate Motion Control basic FoC test w/GSRD

Motor Control
EnDat 2.2
BLDC FOC

Focus Application GSRD/GHRD

- **Soft SoC Design for Embedded Systems**
  - Soft SoC for Lattice Nexus and Lattice Avant with MB with FreeRTOS, Zephyr Linux support
  - eBOOT enabled Soft SOC ref design
  - Application areas: SMART sensor, RT-Ethernet motor control, robotic
- **Lattice FPGA Offering**
  - Ref. Design for C2NX, CPNX, and Lattice Avant-E devices
    - Version 3.0 released October 31st
  - Low latency, low power, extremely flexible & scalable
  - Soft SoC design used in motor control and EtherCat demo
- **Ecosystem**
  - Supplier ecosystem partners: motor control boards, interface & adapter cards, FPGA IP, design services and protocol stack

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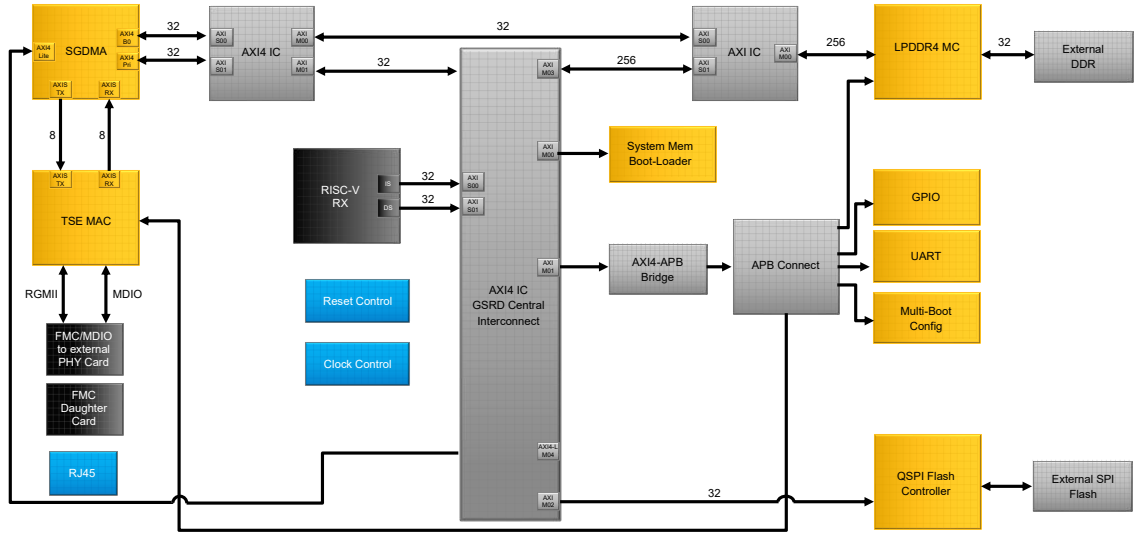

Ecosystem Partnerships

ANALOG DEVICES · ARROW · ASHLING · BECKHOFF · bluespec · EtherCAT · MOSCHIP · NXP · RT-LABS

Lattice CrossLinkU™-NX USB3 Vision Reference Design

BACKGROUND

Application:	Industrial Camera
Lattice Device:	CLNX-33U
Socket Function:	USB3 Vision with Zephyr OS
Customer Requirements:	Small, low power, low latency, flash-based FPGA

HOW LATTICE WON

Lattice Advantages:	▪ Single chip solution ▪ Low power & small FF leadership ▪ Partnership with SLS ▪ Outstanding technical, sales and marketing support
Actions Taken to Win:	▪ Demonstrate USB3 vision on single chip ▪ Close collaboration with SLS ▪ Design service in house SSAE team (engage vertical apps team) ▪ Executive alignment

CALL TO ACTION:

- Leverage Lattice U3V/GSRD deference design; explore new business opportunities
- Provide engineering services around industrial SoftSOC (Partnership with SLS, Bluespec or Moschip)

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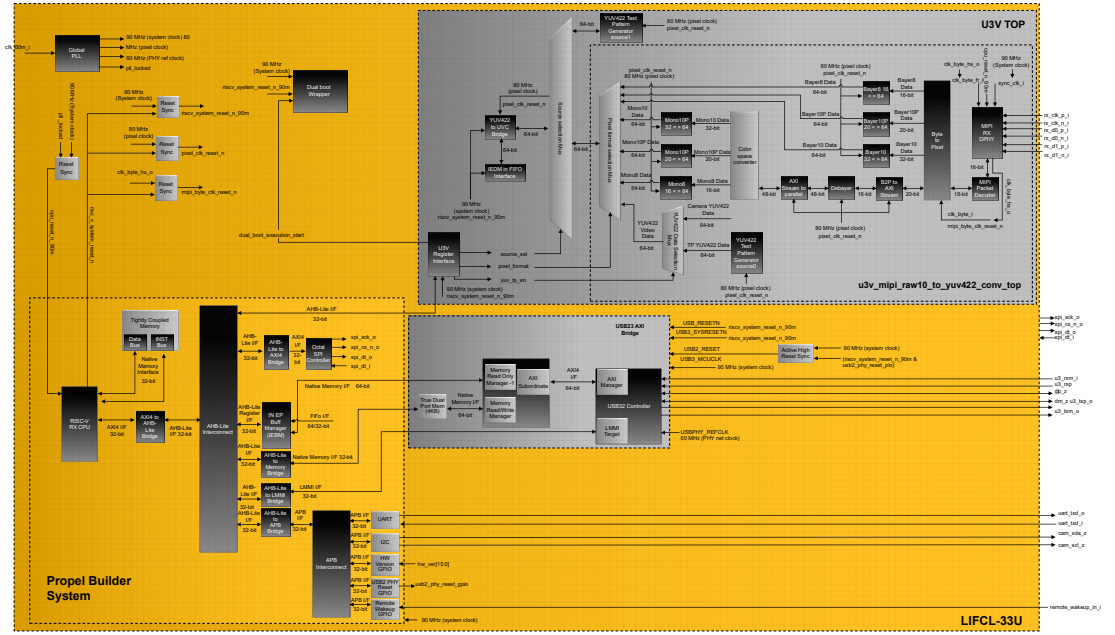


Ecosystem Partnerships

bluespec https://info.bluespec.com/latticefpga Linux

MOSCHIP® https://moschip.com/semiconductor/getting-started-with-risc-v-and-its-architecture/

LATTICE SEMICONDUCTOR

SECURITY/SERVERS

Mamta Gupta
AVP, Datacenter, Telcom, Security

Urgent Need for Post-Quantum Crypto for Future Proof Security

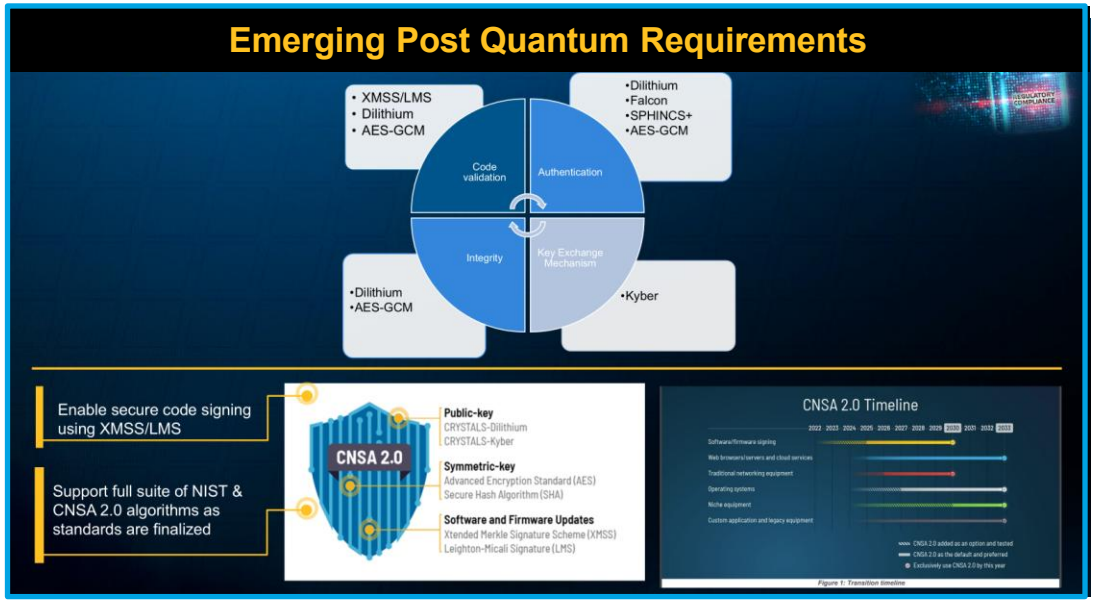
Rising Threats to Digital Trust

- Nation-state actors and sophisticated cybercriminals are targeting critical systems
- IoT, datacenter, and edge devices are proliferating—each a new attack surface
- Quantum computers are evolving, threatening today's encryption
- Classical cryptography is no longer future-proof

What's Forcing the Shift – The Impetus for Post-Quantum Crypto

- Harvest Now, Decrypt Later (HNDL): Attackers are storing encrypted data today to decrypt once quantum computers are viable
- Regulatory Pressure: CNSA 2.0, NIST, EU ENISA, and ETSI
- Ecosystem Shift: Software and cloud vendors are transitioning to PQC

Emerging Post Quantum Requirements



Lattice Offers Industry First Post-Quantum Safe FPGA: Lattice MachXO5™-NX TDQ

- Full CNSA 2.0 Compliant PQC Algorithms
- Advanced Cryptography with Crypto Agility
- Hardware Root of Trust
- Secure Bitstream Key Management

Ecosystem Partnerships

ami · PQ SHIELD · Quside · SECURE-IC THE SECURITY SCIENCE COMPANY

Extensible Crypto Functions

- Crypto-Agile block supports classical (ECC 384 and above) and Post-Quantum Crypto (LMS/ XMSS, ML-KEM, ML DSA)
- NIST and CNSA 2.0 approved algorithms
- Verifiable quantum entropy solutions

- Integrated flash
- External-boot via SPI interface
  - Support for classical and PQC algorithms

Key Applications

- PQC and hybrid secure boot
- PQC enabled PFR in datacenter
- Verifiable entropy with QRNG
- Telecommunications
- Industrial

Call To Action

- Accelerate innovation by co-developing reference designs, differentiated applications and solutions leveraging Lattice's PQC FPGAs
- Engage in joint go-to-market activities, technical workshops, and customer success stories to showcase our joint PQC leadership
- Represent together in industry consortia and standards bodies to advocate for quantum safe security

THANK YOU PARTNERS!

Let’s Win Together in 2026 and Beyond!

LATTICE SEMICONDUCTOR

The Low Power Programmable Leader