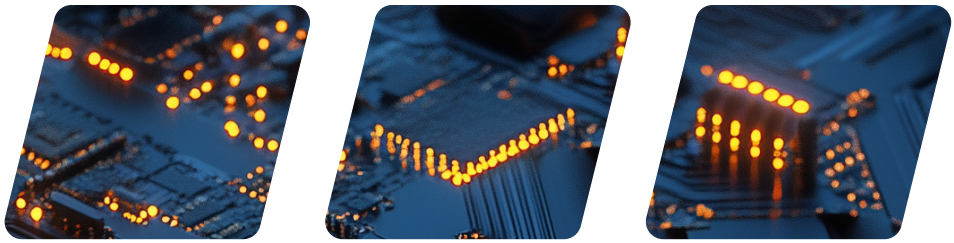
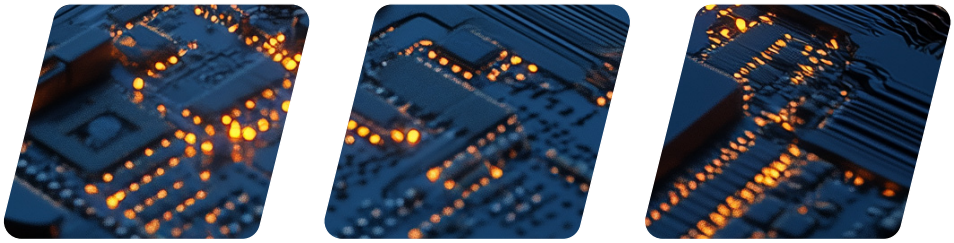


Advantages of Using Lattice FPGAs for Field-Oriented Control of Brushless Three-Phase Motors



White Paper

Author:
Michael Weitzel, Senior Staff Applications Engineer, Lattice Semiconductor
Ivan Teh, Director for Solutions Engineering, Lattice Semiconductor
Karl Wachswender, Senior Principal System Architect, Lattice Semiconductor

DISCLAIMERS

Lattice makes no warranty, representation, or guarantee regarding the accuracy of information contained in this document or the suitability of its products for any particular purpose. All information herein is provided AS IS, with all faults, and all associated risk is the responsibility entirely of the Buyer. The information provided herein is for informational purposes only and may contain technical inaccuracies or omissions, and may be otherwise rendered inaccurate for many reasons, and Lattice assumes no obligation to update or otherwise correct or revise this information. Products sold by Lattice have been subject to limited testing and it is the Buyer's responsibility to independently determine the suitability of any products and to test and verify the same. Lattice products and services are not designed, manufactured, or tested for use in life or safety critical systems, hazardous environments, or any other environments requiring fail-safe performance, including any application in which the failure of the product or service could lead to death, personal injury, severe property damage or environmental harm (collectively, "high-risk uses"). Further, buyer must take prudent steps to protect against product and service failures, including providing appropriate redundancies, fail-safe features, and/or shut-down mechanisms. Lattice expressly disclaims any express or implied warranty of fitness of the products or services for high-risk uses. The information provided in this document is proprietary to Lattice Semiconductor, and Lattice reserves the right to make any changes to the information in this document or to any products at any time without notice.

INCLUSIVE LANGUAGE

This document was created consistent with Lattice Semiconductor's inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice's inclusive language FAQ 6878 for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

ABSTRACT

This white paper explores the benefits of using Lattice FPGAs for implementing Field-Oriented Control (FOC) in brushless three-phase motor applications. FOC enables precise torque and speed control by transforming motor currents into a rotating reference frame. Traditionally handled by MCUs or DSPs, FPGAs offer superior performance through parallel processing, low latency, and deterministic timing. Lattice FPGAs provide advantages in real-time execution, scalability, system integration, and reliability, making them ideal for compact, power-efficient motor control systems. The paper presents two example designs showcasing small-form-factor motor drivers using Lattice Certus™-NX FPGAs, detailing component selection, PCB layout, and communication interfaces. These designs demonstrate how Lattice FPGAs can meet the demands of modern motor control applications in robotics, industrial automation, and beyond.

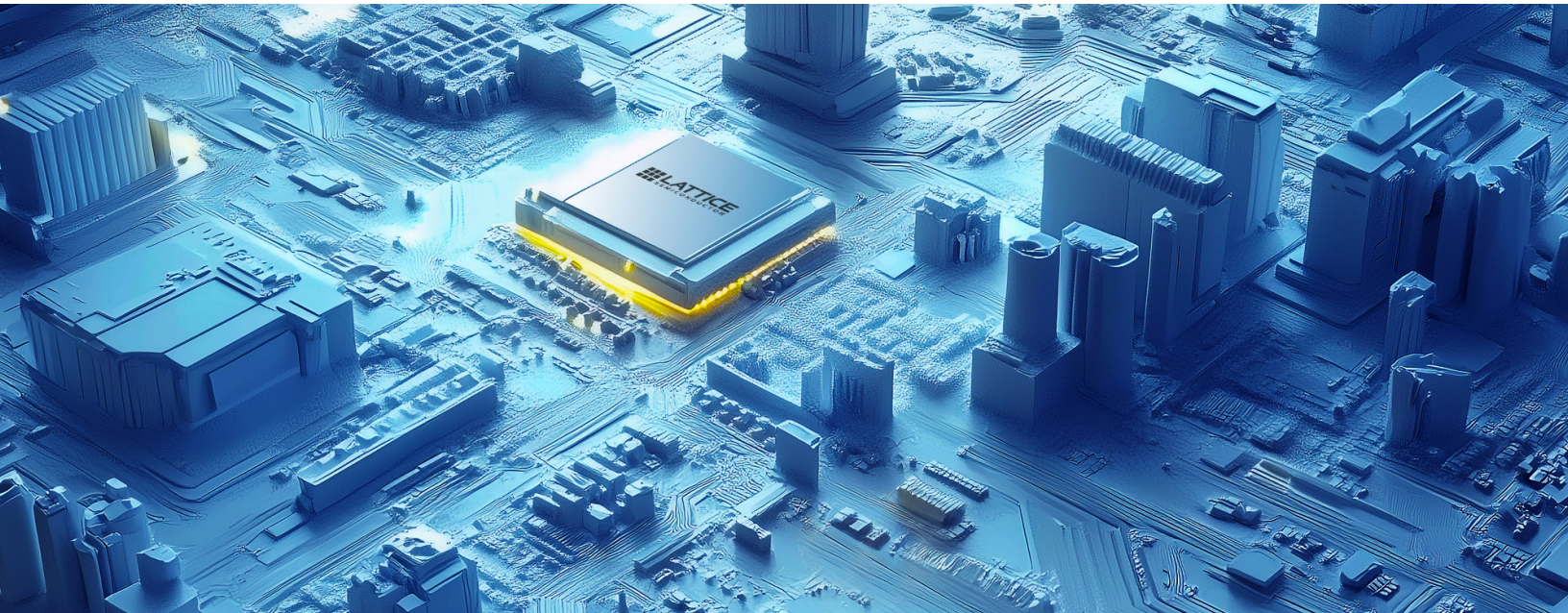


TABLE OF CONTENTS

Introduction

Brushless three-phase motors are widely used in industrial automation, robotics, electric vehicles, and aerospace due to their high efficiency, reliability, and power density. To fully exploit their performance potential, advanced control techniques like FOC are employed. FOC enables precise torque and speed regulation by decoupling stator current into orthogonal components aligned with the rotor's magnetic field.

Traditionally, FOC has been implemented using microcontrollers (MCUs) or digital signal processors (DSPs). However, Field Programmable Gate Arrays (FPGAs) are offering significant advantages in speed, flexibility, and scalability.

Overview of Field-Oriented Control

FOC transforms three-phase motor currents into a rotating reference frame using Clarke and Park transformations. This allows independent control of torque and flux, akin to DC motor behavior. The control loop typically includes:

- Current control (inner loop)
- Speed control (outer loop)
- Position sensing (via encoders or resolvers)
- Pulse Width Modulation (PWM) generation for inverter switching

These operations require high-speed computation, low latency, and deterministic timing - areas where Lattice FPGAs excel.

FPGA Architecture and Capabilities

Lattice FPGAs are reconfigurable silicon devices composed of logic blocks, DSP slices, memory elements, and I/O interfaces. Unlike sequential processors like microcontrollers or DSPs, FPGAs execute tasks in parallel, enabling real-time performance for complex control algorithms.

Key architectural features include:

- Efficiency: Low power FPGAs with multiple FOC implementations
- Parallelism: Multiple control loops and signal processing tasks run concurrently
- Low Latency and Deterministic Timing: Hardware-level scheduling eliminates jitter
- Customizability: Designers can tailor logic to specific motor and application requirements

Advantages of Lattice FPGA-based FOC

Lattice FPGA-based (FOC) solutions offer real-time performance, flexible scalability, and seamless system integration. These advantages enable precise motor control, support for multiple channels, and efficient connectivity with a variety of interfaces and protocols.

Real-Time Performance

- Real-time execution of Clarke/Park transforms, PI controllers, and space vector modulation
- Deterministic latency improves dynamic response and stability
- Enables high switching frequencies for smoother torque output

Flexibility and Scalability

- Supports multiple motor control channels on a single device
- Easily integrates custom IP blocks (e.g., encoder interfaces and fault detection)
- Real time communication (e.g. EtherCAT®, TSN, and SPE)

System Integration

- Interfaces with ADCs, DACs, encoders, and communication protocols (CAN, SPI, and EtherCAT)
- Reduces system complexity and BOM
- Facilitates real-time diagnostics and telemetry

Reliability and Safety

- Hardware-level fault detection (overcurrent, undervoltage, stall conditions, etc.)
- Redundant logic paths for safety-critical systems
- Predictable behavior under all operating conditions
- Performing fault logging and storing error timestamps for debugging and maintenance
- Calculating the rate of temperature increase, speed fluctuations, and frequency of motor stall
- Enabling predictive maintenance features

Designing an FPGA-based FOC Motor Controller

An FPGA based 3-phase FOC motor controller design requires the following basic components:

Power Electronics

- 3-phase inverter consisting of power Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFETs) or Insulated Gate Bipolar Transistor (IGBTs)
- Gate drivers to convert the FPGA PWM signals to the necessary voltage and current levels
- DC power source and regulators to provide power for the motor and control electronics

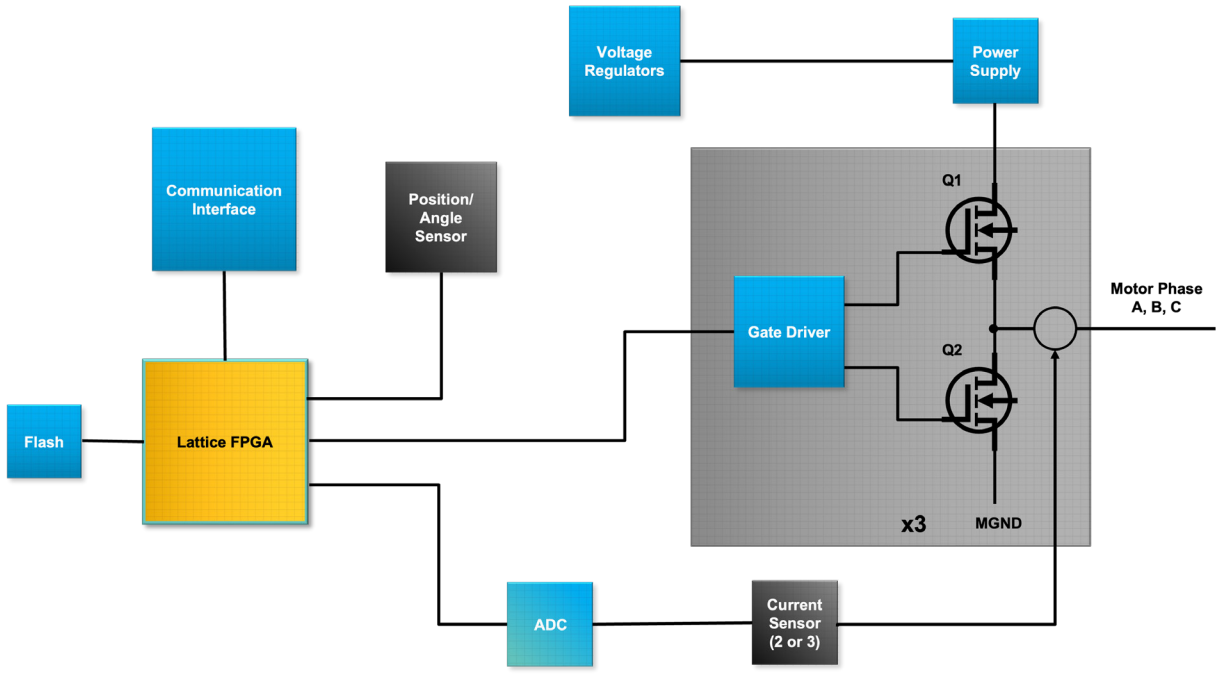
Sensors And Feedback

- Current sensor to measure current from at least 2 of the 3 motor phases
- A position sensor such as an encoder, resolver, or Hall effect
- Analog to digital converter (ADC) to acquire motor phase current and/or voltage

Communication Interface

- Standard interfaces such as EtherCAT, CAN-FD, or a custom physical layer to communicate with a host system

Figure 1: High-Level Block Diagram of an FPGA-Based FOC Motor Controller



For many motor control applications such as humanoid robots, mechanical and thermal constraints require the motor driver to be as small and power efficient as possible. Lattice FPGAs come in very small packages and are designed for low power.

When designing a small printed circuit board (PCB), several factors influence the minimum size of the board. The following is a list of some of the considerations:

- The voltage supplied to the motor drive and logic circuits is known as the bus voltage. When higher bus voltages are used, larger components such as voltage regulators, MOSFETs, and capacitors are required to handle the increased electrical demands.
- The maximum current needed by the motor to achieve the desired torque and speed will influence the size of the voltage regulators and MOSFETs, as well as the amount of power the board must dissipate.
- The type of physical communication link used to connect with the host system or other motor driver boards also impacts component selection. For example, using a physical layer like Multipoint-LVDS (M-LVDS) instead of an Ethernet PHY typically allows for fewer and smaller components.
- The choice of physical communication link for connecting to the host system or other motor driver boards also affects which components are needed. For instance, selecting Multipoint-LVDS (M-LVDS) instead of an Ethernet PHY usually means you can use fewer and smaller components.

Example Design 1

The first example design features a compact 3-phase motor driver that includes all the essential functions needed for FOC motor control within a small footprint. See table 1 for the bill of materials.

Specifications

- FPGA – Lattice Certus-NX 196-pin 0.8 mm pitch BGA (LFD2NX-40-7BG196I)
- Voltage supply – 48 V
- Board power consumption – 1.5 W (does not include power delivered to motor)
- Motor current – Measured in line with each phase
- Encoder interface – BISS-C (RS-485)
- UVW Hall sensor interface
- ADC – 3MSPS quad simultaneous sampling 12-bit
- Communication interface – EtherCAT
- Board size – 50 mm-by-50 mm
- Board layers – 4

Half-Bridge Drivers

When selecting the MOSFETs for the half-bridge circuits, choose a component that has a maximum drain-to-source voltage rating of at least 1.5 times the motor bus voltage. This design uses MOSFETs with a 100 V drain-to-source voltage rating and a typical drain-source on-resistance (RDS(on)) of 49 mΩ in a 2 mm-by-2 mm package. Next, a gate driver is required for the FPGA to control the state of the MOSFETs. Here a half-bridge gate driver, also in a 2 mm-by-2 mm package, was chosen that has a maximum boost voltage rating of 105 V. The boost voltage rating must be greater than the motor bus voltage plus the gate-to-source threshold voltage of the MOSFET to fully turn on the high-side MOSFET. The gate driver must also be able to source and sink enough current to quickly turn on and off the MOSFETs. The amount of current needed depends on the total gate charge of the MOSFETs.

Power Supplies

Several voltage regulators will be required to provide the necessary voltages. This design requires five different voltages; 12 V, 3.3 V, 1.8 V, 1.0 V and 0.9 V. The first regulator will convert the 48 V motor bus-voltage down to 12 V to supply power to the half-bridge gate driver. This voltage regulator will also be used to supply power to the other DC-DC converters. This regulator must be a switching regulator with high efficiency to keep the total power consumption below 1.5 W. For this design, a step-down switching regulator with a nominal peak efficiency of 90% with a maximum output current of 150 mA was selected.

For the next two voltages, 3.3 V and 1.8 V, the same step-down switching regulator was chosen. The regulator is a high efficiency buck regulator that includes both the switch and inductor in a 3 mm-by-2 mm package. At the expected operating current, these regulators have greater than 88% efficiency. The 3.3 V regulator will be powered by 12 V and the 1.8 V regulator will be powered by the 3.3 V regulator.

The final two voltage regulators supply 1.0 V for the FPGA core and 0.9 V for the EtherCAT PHY. A high-PSRR LDO regulator in a 1 mm square package, powered by the 1.8 V rail, generates the 1.0 V core voltage. Then, a 0.71 mm-by-1 mm LDO, powered by the 1.0 V output, provides the 0.9 V required for the EtherCAT core.

Current Measurement

- Analog to Digital Converter

  The FOC motor control algorithm requires measuring at least two out of the three phase currents. These currents should be measured simultaneously for the best control. The measurement method must be capable of measuring the current flow in both directions if the measurement is taken in line with the motor phase. A unidirectional sensing method can be used for low or high side current measurement. The ADC sampling rate should be at least 5 times the PWM frequency. For most motor control applications, a 12-bit ADC resolution is sufficient to obtain precise current measurements. The quad simultaneously sampling ADC comes in a 4 mm-by-4 mm package.

- Current Sense Amplifier

  In this design example, each phase current is measured using a 3 mm-by-3 mm linear Hall-effect current sensor that outputs a ratiometric voltage centered around the sensor voltage supply that is proportional to the current.

Motor Position Measurement

- Hall-Effect Sensors

  When implementing a FOC motor control algorithm, it is beneficial to utilize Hall-effect sensors for startup under load or when high torque is required at low speeds. If implementing sensorless control, the motor's BEMF can be measured and used to determine rotor position. The electrical interface for Hall sensors for this design is implemented using a non-inverting Schmitt trigger buffer in a 1 mm-by-1.95 mm package. Series resistors and clamping diodes are added to protect the board from shorts of the Hall-effect sensors to the motor phases.

- Motor Position Encoder

  The motor encoder provides precise position information of the rotation angle of the motor. This information is used by the FOC algorithm for the position/speed control loop. Commonly used interfaces for motor encoders include serial protocols, such as SSI, EnDat, and BiSS. This example design uses a RS-485 full/half-duplex interface, which is compatible with SSI, BiSS, and EnDat encoders. The circuit is implemented using an RS-485 transceiver, in a 3 mm-by-3 mm package, capable of data rates up to 50 Mbps.

Communication Interface

There are several common interfaces used for host communications in motor control applications, such as EtherCAT, PROFINET, or PROFIBUS. Motor control systems rely on robust communication interfaces to ensure precise coordination between the host controller and the motor driver. EtherCAT is a high-speed industrial Ethernet protocol used for synchronized, deterministic communication. This example design uses two EtherCAT-G PHYs to support a ring topology which are supplied in a 6 mm-by-6 mm package.

Connectors

Choosing connectors for a small form-factor PCB is challenging. You must also ensure that the power connectors can handle the required current. For the power input and motor connections, the example design utilizes single pin quick connect blade connectors. For host communications, the EtherCAT PHYs use IX Industrial connectors that are compact and rugged. The encoder and hall sensor interfaces use 1.25 mm pitch latching connectors.

Table 1: Bill of Materials for Design Example 1

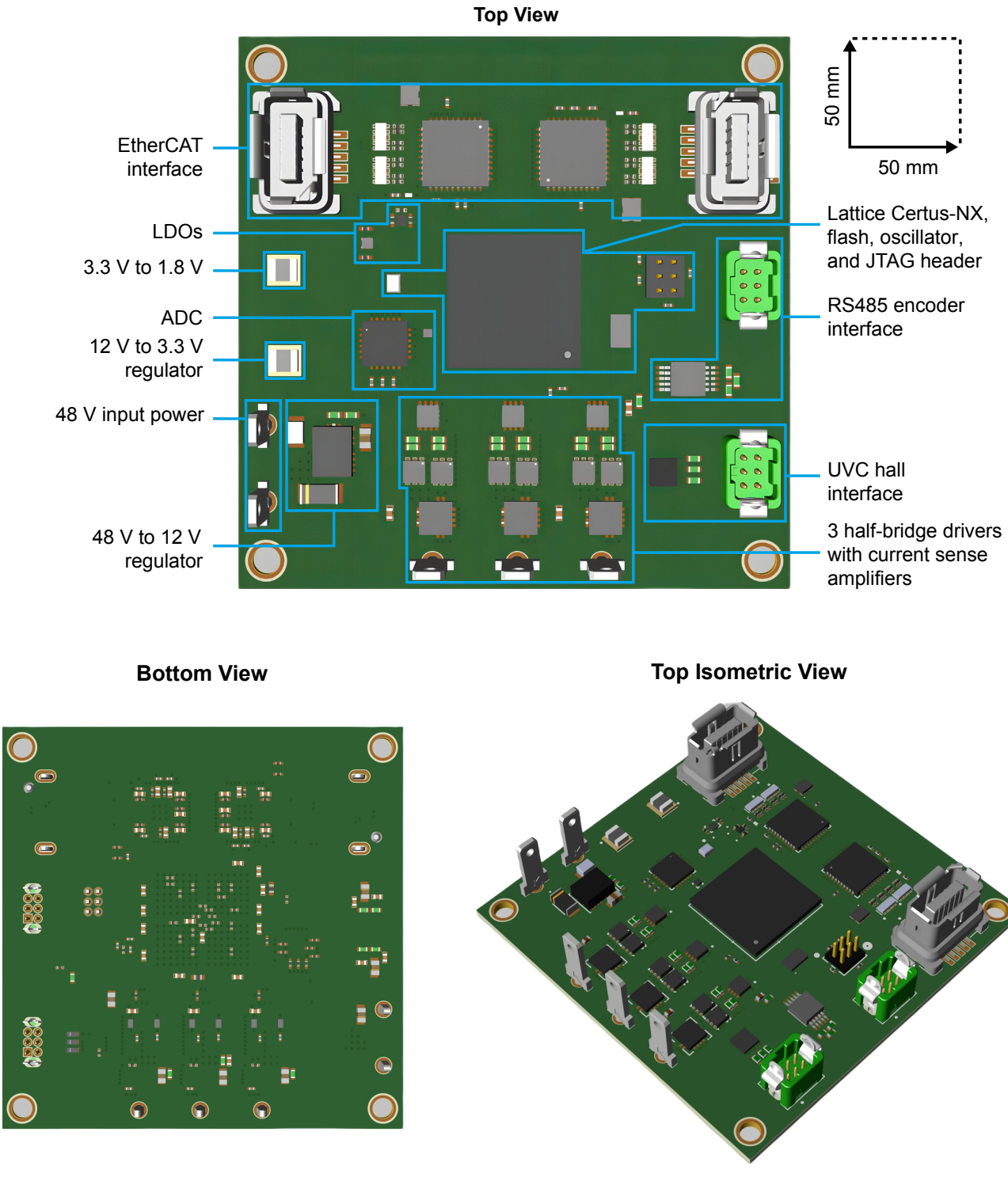
The following list shows the components used in this example, excluding passive parts.

QTY	PART NUMBER	MANUFACTURER	DESCRIPTION
3	NSR10F20NXT5G	ONSEMI	Diode 20 V 1 A Surface Mount 2-DSN (1.4x0.6)
6	SM5819L2-TP	MCC	Diode 40 V 1 A Surface Mount 2-DFN1006
1	GRPB032VWVN-RC	Sullins	Connector Header Through Hole 6 position 0.050" (1.27 mm)
5	1211	Keystone Electronics	0.110" (2.79 mm) Quick Connect Male Solder Connector Non-Insulated
2	ND9BS2200	Amphenol	10 Position Multi-Purpose Receptacle Connector Solder Surface Mount
2	G125-MV10605L1P	Harwin Inc.	Connector Header Through Hole 6 position 0.049" (1.25 mm)
6	CSD19538Q2	Texas Instruments	N-Channel 100 V 14.4 A (Ta) 2.5 W (Ta), 20.2 W (Tc) Surface Mount 6-WSON (2x2)
3	MCS1826GQTE-05-P	Monolithic Power Systems	Current Sensor ±5 A 1 Channel Hall Effect Bidirectional 12-PowerWFQFN
3	LM2005DSGR	Texas Instruments	Half-Bridge Gate Driver IC CMOS, TTL 8-WSON (2x2)
2	TPS82150SILR	Texas Instruments	Non-Isolated PoL Module DC DC Converter 1 Output 0.9 ~ 6 V 1 A 3 V - 17 V Input
1	TLV77410PDQNR	Texas Instruments	Linear Voltage Regulator IC Positive Fixed 1 Output 300 mA 4-X2SON (1x1)
1	TPS7A1309PYCKR	Texas Instruments	Linear Voltage Regulator IC Positive Fixed 1 Output 300 mA 6-DSBGA (0.67x0.96)
1	TPSM365R6RDNR	Texas Instruments	Non-Isolated PoL Module DC DC Converter 1 Output 1 ~ 13 V 600 mA 3 V - 65 V Input
1	W25Q64JVBYIQ	Winbond	FLASH - NOR (SLC) Memory IC 64 Mbit SPI - Quad I/O, QPI 133 MHz 6 ns 12-WLCSP
2	ADIN1300CCPZ-R7	Analog Devices	4/4 Transceiver Full, Half IEEE 802.3 40-LFCSP-WQ (6x6)
1	AD7388-4BCPZ	Analog Devices	12 Bit Analog to Digital Converter 8 Input 4 SAR 24-LFCSP (4x4)
1	REF35300YBHR	Texas Instruments	Series Voltage Reference IC Fixed 3 V V ±0.05% 10 mA 4-DSBGA
1	74LVC3G17GT,115	Nexperia	Buffer, Non-Inverting 3 Element 1 Bit per Element Push-Pull Output 8-XSON, SOT833-1 (1.95x1)
1	THVD1452DGSR	Texas Instruments	1/1 Transceiver Full RS485 10-VSSOP
1	LFD2NX-40-7BG196I	Lattice	Lattice Certus-NX Field Programmable Gate Array (FPGA) IC 150 1548288 39000 196-LFBGA
1	ECS-1612MV-500-CN	ECS	50 MHz XO (Standard) CMOS Oscillator 1.6 V ~ 3.63 V Standby (Power Down) 4-SMD, No Lead
2	ECS-250-12-37B-CWY-TR3	ECS	25 MHz ±10 ppm Crystal 12 pF 50 Ohms 4-SMD, No Lead

BOARD LAYOUT

The cost of manufacturing a small form factor PCB will depend upon several factors which include the number of layers, board size, trace width/spacing and via size/type to name a few. Copper thickness is important to consider as the higher currents require thicker copper to reduce power loss and dissipate heat. When dealing with small pitch BGA's, the number of required board layers is influenced by the signal fan out. See figure 2.

Figure 2: Images of the 3D Generated PCB Assembly



Design Example 2

This example refines the first design to achieve an even smaller PCB footprint while still providing all the necessary FOC functions. Key changes include using an FPGA with a lower pin count and smaller pitch BGA, replacing the quad simultaneous sampling ADC with three individual devices, and switching the EtherCAT interface to Multipoint-LVDS. Only these differences are described below. See table 2 for the bill of materials.

Specifications

- FPGA – Lattice Certus-NX 121-pin 0.5 mm pitch BGA (LFD2NX-40-7MG121A)
- Voltage supply – 48 V
- Board power consumption – 1.5 W (does not include power delivered to motor)
- Motor current – Measured in line with each phase
- Encoder interface – BISS-C (RS-485)
- UVW Hall sensor interface
- ADC – 3 SAR 1MSPS 12-bit
- Communication interface – Multipoint-LVDS
- Board diameter – 40 mm
- Board layers – 4

Power Supplies

This design requires one less voltage regulator than the original. Since the EtherCAT PHY is not used, the 0.9 V LDO is removed.

Communication Interface

Since Lattice FPGAs can support custom protocols, this design uses a multi-point LVDS physical layer interface which requires fewer I/O than an Ethernet based protocol and has the advantage of reducing the cabling requirements. To implement the protocol, two full-duplex Type-1 Multipoint-LVDS transceivers, in 4 mm-by-4 mm packages, are used for clock and data transmission at speeds up to 200 Mbps.

Connectors

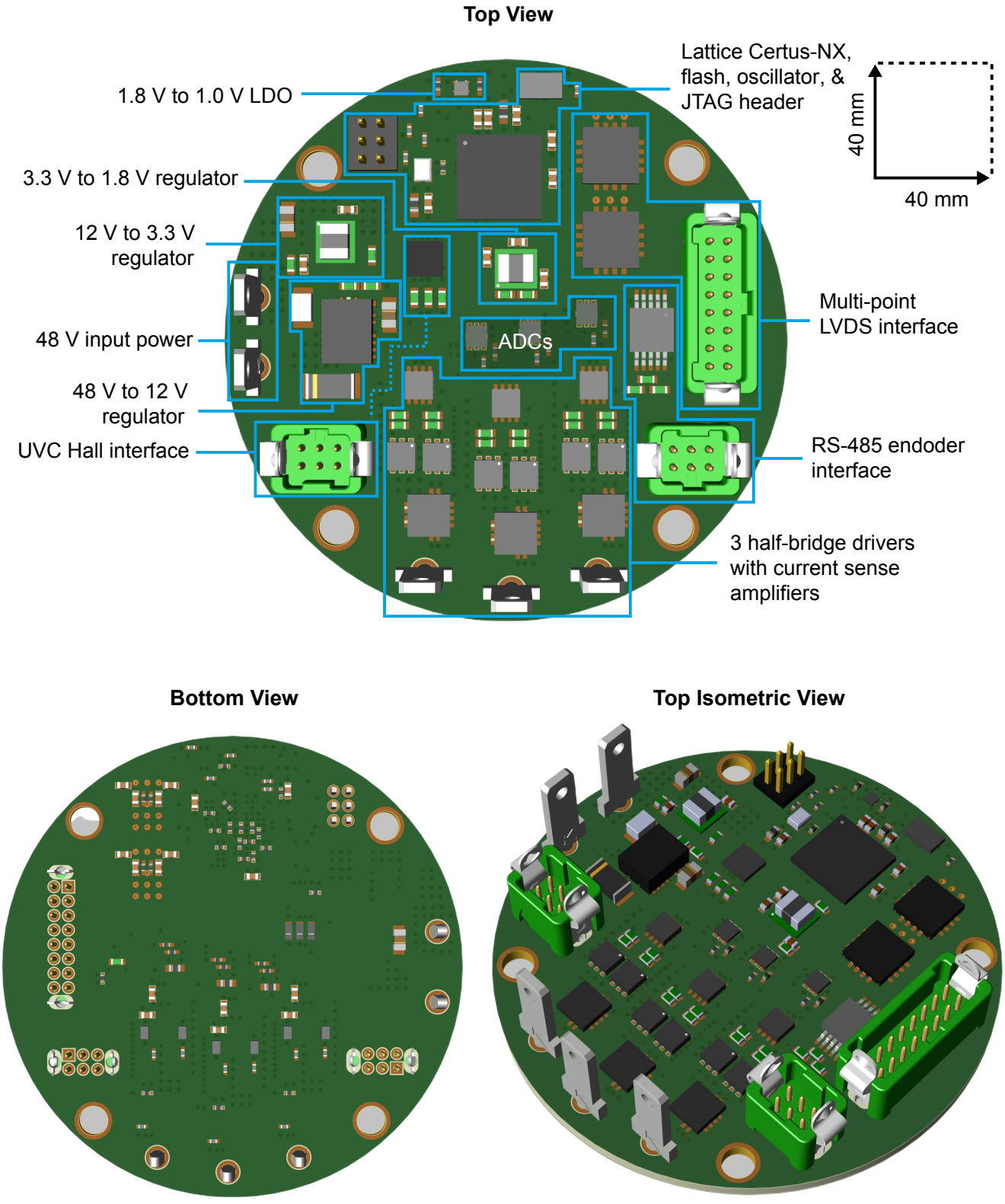
For Multipoint-LVDS communications, only a single connector is required. The 16-pin version of the 1.25 mm pitch latching connector was used and requires less board space.

Table 2: Bill of Materials for Design Example 2

The following list shows the components used in this example, excluding passive parts.

QTY	PART NUMBER	MANUFACTURER	DESCRIPTION
6	SM5819L2-TP	MCC	Diode 40 V 1 A Surface Mount 2-DFN1006
3	NSR10F20NXT5G	ONSEMI	Diode 20 V 1 A Surface Mount 2-DSN (1.4x0.6)
1	GRPB032VWVN-RC	Sullins	Connector Header Through Hole 6 position 0.050" (1.27 mm)
5	1211	Keystone Electronics	0.110" (2.79 mm) Quick Connect Male Solder Connector Non-Insulated
1	G125-MV11605L1P	Harwin Inc.	Connector Header Through Hole 16 position 0.049" (1.25 mm)
2	G125-MV10605L1P	Harwin Inc.	Connector Header Through Hole 6 position 0.049" (1.25 mm)
6	CSD19538Q2	Texas Instruments	N-Channel 100 V 14.4 A (Ta) 2.5 W (Ta), 20.2 W (Tc) Surface Mount 6-WSON (2x2)
3	MCS1826GQTE-05-P	Monolithic Power Systems	Current Sensor ±5 A 1 Channel Hall Effect Bidirectional 12-PowerWFQFN
3	LM2005DSGR	Texas Instruments	Half-Bridge Gate Driver IC CMOS, TTL 8-WSON (2x2)
2	TPSM82901SISR	Texas Instruments	Non-Isolated PoL Module DC DC Converter 1 Output 0.4 ~ 5.5 V 1 A 3 V - 17 V Input
1	TLV77410PDQNR	Texas Instruments	Linear Voltage Regulator IC Positive Fixed 1 Output 300 mA 4-X2SON (1x1)
1	TPSM365R15RDNR	Texas Instruments	Non-Isolated PoL Module DC DC Converter 1 Output 1 ~ 13 V 150 mA 3 V - 65 V Input
1	W25Q64JVBYIQ	Winbond	FLASH - NOR (SLC) Memory IC 64 Mbit SPI - Quad I/O, QPI 133 MHz 6 ns 12-WLCSP
2	SN65MLVD203BRUMR	Texas Instruments	1/1 Transceiver Full 16-WQFN (4x4)
3	ADS7042IRUGR	Texas Instruments	12 Bit Analog to Digital Converter 1 Input 1 SAR 8-X2QFN (1.5x1.5)
1	74LVC3G17GT,115	Nexperia	Buffer, Non-Inverting 3 Element 1 Bit per Element Push-Pull Output 8-XSON, SOT833-1 (1.95x1)
1	THVD1452DGSR	Texas Instruments	1/1 Transceiver Full RS485 10-VSSOP
1	LFD2NX-40-7MG121A	Lattice	Lattice Certus-NX Field Programmable Gate Array (FPGA) IC 71 1548288 39000 121-VFBGA, CSPBGA
1	ECS-1612MV-500-CN	ECS	50 MHz XO (Standard) CMOS Oscillator 1.6 V ~ 3.63 V Standby (Power Down) 4-SMD, No Lead

Figure 3: Images of the 3D Generated Assembly



Conclusion

Lattice FPGAs offer a transformative approach to Field-Oriented Control of brushless three-phase motors. Their parallelism, determinism, and configurability make them ideal for demanding applications where performance, reliability, and integration matter most. As motor control requirements evolve, Lattice FPGAs provide a future-proof platform for innovation.

Acronyms in This Document

Acronym	Definition
ADC	Analog to Digital Converter
BEMF	Back Electro-Motive Force
BOM	Bill of Materials
BISS	Bidirectional Synchronous Serial
CAN	Controller Area Network
DC	Direct Current
DAC	Digital to Analog Converter
DSP	Digital Signal Processor
EnDAT	Encoder Data
EtherCAT	Ethernet for Control Automation Technology
FOC	Field-Oriented Control
FPGA	Field Programmable Gate Array
IGBT	Insulated Gate Bipolar Transistor
I/O	Input Output
JTAG	Joint Test Action Group
LDO	Low-Dropout (linear) Regulator
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
M-LVDS	Multipoint Low-Voltage Differential Signaling
MCU	Microcontroller Unit
PCB	Printed Circuit Board
PHY	Physical Layer
PSRR	Power Supply Rejection Ratio
PWM	Pulse Width Modulation
RDS(on)	Drain-Source ON-Resistance
SAR	Successive Approximation Register
SPE	Single-Pair Ethernet
SPI	Serial Peripheral Interface
SSI	Synchronous Serial Interface
TSN	Time-Sensitive Networking

READY TO LEARN MORE?

To learn more about Lattice low power FPGA-based solutions for industrial, automotive, communications, computing, and consumer applications, visit **www.latticesemi.com** or contact us at **www.latticesemi.com/contact** or **www.latticesemi.com/buy**.

TECHNICAL SUPPORT ASSISTANCE

Submit a technical support case through **www.latticesemi.com/techsupport**.
For frequently asked questions, please refer to the Lattice Answer Database at **www.latticesemi.com/Support/AnswerDatabase.**

V.1 WP0048