Lattice Radiant 2025.2 Software Release Notes

Welcome to Lattice Radiant® software, the complete design environment for Lattice Semiconductor Field Programmable Gate Arrays (FPGAs).

What's New in Radiant 2025.2 Software

- **Device Support:**
  - Certus™-NX (LFD2NX)
    - 9 (-7/-8/-9) 1.00V (COM/IND/AUTO) – CSFBGA121, CABGA196
  - Certus™-N2 (LN2-CT)
    - 20ES1 (-1/-2/-3) 0.82V (COM/IND) – CBG484
  - Lattice™ Avant (LAV-AT)
    - E70 (-1/-2/-3) 0.82V (COM/IND) – CBG484, CSG841, LFG1156, LFG676
  - MachXO4™ (LFMXO4) – This new family supports Reveal Debugger, Power Calculator, and bitstream capability.
    - 010HC (-5/-6) 2.5V/3.3V (COM/IND/AUTO) – TSG100, BSG132
    - 010HC (-5/-6) 2.5V/3.3V (COM/IND) – TSG144
    - 010HE (-5/-6) 1.2V (COM/IND/AUTO) – TSG100, BSG132
    - 010HE (-5/-6) 1.2V (COM/IND) – TSG144
    - 015HC (-5/-6) 2.5V/3.3V (COM/IND/AUTO) – TSG100, BSG132, BBG256
    - 015HC (-5/-6) 2.5V/3.3V (COM/IND) – TSG144, BFG256
    - 015HE (-5/-6) 1.2V (COM/IND/AUTO) – TSG100, BSG132, BBG256
    - 015HE (-5/-6) 1.2V (COM/IND) – UUG36, TSG144, BFG256
    - 025HC (-5/-6) 2.5V/3.3V (COM/IND/AUTO) – TSG100, BSG132, BBG256
    - 025HC (-5/-6) 2.5V/3.3V (COM/IND) – TSG144, BFG256
    - 025HE (-5/-6) 1.2V (COM/IND/AUTO) – TSG100, BSG132, BBG256
    - 025HE (-5/-6) 1.2V (COM/IND) – UUG49, TSG114, BFG256
    - 050HC (-5/-6) 2.5V/3.3V (COM/IND/AUTO) – BSG132, BBG256
    - 050HC (-5/-6) 2.5V/3.3V (COM/IND) – TSG144, BFG256, BBG400
    - 050HE (-5/-6) 1.2V (COM/IND/AUTO) – BSG132, TSG114, BBG256
    - 050HE (-5/-6) 1.2V (COM/IND) – UUG81, BFG256, BBG400

- 080HC (-5/-6) 2.5V/3.3V (COM/IND) – BBG256, BBG400
- 080HE (-5/-6) 1.2V (COM/IND) – BBG256, BBG400
- 110HC (-5/-6) 2.5V/3.3V (COM/IND) – BBG256, BBG400, BBG484
- 110HE (-5/-6) 1.2V (COM/IND) – BBG256, BBG400, BBG484

- **Tool and Other Enhancements:**
  - **Digital Signature Tab** – Support for digital signature has been added in Radiant executables for improve security and authentication.
  - **IP –** Various IP Cores are now bundled with Lattice Radiant Subscription license starting in Radiant 2025.2 release (i.e. PCIe, Ethernet, (10G & below), DDR4, LPDDR4). For complete list, please refer to the Product Bulletin FPGA-PB-02030 1.0 - Lattice Radiant Software & IP Licensing Updates.
  - **LSE –** The LSE top-module identification behavior has been updated. If top-module is not set in the LSE project file, LSE now issues a critical warning in the LSE report file.
  - **Reveal**
    - Reveal Analyzer waveforms have been improved.
    - Reveal SERDES kit now supports SERDES merge.
  - **Synplify Pro**
    - Synplify Pro now uses SLICE for register mapping instead of IOL by default.
    - The IO register is now set to “disabled” by default.
  - **Timing Analysis**
    - The “Overall Summary” section of the timing engine has been updated. Each timing corner now shows one to three lines, depending on the errors found.
    - Nexus Fast Corner STA default setting uses Vccmax for Hold time analysis. Previous releases used Vccmin by default.
  - **Timing Constraints** – A new Constraint Configuration dialog has been added to support using multiple constraint files. This feature allows users to add, remove, reorder, save, and manage individual constraint files. Only top-level constraint files are supported.

Updating Projects from an Earlier Version

If you want to work on a design project created with an earlier version of Radiant software, it may be necessary to re-create some IP, per the procedures described in the following table.

These procedures adapt the project for the changes in Radiant software.

Versions	IP Regeneration Procedures		
	Avant (LAV-AT)	**CrossLink-NX (LIFCL), Certus-N2 (LN2-CT-ES), Certus-NX (LFD2NX), Certus-NX-RT (UT24C), CertusPro-NX (LFCPNX), and CertusPro-NX-RT (UT24CP), MachXO4 (LFMXO4), MachXO5-NX (LFMXO5)**	
2025.2	MPPHY	PLL	These IP used in designs created in Radiant 2025.1.1 or earlier must be re-generated in Radiant 2025.2.
	PLL	DDR_MEM	
	SEDC	MIPI_DPHY	
		MPCS	

Supported Devices

Lattice Radiant software can be used with either a free license or a subscription license. The two licenses provide access to different device families.

Device Family	Free License	Subscription License
iCE40 UltraPlus (iCE40UP)	◄	◄
Lattice Avant (LAV-AT)		◄

Device Family	Free License	Subscription License
CertusPro™-NX (LFCPNX)	Evaluation Mode	◄
Certus-NX (LFD2NX)	◄	◄
Certus-N2 (LN2-CT-ES)		◄
MachXO4 (LFMXO4)	◄	◄
MachXO5-NX (LFMXO5-25)	◄	◄
MachXO5-NX (LFMXO5-100T)	Evaluation Mode	◄
MachXO5-NX (LFMXO5-35)	◄	◄
MachXO5-NX (LFMXO5-35T)	Evaluation Mode	◄
MachXO5-NX (LFMXO5-55TDQ)[1]		◄
MachXO5-NX (LFMXO5-65)	◄	◄
MachXO5-NX (LFMXO5-65T)	Evaluation Mode	◄
MachXO5-NX (LFMXO5-15D)[1]		◄
CrossLink-NX (LIFCL)	◄	◄
CrossLink-NX (LIFCL-33U)	Evaluation Mode	◄
Certus-NX-RT (UT24C)	Evaluation Mode	◄
CertusPro-NX-RT (UT24CP)	Evaluation Mode	◄

Note:

1. To enable this device, please submit a support ticket.

Support for Third-Party Synthesis and Simulator Tools

The Synopsys Synplify Pro® for Lattice synthesis tool and the Siemens QuestaSim® Lattice Edition simulator tools are included in the Radiant software.

- **Synopsys Synplify Pro FPGA synthesis software version W-2025.03LR-SP1**
  - Release Notes for Synplify Pro are located in ..\<*install_directory*>\radiant\2025.2\synpbase\doc\. The file name is release_notes.pdf.
  - A full set of documents for Synplify Pro are also located in \<*install_directory*>\radiant\2025.2\synpbase\doc\.
- **Siemens QuestaSim Lattice Edition 2025.2**
  - Release Notes for QuestaSim Lattice Edition are located in <install_directory>\radiant\2025.2\questasim\. The file names are RELEASE_NOTES.html or RELEASE_NOTES.txt.
  - A full set of documents for QuestaSim Lattice Edition are located in <install_directory>\radiant\2025.2\questasim\docs\pdfdocs.
- **Siemens Questa® 2022.3**
- **Cadence Xcelium® 24.03.003**
- **Synopsys VCS® U-2023.03-SP2**

Help Resources

- Online Help updated with CertusPro-NX (LFCPNX), Certus-NX (LFD2NX), MachXO5-NX (LFMXO5), CrossLink-NX (LIFCL), Certus-NX-RT (UT24C), CertusPro-NX-RT (UT24CP), and Lattice Avant (LAV-AT) content.
- To view the Online Help, start the Lattice Radiant software and select the 

"Getting Started" icon under Information Center.

  Note: The Firefox Snap install is not supported if you are using Ubuntu 20.04 or 18.04 to access the Radiant Help. This is a result of the snap install's inability to open local HTML pages. You may reinstall the latest version of Firefox using Apt install. For installation instructions, please refer to this guide.

System Requirements

The following shows the basic system requirements for Radiant software:

- Intel x86 64-bit or 64-bit-compatible PC
- OS Support:

64-bit OS	Radiant	Synplify Pro	QuestaSim
Windows 10	✓	✓	✓
Windows 11	✓	✓*	✓
Red Hat Enterprise Linux 8.10	✓	✓	✓
Ubuntu version 24.04 LTS	✓	✓*	✓*
Ubuntu version 22.04 LTS	✓	✓*	✓*

***Note**: The third-party tools have been tested by Lattice on the listed platforms, but the vendors do not officially support them.

- Approximately 50GB free disk space
- Computer Memory Requirement:
  - Nexus – 16GB
  - LAV-AT– 32GB Recommended for running a single project. If running multiple projects, the memory requirement will be higher.
- 1024 X 768 graphics display
- Network adapter for license and network connectivity
- A Web browser with JavaScript capability
- Acrobat Reader

Issues Fixed in this Release

The following known issues are fixed in this release. Their workarounds are no longer needed.

Security commands are not available for SSPI embedded programming.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-28999

Post-Synthesis fails due to invalid Clock and Multi-Cycle Path constraints when using “generate” keyword.

Devices affected: All devices

Bug number: DNG-28930

Place & Route (PAR) does not count gated clock correctly.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-28761

There is a mismatch when ECO editor initializes memory readback value.

Device affected: Lattice Avant (LAV-AT)

Bug number: DNG-27777

Timing Analysis for CDC paths may be incorrect if the following conditions are met:

- **PLL has a phase shifted clock**
- **User defined PLL output clock constraints**
- **There is a CDC path with the phase shifted PLL clock**

Device affected: All devices

Bug number: DNG-27414

Incorrect number of PIOs shown in the Device Selector Window for LFD2NX-35/65 CABGA400 packages.

The correct PIO count should be 307.

Devices affected: Certus-NX (LFD2NX-35, LFD2NX-65)

Bug number: DNG-27120

The MPP merge arbiter does not work for PMA registers.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-27079

Incorrect autogenerated clock constraints for PCIEx4 IP create_generated_clock must be used instead of create_clock.

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-26433

The PLL dynamic phase adjustment is inaccurate when phase_dir = 1.

Device affected: Certus-NX (LFD2NX), Certus-NX (LFD2NX), MachXO5-NX (LFMXO5), CrossLink-NX (LIFCL), Certus-NX-RT (UT24C), CertusPro-NX-RT (UT24CP)

Bug number: DNG-26281

Unsupported components may still pass synthesis when using both Synplify Pro and LSE.

SEDCA, UMXSPI, and UXSPI are not available for the E30ES device, but the synthesis step in Radiant project flow may still pass.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-24562

Synplify reports could not find binding for a variable.

Device affected: CrossLink-NX (LIFCL)

Bug number: DNG-21575

Using the Dynamic Clock Enable feature, re-enabled clocks do not start on falling edge of the associated clocks.

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-15105

The CSI-2/DSI D-PHY Transmitter and Receiver Soft IP simulations fail when using Synopsys VCS as simulation tool.

Devices affected: CertusPro-NX (LFCPNX), Certus-NX (LFD2NX), CrossLink-NX (LIFCL), Certus-NX-RT (UT24C), CertusPro-NX-RT (UT24CP)

Bug number: DNG-13225

Known Issues for Radiant 2025.2

The following are known issues for Radiant Software 2025.2. For assistance with these issues, please contact Lattice Technical support.

Mismatch in Radiant's SHAREDEBRINIT=Disable behavior for LFMXO4 compared to XO3 in Diamond.

Devices affected: MachXO4 (LFMXO4)

Bug number: DNG-30070

Post-synthesis TCE does not infer the correct clock frequency from PLL.

Workaround: Use Pre-synthesis constraints editor to constrain the PLL output clocks.

Devices affected: MachXO4 (LFMXO4)

Bug number: DNG-29970

ECO memory initialization is not supported for LFMXO4 device.

Devices affected: MachXO4 (LFMXO4)

Bug number: DNG-29952

Standalone Physical Designer application fails to launch in Linux.

When launching Standalone Physical Designer (or the fpgae GUI) in Red Hat Enterprise Linux 8 OS, a dependency error prompt is shown in the terminal.

Workaround: Use the Radiant built-in Physical Designer.

Devices affected: All devices

Bug number: DNG-29701

The IO mode in Physical Designer is not available for LFMXO4 devices.

Devices affected: MachXO4 (LFMXO4)

Bug number: DNG-29616

If the width of the ROM data in the memory file is wider than the ROM width, Radiant will only issue a warning and ignore the extra bits. This is different operation than Diamond for XO3 which would issue an error.

Devices affected: MachXO4 (LFMXO4)

Bug number: DNG-29440

Incorrect Dual Boot Behaviour with Specific sysCONFIG Settings.

Radiant sysCONFIG settings allow you to configure CONFIGURATION, DUALBOOTGOLDEN, and MASTER_SPI_PORT to enable the Dual Boot feature. By applying specific settings, you can select the desired boot mode.

The issue occurs when the following settings are applied:

- CONFIGURATION = EXTERNAL
- DUALBOOTGOLDEN = INTERNAL
- MASTER_SPI_PORT = ENABLE

Under these settings, it is expected for the device to boot from external SPI flash first and, if configuration fails, attempt to boot from the golden image in internal flash. This fallback behavior is not supported.

Workaround: Use the supported Dual Boot mode (CFG_EXT), which boots from internal flash first and, if configuration fails, attempts to boot from the golden image in external SPI flash.

To enable this mode, set:

- CONFIGURATION = CFG
- DUALBOOTGOLDEN = EXTERNAL
- MASTER_SPI_PORT = ENABLE

Devices affected: MachXO4 (LFMXO4)

Bug number: DNG-29393

IOs are missing in the Physical Designer Placement Mode.

Devices affected: MachXO4 (LFMXO4)

Bug number: DNG-29369

SEI Editor generates incorrect SEI information.

The SEI implementation for LFMXO4 is not yet available, which causes the GUI to display unrealistic values.

Devices affected: MachXO4 (LFMXO4)

Bug number: DNG-29364

The DCC and DCM resource utility in PAR report are missing.

You can still view the usage in the clock report area of the PAR report.

Devices affected: MachXO4 (LFMXO4)

Bug number: DNG-29345

Bitstream generation may error out when specifying custom idcode (MY_ASSP=ON).

When the “MY_ASSP” system configuration interface pin is enabled, the CUSTOM_IDCODE field becomes the device’s JTAG ID. This change leads to an issue during bitstream generation for LFMXO4 devices. The problem only occurs in designs where this field is set, not in all configurations.

Devices affected: MachXO4 (LFMXO4)

Bug number: DNG-29152

Internal device name is visible in DCE device part view.

Devices affected: MachXO4 (LFMXO4-015HE, LFMXO4-015HC, LFMXO4-050HC and LFMXO4-050HE) with specific packages (BFG256, BBG256 and BBG400)

Bug number: DNG-29144

Synplify Pro infers EBR blocks instead of LRAM for several clear-text designs.

Devices affected: MachXO5 (LFMXO5)

Bug number: DNG-30284

When launching Radiant using Ubuntu OS on remote sessions, the Radiant application may fail to start and display the following error: [fatal] unknown:0 - Could not initialize GLX. Aborted (core dumped).

This indicates an OpenGL/GLX initialization failure. Possible causes include:

- Missing or misconfigured GLX libraries.
- Incorrect X11 configuration for OpenGL/GLX.
- Graphics driver or hardware issues.

Workaround: Set the following environment variables before launching Radiant:

```
export QT_XCB_GL_INTEGRATION=none
export QT_QUICK_BACKEND=software
```

Devices affected: All devices

Bug number: DNG-30276

When using Structural Verilog (.vm) in the design flow, information about the synthesis attribute black_box_pad_pin="clk, rst, count" is not available in the online help.

Devices affected: All devices

Bug number: DNG-30152

When using LSE, synthesis may fail with the following error message: “'components' is not compiled in library lav_ate. VHDL-1240 [top.vhd:4]”.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-30117

QuestaSim Lattice-Edition simulation repeatedly shows warning of non-differential clock being used.

Devices affected: Certus-NX (LFD2NX)

Bug number: DNG-30104

PAR's Design Utilization Summary may display more SLICEs used than what is listed as available on the device.

Devices affected: Certus-NX (LFD2NX)

Bug number: DNG-30080

Radiant Programmer does not show bitstream checksum.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG- 30013

Password may still show up even though the Hide/Show Password is checked/unchecked in the bitstream security settings GUI.

Devices affected: All devices

Bug number: DNG-29999

Executing Programmer-specific TCL commands using radiantc.exe script.tcl or pnmainc.exe script.tcl consistently fails.

Devices affected: All devices

Bug number: DNG-29997

Changing Vcc in DCE and Standalone Timing Analyzer does not affect hold analysis. Hold Analysis always uses Vcc Max for analysis.

Devices affected: All devices

Bug number: DNG-29957

LSE Synthesis may fail when CRC_Register attribute is used with an error:" CDC_Register chain cannot be fully determined for register…".

Devices affected: All devices

Bug number: DNG-29431

Radiant may crash in very rare cases during implementation when Pre-synthesis Constraints Editor is open.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-29819

Post synthesis simulation may fail when top-level module is not specified in the project, and the design is compiled from the command-line using LSE synthesis engine in Linux OS.

Workaround: This will not be an issue if the top-level module is specified when running LSE. A CRITICAL warning has been added at the beginning of the LSE flow if there is no top-level module specified in the command line options.

Devices affected: MachXO5 (LFMXO5)

Bug number: DNG-29792

Expected critical warning during LSE synthesis is not available: CRITICAL <35001747> – Bit(s) of a register stuck at '0'.

Devices affected: All devices

Bug number: DNG-29724

Simulation Wizard GUI may issue a false error message “Simulation top parsing failed” when LPDDR4 IP is used. This does not affect the simulation.

Workaround: Click Next and Finish in Simulation Wizard to complete the simulation.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-29676

Inserting Reveal causes change in the hierarchy names when OSC IP is used.

Workaround: Use Post-Synthesis Reveal debug flow.

Devices affected: All devices

Bug number: DNG-29637

Cannot constrain MIPI HSRXEN pin of soft DPHY in both Avant and Nexus devices.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-29657

When an IP's constraints.sdc file contains a set_false_path, the constraint is silently dropped during synthesis.

Timing paths meant to be excluded are analyzed, causing violations and misleading reports. The set_false_path in constraints.sdc is ignored during synthesis due to IP boundary validation failure, dropping the constraint line and sometimes the entire exception block.

Workaround: Add the constraint in the .pdc file.

Devices affected: Lattice Avant (LAV-AT-E70), CrossLink-NX (LIFCL)

Bug number: DNG-29653

The use of Distributed RAM in a design can cause the Delay Element to function incorrectly.

Devices affected: Lattice Avant (LAV-AT-E70)

Bug number: DNG-29618

Pre-Synthesis Constraint Editor may experience a segmentation fault when adding set_max_delay/set_min_delay constraint into the project without any constraint file set in the original project through Pre-Synthesis Timing Constraint Editor.

Devices affected: All devices

Bug number: DNG-29570

Gate-level timing simulation may show an unexpected jitter for PLL.

Devices affected: Lattice Avant (LAV-AT-E70)

Bug number: DNG-29299

LSE synthesis may fail on a design that successfully compiles with Synplify Pro but encounters errors during PAR.

Devices affected: Certus-NX (LFD2NX)

Bug number: DNG-29029

The bitstream hardware data status of LFD2NX-35/65 is missing.

The bitstream hardware data status is Preliminary.

Devices affected: Certus-NX (LFD2NX-35, LFD2NX-65)

Bug number: DNG-28463

Radiant may crash during implementation when DCE is open.

Workaround: Close DCE and run implementation.

Devices affected: Certus-NX (LFD2NX-35, LFD2NX-65)

Bug number: DNG-28678

You may encounter a simulation issue with Certus-NX LRAM IP where, when "DPS" is asserted high, "lram_ready" does not go low.

The expected behavior is that when "DPS" is driven high, "lram_ready" should be low because LRAM is powered down by "DPS".

Devices affected: Certus-NX (LFD2NX)

Bug number: DNG-27555

The des_read_udb command is required to initialize the memory in ECO Editor when running eco_config_memory in Radiantc.

Devices affected: Certus-NX (LFD2NX)

Bug number: DNG-27493

Designs using VM’s instantiated inside another VM fail post-synthesis.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-27317

When using Synplify Pro, the user-defined create_generated_clock SDC constraint for the PLL clock output will be overwritten by auto-generated PLL clock constraints when a Reveal Core is added.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-26270

Certain programming operations using compressed bitstream (RBT format) are currently not functional due to a known software limitation.

Workaround: Use plain or uncompressed bitstream formats.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-26097

Missing Timing Arc: OSCA to CONFIG_CLKRST_CORE for LMMI_CLK clock path.

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-27889

Standalone Timing Analyzer results may differ from RunSTA results, even when using the same pdc file.

Devices affected: Certus-NX (LFD2NX)

Bug number: DNG-27523

Timing analysis and the Tcl command “sta_get_slack -worst” may return different worst slack values.

The command may return a slack value, but it might not be the worst-case slack. The returned slack is valid, but it corresponds to a path that does not represent the worst slack.

In addition, the detailed timing report may contain some arrival values that are incorrect. However, the path of the report, the delays of the connections and arcs along the path, the required value, the arrival value used for slack computation, and the slack of the path are all correct.

Device affected: All devices

Bug number: DNG-27408

The power file revision is shown as advanced in LFMXO5-35/35T/65/65T devices.

The power file revision should be Preliminary.

Devices affected: MachXO5-NX (LFMXO5-35, LFMXO5-35T, LFMXO5-65, LFMXO5-65T)

Bug number: DNG-26755

Internal PLL of MIPI D-PHY does not lock when clocked by an external PLL with fractional clocks.

PLL does not lock when there are clock period fluctuations in its reference clock.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-24807

The location for a secured component (Hard DPHY) cannot be changed.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-24746

In PLL simulation, the phase stops moving when it goes over 360 degrees.

In a Phase-Locked Loop (PLL) simulation, the phase should not stop moving but only reset to stay within a specific range (such as 0°–360).

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-23458

CONFIG_LMMIE and CONFIG_LMMIB RTL simulation fails.

Devices affected: MachXO5-NX (LFMXO5)

Bug number: DNG-22187

The clock, using pclk routing and connected only to fabric registers, has a lower clock MPW at the higher speed grade (-8).

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-21315

Synplify Pro synthesis may fail if the .sdc file contains a user-defined constraint referencing a hierarchical object that includes a dot (.). Example: top.inst/out.

Workaround: Create the constraint in the .pdc file instead of .sdc file.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-20134

Radiant may crash on version 2025.2 due to libbasct.dll.

Workaround: If you encounter this issue, try one of the following solutions:

1. Contact Lattice Technical Support to request for the unencrypted libbasct.dll.
2. Whitelist the specific dll in antivirus software (already documented in troubleshooting guide section).

Devices affected: MachXO5-NX (LFMXO5)

Bug number: DNG-27676

Synplify Pro Fails to Optimize Resource on pmi_fifo design if Reveal Core is inserted causing undesired toggling of the empty flag of the FIFO.

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-24358

You may encounter an issue with CONFIG_LMMI and CONFIG_LMMA's lmmi_ready signal during simulation.

Devices affected: Certus-NX (LFD2NX), CrossLink-NX (LIFCL)

Bug number: DNG-20717