MachXO4 PLL Module

IP Version: v3.0.1

User Guide

FPGA-IPUG-02316-1.0

December 2025

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Inclusive Language

This document was created consistent with Lattice Semiconductor’s inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice’s inclusive language FAQ 6878 for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

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Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviations	Definition
CSR	Control and Status Register
EFB	Embedded Function Block
FPGA	Field-Programmable Gate Array
IP	Intellectual Property
LSE	Lattice Synthesis Engine
PLL	Phase-Locked Loop

1. Introduction

This user guide describes the Phase Locked Loop (PLL) Module. PLL is essential component in digital systems that enable precise clock management, frequency synthesis, and phase alignment.

The PLL Module lets you generate multiple output clocks with configurable frequencies, phases, and duty cycles from a single reference clock input. It support high-speed interfaces, reduce clock jitter, and manages multiple clock domains within a single FPGA.

1.1. Quick Facts

Table 1.1. Summary of the PLL Module

IP Requirements	Supported Devices	MachXO4™
	IP Changes[1]	For a list of changes to the IP, refer to the MachXO4 PLL Module Release Notes (FPGA-RN-02316).
Resource Utilization	Supported User Interface	Native interface.
Design Tool Support	Lattice Implementation	IP Core v3.0.1 – Lattice Radiant™ Software 2025.2.
	Synthesis	Synopsys® Synplify Pro for Lattice, Lattice Synthesis Engine (LSE)
	Simulation	For a list of supported simulators, see the Lattice Radiant Software User Guide.

Note:

1. In some instances, the IP may be updated without changes to the user guide. This user guide may reflect an earlier IP version but remains fully compatible with the later IP version. Refer to the IP Release Notes for the latest updates.

1.2. Features

Key features of the PLL Module:

- Reference input clock:
  - Clock range: 10 MHz to 400 MHz
  - Clock divider range: 1 to 40
  - Dynamic clock source selection
- Feedback Path:
  - Feedback divider range: 1 to 128
  - Supports a Fractional-N divider with up to 16-bit resolution
  - Feedback input selection: internal, external, or user port
- Generated Output Clock
  - Supports up to four individual configurable output clocks
  - Frequency range: 0.0122 MHz to 400 MHz
  - Output divider range: 1 to 128
  - Supports internal clock output cascading
  - Supports bypassing of VCO and divider for output clocks
  - Supports trim and duty cycle adjustment
- Phase Shift Support:
  - Static phase shift: 8 steps (0° to 315°) per output clock
  - Dynamic VCO phase shift supported
- Reset Capability:
  - Full PLL reset
  - Individual output reset for CLKOS2 and CLKOS3
- Lock Detector
- WishBone Interface: Used with Embedded Function Block (EFB) Block for CSR access
- Dynamic Low-Power/Standby Mode Supported

1.3. Licensing and Ordering Information

The PLL Module is provided at no additional cost with the Lattice Radiant software.

1.4. Naming Conventions

1.4.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.4.2. Signal Names

- *_n* are active low (asserted when value is logic 0)
- *_i* are input signals
- *_o* are output signals

2. Functional Description

2.1. Overview of the IP

The top-level block diagram of the PLL Module is shown in Figure 2.1. The PLL Module supports WishBone interface, which must be used with the EFB block to configure the PLL CSR at runtime.

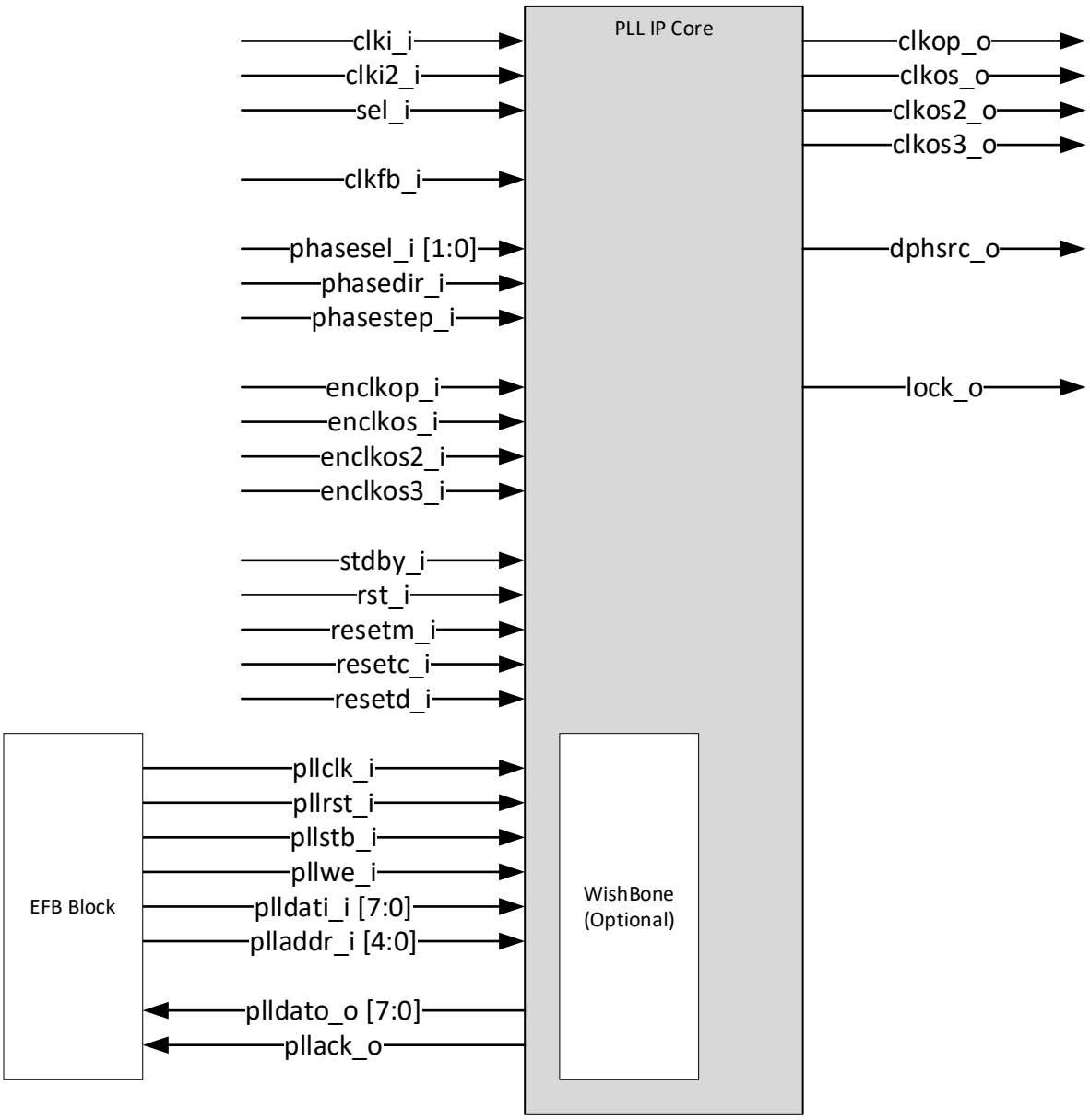

Figure 2.1. PLL Module Top Level Block Diagram

3. IP Parameter Description

The configurable attributes of the PLL Module are shown in the following tables. You can configure the IP by setting the attributes accordingly in the IP Catalog's Module/IP wizard of the Lattice Radiant software.

Wherever applicable, default values are in bold.

3.1. General

Table 3.1. General Attributes

Attribute	Selectable Values	Description
Configuration Mode	**Frequency** Divider	Determines the input type you should provide. • In Frequency mode, enter the desired CLKI and CLKOP frequencies • In Divider mode, enter the desired CLKI frequency and divider settings
VCO Frequency	—	• Displays the calculated VCO frequency based on selected value • Acceptable range: 200 MHz to 800 MHz
Estimate Bandwidth	—	• Displays the calculated bandwidth based on your selected value
Reference Clock (CLKI)		
Frequency (MHz)	7 MHz to 400 MHz	• Specifies the reference input clock frequency • Default is **100 MHz**

Divider Value	1 to 40	• Contains the reference input clock divider value
		  • In Divider Mode, this allows you to enter the value
		  • In Frequency Mode, the calculated value is displayed
		• Default: **1**
		• This value is used to divide upon reference clock frequency to generate the feedback source output frequency

Feedback		

Feedback Mode	**CLKOP**, CLKOS, CLKOS2, CLKOS3, INT_OP, INT_OS, INT_OS2, INT_OS3, UserClock	• Specifies which clock source used as the feedback path
		  • The selection adjusts based on the generated clock enablement
		  • INT_* option indicates use of primitive internal feedback loop path
		• When you select *UserClock* option, additional *clkfb_i* signal is exposed for connection

Feedback Divider Value	1 to 128	• Contains the value for the feedback loop divider value
		  • In Divider Mode, this allows you to enter the value
		  • In Frequency Mode, the calculated value is displayed
		• Default: **1**
		• This value is used to perform multiplication upon reference clock frequency generate the feedback source output frequency

Feedback Fractional-N Divider Enable	Checked **Unchecked**	Determines Fractional-N feature usage. • When checked, feedback divider includes the Fractional-N divider feature

Feedback Fractional-N Divider Value	0 to 65535	• Specifies the value used for the Fractional-N divider
		  • In Divider Mode, this allows you to enter the value
		  • In Frequency Mode, the calculated value is displayed
		• Default: **0**

Clock Output: [n] (n = CLKOP, CLKOS, CLKOS2, CLKOS3)		
[n]: Enable	Checked **Unchecked**	• Determines whether specific generated clock output usage • When checked, enables the generated clock output feature selection and the output signal ([n]_o) • This feature does not apply to CLKOP, which CLKOP is always enabled

Attribute	Selectable Values	Description
[n]: Bypass	Checked **Unchecked**	Determines input source for the generated output clock • When checked, uses the reference input clock • When unchecked, uses VCO output
[n]: Clock Divider Enable	Checked **Unchecked**	Determine whether to apply output division to generate the output clock • When checked, the output clock is divided based on the reference input clock • When unchecked, the output clock matches the reference input clock

[n]: Frequency Desired Value (MHz)	1.5625 MHz to 400 MHz	• Available in Frequency Mode. Allow you to enter the desired generated output clock frequency
		  • Supports minimum frequency of 0.0122 MHz by utilizing internal cascade feature
		  • Not applicable when Bypass feature is used
		• Default: **100 MHz**

[n]: Tolerance	**0.0**, 0.1, 0.2, 0.5, 1.0, 2.0, 5.0, 10.0	Used in Frequency Configuration Mode to specify the acceptance delta between desired frequency and actual frequency.

[n]: Divider Value	1 to 128	• Contains the divider value for the generated output clock
		  • In Divider Mode, this allow you enters the desired value
		  • In Frequency Mode, the calculated value is displayed (If Bypass and Clock Divider are enabled, you must enter value)
		• Default: **5**
		• This value is used to divide upon VCO frequency to generate the output frequency

[n]: Cascade Input Source	—	• Displays the generated output clock is used as the internal cascade source • Cascade mode is supported only in Frequency mode to achieve lower desired output frequency
[n]: Frequency Actual Value (MHz)	—	• Displays the actual generated output frequency based on your settings or per best achievable configuration
[n]: Static Phase Shift (Degrees)	**0**, 45, 90, 135, 180, 225, 270, 31	• Controls the phase shift of the generated output clock signal • This feature does not apply to generated output clock that is used as feedback source set in *Feedback Mode* option
[n]: Duty Trim Enable	Checked **Unchecked**	• Determines whether to enable duty trim feature • When checked, expose the trim feature and selection options • This option does not apply to CLKOS2 and CLKOS3

[n]: Duty Trim Options Mode	**Rising**, Falling	• When the *trimming feature* is enabled, controls which edge of the generated clock signal is trimmed
		  • Rising – Trim happens at the rising edge
		  • Falling – Trim happens at the falling edge
		• This option does not apply to CLKOS2 and CLKOS3

[n]: Duty Trim Options Delay Multiplier	**0**, 1, 2, 4	• When trimming feature is enabled, it controls the amount of time that is trimmed
		  • 0 – No Trim performed
		  • 1 – 70 ps trim on the selected edge
		  • 2 – 140 ps trim on the selected edge
		  • 4 – 280 ps trim on the selected edge
		• This option does not apply to CLKOS2 and CLKOS3

3.2. Optional Signal Control

Table 3.2 contains the selection which exposes one or group of signals. For the details on each signal usage and detail, refer to Signal Description section.

Table 3.2. Optional Signal Control

Attribute	Selectable Values	Description
Dynamic Phase Ports	Checked **Unchecked**	When checked, exposes the ports *phasedir_i*, *phasesel_i[1:0]*, *phasestep_i*, and dphsrc_o.
Clock Enable Ports	Checked **Unchecked**	When checked, exposes the ports *enclkop_i*, *enclkos_i*, *enclkos2_i*, and *enclkos3_i* based on the enable status for each output port.
Standby Ports	Checked **Unchecked**	When checked, exposes the port *stdby_i.*
Enable Clock Select	Checked **Unchecked**	When checked, exposes the ports *clki2_i* and *sel_i*.
PLL Reset Options		
Provide PLL Reset	Checked **Unchecked**	When checked, exposes the port *rst_i.*
Provide PLL M Reset	Checked **Unchecked**	When checked, exposes the port *resetm*_i.
PLL CLKOS2 Reset	Checked **Unchecked**	When checked, exposes the port *resetc_i*.
PLL CLKOS3 Reset	Checked **Unchecked**	When checked, exposes the port *resetd_i*.
Lock Settings		
Provide PLL Lock Signal	Checked **Unchecked**	When checked, exposes the signal *lock_o*.
PLL lock is Sticky	Checked **Unchecked**	• Available only when PLL lock signal is exposed • When checked, the lock signal remains asserted after achieving lock condition until PLL is reset • When unchecked, lock signal de-asserts when the lock condition lost is applied
WishBone Bus		
Provide Wishbone Ports (Requires Instantiation of EFB Block)	Checked **Unchecked**	When checked, exposes the ports *plladdr_i[4:0]*, *pllclk_i*, *plldati_i[7:0]*, *pllrst_i*, *pllstb_i*, *pllwe_i*, and *plldato_o[7:0]*.

4. Signal Description

This section describes the PLL Module ports, in which certain port exposure is controlled by the parameter mentioned in IP Parameter Description section.

4.1. Clock Interface

Table 4.1. Clock Ports

Port	Type	Description
clki_i clki2_i	Input	• These signals are the reference input clock • The signal frequency input must match the value set in the Reference Clock Frequency option in the General section.
sel_i	Input	This signal is used to select the current reference input clock. • 0 = use *clki_i* • 1 = use *clki2_i*
clkfb_i	Input	This signal is used for the user-provided feedback loop
clkop_o	Output	• This signal is the generated CLKOP output clock signal • The output frequency follows the Frequency Actual Value option in General section
clkos_o	Output	• This signal is the generated CLKOS output clock signal • The output frequency follows the Frequency Actual Value option in General section
clkos2_o	Output	• This signal is the generated CLKOS2 output clock signal • The output frequency follows the Frequency Actual Value option in General section
clkos3_o	Output	• This signal is the generated CLKOS3 output clock signal • The output frequency follows the Frequency Actual Value option in General section

4.2. Enable and Reset Interface

Table 4.2. Enable and Reset Ports

Port	Type	Description
enclkop_i	Input	Active high, asynchronous signal that performs clock gated for *clkop_o* output.
enclkos_i	Input	Active high, asynchronous signal that performs clock gated for *clkos_o* output.
enclkos2_i	Input	Active high, asynchronous signal that performs clock gated for *clkos2_o* output.
enclkos3_i	Input	Active high, asynchronous signal that performs clock gated for *clkos3_o* output.
resetc_i	Input	Active high, asynchronous signal that resets *clkos2_o* output when asserted
resetd_i	Input	Active high, asynchronous signal that resets *clkos3_o* output when asserted
resetm_i	Input	Active high, asynchronous signal that resets PLL including the M-divider when asserted
rst_i	Input	Active high, asynchronous signal that reset PLL except the M-divider when asserted

4.3. Control Interface

Table 4.3. Control Ports

Port	Type	Description
lock_o	Output	This signal indicates PLL lock status. • 0 = Not yet archive lock state or at lose lock state • 1 = Archive lock state
phasesel_i [1:0]	Input	This signal selects on which generated output signal the dynamic phase shift applies to: • 00 = Apply to *clkop_o* • 01 = Apply to *clkos_o* • 10 = Apply to *clkos2_o* • 11 = Apply to *clkos3_o*
phasedir_i	Input	This signal determines the dynamic phase shift direction: • 0 = Delay (Lagging) • 1 = Advance (Leading)
phasestep_i	Input	This signal determines when the Dynamic Phase Shift step takes effect.
dphsrc_o	Output	This signal indicates: • 0 = honoring wishbone interface operation • 1 = honoring Dynamic Phase Shift port (*phase*_i*) operation
stdby_i	Input	This signal puts the PLL into a low power standby mode: • 0 = Normal operating mode • 1 = Low power standby mode

Note: *phase*_i* refers to *phasel_i* , *phasedir_i,* and *phasestep_i*.

4.4. WishBone Interface

Table 4.4. WishBone Ports

Port	Type	Description
plladdr_i [4:0]	Input	This signal is the PLL WishBone interface address signal.
pllclk_i	Input	This signal is the PLL WishBone interface clock signal.
plldati_i [7:0]	Input	This signal is the PLL WishBone interface data input signal.
pllrst_i	Input	This active-high signal resets the WishBone interface. It does not reset the PLL CSR.
pllstb_i	Input	This active-high strobe signal indicates which WishBone interface signal is a valid signal.
pllwe_i	Input	This active-high signal is a write enable that indicates the read or write direction.
pllack_o	Output	This signal is the acknowledge signal of the PLL WishBone interface. High indicates the input is acknowledged.
plldato_o [7:0]	Output	This signal is the data output signal of the PLL WishBone interface.

5. Designing with the IP

This section provides information on how to generate the IP Core using the Lattice Radiant software and how to run simulation and synthesis. For more details on the Lattice Radiant software, refer to the Lattice Radiant Software User Guide.

Note: The screenshots provided are for reference only. Details may vary depending on the version of the IP or software being used. If there have been no significant changes to the GUI, a screenshot may reflect an earlier version of the IP.

5.1. Generating and Instantiating the IP

You can use the Lattice Radiant software to generate IP modules and integrate them into the device architecture. The steps below describe how to generate the PLL Module in the Lattice Radiant software.

To generate the PLL Module:

1. Create a new Lattice Radiant software project or open an existing project.
2. Click the **IP Catalog** button to view the **IP Catalog** pane.
3. On the **IP on Local** tab, double-click **PLL** under **IP, Architecture_Module** category. The **Module/IP Block Wizard** opens as shown in Figure 5.1. Enter values in the **Component name** and the **Create in** fields and click **Next**.

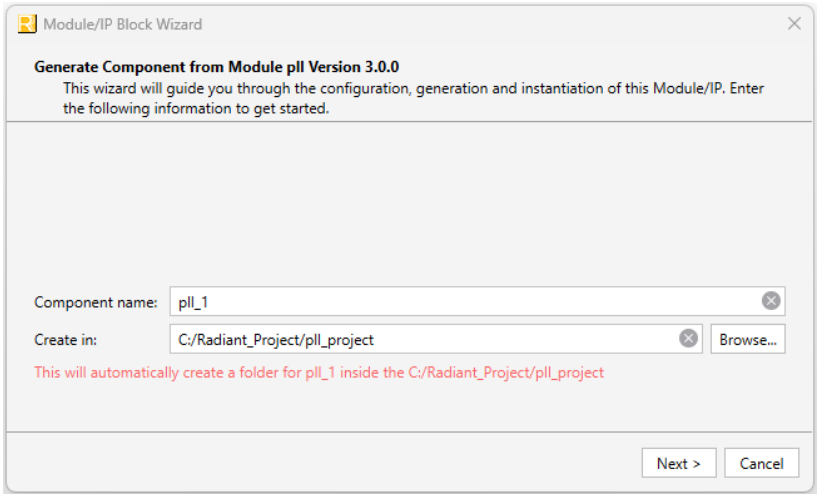

Figure 5.1. Module/IP Block Wizard

4. In the next **Module/IP Block Wizard** window, customize the selected PLL Module using drop-down lists and check boxes. Figure 5.2 shows an example configuration of the PLL Module. For details on the configuration options, refer to the IP Parameter Description section.

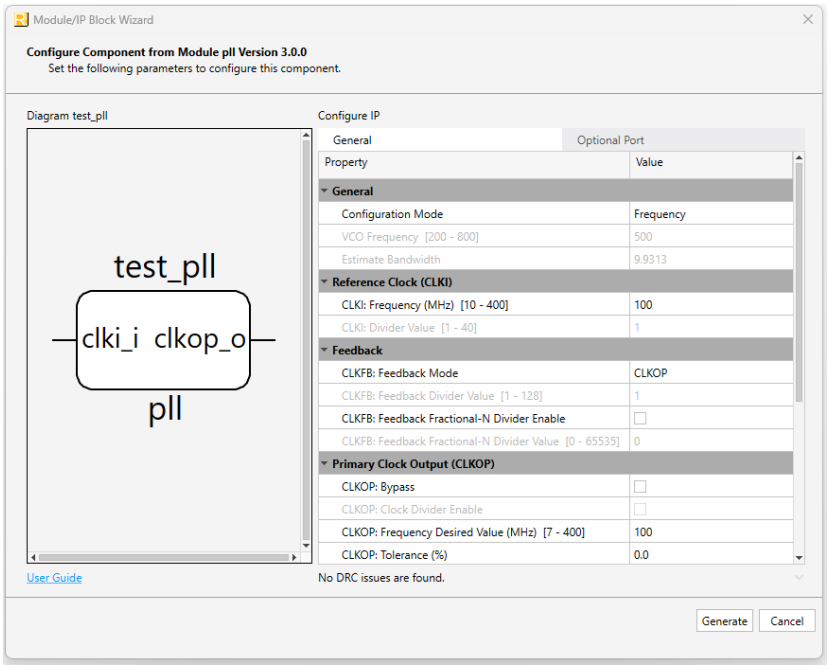

Figure 5.2. IP Configuration

5. Click **Generate**. The **Check Generated Result** dialog box opens, showing design block messages and results as shown in Figure 5.3.

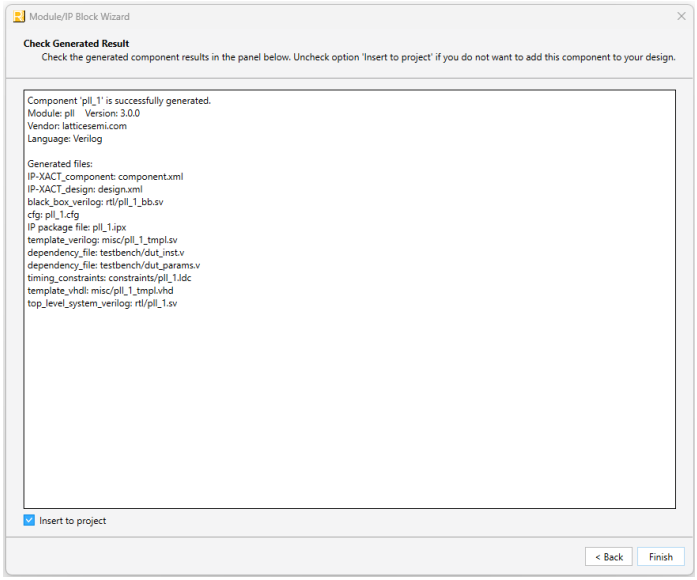

Figure 5.3. Check Generated Result

6. Click **Finish**. All the generated files are placed under the directory paths in the **Create in** and the **Component name** fields shown in Figure 5.1.

5.1.1. Generated Files and File Structure

The generated PLL Module package includes the closed-box (<Component name>_bb.v) and instance templates (<Component name>_tmpl.v/vhd) that can be used to instantiate the core in a top-level design. An example RTL top-level reference source file (<Component name>.v) that can be used as an instantiation template for the module is also provided. You may also use this top-level reference as the starting template for the top-level for their complete design. The generated files are listed in Table 5.1.

Table 5.1. Generated File List

Attribute	Description
<Component name>.ipx	Contains the information on the files associated to the generated IP.
<Component name>.cfg	Contains the parameter values used in IP configuration.
component.xml	Contains the ipxact: component information of the IP.
design.xml	Documents the configuration parameters of the IP in IP-XACT 2014 format.
rtl/<Component name>.sv	Provides an example RTL top file that instantiates the module.
rtl/<Component name>_bb.v	Provides the synthesis closed-box.
misc/<Component name>_tmpl.v misc /<Component name>_tmpl.vhd	Provide instance templates for the module.

5.2. Running Functional Simulation

You can run functional simulation after the IP is generated.

To run functional simulation:

1. Click the  button located on the **Toolbar** to initiate the **Simulation Wizard** shown in Figure 5.4.

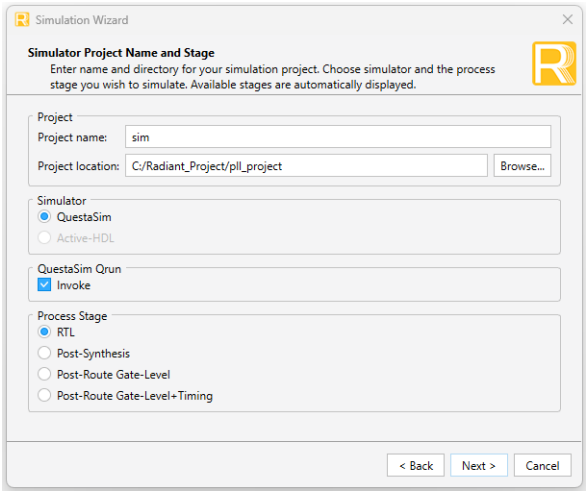

Figure 5.4. Simulation Wizard

2. Click **Next** to open the **Add and Reorder Source** window as shown in Figure 5.5.

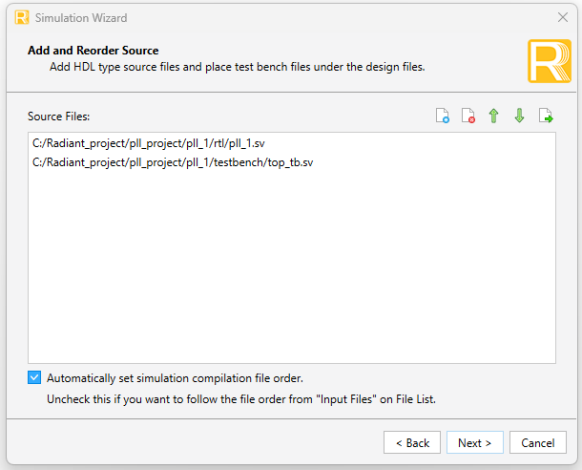

Figure 5.5. Add and Reorder Source

3. Click **Next**. The **Summary** window is shown.
4. Click **Finish** to run the simulation.

The waveform in Figure 5.6 shows an example simulation result.

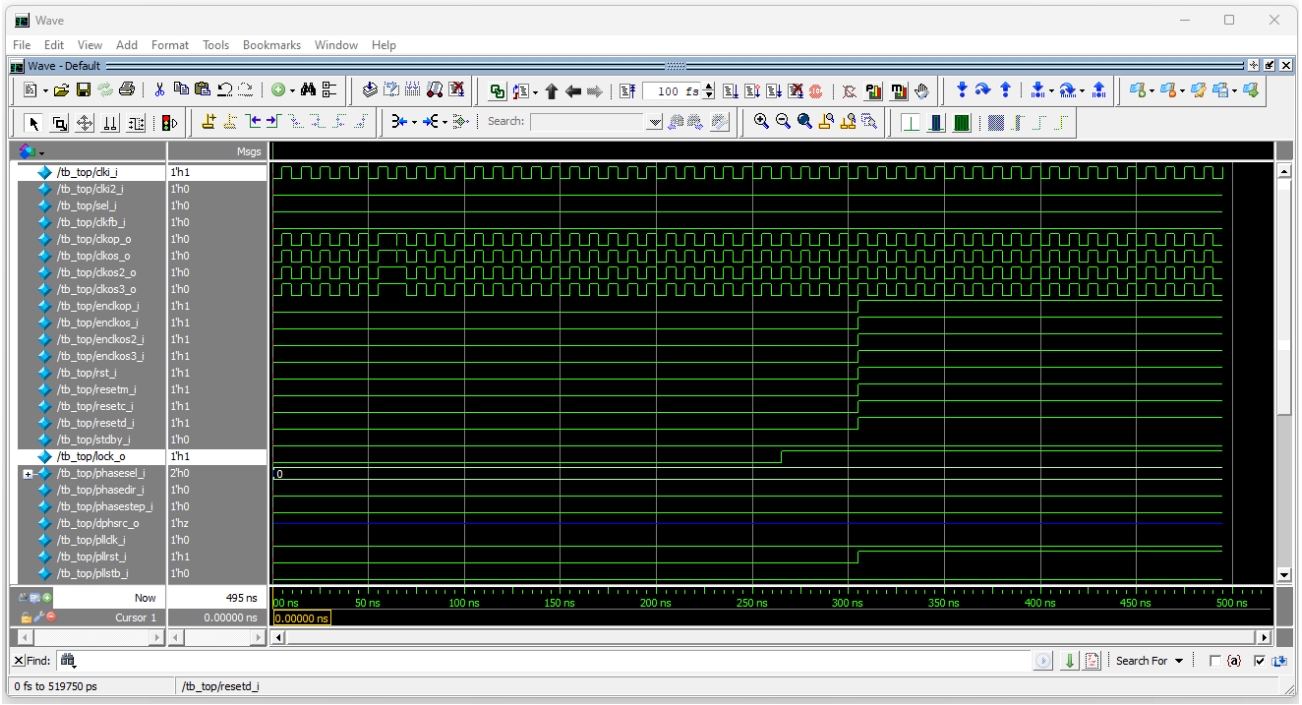

Figure 5.6. Simulation Waveform

5.2.1. Simulation Results

When the simulation is completed successfully, *Simulation Passed* string can be observed in the simulation transcript as shown in Figure 5.7

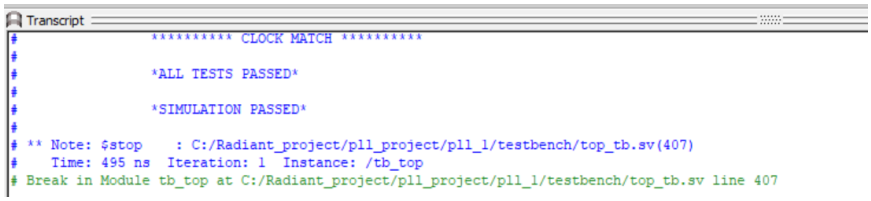

Figure 5.7. Simulation Complete Message

References

- MachXO4 PLL Module Release Notes (FPGA-RN-02316)
- Lattice Radiant Timing Constraints Methodology (FPGA-AN-02059)
- MachXO4 web page
- Lattice Radiant Software web page
- Lattice Solutions IP Cores web page
- Lattice Solutions Reference Designs web page
- Lattice Insights for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, please refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Note: In some instances, the IP may be updated without changes to the user guide. The user guide may reflect an earlier IP version but remains fully compatible with the later IP version. Refer to the IP Release Notes for the latest updates.

Revision 1.0, IP v3.0.1, December 2025

Section	Change Summary
All	Initial release.

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