Unified Interconnect IP

IP Version: v2.0.0

User Guide

FPGA-IPUG-02318-1.1

June 2026

Disclaimers

Lattice makes no warranty, representation, or guarantee regarding the accuracy of information contained in this document or the suitability of its products for any particular purpose. All information herein is provided AS IS, with all faults, and all associated risk is the responsibility entirely of the Buyer. The information provided herein is for informational purposes only and may contain technical inaccuracies or omissions, and may be otherwise rendered inaccurate for many reasons, and Lattice assumes no obligation to update or otherwise correct or revise this information. Products sold by Lattice have been subject to limited testing and it is the Buyer's responsibility to independently determine the suitability of any products and to test and verify the same. LATTICE PRODUCTS AND SERVICES ARE NOT DESIGNED, MANUFACTURED, OR TESTED FOR USE IN LIFE OR SAFETY CRITICAL SYSTEMS, HAZARDOUS ENVIRONMENTS, OR ANY OTHER ENVIRONMENTS REQUIRING FAIL-SAFE PERFORMANCE, INCLUDING ANY APPLICATION IN WHICH THE FAILURE OF THE PRODUCT OR SERVICE COULD LEAD TO DEATH, PERSONAL INJURY, SEVERE PROPERTY DAMAGE OR ENVIRONMENTAL HARM (COLLECTIVELY, "HIGH-RISK USES"). FURTHER, BUYER MUST TAKE PRUDENT STEPS TO PROTECT AGAINST PRODUCT AND SERVICE FAILURES, INCLUDING PROVIDING APPROPRIATE REDUNDANCIES, FAIL-SAFE FEATURES, AND/OR SHUT-DOWN MECHANISMS. LATTICE EXPRESSLY DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY OF FITNESS OF THE PRODUCTS OR SERVICES FOR HIGH-RISK USES. The information provided in this document is proprietary to Lattice Semiconductor, and Lattice reserves the right to make any changes to the information in this document or to any products at any time without notice.

Inclusive Language

This document was created consistent with Lattice Semiconductor’s inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice’s inclusive language FAQ 6878 for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Contents

Contents 3
Abbreviations in This Document 7
1. Introduction 8
1.1. Overview of the IP 8
1.2. Quick Facts 8
1.3. Features 8
1.4. Licensing and Ordering Information 9
1.5. Naming Conventions 9
1.5.1. Nomenclature 9
1.5.2. Signal Names 9
1.5.3. Attribute Names 9
2. Functional Description 10
2.1. IP Architecture Overview 10
2.1.1. Multi-protocol 10
2.1.2. Memory Map 12
2.1.3. AXI4 ID Width Requirement 14
2.1.4. Address Alignment Requirement 14
2.2. Clocking and Reset 15
2.2.1. Reset Overview 16
2.2.2. Without CDC 16
2.2.3. With CDC 16
2.3. External Manager Interface 17
2.4. External Subordinate Interface 17
2.5. Crossbar 18
2.5.1. Shared Address and Multiple Data Channels 18
2.5.2. Shared Address and Shared Data Channels 18
2.5.3. Address Phase Processing Unit 18
2.5.4. Single Slave per Active ID for AXI4 19
2.5.5. Transaction Acceptance Limit 19
2.5.6. Outstanding Transaction 19
2.6. Default Subordinate 19
2.7. Infrastructure Modules 20
2.7.1. Queue 20
2.7.2. Register Slice 20
2.7.3. Protocol Conversion Bridge 20
2.7.4. Error Case Examples during Protocol Conversion 23
3. IP Parameter Description 25
3.1. General 25
3.2. External Manager Settings 25
3.3. External Subordinate Settings 28
3.4. Advanced Settings 30
4. Signal Description 32
4.1. Clock and Reset 32
4.2. AXI4 33
4.2.1. AXI4 External Manager Interface 34
4.2.2. AXI4 External Subordinate Interface 35
4.3. AHB-Lite 37
4.3.1. AHB-Lite External Manager Interface 37
4.3.2. AHB-Lite External Subordinate Interface 38
4.4. APB 39
4.4.1. APB External Manager Interface 39
4.4.2. APB External Subordinate Interface 40

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

5. Example Design 41
6. Designing with the IP 42
6.1. Generating and Instantiating the IP 42
6.1.1. Generated Files and File Structure 44
6.2. Design Implementation 44
6.3. Timing Constraints 45
7. Design Considerations 48
7.1. Limitations 48
7.2. Exporting Manager and Subordinate Interfaces 48
7.3. Design Considerations for Throughput 49
7.3.1. Burst Transfer 49
7.3.2. AXI4 Pipelining Transfer 49
7.3.3. AXI4 Bottleneck Clearance 52
7.4. Design Considerations for Latency 53
7.4.1. Sub-IP Block Latency 53
7.5. Design Considerations for Resource Utilization 55
7.5.1. Exclude Internal Default Subordinate 55
7.5.2. Exclude Redundant AXI Interface Access Type 55
7.5.3. Exclude Redundant Crossbar Route 56
7.5.4. Secondary Interconnect 57
7.6. Design Considerations for Timing (f_{MAX}) 57
7.6.1. Enable Data Register Slice 57
7.6.2. Enable Crossbar Address Decode Pipestage 57
Appendix A. Resource Utilization 58
Maximize Performance Mode 58
Minimize Area Mode 68
CFG 1 Primary Crossbar AXI4 75
CFG 2 Primary Crossbar AHB-Lite 75
Appendix B. Determining the Secondary Protocol Interface Index 76
References 77
Technical Support Assistance 78
Revision History 79

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Figures

Figure 2.1. Lattice Unified Interconnect IP Block Diagram 10
Figure 2.2. Multi-protocol Base Structure 10
Figure 2.3. Primary IC with AXI4 Crossbar (Secondary ICs with AXI4-Lite, AHB-Lite, and APB Crossbars) 11
Figure 2.4. Primary IC with AHB-Lite Crossbar (Secondary ICs with AXI4-Lite and APB Crossbars) 12
Figure 2.5. Primary IC with APB Crossbar (No Secondary IC) 12
Figure 2.6. Base Address Alignment 12
Figure 2.7. Address Fragment Routed by Interconnect to Subordinate 13
Figure 2.8. Partially Unclaimed 1-KiB Block by Subordinate 13
Figure 2.9. Example ES AXI4 Width Requirement for Two EMs 14
Figure 2.10. Clock and Reset Domain Block Diagram without CDC 16
Figure 2.11. Clock and Reset Domain Block Diagram with CDC 17
Figure 2.12. Case 1 – AHB-Lite INCR<n> Burst Write to AXI4-Lite in Mixed-Protocol System with Write Response Error 21
Figure 2.13. Case 2 – AHB-Lite INCR<n> Burst Write to AXI4-Lite in Mixed-Protocol System with Write Response Error 21
Figure 2.14. AxPROT[1] through AXI4 Primary Crossbar 23
Figure 2.15. AxPROT[1] through AHB-Lite Primary Crossbar 23
Figure 2.16. AHB-Lite INCR<n> Burst Write to AHB-Lite in Mixed-Protocol System and ES Interface Early Termination after HRESP = ERROR 24
Figure 2.17. AHB-Lite INCR<n> Burst Read to AHB-Lite in Mixed-Protocol System and External Manager Early Termination after HRESP = ERROR 24
Figure 4.1. Clock and Reset Interface Diagram for CDC Enabled and Disabled 32
Figure 4.2. AXI4 Protocol Interface Diagram 33
Figure 4.3. AHB-Lite Protocol Interface Diagram 37
Figure 4.4. APB Protocol Interface Diagram 39
Figure 6.1. Module/IP Block Wizard 42
Figure 6.2. IP Configuration 43
Figure 6.3. Check Generated Result 43
Figure 7.1. Write Transactions for One Active EM with awlen ≥ 2 49
Figure 7.2. Write Transactions for Four Active EMs with awlen = 2 50
Figure 7.3. Write Transactions for Four Active EMs with awlen ≥ 3 50
Figure 7.4. Read Transactions for One Active EM with Request Interval < arlen 50
Figure 7.5. Read Transactions for One Active EM with arlen ≤ Request Interval 51
Figure 7.6. Read Transactions for Four Active EMs with arlen = 2 51
Figure 7.7. Read Transactions for Four Active EMs with arlen ≥ 3 52

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Tables

Table 1.1. Summary of the Unified Interconnect IP 8
Table 2.1. Multi-protocol Configurations 11
Table 2.2. Maximum Fragment Count for External Subordinate Connected Directly to Primary IC 14
Table 2.3. Maximum Fragment Count for External Subordinate Connected through Secondary IC 14
Table 2.4. Clocking and Reset Domain Summary 15
Table 2.5. AHB-Lite HPROT to or from AXI4 AxPROT and AxCACHE Mappings 22
Table 3.1. General Attributes 25
Table 3.2. External Manager Settings Attributes 25
Table 3.3. External Subordinate Settings Attributes 28
Table 3.4. Advanced Settings Attributes 30
Table 4.1. AXI4 External Manager Interface Ports 34
Table 4.2. AXI4 External Subordinate Interface Ports 35
Table 4.3. AHB-Lite External Manager Interface Ports 37
Table 4.4. AHB-Lite External Subordinate Interface Ports 38
Table 4.5. APB External Manager Interface Ports 39
Table 4.6. APB External Subordinate Interface Ports 40
Table 6.1. Generated File List 44
Table 7.1. Minimum AXI4 Crossbar Latency 53
Table 7.2. Minimum AHB-Lite Crossbar Latency 53
Table 7.3. Minimum APB Crossbar Latency 53
Table 7.4. Additional Latency Introduced by Optional Couplers at EM or ES AXI4 Interface with Primary Crossbar = AXI4 54
Table 7.5. Additional Latency Introduced by Optional Couplers at EM or ES AHB-Lite Interface with Primary Crossbar = AHB-Lite or APB Interface with Primary Crossbar = APB 54
Table 7.6. Additional Latency Introduced by Optional Couplers at EM or ES Interface for Protocol Conversion 54
Table 7.7. Default Subordinate Configuration 55
Table 7.8. Access Type Configuration 55
Table 7.9. External Manager to External Subordinate Connectivity Settings 56
Table 7.10. LUT4 MUX Groupings 56
Table 7.11. Estimated Savings in LUT4 Resource Utilization 56
Table A.1. Resource Utilization and f_{MAX} for 64-bit Data Width in Maximize Performance Mode (4 EMs and 4 ESs) 58
Table A.2. Resource Utilization and f_{MAX} for 64-bit Data Width in Maximize Performance Mode (8 EMs and 8 ESs) 58
Table A.3. Resource Utilization for 32-bit Data Width without CDC in Maximize Performance Mode 58
Table A.4. Resource Utilization for 64-bit Data Width without CDC in Maximize Performance Mode 61
Table A.5. Resource Utilization for 128-bit Data Width without CDC in Maximize Performance Mode 65
Table A.6. Resource Utilization for 32-bit Data Width with CDC in Maximize Performance Mode 68
Table A.7. Resource Utilization for 32-bit Data Width without CDC in Minimize Area Mode 68
Table A.8. Resource Utilization for 64-bit Data Width without CDC in Minimize Area Mode 71
Table A.9. Resource Utilization for 32-bit Data Width with CDC in Minimize Area Mode 74
Table A.10. Resource Utilization for CFG 1 Primary Crossbar AXI4 75
Table A.11. Resource Utilization for CFG 2 Primary Crossbar AHB-Lite 75

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviation	Definition
AHB	Advanced High-Performance Bus
AHB-Lite	Advanced High-Performance Bus Lite
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
AR	Read Address Channel
AW	Write Address Channel
AXI4	Advanced eXtensible Interface 4
AXI4-Lite	Advanced eXtensible Interface 4 Lite
CDC	Clock Domain Crossing
CFG	Configuration
CONV	Protocol Conversion
CPU	Central Processing Unit
DMA	Direct Memory Access
DWC	Data Width Conversion
EBR	Embedded Block RAM
EM	External Manager
ES	External Subordinate
FIFO	First In First Out
FPGA	Field Programmable Gate Array
FWFT	First Word Fall Through
GUI	Graphical User Interface
HDL	Hardware Description Language
IC	Interconnect
ID	Identification
IP	Intellectual Property
LUT	Look-Up Table
MC	Memory Controller
MI	Manager Interface
MUX	Multiplexer
RAM	Random Access Memory
RDATA	Read Data Channel
RO	Read Only
RTL	Register Transfer Level
SAMD	Shared Address and Multiple Data Channels
SASD	Shared Address and Shared Data Channels
SI	Subordinate Interface
SoC	System On Chip
WDATA	Write Data Channel
WO	Write Only
WR	Write Read
XB	Crossbar

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

1. Introduction

This document provides information on the Unified Interconnect IP, essential for IP/system development, verification, integration, testing, and validation. In general, this document covers design specifications from RTL to IP packaging and details the procedures for IP generation and integration.

1.1. Overview of the IP

The unified interconnect is a high-performance and low-latency interconnect fabric for AXI4-, AXI4-Lite-, AHB-Lite-, and APB-based systems. Any AXI4-, AXI4-Lite-, AHB-Lite-, or APB-compliant IP can be integrated into the system. The IP connects one or more memory-mapped *manager* devices to one or more memory-mapped *subordinate* devices and supports optional clock domain crossing (CDC) between interfaces. Each manager can access different subordinates in parallel. When more than one manager tries to reach the same subordinate, access is arbitrated.

1.2. Quick Facts

Table 1.1. Summary of the Unified Interconnect IP

IP Requirements	Supported Devices	CrossLink™-NX, CertusPro™-NX, Certus™-NX, MachXO5™-NX, Lattice Avant™, Certus-N2
	IP Changes[1]	Refer to the Unified Interconnect IP Release Notes (FPGA-RN-02107).
Resource Utilization	Supported User Interface	Advanced eXtensible Interface 4 (AXI4), AXI4-Lite, Advanced High-Performance Bus Lite (AHB-Lite), Advanced Peripheral Bus (APB)
	Resources	Refer to Appendix A. Resource Utilization.
Design Tool Support	Lattice Implementation	IP Core v2.0.0 – Lattice Radiant™ Software 2026.1 Lattice Propel™ Design Environment 2026.1
	Synthesis	Synopsys® Synplify Pro® for Lattice, Lattice Synthesis Engine
	Simulation	Refer to the Lattice Radiant Software User Guide for the list of supported simulators.

Note:

1. In some instances, the IP may be updated without changes to the user guide. This user guide may reflect an earlier IP version but remains fully compatible with the later IP version. Refer to the IP Release Notes for the latest updates.

1.3. Features

Key features of the Unified Interconnect IP include:

- Each external manager (EM) or external subordinate (ES) can be configured to support various protocols.
  - AMBA 4 AXI4
  - AMBA 4 AXI4-Lite
  - AMBA 3 AHB-Lite
  - AMBA 3 APB

  Notes:
  - ARM Ltd. *AMBA AXI and ACE Protocol Specification,* Issue E, ARM IHI 0022E, February 2013. This specification defines the AMBA AXI4 and AXI4-Lite protocols supported by the Unified Interconnect IP.
  - ARM Ltd. *AMBA 3 AHB-Lite Protocol Specification*, Issue A, ARM IHI 0033A, June 2006. This specification defines the AMBA 3 AHB-Lite protocol supported by the Unified Interconnect IP.
  - ARM Ltd. *AMBA 3 APB Protocol Specification*, Issue B, ARM IHI 0024B, August 2004. This specification defines the AMBA 3 APB protocol supported by the Unified Interconnect IP.
- Configurable interface data widths:
  - AXI4: 8, 16, 32, 64, 128, 256, 512, or 1,024 bits
  - AXI4-Lite: 32 or 64 bits
  - AHB-Lite: 8, 16, 32, 64, 128, 256, 512, or 1,024 bits

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

    - APB: 8, 16, or 32 bits
- Address widths:
    - AXI4: Up to 64 bits (11 to 64)
    - AXI4-Lite: Up to 64 bits (11 to 64)
    - AHB-Lite: Up to 32 bits (11 to 32)
    - APB: Up to 32 bits (11 to 32)
- Supports AXI4 with the following characteristics:
    - User width: Up to 128 bits
    - ID width: Up to 6 bits
    - INCR and FIXED bursts.
        - Supports three types of responses:
            - AXI OKAY
            - AXI DECERR – when undefined external subordinate address region is accessed.
            - AXI SLVERR – for pass through from the external subordinate.
- Supports reduced resource optimization, including:
    - Read-only manager and subordinate
    - Write-only manager and subordinate
    - Crossbar paths restriction with configured connectivity map
- Supports up to 16 external managers and/or 16 external subordinates.
- Options to enable streaming queue, first in first out (FIFO) with CDC, and FIFO without CDC for each EM or ES port.
- Supports fragmented address space of up to 16 fragments per external subordinate.
- Selectable arbitration scheme:
    - Round robin (default)
    - Strict priority (fixed priority)

1.4. Licensing and Ordering Information

The Unified Interconnect IP is provided at no additional cost with the Lattice Radiant software and Lattice Propel design environment.

1.5. Naming Conventions

1.5.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.5.2. Signal Names

Signal names that end with:

- *_n* are active low signals (asserted when value is logic 0)
- *_i* are input signals
- *_o* are output signals

1.5.3. Attribute Names

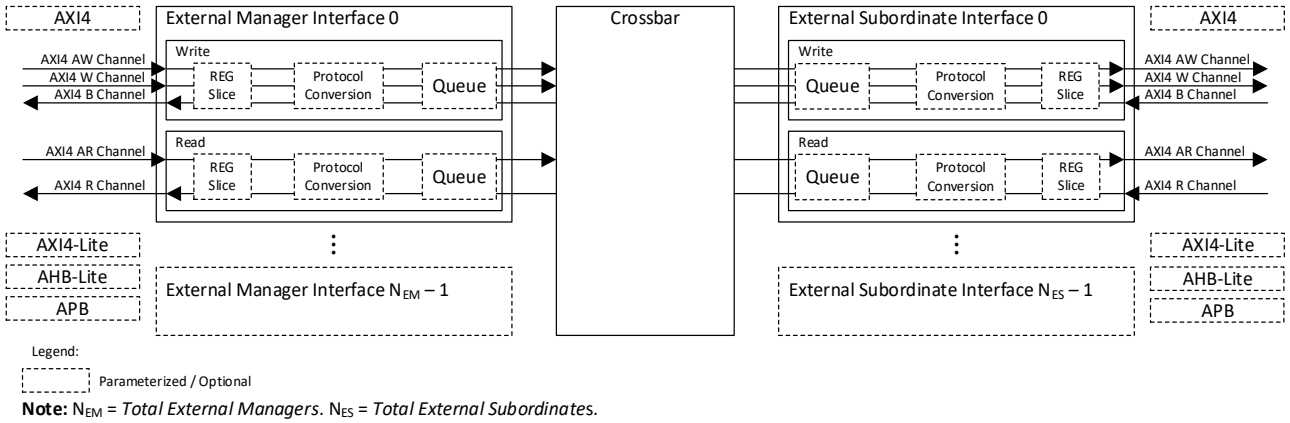
Attribute names in this document are formatted in title case and italicized (*Attribute Name*).

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

2. Functional Description

2.1. IP Architecture Overview

The Unified Interconnect IP allows up to N_{EM} external manager devices to connect to N_{ES} external subordinate devices, subject to constraints of the supported protocols. The crossbar arbitrates and routes resource sharing.



Note: N_{EM} = *Total External Managers*. N_{ES} = *Total External Subordinates*.

Figure 2.1. Lattice Unified Interconnect IP Block Diagram

The Unified Interconnect IP includes the following modules:

- External Manager (EM) Interface
- External Subordinate (ES) Interface
- Crossbar (XB)

2.1.1. Multi-protocol

2.1.1.1. Base Structure

The following figure shows the multi-protocol base structure.

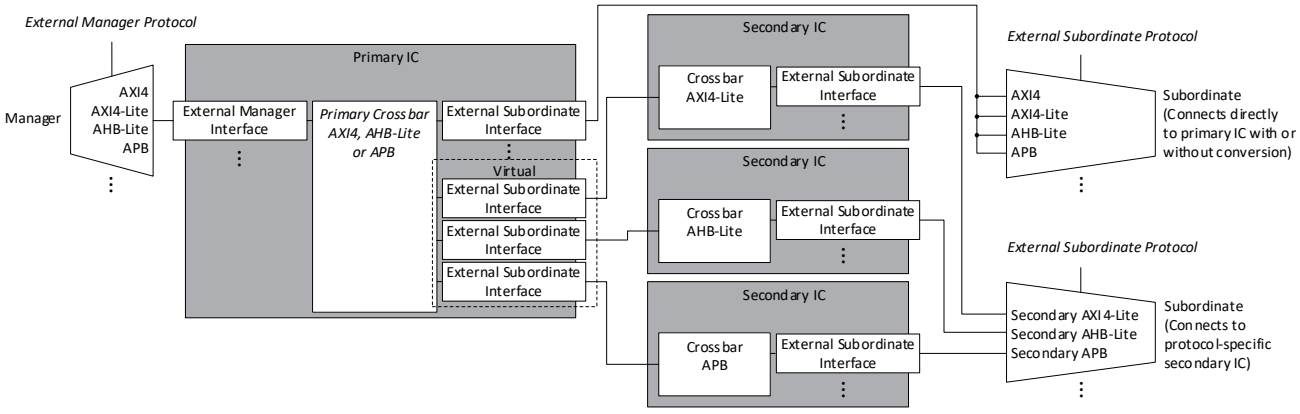


Figure 2.2. Multi-protocol Base Structure

This structure supports the following:

- EM protocol types
  - AXI4
  - AXI4-Lite
  - AHB-Lite

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

- APB (only when all EMs and ESs are configured exclusively for APB)

- ES protocol types
  - Direct connection to primary crossbar with or without protocol conversion
    - AXI4
    - AXI4-Lite
    - AHB-Lite
    - APB
  - Connection through protocol-specific secondary interconnect (IC)
    - Secondary AXI4-Lite
    - Secondary AHB-Lite
    - Secondary APB
- Primary IC multi-protocol conversion
  - AXI4 or AXI4-Lite to AHB-Lite
  - AXI4 or AXI4-Lite to APB
  - AHB-Lite to AXI4 or AXI4-Lite
  - AHB-Lite to APB

  Note: Settings are automatically applied based on the EM or ES protocol type.
- Secondary IC grouping based on shared protocol type, clock domain, and reset domain
  - Only one secondary IC per protocol type is supported. Refer to the Configuration section for configuration (CFG) grouping examples and the Secondary Interconnect section for usage recommendations.

2.1.1.2. Configuration

Table 2.1 outlines the three main multi-protocol configurations available.
Note: A virtual ES port is a primary IC ES port that connects to a secondary IC.

Table 2.1. Multi-protocol Configurations

CFG	Condition	Primary IC Protocol (Primary Crossbar)	Secondary IC Protocol (Secondary Crossbar)
1	Any EM protocol type = AXI4 (including AXI4-Lite) OR Any ES protocol type = AXI4 (excluding AXI4-Lite)	AXI4	AXI4-Lite, AHB-Lite, APB
2	Not CFG 1 AND Any EM protocol type = AHB-Lite	AHB-Lite	AXI4-Lite, APB
3	All EM protocol type = APB AND All ES protocol type = APB	APB	—

CFG1 Example: Primary Crossbar AXI4

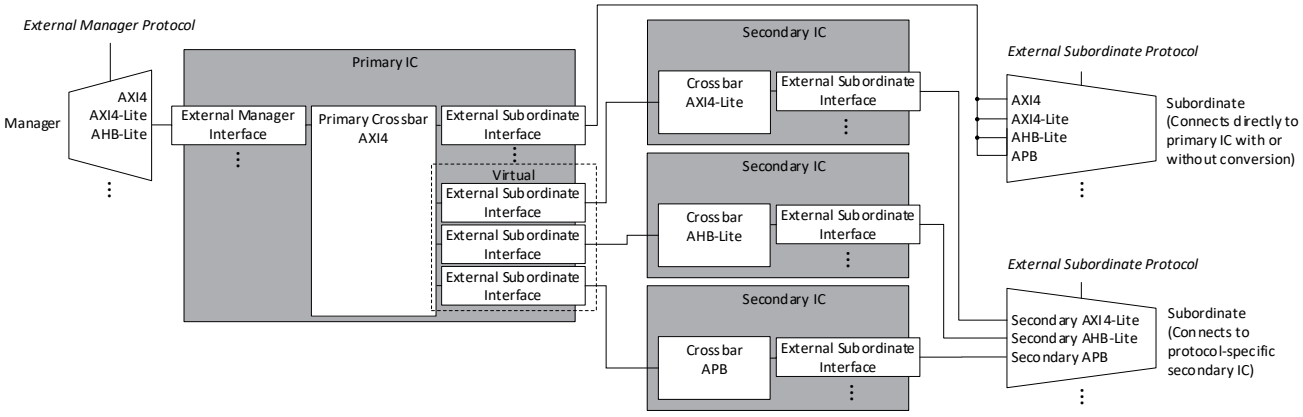


Figure 2.3. Primary IC with AXI4 Crossbar (Secondary ICs with AXI4-Lite, AHB-Lite, and APB Crossbars)

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

CFG2 Example: Primary Crossbar AHB-Lite

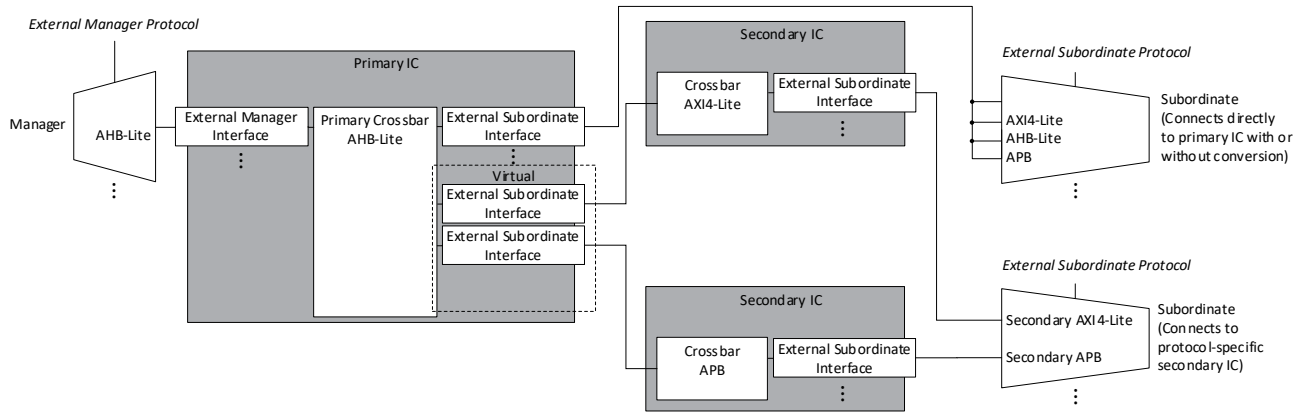


Figure 2.4. Primary IC with AHB-Lite Crossbar (Secondary ICs with AXI4-Lite and APB Crossbars)

CFG3 Example: Primary Crossbar APB

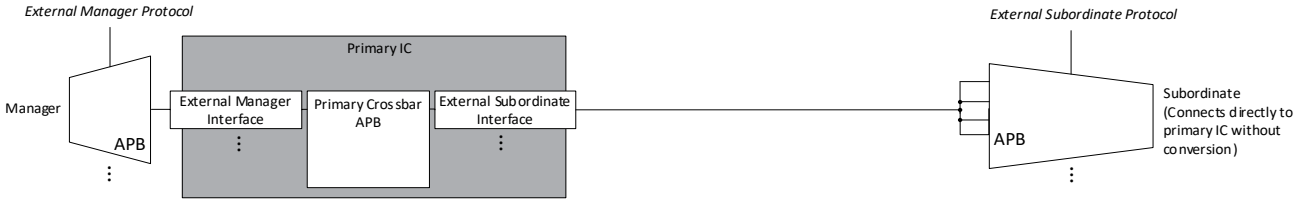


Figure 2.5. Primary IC with APB Crossbar (No Secondary IC)

2.1.2. Memory Map

2.1.2.1. Base Address and End Address Limit Requirements

By default, the AXI4 crossbar decodes the 4 KiB-aligned base address for each fragment. However, it allows 1 KiB-aligned base addresses when any ES protocol type is AHB-Lite, APB, secondary AHB-Lite, or secondary APB. The AHB-Lite and APB crossbars enforce a 1 KiB-aligned base address.

Note: The AXI4 manager must never initiate a burst transfer that crosses the 1-KiB boundary when accessing AHB-Lite or APB subordinates.

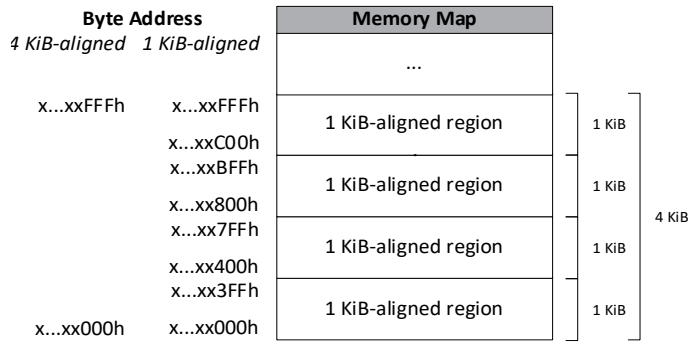
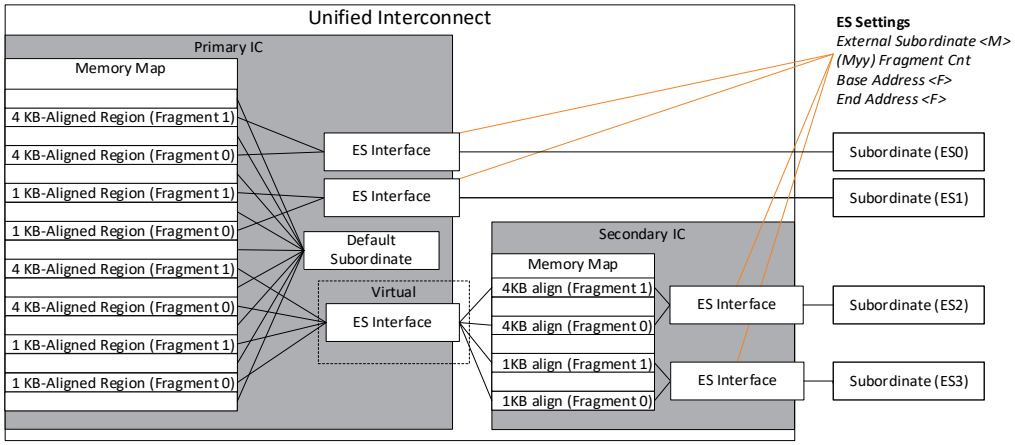


Figure 2.6. Base Address Alignment

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

2.1.2.2. User Configuration

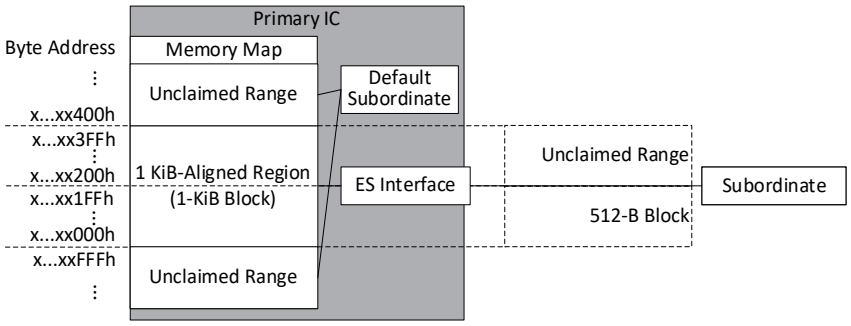
You must configure the base and end addresses for each address fragment that the interconnect routes to a subordinate. These addresses are applied to both the primary and secondary crossbars automatically.



Note: All unclaimed ranges are handled by the default subordinate.

Figure 2.7. Address Fragment Routed by Interconnect to Subordinate

The interconnect does not perform a full address decode. Instead, it routes based on 1 KiB- or 4 KiB-aligned blocks. The address range of any unclaimed 1-KiB or 4-KiB block is handled by the default subordinate in the primary interconnect.



Note: The unclaimed range within the 1-KiB block is not routed to the default subordinate.

Figure 2.8. Partially Unclaimed 1-KiB Block by Subordinate

Subordinates must also respond based on the entire 1-KiB or 4-KiB block. If the subordinate is unable to claim the full 1-KiB or 4-KiB block, the unclaimed range within this block is not routed to the default subordinate. Therefore, no response is returned to the manager.

Only the default subordinate in the primary IC can claim invalid address ranges. There is no default subordinate in the secondary IC.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

2.1.2.3. Maximum Fragment

Table 2.2 and Table 2.3 summarize the maximum fragment count permitted for the ES.

Table 2.2. Maximum Fragment Count for External Subordinate Connected Directly to Primary IC

ES Protocol Type	Maximum Fragment Count
AXI4	16 per ES
AHB-Lite	16 per ES
APB	1 per ES

Table 2.3. Maximum Fragment Count for External Subordinate Connected through Secondary IC

ES Protocol Type	Maximum Fragment Count
Secondary AXI4-Lite	16 across all secondary AXI4-Lite subordinates
Secondary AHB-Lite	16 across all secondary AHB-Lite subordinates
Secondary APB	1 per ES

2.1.3. AXI4 ID Width Requirement

The AXI4 ID width requirement only applies to EM and ES with the AXI4 protocol type. This excludes the AXI4-Lite and secondary AXI4-Lite protocol types. The ES must be configured to support an AXI ID width (AR ID or AW ID) that meets the following condition:

$$AXI\ ID\ Width \geq Maximum\ EM\ AXI\ ID\ Width + \begin{cases} \lceil \log_2(N_{EM}) \rceil, & if\ N_{EM} > 1 \\ 1, & if\ N_{EM} = 1 \end{cases}$$

The following figure shows an example of determining the AXI4 width requirement.

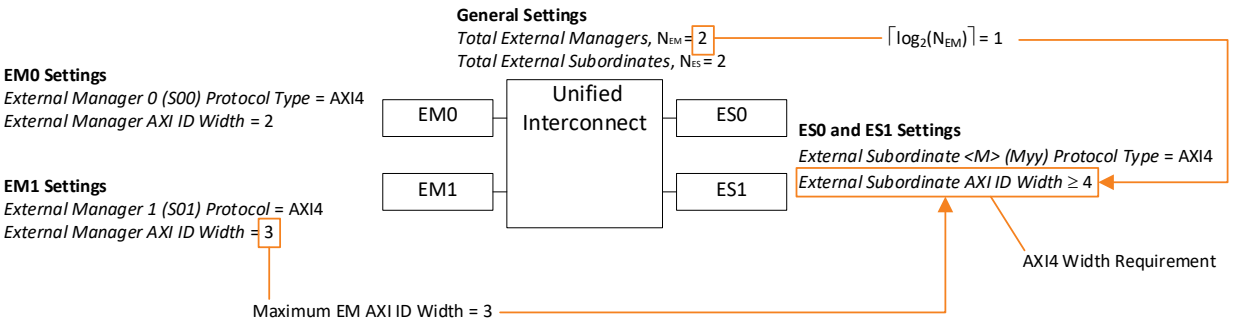


Figure 2.9. Example ES AXI4 Width Requirement for Two EMs

2.1.4. Address Alignment Requirement

The following are the address alignment requirements:

- The AXI4 manager must issue access to AHB-Lite or APB subordinates using addresses aligned to the transfer size. Otherwise, the following occurs:
  - Unaligned access from AXI4 to AHB-Lite is rejected and a SLVERR response is returned.
  - Unaligned access from AXI4 to APB is passed through without modification.
- All AHB-Lite access must be aligned to the transfer size.
- The AXI4 manager is still permitted to access an AXI4 subordinate using addresses that are not aligned to the transfer size.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

2.2. Clocking and Reset

Table 2.4 summarizes the clock and reset domain according to interface and CDC enablement.

Table 2.4. Clocking and Reset Domain Summary

Module	Protocol Selection	CDC	Clock / Reset[1]	Note
External Manager Interface	AXI4, AXI4-Lite, AHB-Lite, APB	ENABLE	Sxx_clk_i / Sxx_resetn_i	CDC enables the EM interface to operate in the specific clock (Sxx_aclk_i) and reset (Sxx_aresetn_i) domain of the port.
	AXI4, AXI4-Lite, AHB-Lite, APB	DISABLE	clk_i / resetn_i	Without CDC, the EM interface operates in the primary interconnect clock (clk_i) and reset (resetn_i) domain.
External Subordinate Interface	AXI4, AXI4-Lite, AHB-Lite, APB	ENABLE	Myy_clk_i / Myy_resetn_i	CDC enables the ES interface to operate in the specific clock (Myy_aclk_i) and reset (Myy_aresetn_i) domain of the port.
	AXI4, AXI4-Lite, AHB-Lite, APB	DISABLE	clk_i / resetn_i	Without CDC, the ES interface operates in the primary interconnect clock (clk_i) and reset (resetn_i) domain.
	Secondary AXI4-Lite	Dependent on AXI4-Lite Secondary IC	Dependent on AXI4-Lite Secondary IC	All ESs with *Secondary AXI4-Lite* selected as the ES protocol type must operate in the same domain.
	Secondary AHB-Lite	Dependent on AHB-Lite Secondary IC	Dependent on AHB-Lite Secondary IC	All ESs with *Secondary AHB-Lite* selected as the ES protocol type must operate in the same domain.
	Secondary APB	Dependent on APB Secondary IC	Dependent on APB Secondary IC	All ESs with *Secondary APB* selected as the ES protocol type must operate in the same domain.
AXI4-Lite Secondary IC	AXI4-Lite	ENABLE	axil_aclk_i / axil_aresetn_i	With CDC, the AXI4-Lite Secondary IC operates in a specific clock (axil_aclk_i) and reset (axil_aresetn_i) domain. All ESs with *Secondary AXI4-Lite* selected as the ES protocol type operate in the same domain.
	AXI4-Lite	DISABLE	clk_i / resetn_i	Without CDC, the AXI4-Lite Secondary IC operates in the primary interconnect clock (clk_i) and reset (resetn_i) domain. All ESs with *Secondary AXI4-Lite* selected as the ES protocol type operate in the same domain.
AHB-Lite Secondary IC	AHB-Lite	ENABLE	AHB-Lite_hclk_i / AHB-Lite_hresetn_i	With CDC, the AHB-Lite Secondary IC operates in specific clock (AHB-Lite_hclk_i) and reset (AHB-Lite_hresetn_i) domain. All ESs with *Secondary AHB-Lite* selected as the ES protocol type operate in the same domain.
	AHB-Lite	DISABLE	clk_i / resetn_i	Without CDC, the AHB-Lite Secondary IC operates in the primary interconnect clock (clk_i) and reset (resetn_i) domain. All ESs with *Secondary AHB-Lite* selected as the ES protocol type operate in the same domain.
APB Secondary IC	APB	ENABLE	apb_pclk_i / apb_presetn_i	With CDC, the APB Secondary IC operates in specific clock (apb_pclk_i) and reset (apb_presetn_i) domain. All ESs with *Secondary APB* selected as the ES protocol type operate in the same domain.
	APB	DISABLE	clk_i / resetn_i	Without CDC, the APB Secondary IC operates in the primary interconnect clock (clk_i) and reset (resetn_i) domain. All ESs with *Secondary APB* selected as the ES protocol type operate in the same domain.

Note:

1. clk_i, resetn_i, Sxx_clk_i, Sxx_resetn_i, Myy_clk_i, and Myy_resetn_i map to axi_aclk_i, axi_aresetn_i, Sxx_aclk_i, Sxx_aresetn_i, Myy_aclk_i, and Myy_aresetn_i, respectively, in IP v1.0.0.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

2.2.1. Reset Overview

The following are the interconnect reset requirements and limitations:

- When the primary *resetn_i signal asserts, the entire interconnect logic must be reset, regardless of CDC enablement in any EM or ES interface.
- Partial reset is not supported. When any EM or ES interface is reset, all EM and ES interfaces must assert their corresponding *resetn_i signals.
- The interconnect de-asserts all valid and ready outputs shortly after the *resetn_i signal asserts asynchronously.
- The assertion period of each *resetn_i signal must overlap across all relevant domains. It is recommended that each *resetn_i signal remains asserted for at least 20 clock cycles to ensure reliable reset synchronization.
- All *resetn_i signals do not need to be de-asserted in the same clock cycle. However, *resetn_i signals must be de-asserted synchronously with their corresponding EM or ES clock domains.

2.2.2. Without CDC

The following figure shows the clock and reset domain block diagram without CDC. All EMs and ESs operate in the same clock and reset domain.

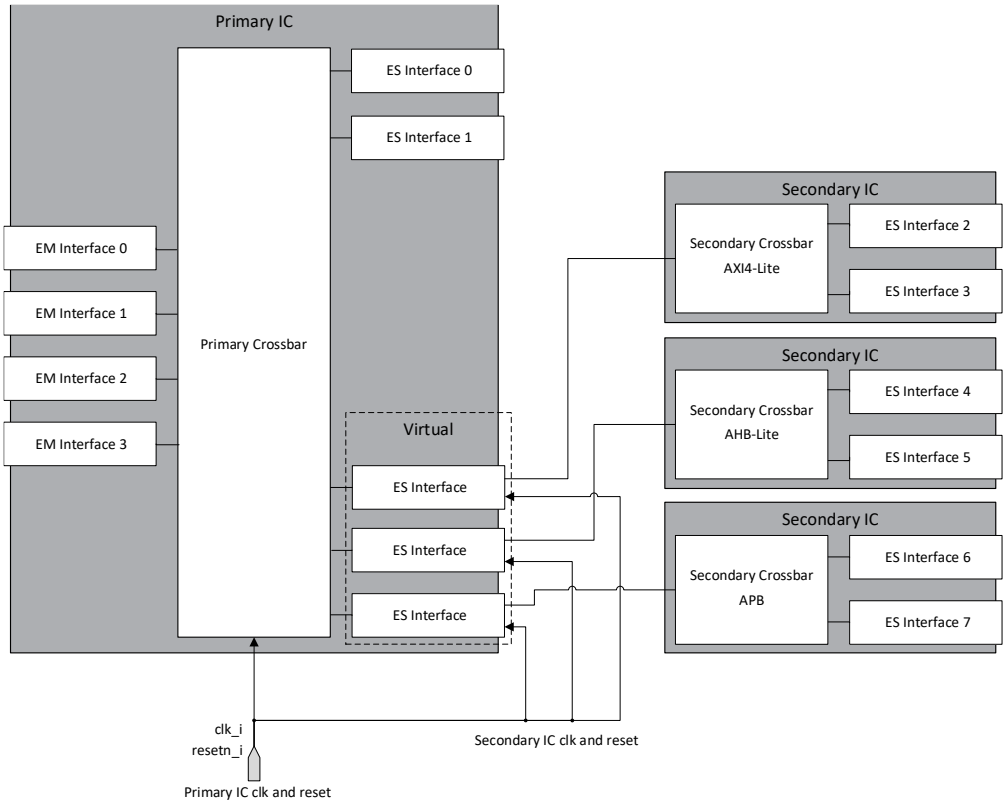


Figure 2.10. Clock and Reset Domain Block Diagram without CDC

2.2.3. With CDC

The following figure shows the clock and reset domain block diagram with CDC. All ESs with the same secondary protocol type operate in the same clock and reset domain:

- Secondary AXI4-Lite: ES operates in the axil_aclk_i and axil_aresetn_i domain.
- Secondary AHB-Lite: ES operates in the ahbl_hclk_i and ahbl_hresetn_i domain.
- Secondary APB: ES operates in the apb_pclk_i and apb_presetn_i domain.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

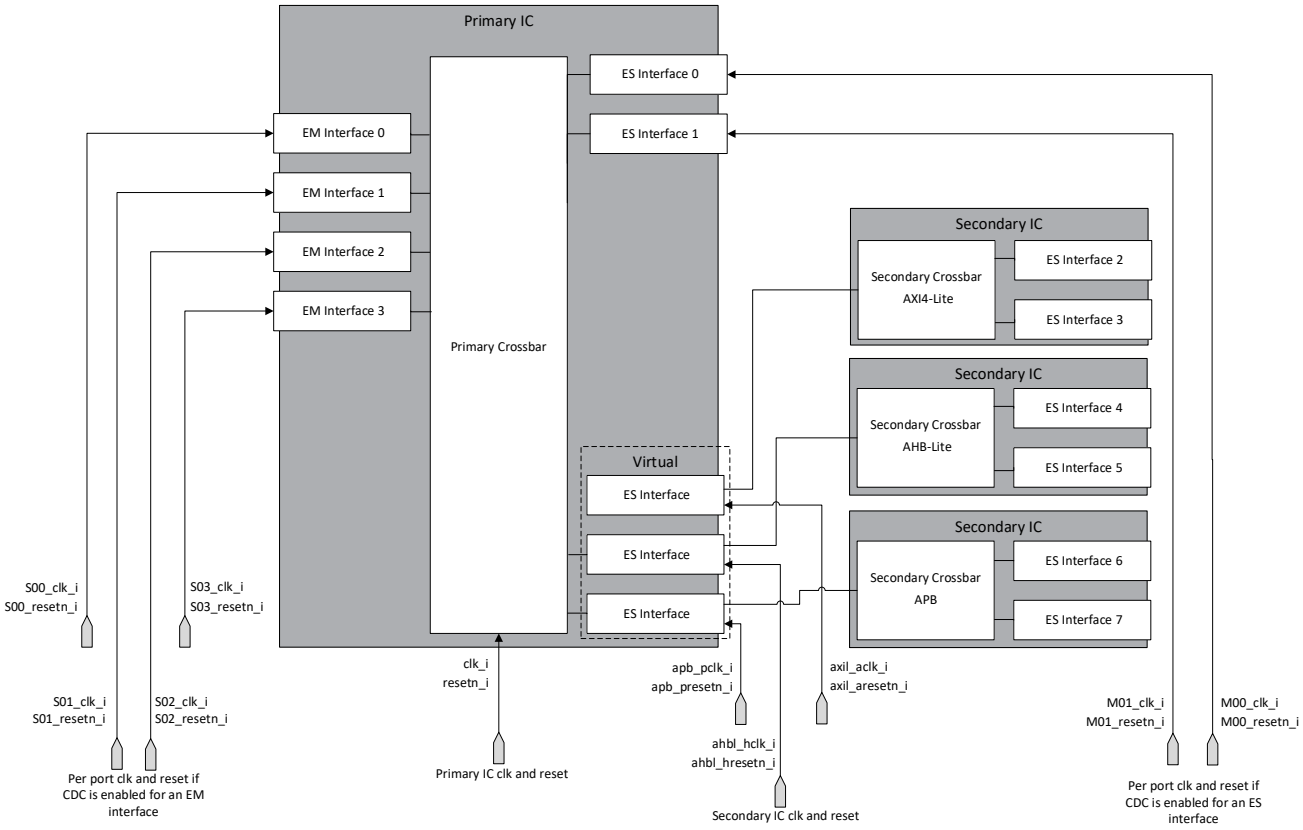


Figure 2.11. Clock and Reset Domain Block Diagram with CDC

2.3. External Manager Interface

The external manager interface operates in the same clock and reset domain as the external manager. It connects to the external manager through protocol-specific interfaces. The following are characteristics of the EM interface:

- Supports CDC.
- Supports register slice.
- Supports protocol conversion between AXI4, AXI4-Lite, AHB-Lite, and APB.
- Supports configurable read ACCEPTANCE_LIMIT and write ACCEPTANCE_LIMIT to limit the number of outstanding transactions from each external manager.

Note: The external manager interface, also known as the subordinate interface (SI), connects to an external manager.

2.4. External Subordinate Interface

The external subordinate interface operates in the same clock and reset domain as the external subordinate. It connects to the external subordinate through protocol-specific interfaces. The following are characteristics of the ES interface:

- Supports CDC.
- Supports register slice.
- Supports protocol conversion between AXI4, AXI4-Lite, AHB-Lite, and APB.

Notes: The external subordinate interface, also known as the manager interface (MI), connects to an external subordinate.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

2.5. Crossbar

The crossbar arbitrates and routes the read or write requests from an external manager device to one or more memory-mapped external subordinate devices. The following are characteristics of the crossbar:

- Routes the write data from the external manager device to the target external subordinate device.
- Routes the response and read data returned from the external subordinate device to the external manager device.
- AXI4 crossbar supports two crossbar architectures: performance-optimized shared address and multiple data channel (SAMD), and area-optimized shared address and shared data channel (SASD).
- AHB-Lite or APB crossbar allows multiple managers to access multiple subordinates.
  - For concurrent access to every subordinate, each manager must target a different subordinate.
  - Arbitration is performed on a per subordinate basis when multiple managers request access to the same subordinate.
    - Each AHB-Lite connection follows the standard AHB-Lite address-data pipelined protocol, with transaction progression controlled by the HREADY handshake. One address phase per manager is active at any given time.
    - Each APB arbitration is resolved during the setup phase when multiple managers contend for the same subordinate. Once a manager is granted access, the selection remains fixed throughout the subsequent access phase until the transfer completes, in accordance with the standard APB two-phase handshake protocol. APB does not support pipelined or outstanding address requests.

2.5.1. Shared Address and Multiple Data Channels

The following are characteristics of the SAMD crossbar architecture:

- Regardless of the number of EM ports enabled, the following are present:
  - One shared read address phase processing unit.
  - One shared write address phase processing unit.
  - One shared write response channel.
- The parallel crossbar route for write and read data channels allows multiple write or read data sources to simultaneously target different destinations. This enables data transfers to proceed independently and concurrently, provided the AXI protocol ordering requirements are satisfied.
- Address phase arbitration latencies typically do not impact the data payload transfer throughput for burst transfers.
- Supports external manager devices with reordering depths of up to 2^n, where n represents the external manager *AXI ID width.*
- Configurable external manager read acceptance limit and external manager write acceptance limit to limit the number of outstanding read or write transactions from an external manager.
- Permits address request based on *single slave per active ID* mechanism to ensure protocol compliance in the response ordering.

2.5.2. Shared Address and Shared Data Channels

The following are characteristics of the SASD crossbar architecture:

- Regardless of the number of EM ports enabled, there is only one shared address phase processing unit to handle both read and write requests.
- Single access mode permits only one outstanding transaction at a time using the shared data and response channel.

2.5.3. Address Phase Processing Unit

The address phase processing unit decodes the address request from the EM to determine the appropriate routing to an ES or internal default subordinate.

- For AXI4 transactions, the unit permits up to 2^n ID threads per EM, where n represents the external manager *AXI ID width*. After address arbitration, there is a two-clock bubble. Consequently, a minimum of three clock cycles is required between successive arbitrations for the same EM.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

- For AHB-Lite transactions, the unit decodes the address presented during the AHB address phase and selects the target subordinate accordingly. Only one address phase per manager is active at any given time, and multiple outstanding address requests are not supported.
- For APB transactions, the unit decodes the address during the APB setup phase to determine the target subordinate. In the event the APB manager issues back-to-back transfers to the same subordinate with the psel signal remaining asserted, the state machine transitions from the enable phase back to the setup phase without entering the idle state. The APB crossbar continues to grant access to the same manager until either the transaction returns to the idle state or the target address changes to a different subordinate.

2.5.4. Single Slave per Active ID for AXI4

For the *single slave per active ID* mechanism, each active ID thread initiated from an EM interface can have an outstanding transaction to only a single ES interface. Read access and write access are treated independently. ES interfaces are still permitted to issue multiple outstanding transactions initiated from multiple EM interfaces. In the case of external manager device access to different external subordinate devices (for example, A and B), using the same AXI ID, the request to B is permitted only after the outstanding transaction to A has completed. This mechanism supports up to 2^n ID threads per EM, where n represents the external manager *AXI ID width*.

2.5.5. Transaction Acceptance Limit

Transaction acceptance limits are configurable parameters to limit the number of outstanding transactions that the crossbar accepts from an EM interface. The following are the configurable parameters:

- External manager read acceptance limit
- External manager write acceptance limit

Each address phase processing unit tracks these limits and active ID threads to determine if a new transaction request from an EM will be temporarily disallowed. Transaction acceptance limits do not take into consideration address transfers that might be accepted and buffered by intermediate modules (for example, register slices, CDC, and bridges) on the address channel of the external manager prior to reaching the crossbar.
AHB-Lite supports only a single outstanding transaction per manager. Therefore, no additional transactions may be issued until the current transaction completes. APB does not support pipelined or outstanding transactions. Therefore, only one transfer may be active at a time per manager.

2.5.6. Outstanding Transaction

An outstanding transaction is a transaction that has not been completed. A transaction is complete when the following occurs:

- AXI4 write: bvalid/bready handshake completed at XB.
- AXI4 read: rvalid/rready handshake completed at XB with rlast asserted.
- AHB-Lite write: Data phase completed with hready asserted.
- AHB-Lite read: Valid read data (hrdata) returned with hready asserted.
- APB write: Write data accepted by subordinate during the access phase with pready asserted.
- APB read: Valid read data (prdata) returned with pready asserted.

2.6. Default Subordinate

There is one default subordinate per address phase processing unit. The following occurs when a request address cannot be mapped to a valid memory region for a memory-mapped external subordinate device:

1. The address phase processing unit stops granting new transaction requests from any EM.
2. The unit waits for all ongoing transactions to be completed, then hands execution over to the default subordinate.
3. Depending on the transaction, the following occurs:
   - For AXI4 read transaction: The default subordinate returns DECERR with Read Data = *don't care* to the EM until the final data transfer of the burst.
   - For AXI4 write transaction: The default subordinate accepts and discards all write data from the EM until the final data transfer of the burst. It then returns DECERR to the EM.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

- For AHB-Lite transaction: The default subordinate returns a two-cycle error response (HRESP = ERROR) in accordance with the AHB-Lite protocol.
- For APB transaction: The default subordinate asserts the error signal (PSLVERR) during the access phase to indicate an invalid address decode.

Note: When the primary crossbar is set to APB and there is only a single subordinate, the default subordinate is disabled. All EMs will only be able to access the valid address range of this single subordinate.

2.7. Infrastructure Modules

2.7.1. Queue

The queue block is part of a standard FIFO module. The following are characteristics of the block:

- When FIFO Depth = 0, the block is bypassed.
- Without CDC enabled, the single clock FIFO is instantiated.
- With CDC enabled, dual-clock FIFO is instantiated to handle the clock domain crossing between the external manager interface or external subordinate interface and the crossbar.
- The *Memory Type of Large FIFOs* attribute specifies whether the queue is implemented using EBR- or LUT-based memory.
- Applicable only when EM or ES protocol type is AXI4.

2.7.2. Register Slice

The register slice connects one MI to one SI through a set of pipeline registers, typically to break up a critical timing path. The following are characteristics of the block:

- For AXI4, contains a pipeline SKID buffer.
- Introduces a one clock latency. For AHB-Lite bursts, the register slice does not pipeline the burst as a continuous sequence. Instead, each beat is forwarded individually, which can introduce additional latency (typically one clock cycle per transfer).
- Can be optionally applied for timing optimization.

2.7.3. Protocol Conversion Bridge

The following protocol conversion bridges are automatically inserted into the unified interconnect based on the EM and ES protocol types:

- AXI4-Lite to AXI4
- AXI4 to AXI4-Lite
- AXI4 to AHB-Lite
- AXI4 to APB
- AHB-Lite to AXI4-Lite
- AHB-Lite to AXI4
- AHB-Lite to APB

2.7.3.1. AXI4-Lite to AXI4

AXI4-Lite does not support burst transfers. Each AXI4-Lite write or read transaction is implemented as a single-beat AXI4 transfer by setting the following:

- For write: awlen = 0 and wlast = 1
- For read: arlen = 0

2.7.3.2. AXI4 to AXI4-Lite

AXI4-Lite does not support burst transfers. An AXI4 transaction is decomposed into individual single-beat AXI4-Lite transfers.

2.7.3.3. AXI4 to AHB-Lite

AHB-Lite handles incrementing bursts differently from AXI4. The implementation is as follows:

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

- AXI4 INCR burst transfers are translated into AHB-Lite INCR bursts of unspecified length.
- AXI4 FIXED burst transfers are not preserved as bursts but instead converted into single-beat AHB-Lite transfers.

2.7.3.4. AXI4 to APB

APB does not support burst transfers. An AXI4 transaction is decomposed into individual single-beat transfers on the APB side. The address and data are passed through without modification. Narrow transfers are not supported. The implementation is as follows:

- For read: Raw APB response is forwarded directly to the AXI4 interface.
- For write: EM performs read-modify-write operations.

2.7.3.5. AHB-Lite to AXI4-Lite

AXI4-Lite does not support burst transactions. An AHB-Lite transaction is decomposed into individual single-beat AXI4-Lite transfers. In multi-protocol CFG1, the AHB-Lite manager accesses the AXI4-Lite subordinate through the AXI4 primary crossbar. The AHB-Lite burst is converted into the AXI4 INCR burst and decomposed into individual single-beat AXI4-Lite transfers. The implementation allows for two possible error cases:

- None of the ES protocol types are AXI4 (excluding AXI4-Lite)
  If BRESP = SLVERR or DECERR is received from the AXI4-Lite subordinate, HRESP = ERROR is asserted to the AHB-Lite manager on the same beat.

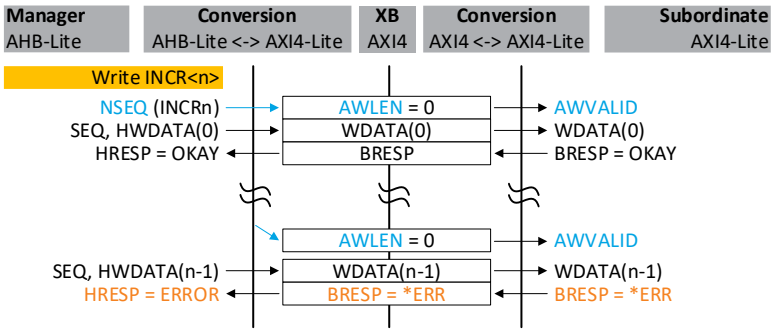


Figure 2.12. Case 1 – AHB-Lite INCR<n> Burst Write to AXI4-Lite in Mixed-Protocol System with Write Response Error

- One or more ES protocol types are AXI4
  Because AXI4 write responses are provided only at the end of a burst, OKAY HRESP is returned on the AHB-Lite side for each beat until the final AXI4 write response is available. If BRESP = SLVERR or DECERR is received from the AXI4-Lite subordinate, HRESP = ERROR is asserted to the AHB-Lite manager on the final beat.

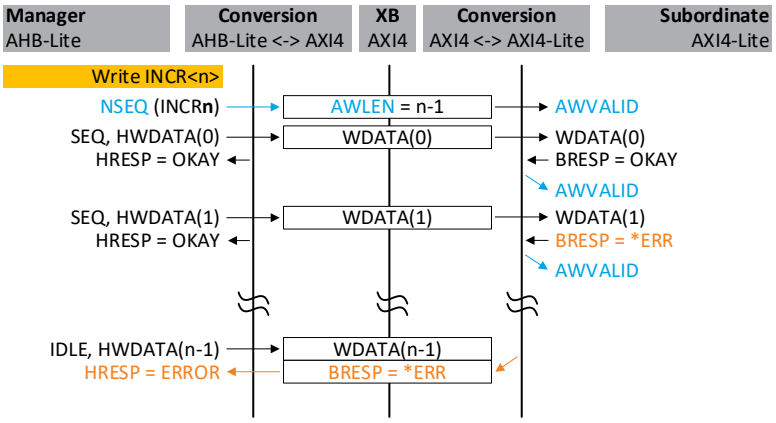


Figure 2.13. Case 2 – AHB-Lite INCR<n> Burst Write to AXI4-Lite in Mixed-Protocol System with Write Response Error

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

2.7.3.6. AHB-Lite to AXI4

AHB-Lite INCR bursts with no defined length are converted into individual single-beat AXI4 transfers. Fixed-length AHB-Lite bursts (INCR4, INCR8, and INCR16) are translated into AXI4 bursts with matching lengths. Because AXI4 write responses are provided only at the end of a burst, OKAY HRESP is returned on the AHB-Lite side for each beat until the final AXI4 write response is available.

2.7.3.7. AHB-Lite to APB

APB does not support burst transfers. An AHB-Lite transaction is decomposed into individual single-beat transfers on the APB side. The address and data are passed through without modification. Narrow transfers are not supported. The implementation is as follows:

- For read: Raw APB response is forwarded directly to the AHB-Lite interface.
- For write: EM performs read-modify-write operations.

2.7.3.8. AHB-Lite Burst Decomposition

AHB-Lite burst transfers are broken down into individual single transfers under the following conditions:
Note: This decomposition might reduce transfer throughput.

- An AHB-Lite manager is configured with one of the following options:
  - *External Manager <N> (Sxx) Data Register Slice Enable* is checked
  - *External Manager <N> (Sxx) CDC Enable* is checked
- An AHB-Lite subordinate directly connected to the primary IC is configured with one of the following options:
  - *External Subordinate <M> (Myy) Data Register Slice Enable* is checked
  - *External Subordinate <M> (Myy) CDC Enable* is checked
- An AHB-Lite subordinate connected through the secondary IC is configured with one of the following options:
  - *External Subordinate <M> (Myy) Data Register Slice Enable* is checked
  - *Common Secondary AXI4-Lite External Subordinate CDC Enable* is checked
- AHB-Lite bursts of undefined length are routed through the AXI4 crossbar.

2.7.3.9. Protocol Conversion Mapping

The mappings between AHB-Lite HPROT transaction attributes and AXI4 AxPROT and AxCACHE transaction attributes are not explicitly defined in the AMBA AHB-Lite or AXI4 specifications. The following table shows the mappings implemented when an AHB-Lite manager accesses an AXI4 or AXI4-Lite subordinate.

Table 2.5. AHB-Lite HPROT to or from AXI4 AxPROT and AxCACHE Mappings

AHB-Lite Transaction Attribute	AHB-Lite Signal Assignment	AXI4 Transaction Attribute	AXI4 Signal Assignment
Data access	HPROT[0] = 1	Data access	AxPROT[2] = 0
Opcode fetch	HPROT[0] = 0	Instruction access	AxPROT[2] = 1
—	*_AXI_SECURE_ACCESS = 1 EXT_SLV_AXI_SECURE_AXIL_ACCESS = 1	Secure access	AxPROT[1] = 0
—	*_AXI_SECURE_ACCESS = 0 EXT_SLV_AXI_SECURE_AXIL_ACCESS = 0	Non-secure access	AxPROT[1] = 1
User access	HPROT[1] = 0	Unprivileged access	AxPROT[0] = 0
Privileged access	HPROT[1] = 1	Privileged access	AxPROT[0] = 1
Not bufferable	HPROT[2] = 0	Non-bufferable	AxCACHE[0] = 0
Bufferable	HPROT[2] = 1	Bufferable	AxCACHE[0] = 1
Not cacheable	HPROT[3] = 0	Non-cacheable	AxCACHE[1] = 0
Cacheable	HPROT[3] = 1	Cacheable	AxCACHE[1] = 1
—	—	No read-allocate	AxCACHE[2] = 0
—	—	Read-allocate	—[1]
—	—	No write-allocate	AxCACHE[3] = 0

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

AHB-Lite Transaction Attribute	AHB-Lite Signal Assignment	AXI4 Transaction Attribute	AXI4 Signal Assignment
—	—	Write-allocate	—[1]

Note:

1. AxCACHE[2] and AxCACHE[3] are forced to zero. Therefore, the read-allocate and write-allocate encodings are not applicable.

The implementation of mappings through crossbars are as follows:

- When the AHB-Lite manager accesses the AXI4 or AXI4-Lite subordinate through the AXI4 primary crossbar:
  - AxPROT[1] is the logical inverse of the EXT_MAS_AXI_SECURE_ACCESS parameter configured in each EM.

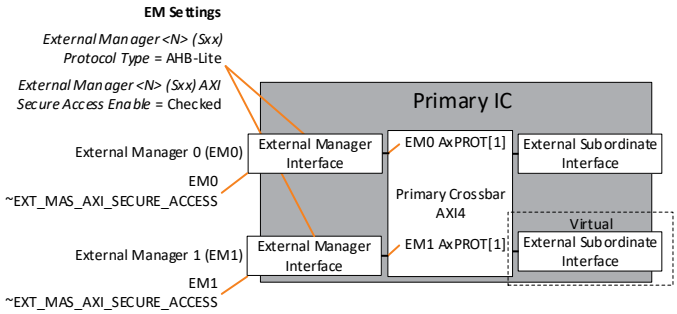


Figure 2.14. AxPROT[1] through AXI4 Primary Crossbar

- When the EM accesses the AXI4 or AXI4-Lite subordinate through the AHB-Lite primary crossbar:
  - If the subordinate connects directly to the primary IC, AxPROT[1] is the logical inverse of the EXT_SLV_AXI_SECURE_ACCESS parameter configured in each ES.
  - If the subordinate connects through the AXI4-Lite secondary IC, AxPROT[1] is the logical inverse of the EXT_SLV_AXI_SECURE_AXIL_ACCESS parameter configured in the ES secondary AXI4-Lite. All subordinates with the secondary AXI4-Lite protocol type refer to the same parameter.

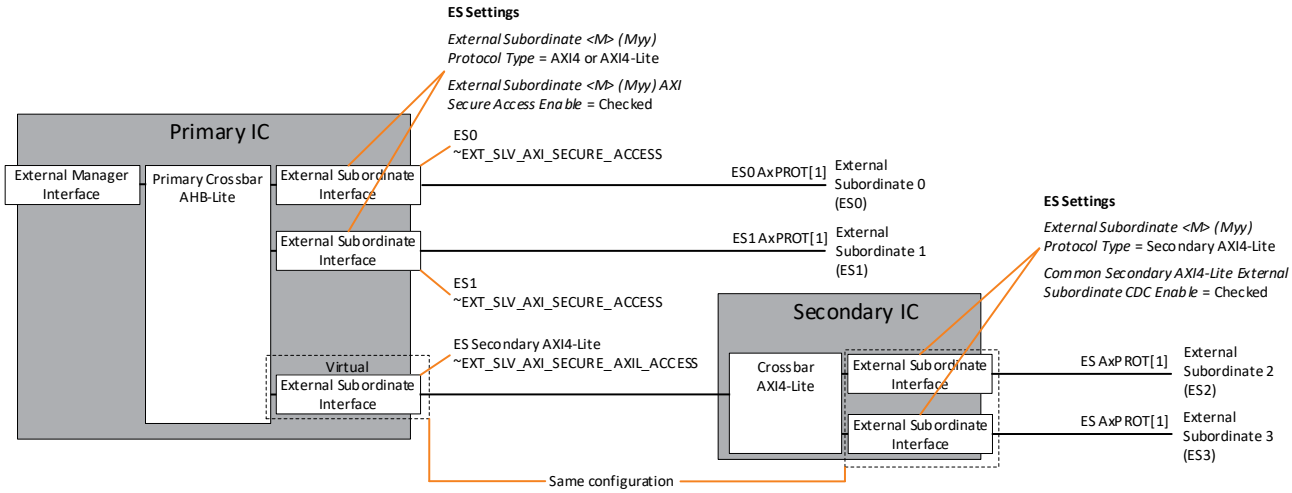


Figure 2.15. AxPROT[1] through AHB-Lite Primary Crossbar

2.7.4. Error Case Examples during Protocol Conversion

2.7.4.1. AHB-Lite Write through AXI4 Crossbar

During an AHB-Lite INCR<n> burst write in a mixed-protocol system, fixed-length AHB-Lite bursts (INCR4, INCR8, and INCR16) are translated into AXI4 bursts with matching lengths. When the HRESP = ERROR is received from the AHB-Lite subordinate, the implementation is as follows:

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

- AXI4-to-AHB-Lite converter within the ES interface terminates the transaction early after receiving the error response from the AHB-Lite subordinate. The external manager continues sending write data to the ES interface. Whatever write data received from the external manager that belongs to the same transaction is flushed.
- Because AXI4 write responses are provided only at the end of a burst, OKAY HRESP is returned on the AHB-Lite manager for each beat until the final AXI4 write response is available. The HRESP = ERROR response from the AHB-Lite subordinate is mapped to BRESP = SLVERR for AXI4.

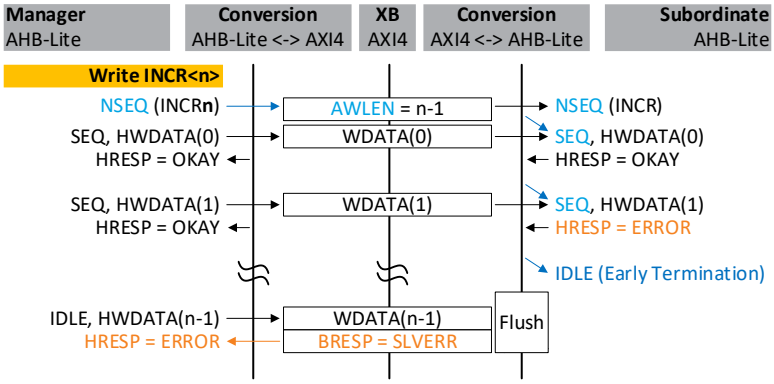


Figure 2.16. AHB-Lite INCR<n> Burst Write to AHB-Lite in Mixed-Protocol System and ES Interface Early Termination after HRESP = ERROR

2.7.4.2. AHB-Lite Read through AXI4 Crossbar

During an AHB-Lite INCR<n> burst read in a mixed-protocol system, fixed-length AHB-Lite bursts (INCR4, INCR8, and INCR16) are translated into AXI4 bursts with matching lengths. When the HRESP = ERROR is received from the AHB-Lite subordinate, the implementation is as follows:

- AXI4 RRESP value is generated based on the specific beat where the AHB-Lite subordinate reports the error. AXI4-to-AHB-Lite converter within the external subordinate interface continues performing read until the end of the burst. Whatever read data received that belongs to the same transaction is flushed in the external manager interface.
- AXI4-to-AHB-Lite converter continues issuing read transfers until the final burst beat is completed. The HRESP = ERROR response from the AHB-Lite subordinate is mapped to RRESP = SLVERR for AXI4.

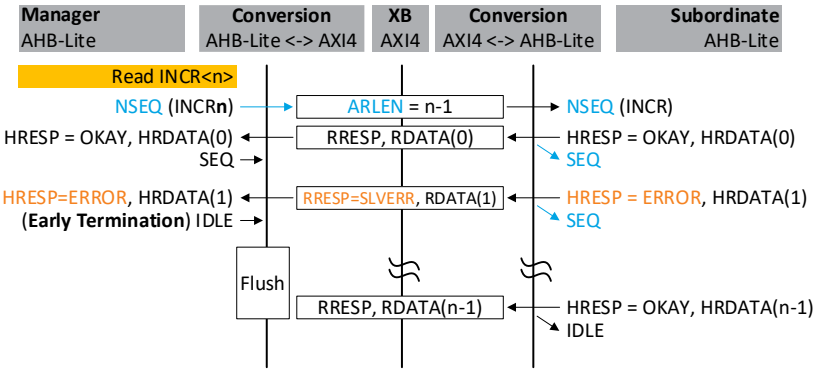


Figure 2.17. AHB-Lite INCR<n> Burst Read to AHB-Lite in Mixed-Protocol System and External Manager Early Termination after HRESP = ERROR

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

3. IP Parameter Description

The configurable attributes of the Unified Interconnect IP are shown in the following tables. You can configure the IP by setting the attributes accordingly in the IP Catalog Module/IP Block Wizard of the Lattice Radiant software.

Wherever applicable, default values are in bold.

3.1. General

Table 3.1. General Attributes

Attribute (Parameter Name)	Selectable Values	Description	Applicable Protocol
General			
Total External Managers (TOTAL_EXTMAS_CNT)	1–16, **2**	Selects the total number of external managers. **Note:** *Total External Managers* and *Total External Subordinates* cannot be set to 1 at the same time.	All
Total External Subordinates (TOTAL_EXTSLV_CNT)	1–16, **2**	Selects the total number of external subordinates. **Note:** *Total External Managers* and *Total External Subordinates* cannot be set to 1 at the same time.	All
AXI User Width (AXI_USER_WIDTH)	**1**–128	Specifies the AXI user width.	AXI4
Memory Type of Large FIFOs (LARGE_FIFO_MEM_TYPE)	**LUT**, EBR	Selects the memory type for larger FIFOs.	All
Crossbar Optimization Strategy (XBAR_MODE_GUI)	**Maximize Performance**, Minimize Area	Selects crossbar mode. Maximize Performance – SAMD Minimize Area – SASD **Note:** The *Minimize Area* option appears only when the AXI4-Lite protocol is selected for all external managers and external subordinates. Refer to the Crossbar section for more information on crossbar modes.	AXI4, AXI4-Lite[1]
Primary Crossbar (XBAR_PRIMARY_MODE)	**AXI4,** AHB-Lite, APB (auto selected)	Current primary crossbar mode. Refer to the Configuration section for information on multi-protocol configurations.	All

Note:

1. Only applicable for CFG1 as defined in the Configuration section.

3.2. External Manager Settings

Table 3.2. External Manager Settings Attributes

Attribute[1, 2] (Parameter Name)	Selectable Values	Description[3]	Applicable Protocol
General			
External Manager AXI ID Width (EXT_MAS_AXI_ID_WIDTH)	1–6, **2**	External manager AXI ID width	AXI4
External Manager Priority (EXT_MAS_PRIORITY_SCHEME)	**Round Robin**, Fixed Priority[3]	External manager priority	All

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Attribute[1, 2] (Parameter Name)	Selectable Values	Description[3]	Applicable Protocol
External Manager AXI Secure Access Settings			
External Manager <N> (Sxx) AXI Secure Access Enable (EXT_MAS_AXI_SECURE_ ACCESS)	**Unchecked**, Checked	Determines the mapping into AxPROT[1] when an AHB-Lite manager accesses an AXI4 or AXI4-Lite subordinate. Refer to the Protocol Conversion Mapping section for more information.	AHB-Lite
External Manager Register Slice Settings			
External Manager <N> (Sxx) Data Register Slice Enable (EXT_MAS_DATA_ REGISTER_SLICE)	**Unchecked**, Checked	Enables external manager data register slice.	All
External Manager Access Type Settings			
External Manager <N> (Sxx) AXI Access Type (EXT_MAS_ACCESS_TYPE)	WO, RO, **WR**	External manager access type WO – Write only port RO – Read only port WR – Write/Read port	AXI4, AXI4-Lite
External Manager Protocol Settings			
External Manager <N> (Sxx) Protocol Type (EXT_MAS_PROTOCOL)	**AXI4**, AXI4-Lite, AHB-Lite, APB	Protocol supported by the external manager. Refer to the Configuration section for information on the possible EM and ES configurations.	All
External Manager CDC Enable Settings			
External Manager <N> (Sxx) CDC Enable (EXT_MAS_CDC_EN)	**Unchecked**, Checked	Enables external manager CDC.	All
External Manager Address Settings			
External Manager <N> (Sxx) Address Width	11–64, **32**	External manager address width	All
External Manager Data Settings			
External Manager <N> (Sxx) Data Width (EXT_MAS_DATA_WIDTH)	8, 16, **32**, 64, 128, 256, 512, 1024	External manager data width **Notes:** • The *External Manager <N> (Sxx) Data Width* setting must match the *External Subordinate <M> (Myy) Data Width* setting. • When *External Manager <N> (Sxx) Protocol Type* = AXI4-Lite, the available options are only 32 and 64. • When *External Manager <N> (Sxx) Protocol Type* = APB, the available options are 8, 16, and 32.	All
External Manager Write Acceptance Limit Settings			
External Manager <N> (Sxx) Write Acceptance Limit (EXT_MAS_AXI_WR_ ACCEPTANCE_LIMIT)	1–32, **2**	Limits the number of outstanding write transactions that the crossbar can accept. When this limit is reached, no additional write transactions are granted for the specified EM. **Note:** When *External Manager <N> (Sxx) Protocol Type* = AXI4-Lite, the available options are 1 and 2.	AXI4, AXI4-Lite
External Manager Read Acceptance Limit Settings			
External Manager <N> (Sxx) Read Acceptance Limit (EXT_MAS_AXI_RD_ ACCEPTANCE_LIMIT)	1–32, **2**	Limits the number of outstanding read transactions that the crossbar can accept. When this limit is reached, no additional read transactions are granted for the specified EM. **Note:** When *External Manager <N> (Sxx) Protocol Type* = AXI4-Lite, the available options are 1 and 2.	AXI4, AXI4-Lite

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Attribute[1, 2] (Parameter Name)	Selectable Values	Description[3]	Applicable Protocol
External Manager Write Address Buffer Depth Settings			
External Manager <N> (Sxx) Write Address Buffer Depth (EXT_MAS_WR_ADDR_ DEPTH)	**0**[4, 5], 2, 4, **8**[5], 16	Sets the number of write address entries from external manager N that can be buffered internally. This setting configures the internal FIFO depth for the Write Address channel.	AXI4, AXI4-Lite
External Manager Read Address Buffer Depth Settings			
External Manager <N> (Sxx) Read Address Buffer Depth (EXT_MAS_RD_ADDR_ DEPTH)	**0**[4, 5], 2, 4, **8**[5], 16	Sets the number of read address entries from external manager N that can be buffered internally. This setting configures the internal FIFO depth for the Read Address channel.	AXI4, AXI4-Lite
External Manager Write Buffer Settings			
External Manager <N> (Sxx) Write Response Buffer Depth (EXT_MAS_BRESP_ FIFO_DEPTH)	**0**[4, 5], 2, 4, **8**[5], 16	Sets the number of write responses from the external subordinate that can be buffered internally before being returned to external manager N. This setting configures the internal FIFO depth for the Write Response channel.	AXI4, AXI4-Lite
External Manager <N> (Sxx) Write Data Buffer Depth (EXT_MAS_WR_DATA_ FIFO_DEPTH)	0[4], **2**[6], 4, **8**[6], 16, 32, 64, 128, 256, 512	Sets the number of write data entries from external manager N that can be buffered internally. This setting configures the internal FIFO depth for the Write Data channel.	AXI4, AXI4-Lite
External Manager Read Buffer Settings			
External Manager <N> (Sxx) Read Data Buffer Depth (EXT_MAS_RD_DATA_ FIFO_DEPTH)	**0**[4, 5], 2, 4, **8**[5], 16, 32, 64, 128, 256, 512	Sets the number of read data from the external subordinate that can be buffered internally before being returned to external manager N. This setting configures the internal FIFO depth for the Read Data channel.	AXI4, AXI4-Lite
External Manager 0 Fixed Priority Settings			
Ext Manager <N> (Sxx) Fixed Priority (EXT_MAS_FIXED_ PRIORITY)	0 to (*Total External Subordinates* –1), **N**	External manager fixed priority	AXI4, AXI4-Lite, AHB-Lite, APB

Notes:

1. N ranges from 0 to (*Total External Managers* – 1).
2. xx denotes the external manager port number ranging from 0 to N, where N = (*Total External Managers* – 1). xx is formatted with a leading 0 when the port number is a single digit.
3. Priority order 0, 1, 2, …, N, with 0 being the highest priority.
4. The selectable value 0 is only available when the external manager CDC is disabled.
5. The following default values apply depending on whether CDC is enabled or disabled:
   - 0 when external manager CDC is disabled.
   - 8 when external manager CDC is enabled.
6. The following default values apply depending on whether CDC is enabled or disabled:
   - 2 when external manager CDC is disabled.
   - 8 when external manager CDC is enabled.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

3.3. External Subordinate Settings

Table 3.3. External Subordinate Settings Attributes

Attribute[1, 2] (Parameter Name)	Selectable Values	Description	Applicable Protocol
General			
External Subordinate AXI ID Width (EXT_SLV_AXI_ID_ WIDTH)	1–10, **4**	External subordinate AXI ID width The setting must satisfy the following condition: *External Subordinate AXI ID width* ≥ *External Manager AXI ID width* + $\log_2$(*Total External Managers*)	AXI4, AXI4-Lite
External Subordinate AXI Secure Access Settings			
External Subordinate <M> (Myy) AXI Secure Access Enable (EXT_SLV_AXI_SECURE_ ACCESS)	**Unchecked**, Checked	Determines the mapping into AxPROT[1] when an AHB-Lite manager accesses an AXI4 or AXI4-Lite subordinate. Refer to the Protocol Conversion Mapping section for more information.	AHB-Lite
Common Secondary AXI4-Lite External Subordinate AXI Secure Access Enable (EXT_SLV_AXI_SECURE_ AXIL_ACCESS)	**Unchecked**, Checked	Determines the mapping into AxPROT[1] when the primary crossbar AHB-Lite accesses the common secondary AXI4-Lite subordinates. Refer to the Protocol Conversion Mapping section for more information.	Secondary AHB-Lite
External Subordinate Register Slice Settings			
External Subordinate <M> (Myy) Data Register Slice Enable (EXT_SLV_DATA_ REGISTER_SLICE)	**Unchecked**, Checked	Enables external subordinate data register slice.	All
External Subordinate Access Type Settings			
External Subordinate <M> (Myy) AXI Access Type (EXT_SLV_ACCESS_TYPE)	WO, RO, **WR**	External subordinate AXI access type WO – Write only port RO – Read only port WR – Write/Read port	AXI4, AXI4-Lite, Secondary AXI4-Lite
External Subordinate Protocol Type Settings			
External Subordinate <M> (Myy) Protocol Type (EXT_SLV_PROTOCOL)	**AXI4**, AXI4-Lite, AHB-Lite, APB, Secondary AXI4-Lite[3], Secondary AHB-Lite[3], Secondary APB[3]	Protocol supported by the external subordinate. Refer to the Multi-protocol section for more information.	All
External Subordinate CDC Enable Settings			
External Subordinate <M> (Myy) CDC Enable (EXT_SLV_CDC_EN)	**Unchecked**, Checked	Enables external subordinate CDC.	AXI4, AXI4-Lite, AHB-Lite, APB
Common Secondary AXI4-Lite External Subordinate CDC Enable (EXT_SLV_CDC_AXIL_EN)	**Unchecked**, Checked	Enables common CDC for all secondary AXI4-Lite external subordinates.	Secondary AXI4-Lite
Common Secondary AHB-Lite External Subordinate CDC Enable (EXT_SLV_CDC_AHBL_EN)	**Unchecked**, Checked	Enables common CDC for all secondary AHB-Lite external subordinates.	Secondary AHB-Lite

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Attribute[1, 2] (Parameter Name)	Selectable Values	Description	Applicable Protocol
Common Secondary APB External Subordinate CDC Enable (EXT_SLV_CDC_APB_EN)	**Unchecked**, Checked	Enables common CDC for all secondary APB external subordinates.	Secondary APB
External Subordinate Address Settings			
External Subordinate <M> (Myy) Address Width (EXT_SLV_ADDR_WIDTH)	11–64, **32**	External subordinate address width	All
External Subordinate Data Settings			
External Subordinate <M> (Myy) Data Width (EXT_SLV_DATA_WIDTH)	8, 16, **32**, 64, 128, 256, 512, 1024	External subordinate data width **Notes:** • All external managers and external subordinates must share the same data width. Data width conversion is not currently supported. • When *External Subordinate <M> (Myy) Protocol Type* = AXI4-Lite, the available options are only 32 and 64. • When *External Subordinate <M> (Myy) Protocol Type* = APB, the available options are only 8, 16, and 32.	All
External Subordinate Write Address Buffer Depth Settings			
External Subordinate <M> (Myy) Write Address Buffer Depth (EXT_SLV_WR_ADDR_ DEPTH)	**0**[4, 5], 2, 4, **8**[5], 16	Sets the number of write address entries from the external manager that can be buffered internally before being returned to external subordinate M. This setting configures the internal FIFO depth for the Write Address channel.	AXI4, AXI4-Lite, Secondary AXI4-Lite
External Subordinate Read Address Buffer Depth Settings			
External Subordinate <M> (Myy) Read Address Buffer Depth (EXT_SLV_RD_ADDR_ DEPTH)	**0**[4, 5], 2, 4, **8**[5], 16	Sets the number of read address entries from the external manager that can be buffered internally before being returned to external subordinate M. This setting configures the internal FIFO depth for the Read Address channel.	AXI4, AXI4-Lite, Secondary AXI4-Lite
External Subordinate Write Buffer Settings			
External Subordinate <M> (Myy) Write Response Buffer Depth (EXT_SLV_BRESP_FIFO_ DEPTH)	**0**[4, 5], 2, 4, **8**[5], 16	Sets the number of write response entries from external subordinate M that can be buffered internally. This setting configures the internal FIFO depth for the Write Response channel.	AXI4, AXI4-Lite, Secondary AXI4-Lite
External Subordinate <M> (Myy) Write Data Buffer Depth (EXT_SLV_WR_DATA_ FIFO_DEPTH)	**0**[4, 5], 2, 4, **8**[5], 16, 32, 64, 128, 256, 512	Sets the number of write data entries from the external manager that can be buffered internally before being returned to external subordinate M. This setting configures the internal FIFO depth for the Write Data channel.	AXI4, AXI4-Lite, Secondary AXI4-Lite
External Subordinate Read Buffer Settings			
External Subordinate <M> (Myy) Read Data Buffer Depth (EXT_SLV_RD_DATA_ FIFO_DEPTH)	**0**[4, 6], **2**[6], 4, **8**[6], 16, 32, 64, 128, 256, 512	Sets the number of read data entries from external subordinate M that can be buffered internally. This setting configures the internal FIFO depth for the Read Data channel.	AXI4, AXI4-Lite, Secondary AXI4-Lite
External Subordinate Fragment Settings			
External Subordinate <M> (Myy) Fragment Cnt (EXT_SLV_FRAGMENT_ CNT)	**1**–16	Sets the external subordinate fragment count. Refer to the Maximum Fragment section for more information.	All except APB, Secondary APB

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Attribute[1, 2] (Parameter Name)	Selectable Values	Description	Applicable Protocol
External Subordinate M Base Address Settings[7]			
Base Address <F> (EXT_SLV_FRAGMENT_BASE_ADDR) [8]	*Base Address F aligned to at least a 1 KiB boundary.*	Base address for external subordinate M fragment F. **Note:** F ranges from 0 to (*External Subordinate <M> (Myy) Fragment Cnt* – 1).	All
External Subordinate M End Address Settings[7]			
End Address <F>[8] (EXT_SLV_FRAGMENT_END_ADDR)	*End Address F = Base Address F + Fragment Size – 1; base address must be aligned to at least a 1 KiB boundary*	End address for external subordinate M fragment F. **Note:** F ranges from 0 to (*External Subordinate <M> (Myy) Fragment Cnt* – 1).	All

Notes:

1. M ranges from 0 to (*Total External Subordinates* – 1).
2. yy denotes the external subordinate port number ranging from 0 to M, where M = (*Total External Subordinates* – 1). yy is formatted with a leading 0 when the port number is a single digit.
3. It is recommended that the same secondary protocol be selected for more than one external subordinate.
4. The selectable value 0 is only available when external subordinate CDC is disabled.
5. The following default values apply depending on whether CDC is enabled or disabled:
   - 0 when external subordinate CDC is disabled.
   - 8 when external subordinate CDC is enabled.
6. The following default values apply depending on whether CDC is enabled or disabled and the *Crossbar Optimization Strategy* setting:
   - 0 when external subordinate CDC is disabled with crossbar mode set to SASD.
   - 2 when external subordinate CDC is disabled with crossbar mode set to SAMD.
   - 8 when external subordinate CDC is enabled.
7. These attributes are hidden and automatically configured in the Lattice Propel Builder software.
8. The minimum size for each of the external subordinate fragments must be a multiple of 1 KiB.
   Examples:
   - Subordinate 0 fragment 0 base address = 'h0000
   - Subordinate 0 fragment 0 end address = 'h03FF
   - Subordinate 0 fragment 1 base address = 'h0400
   - Subordinate 0 fragment 1 end address = 'h07FF

   For AXI4 or AXI4-Lite, it is recommended that the fragment size be 4 KiB and the base address be aligned to a 4 KiB boundary.
   Examples:
   - Subordinate 0 fragment 0 base address = 'h0000
   - Subordinate 0 fragment 0 end address = 'h0FFF
   - Subordinate 0 fragment 1 base address = 'h1000
   - Subordinate 0 fragment 1 end address = 'h1FFF

3.4. Advanced Settings

Table 3.4. Advanced Settings Attributes

Attribute (Parameter Name)	Selectable Values	Description[1, 2]	Applicable Protocol
Timing Optimization Setting			
Enable Crossbar Address Decode Pipestage (PERFORMANCE_FMAX)	**Unchecked**, Checked	Enables the crossbar address decode pipeline stage to maintain timing closure during complex address decoding. This option is recommended for configurations involving high fragment counts, non-contiguous addressing schemes, or designs requiring a high number of unique address bits.	AXI4, AXI4-Lite[3]

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Attribute (Parameter Name)	Selectable Values	Description[1, 2]	Applicable Protocol
Resource Optimization Setting			
Enable Default Subordinate (INVALID_ADDR_ERR_ RESP_EN)	Unchecked, **Checked**	Enables the default subordinate. Applicable only when *Primary Crossbar* == AXI4 **Note**: For a closed system that guarantees all addresses are valid, you may choose to disable the default subordinate.	AXI4, AXI4-Lite, and AHB-Lite
Resource Optimization Setting - Manager <N> (Sxx) Connectivity Setting			
Enable Link to Subordinate <M> (Myy) (CONNECT_EN)	Unchecked, **Checked**	Enables the path from manager N to subordinate M.	All except APB and secondary protocols
Enable Link to Common Secondary AXI4-Lite (SECONDARY_AXI4L_ CONNECT_EN)	Unchecked, **Checked**	Enables the path from manager N to common secondary AXI4-Lite subordinates.	Secondary AXI4-Lite
Enable Link to Common Secondary AHB-Lite (SECONDARY_AHBL_ CONNECT_EN)	Unchecked, **Checked**	Enables the path from manager N to common secondary AHB-Lite subordinates.	Secondary AHB-Lite
Enable Link to Common Secondary APB (SECONDARY_APB_ CONNECT_EN)	Unchecked, **Checked**	Enables the path from manager N to common secondary APB subordinates.	Secondary APB

Notes:

1. N ranges from 0 to (*Total External Managers* – 1).
2. M ranges from 0 to (*Total External Subordinates* – 1).
3. Only applicable for CFG1 as defined in the Configuration section.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

4. Signal Description

This section describes the Unified Interconnect IP ports.

4.1. Clock and Reset

Figure 4.1 shows the clock and reset ports on the Unified Interconnect IP interface. All reset signals are asynchronously asserted but synchronously de-asserted. Refer to the Clocking and Reset section for more information on the clock and reset signals.

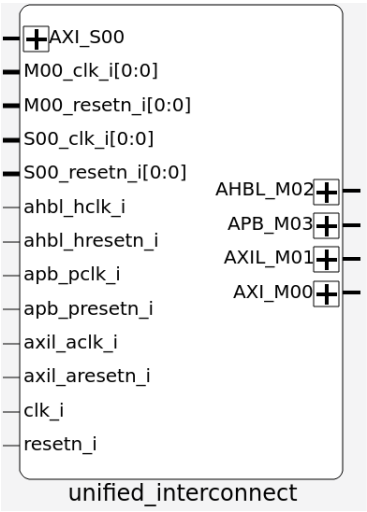


Figure 4.1. Clock and Reset Interface Diagram for CDC Enabled and Disabled

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

4.2. AXI4

Figure 4.2 shows the interface diagram for the Unified Interconnect IP when the AXI4 protocol is selected. All AXI manager and subordinate interface signals are compliant with the AXI4 and AXI4-Lite protocols. Refer to the AMBA AXI Protocol Specification web page for the timing diagrams and more information about the protocol.

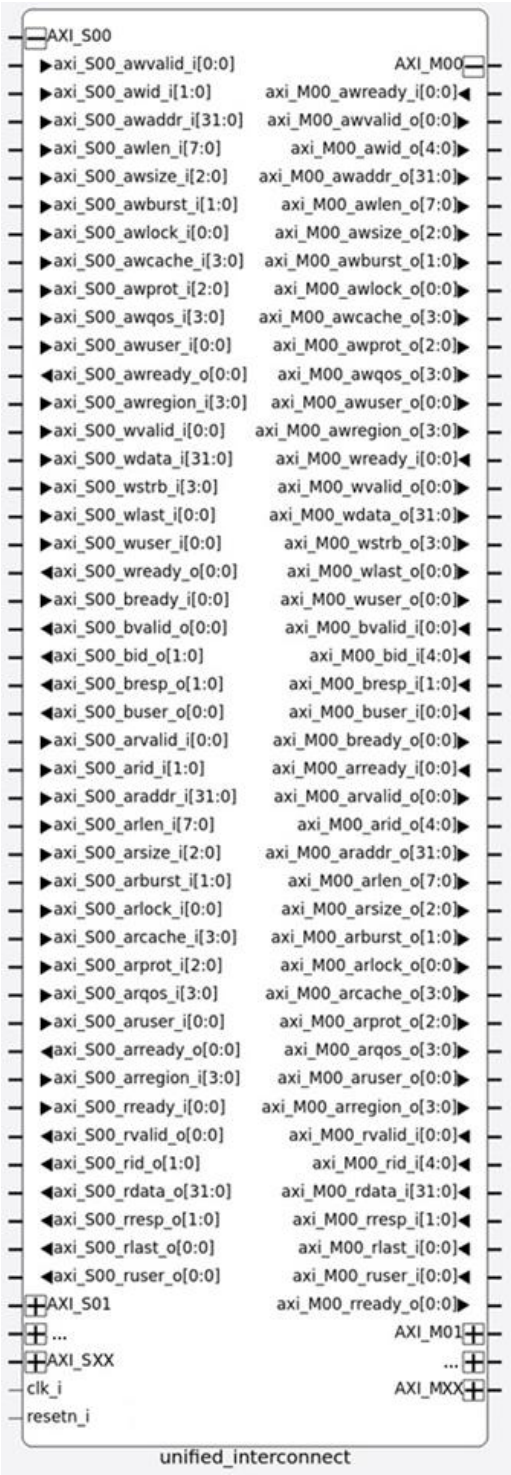


Figure 4.2. AXI4 Protocol Interface Diagram

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

4.2.1. AXI4 External Manager Interface

Table 4.1. AXI4 External Manager Interface Ports

Port[1]	Type	Description
AXI Interconnect Subordinate xx Interface – Connected to External Manager xx[2]		
axi_Sxx_awvalid_i[3]	Input	Write address valid
axi_Sxx_awid_i[x:0][4]	Input	Write address ID **Note:** x = *External Manager AXI ID Width* – 1
axi_Sxx_awaddr_i[x:0][3]	Input	Write address **Note:** x = Maximum Value for *External Manager <N> (Sxx) Address Width* across All Managers – 1
axi_Sxx_awlen_i[7:0][4]	Input	Write address burst length The exact number of transfers in a burst.
axi_Sxx_awsize_i[2:0][4]	Input	Write address burst size The size of each transfer in the burst.
axi_Sxx_awburst_i[1:0][4]	Input	Write address burst type
axi_Sxx_awlock_i[4]	Input	Write address lock type
axi_Sxx_awcache_i[3:0][4]	Input	Write address memory type
axi_Sxx_awprot_i[2:0][3]	Input	Write address protection type
axi_Sxx_awqos_i[3:0][4]	Input	Write address quality of service
axi_Sxx_awregion_i[3:0]	Input	Write address region
axi_Sxx_awuser_i[x:0][4]	Input	Write address user signals **Note:** x = *AXI User Width* – 1
axi_Sxx_awready_o[3]	Output	Write address ready
axi_Sxx_wvalid_i[3]	Input	Write data valid
axi_Sxx_wdata_i[x:0][3]	Input	Write data **Note:** x = *External Manager<N> (Sxx) Data Width* – 1
axi_Sxx_wstrb_i[x:0][3]	Input	Write data strobes **Note:** x = (*External Manager<N> (Sxx) Data Width*/8) – 1
axi_Sxx_wlast_i[4]	Input	AXI4 last write beat/burst
axi_Sxx_wuser_i[x:0][4]	Input	Write data user signal **Note:** x = *AXI User Width* – 1
axi_Sxx_wready_o[3]	Output	Write data ready
axi_Sxx_bvalid_o[3]	Output	Write response valid
axi_Sxx_bid_o[x:0]	Output	Write respond ID **Note:** x = *External Manager AXI ID Width* – 1
axi_Sxx_bresp_o[1:0][3]	Output	Write response
axi_Sxx_buser_o[x:0][4]	Output	Write response user signal **Note:** x = *AXI User Width* – 1
axi_Sxx_bready_i[3]	Input	Write response ready
axi_Sxx_arvalid_i[3]	Input	Read address valid
axi_Sxx_arid_i[x:0][4]	Input	Read address ID **Note:** x = *External Manager AXI ID Width* – 1
axi_Sxx_araddr_i[x:0][3]	Input	Read address **Note:** x = Maximum Value for *External Manager <N> (Sxx) Address Width* across All Managers – 1
axi_Sxx_arlen_i[7:0][4]	Input	Read address burst length
axi_Sxx_arsize_i[2:0][4]	Input	Read address burst size
axi_Sxx_arburst_i[1:0][4]	Input	Read address burst type
axi_Sxx_arlock_i[4]	Input	Read address lock type
axi_Sxx_arcache_i[3:0][4]	Input	Read address memory type

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Port[1]	Type	Description
axi_Sxx_arprot_i[2:0][3]	Input	Read address protection type
axi_Sxx_arqos_i[3:0][4]	Input	Read address quality of service
axi_Sxx_arregion_i[3:0]	Input	Read address region
axi_Sxx_aruser_i[x:0][4]	Input	Read address user signal **Note:** x = *AXI User Width* – 1
axi_Sxx_arready_o[3]	Output	Read address ready
axi_Sxx_rvalid_o[3]	Output	Read data valid
axi_Sxx_rid_o[x:0]	Output	Read data ID **Note:** x = *External Manager AXI ID Width* – 1
axi_Sxx_rdata_o[x:0][3]	Output	Read data **Note:** x = Maximum Value for *External Manager <N> (Sxx) Address Width* across All Managers – 1
axi_Sxx_rresp_o[1:0][3]	Output	Read response
axi_Sxx_rlast_o	Output	Last read data transfer
axi_Sxx_ruser_o[x:0][4]	Output	Read response user signal **Note:** x = *AXI User Width* – 1
axi_Sxx_rready_i[3]	Input	Read ready

Notes:

1. All ports are applicable or optional when the AXI4 protocol is selected. Only selected ports are applicable when the AXI4-Lite protocol is selected as indicated by Note 2. Optional ports for the AXI4 protocol are indicated by Note 4.
2. xx denotes the external manager port number ranging from 0 to N, where N = (*Total External Managers* – 1). xx is formatted with a leading 0 when the port number is a single digit.
3. Applicable when the AXI4-Lite protocol is selected.
4. Optional when the AXI4 protocol is selected.

4.2.2. AXI4 External Subordinate Interface

Table 4.2. AXI4 External Subordinate Interface Ports

Port[1]	Type	Description
AXI Interconnect Manager yy Interface – Connected to External Subordinate yy[2]		
axi_Myy_awvalid_o[3]	Output	Write address valid
axi_Myy_awid_o[x:0]	Output	Write address ID **Note:** x = *External Subordinate AXI ID Width* – 1
axi_Myy_awaddr_o[x:0][3]	Output	Write address **Note:** x = Maximum Value for *External Subordinate <M> (Myy) Address Width* across All Subordinates – 1
axi_Myy_awlen_o[7:0]	Output	Write address burst length The exact number of transfers in a burst.
axi_Myy_awsize_o[2:0]	Output	Write address burst size The size of each transfer in the burst.
axi_Myy_awburst_o[1:0]	Output	Write address burst type
axi_Myy_awlock_o	Output	Write address lock type
axi_Myy_awcache_o[3:0]	Output	Write address memory type
axi_Myy_awprot_o[2:0][3]	Output	Write address protection type
axi_Myy_awqos_o[3:0]	Output	Write address quality of service
axi_Myy_awregion_o[3:0]	Output	Write address region
axi_Myy_awuser_o[x:0]	Output	Write address user signals **Note:** x = *AXI User Width* – 1
axi_Myy_awready_i[3]	Input	Write address ready
axi_Myy_wvalid_o[3]	Output	Write data valid
axi_Myy_wdata_o[x:0][3]	Output	Write data

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Port[1]	Type	Description
		Note: x = *External Subordinate <M> (Myy) Data Width* – 1
axi_Myy_wstrb_o[x:0][3]	Output	Write data strobes **Note:** x = (*External Subordinate <M> (Myy) Data Width*/8) – 1
axi_Myy_wlast_o[4]	Output	AXI4 last write beat/burst
axi_Myy_wuser_o[x:0]	Output	Write data user signal **Note:** x = *AXI User Width* – 1
axi_Myy_wready_i[3]	Input	Write data ready
axi_Myy_bvalid_i[3]	Input	Write response valid
axi_Myy_bid_i[x:0]	Input	Write response ID **Note:** x = *External Subordinate AXI ID Width* – 1
axi_Myy_bresp_i[1:0][3]	Input	Write response
axi_Myy_buser_i[x:0]	Input	Write response user signal **Note:** x = *AXI User Width* – 1
axi_Myy_bready_o[3]	Output	Write response ready
axi_Myy_arvalid_o[3]	Output	Read address valid
axi_Myy_arid_o[x:0]	Output	Read address ID **Note:** x = *External Subordinate AXI ID Width* – 1
axi_Myy_araddr_o[x:0][3]	Output	Read address **Note:** x = Maximum Value for *External Subordinate <M> (Myy) Address Width* across All Subordinates – 1
axi_Myy_arlen_o[7:0]	Output	Read address burst length
axi_Myy_arsize_o[2:0]	Output	Read address burst size
axi_Myy_arburst_o[1:0]	Output	Read address burst type
axi_Myy_arlock_o	Output	Read address lock type
axi_Myy_arcache_o[3:0]	Output	Read address memory type
axi_Myy_arprot_o[2:0][3]	Output	Read address protection type
axi_Myy_arqos_o[3:0]	Output	Read address quality of service
axi_Myy_arregion_o[3:0]	Output	Read address region
axi_Myy_aruser_o[x:0]	Output	Read address user signal **Note:** x = *AXI User Width* – 1
axi_Myy_arready_i[3]	Input	Read address ready
axi_Myy_rvalid_i[3]	Input	Read valid
axi_Myy_rid_i[x:0]	Input	Read data ID **Note:** x = *External Subordinate AXI ID Width* – 1
axi_Myy_rdata_i[x:0][3]	Input	Read data **Note:** x = *External Subordinate <M> (Myy) Data Width* – 1
axi_Myy_rresp_i[1:0][3]	Input	Read response
axi_Myy_rlast_i	Input	Last read data transfer
axi_Myy_ruser_i[x:0][4]	Input	Read response user signal **Note:** x = *AXI User Width* – 1
axi_Myy_rready_o[3]	Output	Read ready

Notes:

1. All ports are applicable or optional when the AXI4 protocol is selected. Only selected ports are applicable when the AXI4-Lite protocol is selected as indicated by Note 3. Optional ports for the AXI4 protocol are indicated by Note 4.
2. yy denotes the external subordinate port number ranging from 0 to M, where M = (*Total External Subordinates* – 1). yy is formatted with a leading 0 when the port number is a single digit.
3. Applicable when the AXI4-Lite protocol is selected.
4. Optional when the AXI4 protocol is selected.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

4.3. AHB-Lite

Figure 4.3 shows the interface diagram for the Unified Interconnect IP when the AHB-Lite protocol is selected. All AHB-Lite manager and subordinate interface signals are compliant with the AHB-Lite protocol. Refer to the AHB-Lite Protocol Specification web page for the timing diagrams and more information about the protocol.

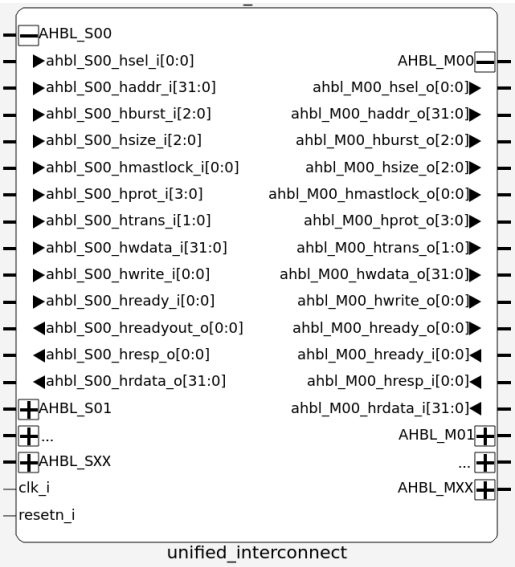


Figure 4.3. AHB-Lite Protocol Interface Diagram

4.3.1. AHB-Lite External Manager Interface

Table 4.3. AHB-Lite External Manager Interface Ports

Port	Type	Description
AHB-Lite Interconnect Subordinate xx Interface – Connected to External Manager xx[1]		
ahbl_Sxx hsel_i	Input	Subordinate select
ahbl_Sxx_haddr_i[x:0]	Input	Address **Note:** x = Maximum Value for *External Manager <N> (Sxx) Address Width* across All Managers – 1
ahbl_Sxx_hburst_i[2:0]	Input	Burst type (SINGLE, INCR, INCR4/8/16)
ahbl_Sxx_hsize_i[2:0]	Input	Transfer size (8, 16, 32, 64, 128, 256, 512, 1024)
ahbl_Sxx_hmastlock_i	Input	Current transfer is part of a locked transfer
ahbl_Sxx_hprot_i[3:0]	Input	Protection control
ahbl_Sxx_htrans_i[1:0]	Input	Transfer type of the current transfer (IDLE, BUSY, NSEQ, SEQ)
ahbl_Sxx_hwdata_i[x:0]	Input	Write data bus **Note:** x = *External Manager <N> (Sxx) Data Width* – 1
ahbl_Sxx_hwrite_i	Input	Indicates the transfer direction. 0 – Read transfer 1 – Write transfer
ahbl_Sxx_hready_i	Input	Indicates transfer completion.
ahbl_Sxx_hreadyout_o	Output	Indicates transfer completion. This signal is driven low by the subordinate to extend the transfer.
ahbl_Sxx_hresp_o	Output	Subordinate response (OKAY, ERROR)
ahbl_Sxx_hrdata_o[x:0]	Output	Read data bus **Note:** x = *External Manager <N> (Sxx) Data Width* – 1

Note:

1. xx denotes the external manager port number ranging from 0 to N, where N = (*Total External Managers* – 1). xx is formatted with a leading 0 when the port number is a single digit.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

4.3.2. AHB-Lite External Subordinate Interface

Table 4.4. AHB-Lite External Subordinate Interface Ports

Port[1]	Type	Description
AHB-Lite Interconnect Manager yy Interface – Connected to External Subordinate yy[1]		
ahbl_Myy_hsel_o	Output	Subordinate select
ahbl_Myy_haddr_o[x:0]	Output	Address **Note:** x = Maximum Value for *External Subordinate <M> (Myy) Address Width* across All Subordinates – 1
ahbl_Myy_hburst_o[2:0]	Output	Burst type (SINGLE, INCR, INCR4/8/16)
ahbl_Myy_hsize_o[2:0]	Output	Transfer size (8, 16, 32, 64, 128, 256, 512, 1024)
ahbl_Myy_hmastlock_o	Output	Current transfer is part of a locked transfer.
ahbl_Myy_hprot_o[3:0]	Output	Protection control
ahbl_Myy_htrans_o[1:0]	Output	Transfer type of the current transfer (IDLE, BUSY, NSEQ, SEQ)
ahbl_Myy_hwdata_o[x:0]	Output	Write data bus **Note:** x = *External Subordinate <M> (Myy) Data Width* – 1
ahbl_Myy_hwrite_o	Output	Indicates the transfer direction. 0 – Read transfer 1 – Write transfer
ahbl_Myy_hready_o	Output	Indicates transfer completion.
ahbl_Myy_hready_i	Input	Indicates transfer completion. This signal is driven low by the subordinate to extend the transfer.
ahbl_Myy_hresp_i	Input	Subordinate response (OKAY, ERROR)
ahbl_Myy_hrdata_i[x:0]	Input	Read data bus **Note:** x = *External Subordinate <M> (Myy) Data Width* – 1

Note:

1. yy denotes the external subordinate port number ranging from 0 to M, where M = (*Total External Subordinates* – 1). yy is formatted with a leading 0 when the port number is a single digit.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

4.4. APB

Figure 4.4 shows the interface diagram for the Unified Interconnect IP when the APB protocol is selected. All APB manager and subordinate interface signals are compliant with the APB protocol. Refer to the APB Protocol Specification web page for the timing diagrams and more information about the protocol.

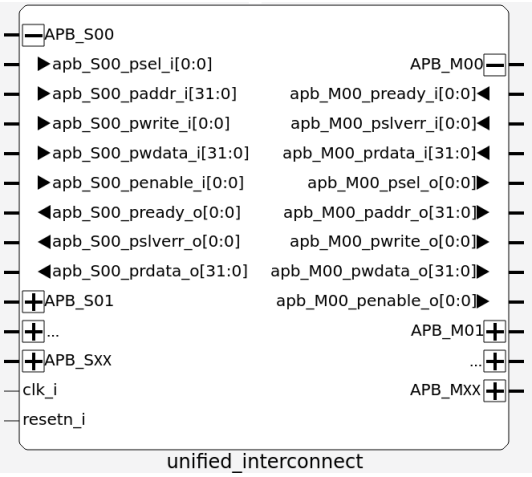


Figure 4.4. APB Protocol Interface Diagram

4.4.1. APB External Manager Interface

Table 4.5. APB External Manager Interface Ports

Port	Type	Description
APB Interconnect Subordinate xx Interface – Connected to External Manager xx[1]		
apb_Sxx_psel_i	Input	Select signal Indicates that this APB interface is selected and that a data transfer is required.
apb_Sxx_paddr_i[x:0]	Input	Address **Note:** x = Maximum Value for *External Manager <N> (Sxx) Address Width* across All Managers – 1
apb_Sxx_pwdata_i[x:0]	Input	Write data signal **Note:** x = *External Manager <N> (Sxx) Data Width* – 1
apb_Sxx_pwrite_i	Input	Indicates the transfer direction. 0 – Read transfer 1 – Write transfer
apb_Sxx_penable_i	Input	Enable signal Indicates the second and subsequent cycles of an APB transfer.
apb_Sxx_pready_o	Output	Ready signal Indicates transfer completion. This signal is used to extend an APB transfer.
apb_Sxx_pslverr_o	Output	Error signal Indicates a transfer failure.
apb_Sxx_prdata_o[x:0]	Output	Read data signal **Note:** x = *External Manager <N> (Sxx) Data Width* – 1

Note:

1. xx denotes the external manager port number ranging from 0 to N, where N = (*Total External Managers* – 1). xx is formatted with a leading 0 when the port number is a single digit.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

4.4.2. APB External Subordinate Interface

Table 4.6. APB External Subordinate Interface Ports

Port[1]	Type	Description
APB Interconnect Manager yy Interface – Connected to External Subordinate yy[1]		
apb_Myy_psel_o	Output	Select signal Indicates that the completer device is selected and that a data transfer is required.
apb_Myy_paddr_o[x:0]	Output	Address **Note:** x = Maximum Value for *External Subordinate <M> (Myy) Address Width* across All Subordinates – 1
apb_Myy_pwdata_o[x:0]	Output	Write data signal **Note:** x = *External Subordinate <M> (Myy) Data Width* – 1
apb_Myy_pwrite_o	Output	Indicates the transfer direction. 0 – Read transfer 1 – Write transfer
apb_Myy_penable_o	Output	Enable signal Indicates the second and subsequent cycles of an APB transfer.
apb_Myy_pready_i	Input	Ready signal Indicates transfer completion. Completer uses this signal to extend an APB transfer.
apb_Myy_pslverr_i	Input	Error signal Indicates a transfer failure. In case APB completer does not have this signal, it should be tied to 1'b0.
apb_Myy_prdata_i[x:0]	Input	Read data signal **Note:** x = *External Subordinate <M> (Myy) Data Width* – 1

Note:

1. yy denotes the external subordinate port number ranging from 0 to M, where M = (*Total External Subordinates* – 1). yy is formatted with a leading 0 when the port number is a single digit.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

5. Example Design

System on chip (SoC) templates are available in the Lattice Propel Builder design environment. SoC templates are pre-configured SoC designs that can be used as a starting point to quickly build and customize a system.

The following are the SoC templates that support the Unified Interconnect IP:

- Low Power Project
- SHA-3 CXU Project

Refer to the Lattice Propel Builder User Guide for more information.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

6. Designing with the IP

This section provides information on how to generate the IP core using the Lattice Radiant software. For more details on the Lattice Radiant software, refer to the Lattice Radiant Software User Guide.

Notes:

- Similar information applies for the Lattice Propel design environment. For more information, refer to the Lattice Propel Builder User Guide.
- The screenshots provided are for reference only. Details may vary depending on the version of the IP or software being used. If there have been no significant changes to the GUI, a screenshot may reflect an earlier version of the IP.

6.1. Generating and Instantiating the IP

You can use the Lattice Radiant software to generate IP modules and integrate them into the device architecture. The steps below describe how to generate the Unified Interconnect IP in the Lattice Radiant software.

To generate the Unified Interconnect IP:

1. Create a new Lattice Radiant software project or open an existing project.
2. Click the **IP Catalog** button to view the **IP Catalog** pane.
3. On the **IP on Local** tab, double-click **Unified Interconnect** under **IP/…/Processors_Controllers_and_Peripherals** category. The **Module/IP Block Wizard** opens.
   Note: If the IP is not available on the **IP on Local** tab, download the IP from the **IP on Server** tab.

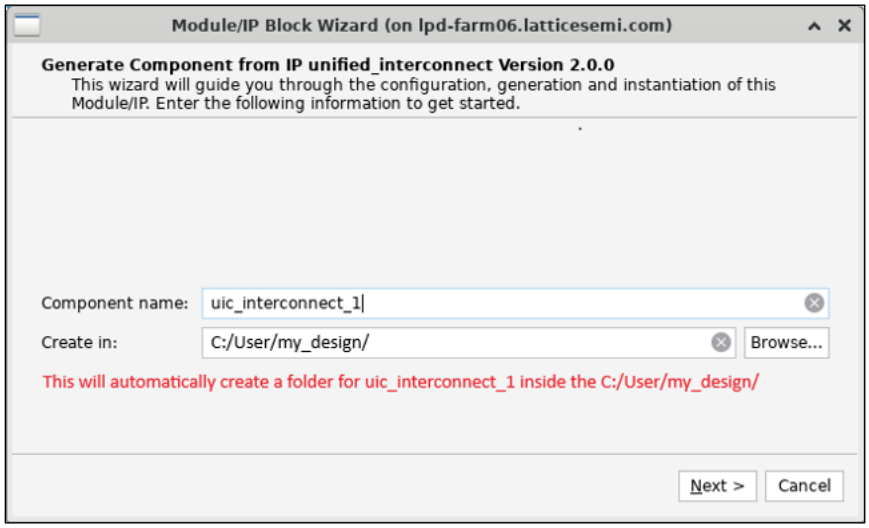


Figure 6.1. Module/IP Block Wizard

4. Enter values in the **Component name** and **Create in** fields, then click **Next**.
5. Customize the selected Unified Interconnect IP using drop-down lists and check boxes. Figure 6.2 shows an example configuration of the Unified Interconnect IP. For details on the configuration options, refer to the IP Parameter Description section.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

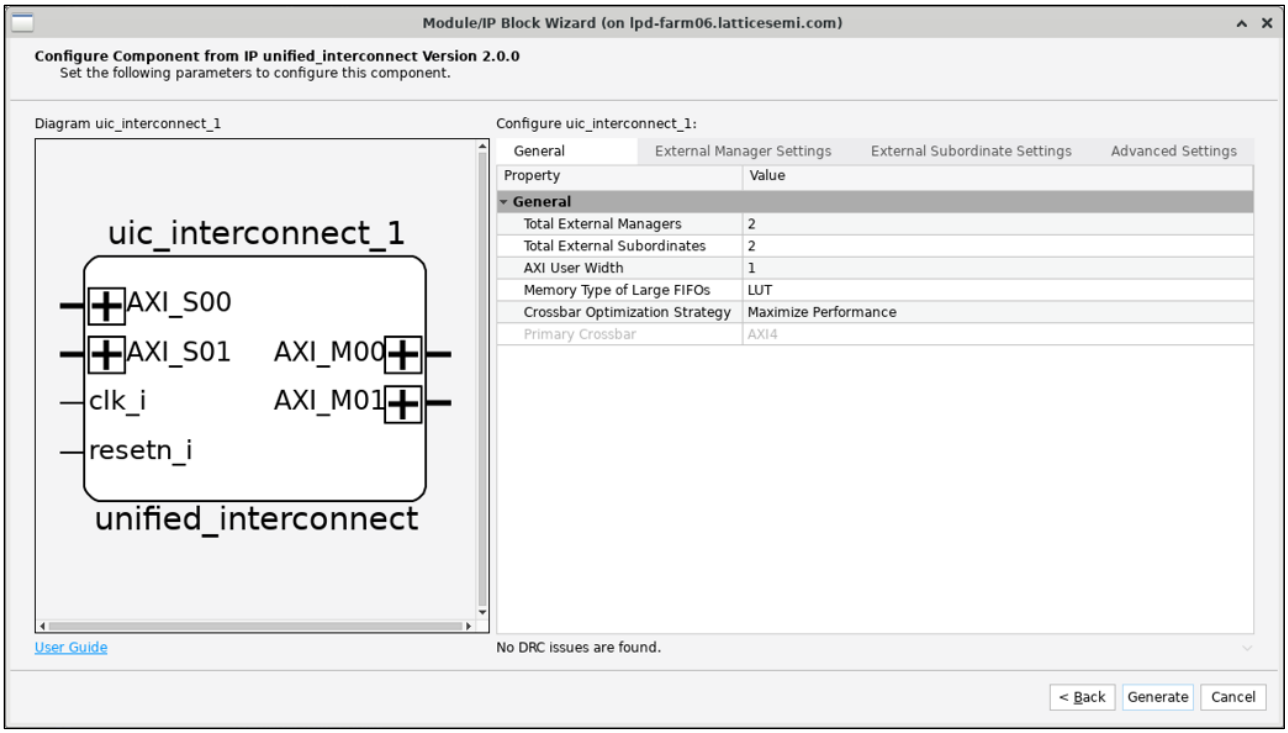


Figure 6.2. IP Configuration

6. Click **Generate**. The **Check Generated Result** window opens. This window shows design block messages and results.

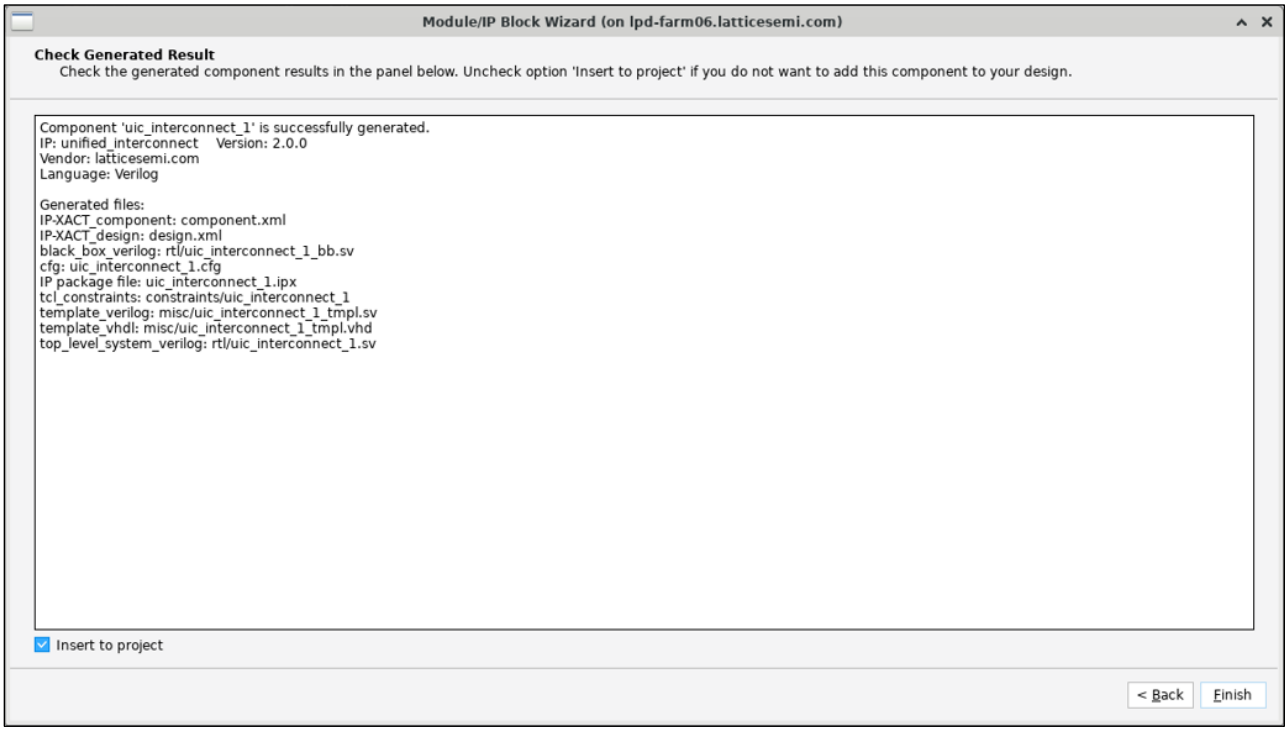


Figure 6.3. Check Generated Result

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

7. Click **Finish**. All generated files are placed in the directory specified by the **Component name** and **Create in** fields shown in Figure 6.1.

6.1.1. Generated Files and File Structure

The generated Unified Interconnect module package includes the closed-box (*<Component name>_bb.v*) and instance templates (*<Component name>_tmpl.v/vhd*) that can be used to instantiate the core in a top-level design. An example RTL top-level reference source file (*<Component name>.v*) that can be used as an instantiation template for the module is also provided. You may also use this example as the starting template for your top-level design. The generated files are listed in Table 6.1.

Table 6.1. Generated File List

Attribute	Description
<Component name>.ipx	Contains the information on the files associated with the generated IP.
<Component name>.cfg	Contains the parameter values used in IP configuration.
component.xml	Contains the ipxact: component information of the IP.
design.xml	Documents the configuration parameters of the IP in IP-XACT 2014 format.
rtl/<Component name>.v	Provides an example RTL top file that instantiates the module.
rtl/<Component name>_bb.v	Provides the synthesis closed-box.
misc/<Component name>_tmpl.v misc /<Component name>_tmpl.vhd	Provide instance templates for the module.

6.2. Design Implementation

Completing your design includes additional steps to specify analog properties, pin assignments, and timing and physical constraints. You can add and edit the constraints using the Device Constraint Editor or by manually creating a .pdc file.

Post-Synthesis constraint files (.pdc) contain both timing and non-timing *constraint.pdc* source files for storing logical timing/physical constraints. Constraints that are added using the Device Constraint Editor are saved to the active .pdc file. The active post-synthesis design constraint file is then used as input for post-synthesis processes.

Refer to the relevant sections in the Lattice Radiant Software User Guide for more information on how to create or edit constraints and how to use the Device Constraint Editor.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

6.3. Timing Constraints

The timing constraints are based on the clock frequency used. The timing constraints for the IP are defined in relevant constraint files. There are six clock groups in the Unified Interconnect IP as follows:

- Interconnect primary clock (clk_i) – required by the IP

```
create_clock [get_ports {clk_i}] -name clk -period <clock period in ns>
```

- Individual EM clock (Sxx_clk_i) – when *External Manager <N> (Sxx) CDC Enable* is checked and *External Manager <N> (Sxx) Protocol Type* is AXI4, AXI4-Lite, AHB-Lite, or APB

```
create_clock [get_ports {Sxx_clk_i[0]}] -name cdc_sxx_clk -period <Sxx clock
period in ns>
```

- Individual ES clock (Myy_clk_i) – when *External Subordinate <M> (Myy) CDC Enable* is checked and *External Subordinate <M> (Myy) Protocol Type* is AXI4, AXI4-Lite, AHB-Lite, or APB

```
create_clock [get_ports {Myy_clk_i[0]}] -name cdc_myy_clk -period <Myy clock
period in ns>
```

- Individual ES clock (axil_aclk_i) – when *Common Secondary AXI4-Lite External Subordinate CDC Enable* is checked and *External Subordinate <M> (Myy) Protocol Type* is Secondary AXI4-Lite

```
create_clock [get_ports {axil_aclk_i[0]}] -name cdc_axil_aclk -period <Myy
clock period in ns>
```

- Individual ES clock (ahbl_hclk_i) – when *Common Secondary AHB-Lite External Subordinate CDC Enable* is checked and *External Subordinate <M> (Myy) Protocol Type* is Secondary AHB-Lite

```
create_clock [get_ports {ahbl_hclk_i[0]}] -name cdc_ahbl_hclk -period <Myy
clock period in ns>
```

- Individual ES clock (apb_clk_i) – when *Common Secondary APB External Subordinate CDC Enable* is checked and *External Subordinate <M> (Myy) Protocol Type* is Secondary APB

```
create_clock [get_ports {apb_pclk_i[0]}] -name cdc_apb_pclk -period <Myy
clock period in ns>
```

Note: xx denotes the external manager port number ranging from 0 to N, where N = (*Total External Managers* – 1). xx is formatted with a leading 0 when the port number is a single digit. yy denotes the external subordinate port number ranging from 0 to M, where M = (*Total External Subordinates* – 1). yy is formatted with a leading 0 when the port number is a single digit.

The following timing constraints are optional and can relax timing requirements depending on the IP configuration:

- When *Primary Crossbar* is AHB-Lite:
  - If *External Manager <N> (Sxx) CDC Enable* is checked

```
set_max_delay -from [get_cells */*/*MAS_BLK*<N>*/*/*/s_*_latched*reg*] -to
[get_cells */*/*MAS_BLK*<N>*/*/*/m_*_latched*.*] <choose the lowest value
of clock period in ns and Sxx clock period in ns >
set_max_delay -from [get_cells */*/*MAS_BLK*<N>*/*/*/m_*_latched*reg*] -to
[get_cells */*/*MAS_BLK*<N>*/*/*/s_*_latched*.*] <choose the lowest value
of clock period in ns and Sxx clock period in ns>
```

  - If *External Subordinate <M> (Myy) CDC Enable* is checked and *External Subordinate <M> (Myy) Protocol Type* is AHB-Lite or AXI4-Lite

```
set_max_delay -from [get_cells */*/*SLV_BLK*<M>*/*/*/s_*_latched*reg*] -to
[get_cells */*/*SLV_BLK*<N>*/*/*/m_*_latched*.*] <choose the lowest value
of clock period in ns and Myy clock period in ns>
set_max_delay -from [get_cells */*/*SLV_BLK*<M>*/*/*/m_*_latched*reg*] -to
[get_cells */*/*SLV_BLK*<M>*/*/*/s_*_latched*.*] < choose the lowest value
of clock period in ns and Myy clock period in ns>
```

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

- If *External Subordinate <M> (Myy) CDC Enable* is checked and *External Subordinate <M> (Myy) Protocol Type* is APB

```
set_max_delay -from [get_cells */*/*SLV_BLK*<M>*/*/apb_paddr_r_reg*] -to
[get_cells */*/*SLV_BLK*<M>*/*/*p_paddr_r*] <choose the lowest value of
clock period in ns and Myy clock period in ns>
set_max_delay -from [get_cells */*/*SLV_BLK*<M>*/*/apb_pwrite_r_reg*] -to
[get_cells */*/*SLV_BLK*<M>*/*/*p_pwrite_r*] <choose the lowest value of
clock period in ns and Myy clock period in ns>
set_max_delay -from [get_cells */*/*SLV_BLK*<M>*/*/apb_pwdata_r_reg*] -to
[get_cells */*/*SLV_BLK*<M>*/*/*p_pwdata_r*] <choose the lowest value of
clock period in ns and Myy clock period in ns>
set_max_delay -from [get_cells */*/*SLV_BLK*<M>*/*/*p_prdata_r*.*] -to
[get_cells */*/*SLV_BLK*<M>*/*/*hrdata_o*.*] <choose the lowest value of
clock period in ns and Myy clock period in ns>
```

- If *Common Secondary AXI4-Lite External Subordinate CDC Enable* is checked and *External Subordinate <M> (Myy) Protocol Type* is Secondary AXI4-Lite

```
set_max_delay -from [get_cells */*/*SLV_BLK*<secondary protocol interface
index>*/*/*/s_*_latched*reg*]] -to [get_cells */*/*SLV_BLK*<secondary
protocol interface index[1]>*/*/*/m_*_latched*.*] <choose the lowest value of
clock period in ns and Myy clock period in ns>
set_max_delay -from [get_cells */*/*SLV_BLK*<secondary protocol interface
index>*/*/*/m_*_latched*reg*] -to [get_cells */*/*SLV_BLK*< secondary
protocol interface index[1]>*/*/*/s_*_latched*.*] <choose the lowest value of
clock period in ns and Myy clock period in ns>
```

- If *Common Secondary APB External Subordinate CDC Enable* is checked and *External Subordinate <M> (Myy) Protocol Type* is Secondary APB

```
set_max_delay -from [get_cells */*/*SLV_BLK*<secondary protocol interface
index>*/*/apb_paddr_r_reg*] -to [get_cells */*/*SLV_BLK*<secondary
protocol interface index[1]>*/*/*p_paddr_r*] <choose the lowest value of
clock period in ns and Myy clock period in ns>
set_max_delay -from [get_cells */*/*SLV_BLK*<secondary protocol interface
index>*/*/apb_pwrite_r_reg*] -to [get_cells */*/*SLV_BLK*<secondary
protocol interface index[1]>*/*/*p_pwrite_r*] <choose the lowest value of
clock period in ns and Myy clock period in ns>
set_max_delay -from [get_cells */*/*SLV_BLK*<secondary protocol interface
index>*/*/apb_pwdata_r_reg*] -to [get_cells */*/*SLV_BLK*<secondary
protocol interface index[1]>*/*/*p_pwdata_r*] <choose the lowest value of
clock period in ns and Myy clock period in ns>
set_max_delay -from [get_cells */*/*SLV_BLK*<secondary protocol interface
index>*/*/*p_prdata_r*.*] -to [get_cells */*/*SLV_BLK*<secondary protocol
interface index[1]>*/*/*hrdata_o*.*] <choose the lowest value of clock period
in ns and Myy clock period in ns>
```

Note: The secondary protocol interface index can be determined as follows. First, count all primary protocols regardless of type to obtain the base interface index for secondary protocols. Then, identify each unique secondary protocol in the order of its first appearance. Assign each unique secondary protocol a sequential interface index starting from the base interface index. Refer to Appendix B. Determining the Secondary Protocol Interface Index for a Python script to assist with this task.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

- When *Primary Crossbar* is APB
  - If *External Manager <N> (Sxx) CDC Enable* is checked

```
set_max_delay -from [get_cells */*/*MAS_BLK*<N>*/*/*/*s_latched*reg*] -to
[get_cells */*/*MAS_BLK*<N>*/*/*/*m_p*reg*] <choose the lowest value of
clock period in ns and Sxx clock period in ns>
set_max_delay -from [get_cells */*/*MAS_BLK*<N>*/*/*/*m_latched*reg*] -to
[get_cells */*/*MAS_BLK*<N>*/*/*/*s_p*reg*] <choose the lowest value of
clock period in ns and Sxx clock period in ns>
```

  - If *External Subordinate <M> (Myy) CDC Enable* is checked

```
set_max_delay -from [get_cells */*/*SLV_BLK*<M>*/*/*/*s_latched*reg*] -to
[get_cells */*/*SLV_BLK*<M>*/*/*/*m_p*reg*] <choose the lowest value of
clock period in ns and Myy clock period in ns>
set_max_delay -from [get_cells */*/*SLV_BLK*<M>*/*/*/*m_latched*reg*] -to
[get_cells */*/*SLV_BLK*<M>*/*/*/*s_p*reg*] <choose the lowest value of
clock period in ns and Myy clock period in ns>
```

The example below shows the IP timing constraints generated for the Unified Interconnect IP for the following IP configuration:

- Crossbar clock = 125 MHz
- Two external managers
- External manager 0: CDC enabled, supplied clock = 120 MHz
- Two external subordinates
- External subordinate 0: CDC enabled, supplied clock = 80 MHz

For timing closure, add the following timing constraints in the .pdc file:

```
create_clock [get_ports {clk_i}] -name clk -period 8.000
create_clock [get_ports {S00_clk_i}] -name cdc_s00_clk -period 8.333
create_clock [get_ports {M00_clk_i}] -name cdc_m00_clk -period 12.500
```

For more information on timing constraints, refer to the Lattice Radiant Timing Constraints Methodology (FPGA-AN-02059).

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

7. Design Considerations

7.1. Limitations

Limitations of the Unified Interconnect IP include the following:

- All external managers and external subordinates must share the same data width. Data width conversion is not currently supported.
- The maximum value for *External Subordinate <M> (Myy) Address Width* across all subordinates must not be less than the maximum value for *External Manager <N> (Sxx) Address Width* across all managers.
- WRAP bursts are not supported for AXI4 to AXI4-Lite conversion.
- For a read transaction, the default subordinate returns RRESP = DECERR. Because the default subordinate does not provide a valid read data, the RDATA value is undefined and may contain residual data from a previous transfer. Therefore, software or logic must ignore the read data when a DECERR response is returned.
- During an AXI4 external manager request to the AXI4 external subordinate:
  - AxQOS, AxREGION, AxUSER, AxCACHE, and AxLOCK signals are ignored when transactions are forwarded to an external AXI4-Lite subordinate interface.
  - AxQOS, AxREGION, AxUSER, AxCACHE, AxLOCK, and AxPROT signals are preserved when transactions are forwarded to an external AXI4 subordinate interface.
  - AXI4 exclusive access tracking is not supported.
- For protocol conversion:
  - AHB-Lite to AXI4
    - Locked transfers issued on the AHB-Lite interface (HMASTLOCK asserted) are not supported when crossing to AXI4 and are therefore ignored.
  - AXI4 to APB
    - The BUSER signal returned on the AXI4 write response channel reflects the value captured from the corresponding AWUSER field while the RUSER signal returned on the AXI4 read data channel reflects the value captured from the corresponding ARUSER field.
    - The AXI4 address-related attributes AxQOS, AxREGION, AxUSER, AxCACHE, AxLOCK, and AxPROT are not used by the APB interface and are therefore ignored by the bridge.
    - Unaligned AXI4 addresses are forwarded to the APB external subordinate without modification. Read data returned from the APB interface is forwarded back to the AXI4 external manager without address-based adjustment or data realignment performed by the bridge.
  - AXI4 to AHB-Lite
    - The AXI4 attributes and signals AxQOS, AxREGION, AxUSER, AxCACHE, AxLOCK, and WSTRB are not supported by the AHB-Lite interface and are therefore ignored.
    - Unaligned AXI4 addresses are not supported for burst transfers. Any burst transaction issued with an unaligned address consistently results in an AXI4 error response (SLVERR).
  - All connected external managers and subordinates are required to use an identical data bus width. Mismatched interface widths are not supported in this version of the IP.

7.2. Exporting Manager and Subordinate Interfaces

Beginning with Lattice Propel Builder software 2026.1, feedthrough IPs are no longer required to export AXI4, AHB-Lite, and APB external manager and subordinate interfaces out of the subsystem created in Propel. Refer to the Lattice Propel Builder User Guide for more information.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

7.3. Design Considerations for Throughput

7.3.1. Burst Transfer

The following are design considerations when implementing burst transfer:

- In the SAMD crossbar architecture, to prevent bubbles in the WDATA or RDATA channel during performance-critical AXI4 transfers, the burst length must be greater than or equal to the shared address channel grant and routing latency. This ensures that bubbles are not introduced in the WDATA or RDATA channel.
- You can optionally configure the queue depth at the EM or ES interface, through the *External Manager Write Address Buffer Depth N*, *External Manager Read Address Buffer N*, *External Subordinate Write Address Buffer Depth M*, or *External Subordinate Read Address Buffer Depth M* attributes as applicable, to reduce the impact of address grant bottlenecks. For example, EM1-to-ES1 transfers can be queued behind stalled EM0-to-ES0 transfers.
- With a shared write response channel, there is a small grant delay in the write response (B channel). You can optionally configure the external manager response FIFO, through the *External Manager Write Response Buffer Depth N* attribute, to minimize the impact of response path bottlenecks.

7.3.2. AXI4 Pipelining Transfer

In pipelining transfer, a new transaction is accepted before the previous transaction is completed. The following sections describe design considerations when pipelining for write and read transactions and performing bottleneck clearance.

Note: The examples discussed in this section are based on the SAMD crossbar architecture with the Round Robin arbiter scheme setting for the *External Manager Priority* attribute.

7.3.2.1. Write Transaction

After the address phase grant for an EM, a two-clock bubble occurs. This results in a minimum of three clock cycles between successive arbitrations by the same EM due to internal tracking pipe stages. For example:

- With only one EM actively issuing transaction requests:
  - After granting an ES to the EM, the address phase processing unit will not grant to the same EM for two clock cycles.
  - If awlen ≥ 2, no bubble is introduced in WDATA.

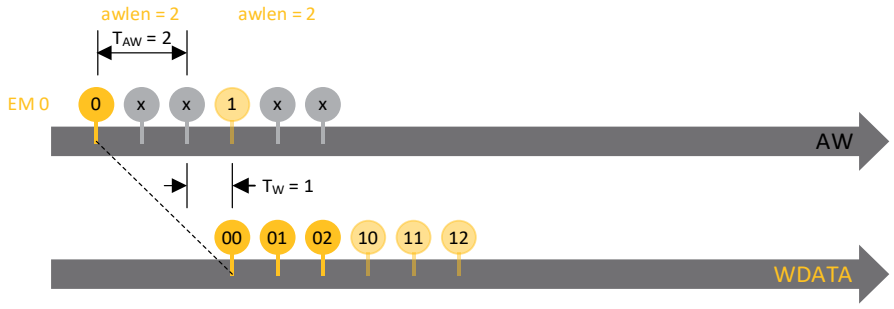


Figure 7.1. Write Transactions for One Active EM with awlen ≥ 2

- With up to four EMs actively issuing transaction requests:
  - The address phase processing unit grants to the EMs back-to-back.
  - When there are many EMs actively issuing transaction requests, a larger burst awlen might be required to avoid bubbles in WDATA.
    - If burst awlen = 2 for four EMs, a bubble is introduced in WDATA for each transaction.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

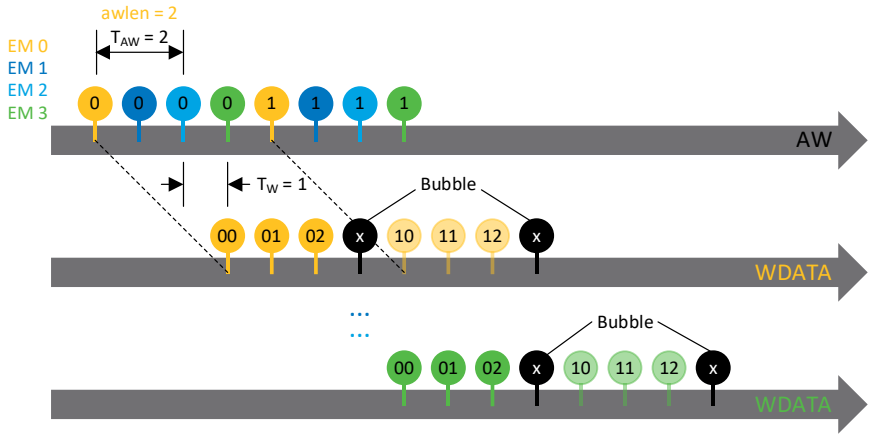


Figure 7.2. Write Transactions for Four Active EMs with awlen = 2

- If burst awlen ≥ 3 for four EMs, no bubble is introduced in WDATA.

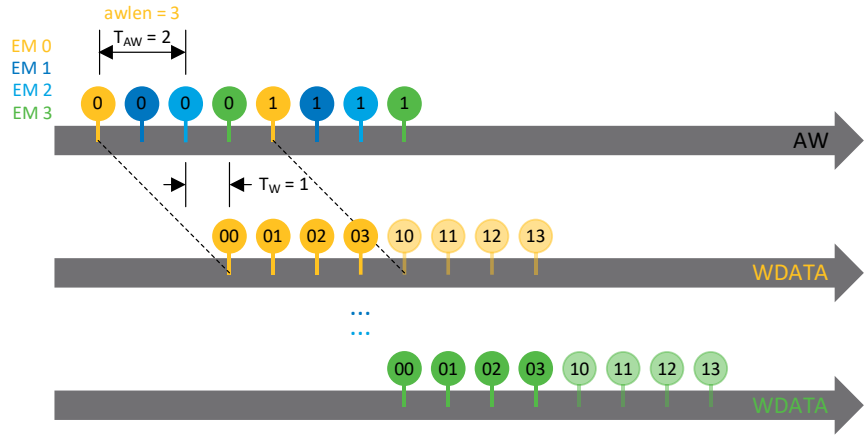


Figure 7.3. Write Transactions for Four Active EMs with awlen ≥ 3

7.3.2.2. Read Transaction

After the address phase grant for an EM, a two-clock bubble occurs. This results in a minimum of three clock cycles between successive arbitrations by the same EM due to internal tracking pipeline stages. For example:

- With only one EM actively issuing transaction requests:
  - After granting an ES to the EM, the address phase processing unit will not grant to the same EM for two clock cycles.
  - If the back-to-back read address request interval < burst arlen, no bubble is introduced in RDATA.

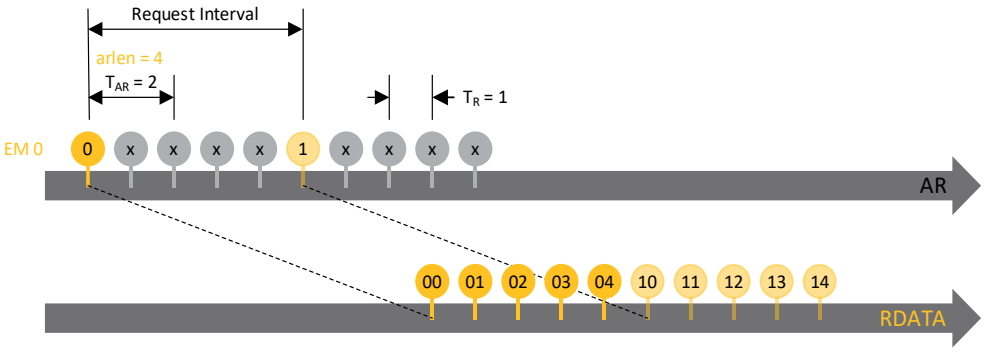


Figure 7.4. Read Transactions for One Active EM with Request Interval < arlen

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

- If the back-to-back AR request interval > burst arlen, bubbles are introduced in RDATA.

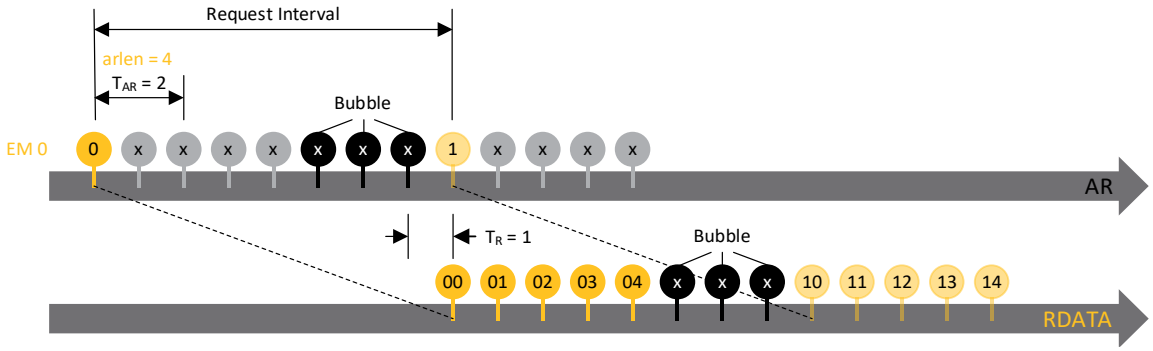


Figure 7.5. Read Transactions for One Active EM with arlen ≤ Request Interval

- To ensure back-to-back read data requests do not introduce bubbles in RDATA, the following condition must be met:
- *External Manager <N> (Sxx) Read Acceptance Limit* × [Time to transfer (arlen + 1) × arsize] ≥ Memory Read Round Trip Latency

  Note: Memory Read Round Trip Latency is defined as the time from the read address request to an external subordinate device until the first beat of read data return arrives at the external manager.

- With up to four EMs actively issuing transaction requests:
  - The address phase processing unit grants to the EMs back-to-back.
  - When there are many EMs actively issuing transaction requests, a larger burst arlen might be required to avoid bubbles in RDATA.
    - If burst arlen = 2 for four EMs, a bubble is introduced in RDATA for each transaction.

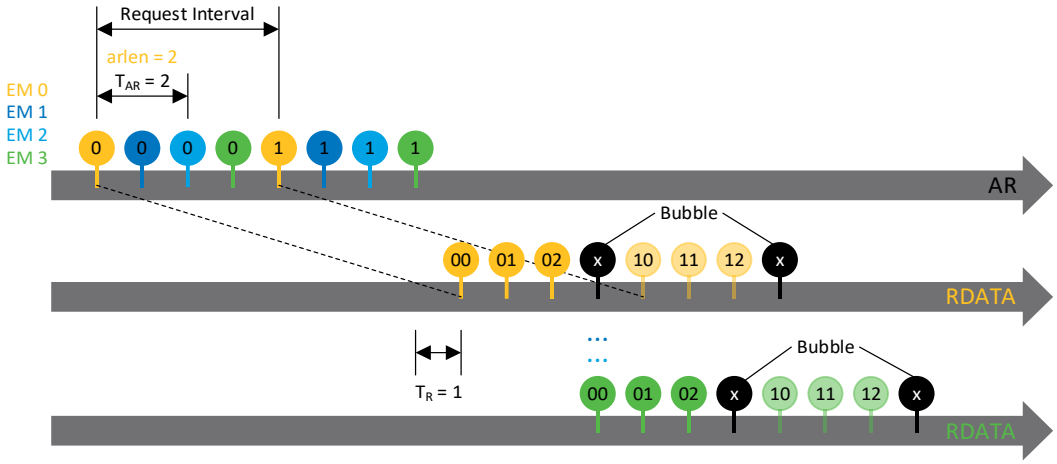


Figure 7.6. Read Transactions for Four Active EMs with arlen = 2

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

- If burst arlen ≥ 3 for four EMs, no bubble is introduced in RDATA.

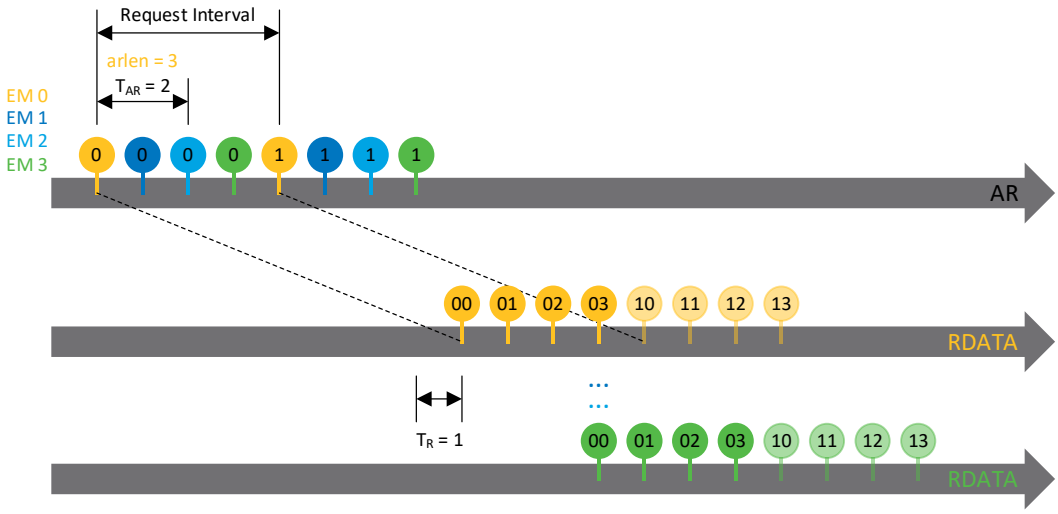


Figure 7.7. Read Transactions for Four Active EMs with arlen ≥ 3

7.3.3. AXI4 Bottleneck Clearance

The following are design considerations to address various bottlenecks:

- Handling low-performance or slow external subordinate devices
  - To prevent back-pressure from propagating to the shared address processing unit, allocate the optional queue at the external subordinate. This queue acts as a buffer to temporarily store transactions and avoid stalling upstream components.
  - Similarly, allocate the read data channel queue at the external subordinate to handle incoming read data. This queue accumulates read data until the system is ready to route it back to the external manager. This ensures smooth data flow and prevents data delays.
- Handling slow external manager devices
  - Allocate the optional queue at the external manager. This queue accumulates write data until the path to the external subordinate is granted.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

7.4. Design Considerations for Latency

Notes:

- T_{EM} and T_{ES} denote the EM interface and ES interface latencies, respectively.
- T_{DP} denotes the latency introduced by the additional pipestage added within the address decoder, which is applicable only when *Primary Crossbar* = AXI4. The default T_{DP} is 0 clock cycles. If *Enable Crossbar Address Decode Pipestage* is checked, T_{DP} is 1 clock cycle.

7.4.1. Sub-IP Block Latency

7.4.1.1. Crossbar Latency

Table 7.1 shows the minimum AXI4 crossbar latency for the SAMD and SASD crossbar architecture.

Table 7.1. Minimum AXI4 Crossbar Latency

Channel	Latency (Clock Cycle)
Read Address	2 + T_{DP}
Write Address	2 + T_{DP}
Write Data	0
Write Response	1
Read Data	0 (SAMD); 1 (SASD)

Table 7.2 shows the minimum AHB-Lite crossbar latency. Note that for the AHB-Lite protocol, the baseline latency is two clock cycles: one clock cycle for the address phase and one clock cycle for the data phase. Latency only increases if the data phase is extended by HREADY wait states.

Table 7.2. Minimum AHB-Lite Crossbar Latency

Phase	Latency (Clock Cycle)
Read Request	0
Write Request	0
Write Response	0
Read Data and Response	0

Table 7.3 shows the minimum APB crossbar latency. Note that for the APB protocol, the baseline latency is two clock cycles: one clock cycle for the setup phase and one clock cycle for the access phase. Latency only increases if the access phase is extended by PREADY wait states with no pipelining between transfers.

Table 7.3. Minimum APB Crossbar Latency

Phase	Latency (Clock Cycle)
Read Request	1
Write Request	1
Write Response	0
Read Data and Response	0

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

7.4.1.2. EM or ES Interface Latency

Table 7.4 shows additional latencies introduced by the EM or ES AXI4 interface. When CDC and register slice are enabled, clock cycles are measured with respect to the slower clock domain.

Table 7.4. Additional Latency Introduced by Optional Couplers at EM or ES AXI4 Interface with Primary Crossbar = AXI4

Channel	Latency (Clock Cycle), T_{EM} or T_{ES}				
	Queue without CDC		Queue with CDC		Enable Data Register Slice
	LUT	EBR	LUT	EBR	LUT
Address	1	3	7	7	1
Write Data	1	3	7	7	1
Write Response	1	3	7	7	1
Read Data and Response	1	3	7	7	1

Table 7.5 shows additional latencies introduced by the EM or ES AHB-Lite or APB interface.

Table 7.5. Additional Latency Introduced by Optional Couplers at EM or ES AHB-Lite Interface with Primary Crossbar = AHB-Lite or APB Interface with Primary Crossbar = APB

Phase	Latency[1] (Clock Cycle), T_{EM} or T_{ES}	
	CDC Enable	Enable Data Register Slice
Read Request	4	2
Write Request	5	3
Write Response	5	3
Read Data and Response	5	3

Note:

1. If both CDC and register slice are enabled, latency is determined solely by *CDC Enable*. This is because both features share the same module.

Table 7.6 shows additional latencies introduced by the EM or ES interface for protocol conversion.

Table 7.6. Additional Latency Introduced by Optional Couplers at EM or ES Interface for Protocol Conversion

Bridge	Symbol	Latency (Clock Cycle)
AXI4/AXI4-Lite to AHB-Lite Write Request	$T_{WR_AXI4toAHBL}$	3
AXI4/AXI4-Lite to AHB-Lite Read Request	$T_{RR_AXI4toAHBL}$	1
AXI4/AXI4-Lite to AHB-Lite Write Resp	$T_{WRSP_AXI4toAHBL}$	2
AXI4/AXI4-Lite to AHB-Lite Read Resp	$T_{RRSP_AXI4toAHBL}$	1
AXI4/AXI4-Lite to APB Write Request	$T_{WR_AXI4toAPB}$	3
AXI4/AXI4-Lite to APB Read Request	$T_{RR_AXI4toAPB}$	2
AXI4/AXI4-Lite to APB Write Resp	$T_{WRSP_AXI4toAPB}$	2
AXI4/AXI4-Lite to APB Read Resp	$T_{RRSP_AXI4toAPB}$	1
AHB-Lite to AXI4 Write Request	$T_{WR_AHBLtoAXI4}$	3
AHB-Lite to AXI4 Read Request	$T_{RR_AHBLtoAXI4}$	2
AHB-Lite to AXI4 Write Resp	$T_{WRSP_AHBLtoAXI4}$	2
AHB-Lite to AXI4 Read Resp	$T_{RRSP_AHBLtoAXI4}$	2
AHB-Lite to AXI4-Lite Write Request	$T_{WR_AHBLtoAXI4L}$	4
AHB-Lite to AXI4-Lite Read Request	$T_{RR_AHBLtoAXI4L}$	2
AHB-Lite to AXI4-Lite Write Resp	$T_{WRSP_AHBLtoAXI4L}$	2
AHB-Lite to AXI4-Lite Read Resp	$T_{RRSP_AHBLtoAXI4L}$	2
AHB-Lite to APB Write Request	$T_{WR_AHBLtoAPB}$	2
AHB-Lite to APB Read Request	$T_{RR_AHBLtoAPB}$	1
AHB-Lite to APB Write Resp	$T_{WRSP_AHBLtoAPB}$	1

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Bridge	Symbol	Latency (Clock Cycle)
AHB-Lite to APB Read Resp	$T_{RRSP_AHBLtoAPB}$	1

7.5. Design Considerations for Resource Utilization

The following sections describe options to reduce resource utilization within the internal logic.

7.5.1. Exclude Internal Default Subordinate

For a closed system that guarantees all addresses are valid, you may choose to disable the default subordinate.

Table 7.7. Default Subordinate Configuration

Primary Crossbar	*Enable Default Subordinate*	Description
AXI4	Unchecked	Default subordinate logic is excluded.
AHB-Lite	—	—
APB	—	—

7.5.2. Exclude Redundant AXI Interface Access Type

You can exclude an unused AXI4 channel. Do not initiate any transfers targeting the invalid AXI4 channel. The following access operations are illegal:

- Write access to external subordinate with **Access Type* = RO
- Read access to external subordinate with **Access Type* = WO

Table 7.8. Access Type Configuration

Interface	Attributes				Description
	Primary Crossbar	*Enable Default Subordinate*	**Protocol Type*	**Access Type*	
External Manager	Any	—	AXI4 or AXI4-Lite	WO	Read channel signals (axi_Sxx_ar* and axi_Sxx_r*) and related logic are excluded.
	Any	—	AXI4 or AXI4-Lite	RO	Write channel signals (axi_Sxx_aw*, axi_Sxx_w* and axi_Sxx_b*) and related logic are excluded.
External Subordinate	AXI4	Checked[1]	AXI4 or AXI4-Lite	WO	Read channel signals (axi_Myy_ar* and axi_Myy_r*) and related logic are excluded.
	AHB-Lite	—	AXI4 or AXI4-Lite		
	Any	Checked[1]	Secondary AXI4-Lite		
	AXI4	Checked[1]	AXI4 or AXI4-Lite	RO	Write channel signals (axi_Myy_aw*, axi_Myy_w* and axi_Mxx_b*) and related logic are excluded.
	AHB-Lite	—	AXI4 or AXI4-Lite		
	Any	Checked[1]	Secondary AXI4-Lite		

Note:

1. Invalid access is routed to the default subordinate on the primary crossbar.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

7.5.3. Exclude Redundant Crossbar Route

For a system with a known access path, redundant routes can be excluded through crossbar path restrictions with a configured connectivity map. Invalid access is routed to the internal default subordinate.

Table 7.9. External Manager to External Subordinate Connectivity Settings

Primary IC (Primary Crossbar)	Connectivity Setting	Description
AXI4, AHB-Lite	*Enable Link to Subordinate** (an EM to an ES)	Excludes an EM read or write access path to an ES with **Protocol Type* = AXI4, AXI4-Lite, AHB-Lite, or APB.
AXI4, AHB-Lite	*Enable Link to Common Secondary AXI4-Lite* (an EM to any ES with similar protocol type)	Excludes an EM read or write access path to all ESs with **Protocol Type* = Secondary AXI4-Lite.
AXI4	*Enable Link to Common Secondary AHB-Lite* (an EM to any ES with similar protocol type)	Excludes an EM read or write access path to all ESs with **Protocol Type* = Secondary AHB-Lite.
AXI4, AHB-Lite	*Enable Link to Common Secondary APB* (an EM to any ES with similar protocol type)	Excludes an EM read or write access path to all ESs with **Protocol Type* = Secondary APB.
APB	—	—

For example, consider the following configuration:

- *Total External Manager* = 4
- *Total External Subordinates* = 4
- Only one EM (EM0) accesses an ES (ES0) with **Protocol Type* = APB (primarily for register access)
- *Enable Link to Subordinate 0 (M00)* is unchecked for EM1, EM2, and EM3.

The following are characteristics of this configuration:

- ES0 accepts only write data from EM0. The write data multiplexer (MUX) is downgraded from a 4:1 MUX (group 2) to no MUX (group 0), thereby freeing 2 × Data Width of LUT4 elements.
- EM0 continues accepting read data returned from ES0, ES1, ES2, and ES3. There is no optimization to the read data MUX.

Table 7.10 shows the MUX groupings and LUT4 resource utilization. Table 7.11 shows the estimated savings in LUT4 resource utilization.

Table 7.10. LUT4 MUX Groupings

Group	MUX Gang	Number of LUT4 Elements per Data Bit through MUX
0	No MUX	0 × Data Width
1	2:1	1 × Data Width
2	3:1 to 4:1	2 × Data Width
3	5:1 to 8:1	4 × Data Width
4	9:1 to 16:1	8 × Data Width

Table 7.11. Estimated Savings in LUT4 Resource Utilization

Initial Grouping	Downgraded Grouping	LUT4 Resource Utilization Savings
Any	0	100%
2	1	50%
3	1	75%
4	1	87.5%
3	2	50%
4	2	75%
4	3	50%

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

7.5.4. Secondary Interconnect

The secondary IC should be enabled only when there are multiple subordinates that can be grouped together based on protocol, clock domain, and reset domain. Otherwise, connection through the primary IC is recommended to avoid unnecessary hierarchy and overhead. For external subordinates operating on a protocol different from the primary crossbar protocol:

- If an external subordinate connects directly to the primary IC, a dedicated internal protocol conversion bridge is required, along with any necessary CDC logic.
- When multiple subordinates share the same protocol type and common clock and reset domains, grouping them by selecting *External Subordinate * Protocol Type = Secondary** enables a shared protocol conversion path. This ganging approach reduces the number of protocol conversion bridges, minimizes CDC logic, and improves overall resource utilization.

7.6. Design Considerations for Timing (f_{MAX})

7.6.1. Enable Data Register Slice

You may optionally configure the following register slice options to improve interface timing:

- *External Manager * Data Register Slice Enable* to improve timing on interface signals to and from a manager unit.
- *External Subordinate * Data Register Slice Enable* to improve timing on interface signals to and from a subordinate unit.

Enabling register slices introduces additional latency as follows:

- AXI4 interface: Introduces one additional clock cycle of latency on each channel.
- AHB-Lite interface: AHB-Lite bursts are decomposed into individual single transfers. Refer to the AHB-Lite Burst Decomposition section for details.
- APB interface: Introduces one additional clock cycle of latency in each direction.

7.6.2. Enable Crossbar Address Decode Pipestage

As the number of external subordinate fragments increases, the address decoding logic may become more complex. To improve timing, you may optionally enable the crossbar address decode pipeline stage to optimize the AXI4 AR and AW address decoding paths. Enabling this option introduces an additional one clock cycle of latency on the AXI4 AR and AW channels.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Appendix A. Resource Utilization

Note: Resource utilization values in this section are provided for reference only and may change based on the compilation strategy and selected tool options.

Table A.1 through Table A.11 show sample resource utilizations of the Unified Interconnect IP core on CertusPro-NX (LFCPNX-100-8ASG256I) and Avant (LAV-AT-X70-1LFG1156C) devices, where applicable.

Maximize Performance Mode

For the sample resource utilizations shown in this section, the following IP configuration applies:

- *External Manager <N> (Sxx) Protocol Type* = AXI4
- *External Subordinate <M> (Myy) Protocol Type* = AXI4
- *Crossbar Optimization Strategy* = Maximize Performance
- *External Manager <N> (Sxx) Address Width* = 32 bits
- *External Subordinate <M> (Myy) Address Width* = 32 bits
- *External Manager AXI ID width* = 2 bits
- *External Subordinate <M> (Myy) Fragment Cnt* = 1
- *External Manager Priority* = Round Robin
- *External Manager <N> (Sxx) Write Acceptance Limit* = 4
- *External Manager <N> (Sxx) Read Acceptance Limit* = 4
- No CDC unless otherwise specified

Table A.1. Resource Utilization and f_{MAX} for 64-bit Data Width in Maximize Performance Mode (4 EMs and 4 ESs)

Device	Total EMs	Total ESs	LUTs	Registers	f_{MAX} (MHz)
CertusPro-NX	4	4	3619	1976	150
Avant	4	4	3569	1978	200

Table A.2. Resource Utilization and f_{MAX} for 64-bit Data Width in Maximize Performance Mode (8 EMs and 8 ESs)

Device	Total EMs	Total ESs	LUTs	Registers	f_{MAX} (MHz)
CertusPro-NX	8	8	12356	3894	130
Avant	8	8	12422	3900	180

Table A.3. Resource Utilization for 32-bit Data Width without CDC in Maximize Performance Mode

Device	Total EMs	Total ESs	LUTs	Registers
CertusPro-NX	1	2	489	630
	1	3	682	743
	1	4	836	851
	1	5	1034	964
	1	6	1264	1072
	1	7	1519	1180
	1	8	1727	1286
	2	1	676	646
	2	2	1012	791
	2	3	1290	924
	2	4	1564	1047
	2	5	1973	1180

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Device	Total EMs	Total ESs	LUTs	Registers
	2	6	2322	1303
	2	7	2677	1432
	2	8	3003	1558
	3	1	1016	776
	3	2	1501	947
	3	3	1919	1102
	3	4	2284	1242
	3	5	2790	1397
	3	6	3332	1537
	3	7	3881	1718
	3	8	4353	1872
	4	1	1217	899
	4	2	1770	1094
	4	3	2366	1269
	4	4	2733	1424
	4	5	3298	1599
	4	6	3918	1754
	4	7	4558	1962
	4	8	5036	2127
	5	1	1634	1029
	5	2	2309	1250
	5	3	2983	1447
	5	4	3635	1627
	5	5	4330	1837
	5	6	5172	2046
	5	7	5779	2215
	5	8	6425	2403
	6	1	2017	1152
	6	2	2837	1402
	6	3	3671	1614
	6	4	4355	1801
	6	5	5174	2018
	6	6	6081	2247
	6	7	7083	2478
	6	8	7545	2669
	7	1	2480	1275
	7	2	3388	1553
	7	3	4210	1791
	7	4	4942	1994
	7	5	6014	2237
	7	6	7239	2475

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Device	Total EMs	Total ESs	LUTs	Registers
	7	7	7878	2669
	7	8	9138	2919
	8	1	2687	1406
	8	2	3759	1704
	8	3	4792	1976
	8	4	5583	2178
	8	5	6620	2463
	8	6	7626	2694
	8	7	8784	2925
	8	8	9666	3177
Avant	1	2	504	630
	1	3	698	743
	1	4	896	851
	1	5	1092	964
	1	6	1300	1087
	1	7	1632	1205
	1	8	1776	1316
	2	1	682	650
	2	2	1040	795
	2	3	1357	928
	2	4	1585	1053
	2	5	1961	1187
	2	6	2387	1312
	2	7	2825	1439
	2	8	3061	1567
	3	1	1048	782
	3	2	1567	953
	3	3	2042	1108
	3	4	2393	1251
	3	5	2930	1403
	3	6	3510	1552
	3	7	4061	1702
	3	8	4543	1848
	4	1	1293	907
	4	2	1830	1108
	4	3	2351	1281
	4	4	2855	1438
	4	5	3441	1622
	4	6	4169	1801
	4	7	4750	1940
	4	8	5470	2099

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Device	Total EMs	Total ESs	LUTs	Registers
	5	1	1782	1044
	5	2	2353	1260
	5	3	2996	1464
	5	4	3598	1638
	5	5	4239	1841
	5	6	5099	2057
	5	7	5788	2231
	5	8	6371	2407
	6	1	2138	1169
	6	2	2934	1423
	6	3	3615	1632
	6	4	4381	1830
	6	5	5263	2099
	6	6	6075	2275
	6	7	6728	2418
	6	8	7647	2654
	7	1	2567	1302
	7	2	3413	1577
	7	3	4322	1808
	7	4	5026	2003
	7	5	6043	2265
	7	6	7013	2501
	7	7	8196	2711
	7	8	9120	2924
	8	1	2735	1425
	8	2	3742	1724
	8	3	4797	1986
	8	4	5552	2206
	8	5	6742	2484
	8	6	7798	2721
	8	7	8868	2925
	8	8	10056	3176

Table A.4. Resource Utilization for 64-bit Data Width without CDC in Maximize Performance Mode

Device	Total EMs	Total ESs	LUTs	Registers
CertusPro-NX	1	2	617	830
	1	3	882	1007
	1	4	1082	1179
	1	5	1324	1356
	1	6	1642	1528
	1	7	1894	1700

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Device	Total EMs	Total ESs	LUTs	Registers
	1	8	2134	1890
	2	1	793	858
	2	2	1298	1067
	2	3	1702	1266
	2	4	2076	1451
	2	5	2520	1653
	2	6	3013	1835
	2	7	3529	2041
	2	8	3879	2226
	3	1	1232	1062
	3	2	1899	1297
	3	3	2540	1516
	3	4	2970	1722
	3	5	3729	1940
	3	6	4508	2143
	3	7	5154	2374
	3	8	5717	2633
	4	1	1512	1259
	4	2	2245	1518
	4	3	3032	1757
	4	4	3619	1976
	4	5	4522	2215
	4	6	5291	2466
	4	7	6089	2700
	4	8	6644	2910
	5	1	1969	1463
	5	2	2907	1748
	5	3	3904	2009
	5	4	4720	2245
	5	5	5648	2540
	5	6	6676	2780
	5	7	7756	3010
	5	8	8472	3313
	6	1	2316	1660
	6	2	3512	1977
	6	3	4866	2264
	6	4	5729	2513
	6	5	6787	2792
	6	6	8078	3084
	6	7	9220	3338
	6	8	10262	3628

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Device	Total EMs	Total ESs	LUTs	Registers
	7	1	2869	1865
	7	2	4319	2190
	7	3	5627	2499
	7	4	6515	2762
	7	5	8116	3083
	7	6	9317	3358
	7	7	10911	3661
	7	8	12069	3936
	8	1	3179	2063
	8	2	4793	2434
	8	3	6224	2749
	8	4	7162	3023
	8	5	8741	3359
	8	6	10342	3669
	8	7	11987	3939
	8	8	12916	4256
Avant	1	2	634	830
	1	3	933	1007
	1	4	1076	1179
	1	5	1399	1356
	1	6	1760	1532
	1	7	1905	1714
	1	8	2208	1892
	2	1	808	858
	2	2	1319	1073
	2	3	1743	1264
	2	4	2062	1453
	2	5	2644	1653
	2	6	3187	1844
	2	7	3625	2032
	2	8	3999	2224
	3	1	1302	1062
	3	2	1941	1297
	3	3	2682	1516
	3	4	3145	1725
	3	5	3939	1939
	3	6	4650	2158
	3	7	5323	2362
	3	8	5924	2589
	4	1	1535	1259
	4	2	2395	1518

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Device	Total EMs	Total ESs	LUTs	Registers
	4	3	3122	1763
	4	4	3569	1978
	4	5	4515	2226
	4	6	5458	2463
	4	7	6317	2676
	4	8	7070	2909
	5	1	2104	1471
	5	2	2979	1757
	5	3	3916	2017
	5	4	4682	2263
	5	5	5911	2543
	5	6	6762	2786
	5	7	7876	3035
	5	8	8582	3295
	6	1	2521	1665
	6	2	3694	1981
	6	3	4894	2257
	6	4	5636	2519
	6	5	6776	2831
	6	6	8157	3074
	6	7	9395	3352
	6	8	10113	3610
	7	1	3025	1866
	7	2	4292	2200
	7	3	5687	2507
	7	4	6623	2777
	7	5	8174	3106
	7	6	9732	3405
	7	7	10964	3662
	7	8	11923	3950
	8	1	3235	2065
	8	2	4705	2427
	8	3	6217	2761
	8	4	7258	3025
	8	5	8843	3395
	8	6	10289	3672
	8	7	11917	3944
	8	8	12924	4247

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Table A.5. Resource Utilization for 128-bit Data Width without CDC in Maximize Performance Mode

Device	Total EMs	Total ESs	LUTs	Registers
CertusPro-NX	1	2	893	1230
	1	3	1270	1535
	1	4	1514	1835
	1	5	1944	2140
	1	6	2334	2440
	1	7	2764	2744
	1	8	3056	3037
	2	1	1079	1274
	2	2	1818	1611
	2	3	2515	1936
	2	4	3004	2251
	2	5	3744	2576
	2	6	4606	2891
	2	7	5339	3228
	2	8	5828	3540
	3	1	1649	1622
	3	2	2734	1985
	3	3	3777	2332
	3	4	4434	2672
	3	5	5602	3013
	3	6	6734	3351
	3	7	7847	3725
	3	8	8580	4012
	4	1	1962	1963
	4	2	3233	2350
	4	3	4463	2717
	4	4	5211	3064
	4	5	6503	3431
	4	6	7926	3825
	4	7	9113	4172
	4	8	9898	4534
	5	1	2578	2311
	5	2	4178	2724
	5	3	5778	3113
	5	4	6789	3477
	5	5	8286	3866
	5	6	10102	4248
	5	7	11640	4642
	5	8	12799	5041
	6	1	3160	2652

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Device	Total EMs	Total ESs	LUTs	Registers
	6	2	5071	3089
	6	3	6993	3508
	6	4	8291	3888
	6	5	10173	4332
	6	6	12171	4720
	6	7	13944	5058
	6	8	15397	5494
	7	1	3760	2994
	7	2	6138	3454
	7	3	8429	3906
	7	4	9622	4284
	7	5	12010	4746
	7	6	14103	5125
	7	7	16620	5557
	7	8	18095	5974
	8	1	4219	3346
	8	2	6599	3833
	8	3	9100	4284
	8	4	10505	4711
	8	5	13185	5191
	8	6	15443	5579
	8	7	17889	5970
	8	8	19489	6437
Avant	1	2	892	1230
	1	3	1291	1535
	1	4	1548	1835
	1	5	1951	2140
	1	6	2468	2440
	1	7	2764	2740
	1	8	3191	3068
	2	1	1087	1274
	2	2	1842	1613
	2	3	2580	1938
	2	4	3068	2254
	2	5	3841	2576
	2	6	4621	2902
	2	7	5429	3213
	2	8	5873	3533
	3	1	1722	1622
	3	2	2782	1985
	3	3	3836	2332

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Device	Total EMs	Total ESs	LUTs	Registers
	3	4	4563	2667
	3	5	5709	3011
	3	6	6841	3351
	3	7	8009	3692
	3	8	8788	4035
	4	1	2018	1963
	4	2	3304	2350
	4	3	4504	2721
	4	4	5297	3075
	4	5	6594	3445
	4	6	8193	3795
	4	7	9326	4145
	4	8	10193	4517
	5	1	2637	2313
	5	2	4216	2728
	5	3	5766	3123
	5	4	6738	3483
	5	5	8532	3881
	5	6	9982	4277
	5	7	11699	4653
	5	8	12671	5014
	6	1	3302	2657
	6	2	5222	3099
	6	3	7171	3515
	6	4	8374	3892
	6	5	10189	4333
	6	6	12410	4741
	6	7	14005	5096
	6	8	15187	5459
	7	1	3961	3006
	7	2	6084	3459
	7	3	8349	3898
	7	4	9669	4295
	7	5	12166	4782
	7	6	14385	5155
	7	7	16700	5570
	7	8	18143	5956
	8	1	4243	3350
	8	2	6639	3838
	8	3	9080	4294
	8	4	10487	4702

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Device	Total EMs	Total ESs	LUTs	Registers
	8	5	13285	5169
	8	6	15558	5619
	8	7	18021	6000
	8	8	19502	6435

Table A.6. Resource Utilization for 32-bit Data Width with CDC in Maximize Performance Mode

Device	Total EMs	Total ESs	LUTs	Registers
CertusPro-NX	4	4	6665	5847
Avant	4	4	6662	5832

Note: CDC is enabled for all external managers and external subordinates.

Minimize Area Mode

For the sample resource utilizations shown in this section, the following IP configuration applies:

- *External Manager <N> (Sxx) Protocol Type* = AXI4-Lite
- *External Subordinate <M> (Myy) Protocol Type* = AXI4-Lite
- *Crossbar Optimization Strategy* = Minimize Area (Single Access Mode)
- *External Manager N Address width* = 32 bits
- *External Subordinate <M> (Myy) Address Width* = 32 bits
- *External Subordinate <M> (Myy) Fragment Cnt* = 1
- *External Manager Priority* = Round Robin
- No CDC unless otherwise specified

Table A.7. Resource Utilization for 32-bit Data Width without CDC in Minimize Area Mode

Device	Total EMs	Total ESs	LUTs	Registers
CertusPro-NX	1	2	423	601
	1	3	585	703
	1	4	714	803
	1	5	897	905
	1	6	1089	1005
	1	7	1307	1105
	1	8	1456	1202
	2	1	590	619
	2	2	885	747
	2	3	1145	863
	2	4	1431	975
	2	5	1782	1091
	2	6	2071	1203
	2	7	2456	1315
	2	8	2780	1457
	3	1	924	738
	3	2	1338	886
	3	3	1799	1018
	3	4	2222	1144

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Device	Total EMs	Total ESs	LUTs	Registers
	3	5	2607	1278
	3	6	3136	1402
	3	7	3728	1566
	3	8	4093	1711
	4	1	1095	850
	4	2	1626	1016
	4	3	2162	1162
	4	4	2549	1300
	4	5	3181	1446
	4	6	3609	1584
	4	7	4302	1748
	4	8	4961	1948
	5	1	1477	969
	5	2	2131	1155
	5	3	2752	1317
	5	4	3292	1469
	5	5	4071	1658
	5	6	4795	1840
	5	7	5563	1977
	5	8	6005	2150
	6	1	1914	1081
	6	2	2619	1285
	6	3	3312	1466
	6	4	4049	1638
	6	5	4799	1801
	6	6	5903	2013
	6	7	6530	2199
	6	8	7195	2406
	7	1	2184	1193
	7	2	3158	1427
	7	3	3993	1619
	7	4	4626	1798
	7	5	5722	2009
	7	6	6820	2236
	7	7	7982	2415
	7	8	8506	2581
	8	1	2557	1345
	8	2	3396	1550
	8	3	4403	1762
	8	4	5064	1968
	8	5	6214	2181

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Device	Total EMs	Total ESs	LUTs	Registers
	8	6	7284	2391
	8	7	8435	2598
	8	8	9034	2802
Avant	1	2	431	601
	1	3	607	703
	1	4	772	803
	1	5	941	905
	1	6	1168	1005
	1	7	1482	1109
	1	8	1482	1212
	2	1	602	619
	2	2	938	747
	2	3	1251	863
	2	4	1466	977
	2	5	1796	1094
	2	6	2176	1203
	2	7	2721	1320
	2	8	2916	1455
	3	1	962	738
	3	2	1405	886
	3	3	1877	1020
	3	4	2208	1144
	3	5	2712	1281
	3	6	3300	1410
	3	7	3810	1550
	3	8	4274	1675
	4	1	1109	850
	4	2	1717	1016
	4	3	2177	1162
	4	4	2589	1300
	4	5	3261	1451
	4	6	4142	1598
	4	7	4488	1758
	4	8	5163	1929
	5	1	1570	974
	5	2	2125	1157
	5	3	2813	1323
	5	4	3375	1469
	5	5	4197	1702
	5	6	4924	1867
	5	7	5500	2001

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Device	Total EMs	Total ESs	LUTs	Registers
	5	8	6090	2158
	6	1	1831	1088
	6	2	2673	1293
	6	3	3408	1461
	6	4	4020	1627
	6	5	5004	1904
	6	6	5709	2033
	6	7	6614	2197
	6	8	7371	2399
	7	1	2284	1193
	7	2	3122	1419
	7	3	4027	1617
	7	4	4806	1801
	7	5	5949	2052
	7	6	6878	2243
	7	7	7824	2425
	7	8	8492	2596
	8	1	2472	1308
	8	2	3447	1562
	8	3	4492	1769
	8	4	5140	1986
	8	5	6253	2232
	8	6	7322	2440
	8	7	8753	2636
	8	8	9113	2809

Table A.8. Resource Utilization for 64-bit Data Width without CDC in Minimize Area Mode

Device	Total EMs	Total ESs	LUTs	Registers
CertusPro-NX	1	2	558	801
	1	3	774	967
	1	4	950	1131
	1	5	1179	1297
	1	6	1478	1461
	1	7	1793	1625
	1	8	1914	1786
	2	1	726	827
	2	2	1175	1019
	2	3	1584	1199
	2	4	1903	1375
	2	5	2358	1555
	2	6	2848	1733

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Device	Total EMs	Total ESs	LUTs	Registers
	2	7	3433	1921
	2	8	3682	2080
	3	1	1134	1018
	3	2	1763	1230
	3	3	2389	1426
	3	4	2859	1624
	3	5	3534	1812
	3	6	4234	2002
	3	7	4954	2227
	3	8	5487	2438
	4	1	1359	1202
	4	2	2095	1432
	4	3	2821	1645
	4	4	3429	1844
	4	5	4148	2060
	4	6	4873	2256
	4	7	5800	2512
	4	8	6366	2715
	5	1	1782	1393
	5	2	2774	1643
	5	3	3682	1869
	5	4	4331	2085
	5	5	5402	2311
	5	6	6367	2588
	5	7	7580	2815
	5	8	8110	3045
	6	1	2292	1577
	6	2	3330	1845
	6	3	4436	2085
	6	4	5455	2313
	6	5	6569	2573
	6	6	7854	2826
	6	7	9002	3087
	6	8	9846	3325
	7	1	2738	1761
	7	2	3981	2047
	7	3	5346	2310
	7	4	6305	2561
	7	5	7644	2840
	7	6	9075	3075
	7	7	10548	3346

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Device	Total EMs	Total ESs	LUTs	Registers
	7	8	11714	3613
	8	1	3028	1963
	8	2	4345	2269
	8	3	5787	2534
	8	4	6754	2807
	8	5	8402	3105
	8	6	9962	3369
	8	7	11460	3610
	8	8	12356	3894
Avant	1	2	575	801
	1	3	801	967
	1	4	1029	1131
	1	5	1281	1297
	1	6	1591	1465
	1	7	1838	1627
	1	8	2025	1807
	2	1	755	827
	2	2	1229	1019
	2	3	1665	1199
	2	4	1967	1375
	2	5	2472	1558
	2	6	2967	1733
	2	7	3413	1923
	2	8	3800	2119
	3	1	1174	1018
	3	2	1850	1230
	3	3	2536	1430
	3	4	2966	1616
	3	5	3675	1817
	3	6	4376	2012
	3	7	5154	2231
	3	8	5718	2425
	4	1	1386	1202
	4	2	2183	1432
	4	3	2926	1642
	4	4	3426	1846
	4	5	4569	2055
	4	6	5212	2280
	4	7	6094	2489
	4	8	6857	2726
	5	1	1893	1393

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Device	Total EMs	Total ESs	LUTs	Registers
	5	2	2741	1645
	5	3	3747	1873
	5	4	4468	2085
	5	5	5525	2368
	5	6	6613	2589
	5	7	7595	2827
	5	8	8196	3028
	6	1	2235	1577
	6	2	3426	1853
	6	3	4543	2085
	6	4	5305	2315
	6	5	6604	2639
	6	6	7657	2809
	6	7	9099	3055
	6	8	9840	3314
	7	1	2756	1761
	7	2	4025	2053
	7	3	5364	2309
	7	4	6521	2578
	7	5	8021	2904
	7	6	9217	3111
	7	7	10703	3348
	7	8	11379	3574
	8	1	2981	1945
	8	2	4436	2272
	8	3	5925	2539
	8	4	6870	2811
	8	5	8412	3127
	8	6	10029	3373
	8	7	11656	3615
	8	8	12422	3900

Table A.9. Resource Utilization for 32-bit Data Width with CDC in Minimize Area Mode

Device	Total EMs	Total ESs	LUTs	Registers
CertusPro-NX	4	4	6500	5700
Avant	4	4	6452	5701

Note: CDC is enabled for all external managers and external subordinates.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

CFG 1 Primary Crossbar AXI4

For the sample resource utilizations shown in this section, the following IP configuration applies:

- *Primary Crossbar* = AXI4
- *External Manager 0 (S00) Protocol Type* = AXI4
- *External Manager 1 (S01) Protocol Type* = AHB-Lite
- *External Manager 2 (S02) Protocol Type* = AXI4-Lite
- *External Subordinate 0 (M00) Protocol Type* = Secondary AXI4-Lite
- *External Subordinate 1 (M01) Protocol Type* = Secondary APB
- *External Subordinate 2 (M02) Protocol Type* = AXI4
- *External Subordinate 3 (M03) Protocol Type* = Secondary AHB-Lite
- *External Subordinate 4 (M04) Protocol Type* = Secondary AHB-Lite
- *External Subordinate 5 (M05) Protocol Type* = AXI4
- *External Subordinate 6 (M06) Protocol Type* = Secondary APB
- *External Subordinate 7 (M07) Protocol Type* = Secondary AXI4-Lite

Table A.10. Resource Utilization for CFG 1 Primary Crossbar AXI4

Device	Total EMs	Total ESs	LUTs	Registers
CertusPro-NX	3	8	4330	2265
Avant	3	8	4527	2273

CFG 2 Primary Crossbar AHB-Lite

For the sample resource utilizations shown in this section, the following IP configuration applies:

- *Primary Crossbar* = AHB-Lite
- *External Manager 0 (S00) Protocol Type* = AHB-Lite
- *External Manager 1 (S01) Protocol Type* = AHB-Lite
- *External Manager 2 (S02) Protocol Type* = AHB-Lite
- *External Subordinate 0 (M00) Protocol Type* = Secondary AXI4-Lite
- *External Subordinate 1 (M01) Protocol Type* = Secondary APB
- *External Subordinate 2 (M02) Protocol Type* = AHB-Lite
- *External Subordinate 3 (M03) Protocol Type* = Secondary AXI4-Lite
- *External Subordinate 4 (M04) Protocol Type* = APB
- *External Subordinate 5 (M05) Protocol Type* = APB
- *External Subordinate 6 (M06) Protocol Type* = Secondary APB
- *External Subordinate 7 (M07) Protocol Type* = Secondary APB

Table A.11. Resource Utilization for CFG 2 Primary Crossbar AHB-Lite

Device	Total EMs	Total ESs	LUTs	Registers
CertusPro-NX	3	8	3541	1355
Avant	3	8	3824	1469

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Appendix B. Determining the Secondary Protocol Interface Index

The following Python script can be used to determine the secondary protocol interface indices.

```
n = int(input("Enter Total External Subordinates: "))
print("Total External Subordinates,", n)

print("Protocol mapping/n")
print("1 = AXI4")
print("2 = AXI4-Lite")
print("3 = AHB-Lite")
print("4 = APB")
print("5 = Secondary AXI4-Lite")
print("6 = Secondary AHB-Lite")
print("7 = Secondary APB")

values = []

for i in range(n):
    val = int(input(f"External Subordinate {i} (M{i:02}) Protocol Type in
numeric: "))
    values.append(val)

interface_number = 0
s_AXI4L_detected = 0
s_AHBL_detected = 0
s_APB_detected = 0
for j, val in enumerate(values):
    if(val <= 4):
        interface_number = interface_number + 1
for j, val in enumerate(values):
    if(val == 5 and s_AXI4L_detected == 0):
        print(f"The Secondary AXI4-Lite virtual interface index is
{interface_number}")
        s_AXI4L_detected = 1
        interface_number = interface_number + 1
    if(val == 6 and s_AHBL_detected == 0):
        print(f"The Secondary AHB-Lite virtual interface index is
{interface_number}")
        s_AHBL_detected = 1
        interface_number = interface_number + 1
    if(val == 7 and s_APB_detected == 0):
        print(f"The Secondary APB virtual interface index is
{interface_number}")
        s_APB_detected = 1
        interface_number = interface_number + 1
```

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

References

- Unified Interconnect IP Release Notes (FPGA-RN-02107)
- Lattice Radiant Timing Constraints Methodology (FPGA-AN-02059)
- AMBA AXI Protocol Specification web page
- AHB-Lite Protocol Specification web page
- APB Protocol Specification web page
- Avant-E web page
- Avant-G web page
- Avant-X web page
- Certus-N2 web page
- Certus-NX web page
- CertusPro-NX web page
- CrossLink-NX web page
- MachXO5-NX web page
- Unified Interconnect IP Core web page
- Lattice Radiant Software web page
- Lattice Propel Design Environment web page
- Lattice Solutions IP Cores web page
- Lattice Solutions Reference Designs web page
- Lattice Insights for Lattice Semiconductor training courses and learning plans

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Revision History

Note: In some instances, the IP may be updated without changes to the user guide. The user guide may reflect an earlier IP version but remains fully compatible with the later IP version. Refer to the IP Release Notes for the latest updates.

Revision 1.1, IP v2.0.0, June 2026

Section	Change Summary
All	• Standardized attribute names across document where applicable. • Made minor editorial changes.
Abbreviations in This Document	Added *AHB-Lite*, *AXI4-Lite*, *CFG*, *IC*, *MUX*, *RO*, *SoC*, *WO*, and *WR*.

Introduction	• Removed note on support for only AXI4 interconnection.
	• In the Overview of the IP section:
	  • Updated description to include AHB-Lite- and APB-based systems.
	  • Standardized terms in description from *initiator* to *manager* and *target* to *subordinate*.
	• In Table 1.1. Summary of the Unified Interconnect IP:
	  • Added AHB-Lite and APB to *Supported User Interface*.
	  • Updated IP core version and software version in *Lattice Implementation*.
	• In the Features section:
	  • Added AMBA 3 AHB-Lite and APB.
	  • Added references for the AHB-Lite and APB protocols.
	  • Added 8 and 16 bits to AXI4 data widths.
	  • Added data widths for AHB-Lite and APB.
	  • Updated minimum address width for AXI4 and AXI4-Lite to 11.
	  • Added address widths for AHB-Lite and APB.
	  • Added crossbar paths restriction with configured connectivity map to the reduced resource optimization list.
	  • Updated number of external managers and/or external subordinates supported to 16.

Functional Description	• In the IP Architecture Overview section:
	  • Updated Figure 2.1. Lattice Unified Interconnect IP Block Diagram.
	  • Added the Multi-protocol, Memory Map, AXI4 ID Width Requirement, and Address Alignment Requirement sections.
	• In the Clocking and Reset section:
	  • In Table 2.4. Clocking and Reset Domain Summary:
	  • For external manager interface:
	  • Added AHB-Lite and APB to protocol selections.
	  • Updated clock signal names to Sxx_clk_i and clk_i.
	  • Updated reset signal names to Sxx_resetn_i and resetn_i.
	  • For external subordinate interface:
	  • Added AHB-Lite and APB to protocol selections.
	  • Updated clock signal names to Myy_clki and clk_i.
	  • Updated reset signal names to Myy_resetn_i and resetn_i.
	  • Added clock and reset domain for Secondary AXI4-Lite, Secondary AHB-Lite, and Secondary APB protocol selections.
	  • Added AXI4-Lite secondary IC, AHB-Lite secondary IC, and APB secondary IC modules for CDC enabled and disabled.
	  • Added note on mapping of clock and reset signals from IP v1.0.0.
	  • Added the Without CDC and With CDC sections.
	• In the External Manager Interface section:
	  • Updated statement on CDC support.
	  • Added support for register slice.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Section	Change Summary
	• Updated protocol conversion statement to include AHB-Lite and APB. • Updated note to reference *external manager* instead of *AXI manager*. • In the External Subordinate Interface section: • Updated statement on CDC support. • Added support for register slice. • Updated protocol conversion statement to include AHB-Lite and APB. • Updated note to reference *external subordinate* instead of *AXI subordinate*. • In the Crossbar section: • Updated crossbar statement to explicitly mention AXI4. • Added crossbar statements for AHB-Lite and APB. • In the Address Phase Processing Unit section: • Reorganized AXI4 transaction details into a bullet point. • Added descriptions for AHB-Lite and APB transactions. • Updated the Single Slave per Active ID for AXI4 section title to explicitly identify AXI4. • In the Transaction Acceptance Limit section: • Added clarification that transaction acceptance limits do not account for address transfers buffered by intermediate modules upstream of the crossbar. • Added descriptions for transaction acceptance limit for AHB-Lite and APB. • In the Outstanding Transaction section: • Added descriptions for transaction completion for AHB-Lite and APB. • In the Default Subordinate section: • Added descriptions for AHB-Lite and APB in Step 3. • Added note on conditions when the primary crossbar is set to APB. • In the Infrastructure Modules section: • In the Queue section: • Added bullet points for *Memory Type of Large FIFOs* attribute and block applicability. • Added the Register Slice section. • Removed the Protocol Conversion section. • Added the Protocol Conversion Bridge and Error Case Examples during Protocol Conversion sections. • Reorganized sections under *Other IP Specific Blocks/Layers/Interfaces* by moving the child sections up one level and removing the parent section.
IP Parameter Description	• In Table 3.1. General Attributes: • Added *Parameter Name* to the *Attribute* column. • Added *Applicable Protocol* column. • Updated the selectable values for the following attributes: • Total External Managers • Total External Subordinates • Added cross reference in description of *Crossbar Optimization Strategy*. • Added the *Primary Crossbar* attribute. • In Table 3.2. External Manager Settings Attributes: • Added *Parameter Name* to the *Attribute* column. • Added *Applicable Protocol* column. • Removed the following attributes: • Manager Max Address Width(bits) • Manager Max Data Width(bits) • Added the following sections and attributes: • External Manager AXI Secure Access Settings section • External Manager <N> (Sxx) AXI Secure Access Enable • External Manager Register Slice Settings section

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Section	Change Summary
	• External Manager <N> (Sxx) Data Register Slice Enable • Updated name and description of the following attributes: • External Manager <N> (Sxx) AXI Access Type • External Manager <N> (Sxx) CDC Enable • External Manager <N> (Sxx) Data Width • External Manager <N> (Sxx) Write Acceptance Limit • External Manager <N> (Sxx) Read Acceptance Limit • External Manager <N> (Sxx) Write Address Buffer Depth • External Manager <N> (Sxx) Read Address Buffer Depth • External Manager <N> (Sxx) Write Response Buffer Depth • External Manager <N> (Sxx) Write Data Buffer Depth • External Manager <N> (Sxx) Read Data Buffer Depth • Ext Manager <N> (Sxx) Fixed Priority • Updated name, selectable values, and description of the following attributes: • External Manager <N> (Sxx) Protocol Type • External Manager <N> (Sxx) Address Width • Added notes on <N> and *xx*, and renumbered existing notes. • In Table 3.3. External Subordinate Settings Attributes: • Added *Parameter Name* to the *Attribute* column. • Added *Applicable Protocol* column. • Updated the selectable values of the following attribute: • External Subordinate AXI ID Width • Removed the following attributes: • Subordinate Max Address Width(bits) • Subordinate Max Data Width(bits) • Subordinate Max Fragment count • Added the following sections and attributes: • External Subordinate AXI Secure Access Settings section • External Subordinate <M> (Myy) AXI Secure Access Enable • Common Secondary AXI4-Lite External Subordinate AXI Secure Access Enable • External Subordinate Register Slice Settings section • External Subordinate <M> (Myy) Data Register Slice Enable • Updated name and description of the following attributes: • External Subordinate <M> (Myy) AXI Access Type • External Subordinate <M> (Myy) CDC Enable • External Subordinate <M> (Myy) Data Width • External Subordinate <M> (Myy) Write Address Buffer Depth • External Subordinate <M> (Myy) Read Address Buffer Depth • External Subordinate <M> (Myy) Write Response Buffer Depth • External Subordinate <M> (Myy) Write Data Buffer Depth • External Subordinate <M> (Myy) Read Data Buffer Depth • External Subordinate <M> (Myy) Fragment Cnt • Updated name, selectable values, and description of the following attributes: • External Subordinate <M> (Myy) Protocol Type • External Subordinate <M> (Myy) Address Width • Base Address <F> • End Address <F> • Added the following attributes: • Common Secondary AXI4-Lite External Subordinate CDC Enable • Common Secondary AHB-Lite External Subordinate CDC Enable • Common Secondary APB External Subordinate CDC Enable

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Section	Change Summary
	• Added notes on <M>, *yy*, and recommended number of external subordinates, and renumbered existing notes. • Updated Note 8 on minimum size of each of the external subordinate fragments. • Added the Advanced Settings section.

Signal Description	• Added the Clock and Reset section.
	• Removed the Unified Interconnect IP Interface Diagram without CDC figure.
	• Removed the Unified Interconnect IP Interface Diagram with External Manager 0 and External Subordinate 0 CDC Enabled figure.
	• Removed the AXI4 Crossbar Interface section.
	• Reorganized AXI4 content into the AXI4 section.
	• In the AXI4 section:
	  • Added Figure 4.2. AXI4 Protocol Interface Diagram.
	  • Revised description by removing references to clock and reset.
	  • In Table 4.1. AXI4 External Manager Interface Ports:
	  • Removed the AXI Interconnect Subordinate xx Clock and Reset (Available if CDC is Enabled for Port Sxx) section and signals.
	  • Updated *Manager Max Address Width(bits)* attribute to term *Maximum Value for External Manager <N> (Sxx) Address Width across All Managers*.
	  • Updated *Manager Max Data Width(bits)* attribute to *External Manager<N> (Sxx) Data Width* attribute.
	  • Updated descriptions for axi_Sxx_wvalid_i, axi_Sxx_wstrb_i[x:0], axi_Sxx_wready_o, axi_Sxx_bready_i3, axi_Sxx_rvalid_o3, axi_Sxx_rid_o[x:0], and axi_Sxx_rlast_o.
	  • Updated Note 2 on xx.
	  • In Table 4.2. AXI4 External Subordinate Interface Ports:
	  • Removed the AXI Interconnect Manager yy Clock and Reset (Available if CDC is Enabled for Port Myy) section and signals.
	  • Updated *Subordinate Max Address Width(bits)* attribute to term *Maximum Value for External Subordinate <M> (Myy) Address Width across All Subordinates*.
	  • Updated *Subordinate Max Data Width(bits)* attribute to *External Subordinate <M> (Myy) Data Width* attribute.
	  • Updated descriptions for axi_Myy_wvalid_o, axi_Myy_wstrb_o[x:0], axi_Myy_wuser_o[x:0], aaxi_Myy_wready_i, axi_Myy_buser_i[x:0], axi_Myy_bready_o, axi_Myy_rid_i[x:0], and axi_Myy_rlast_i.
	  • Updated Note 2 on yy.
	• Added the AHB-Lite and APB sections.

Example Design	Added new section.

Designing with the IP	• Updated Figure 6.1. Module/IP Block Wizard, Figure 6.2. IP Configuration, and Figure 6.3. Check Generated Result.
	• In the Timing Constraints section:
	  • Updated port names, conditions, and code for existing clock groups.
	  • Added additional clock groups.
	  • Updated note on xx and yy.
	  • Added optional timing constraints for relaxing timing requirements.
	  • Updated example timing constraints for timing closure.

Design Considerations	• Updated limitations in the Limitations section.
	• Added the Exporting Manager and Subordinate Interfaces section.
	• Updated section titles to the following:
	  • AXI4 Pipelining Transfer
	  • AXI4 Bottleneck Clearance
	• In the Design Considerations for Latency section:
	  • Added notes on T_{EM}, T_{ES}, and T_{DP}.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Section	Change Summary

	• Removed the Minimum Crossbar Latency section.
	• Removed the Default AXI4 Use Case without CDC section.
	• Added the Sub-IP Block Latency section.
	• In the Sub-IP Block Latency section:
	  • Added the Crossbar Latency section.
	  • Moved the EM or ES Interface Latency section into this section.
	• In the EM or ES Interface Latency section:
	  • Updated description.
	  • In Table 7.4. Additional Latency Introduced by Optional Couplers at EM or ES AXI4 Interface with Primary Crossbar = AXI4:
	  • Updated title and header.
	  • Added Enable Data Register Slice column.
	  • Updated channel to Read Data and Response.
	  • Added Table 7.5. Additional Latency Introduced by Optional Couplers at EM or ES AHB-Lite Interface with Primary Crossbar = AHB-Lite or APB Interface with Primary Crossbar = APB and Table 7.6. Additional Latency Introduced by Optional Couplers at EM or ES Interface for Protocol Conversion.
	• Added the Design Considerations for Resource Utilization and Design Considerations for Timing (fMAX) sections.

Appendix A. Resource Utilization	• Added note on resource utilization values.
	• Removed note on f_{MAX} values.
	• Added the following tables:
	  • Table A.1. Resource Utilization and fMAX for 64-bit Data Width in Maximize Performance Mode (4 EMs and 4 ESs)
	  • Table A.2. Resource Utilization and fMAX for 64-bit Data Width in Maximize Performance Mode (8 EMs and 8 ESs)
	• Updated and added resource utilization values and removed f_{MAX} column in the following tables:
	  • Table A.3. Resource Utilization for 32-bit Data Width without CDC in Maximize Performance Mode
	  • Table A.4. Resource Utilization for 64-bit Data Width without CDC in Maximize Performance Mode
	  • Table A.5. Resource Utilization for 128-bit Data Width without CDC in Maximize Performance Mode
	  • Table A.7. Resource Utilization for 32-bit Data Width without CDC in Minimize Area Mode
	  • Table A.8. Resource Utilization for 64-bit Data Width without CDC in Minimize Area Mode
	• Updated resource utilization values and removed f_{MAX} column in the following tables:
	  • Table A.6. Resource Utilization for 32-bit Data Width with CDC in Maximize Performance Mode
	  • Table A.9. Resource Utilization for 32-bit Data Width with CDC in Minimize Area Mode
	• Added the CFG 1 Primary Crossbar AXI4 and CFG 2 Primary Crossbar AHB-Lite sections.

Appendix B. Determining the Secondary Protocol Interface Index	Added new section.
References	• Added the AHB-Lite Protocol Specification web page. • Added the APB Protocol Specification web page. • Added Unified Interconnect IP Core web page.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Revision 1.0, IP v1.0.0, December 2025

Section	Change Summary
All	Initial release.

© 2026 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

www.latticesemi.com