Unified Interconnect IP

IP Version: v1.0.0

User Guide

FPGA-IPUG-02318-1.0

December 2025

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This document was created consistent with Lattice Semiconductor’s inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice’s inclusive language FAQ 6878 for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

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Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviation	Definition
AHB	Advanced High-performance Bus
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
AR	Read Address Channel
AW	Write Address Channel
AXI4	Advanced eXtensible Interface 4
CDC	Clock Domain Crossing
CONV	Protocol Conversion
CPU	Central Processing Unit
DMA	Direct Memory Access
DWC	Data Width Conversion
EBR	Embedded Block RAM
EM	External Manager
ES	External Subordinate
FIFO	First In First Out
FPGA	Field Programmable Gate Array
FWFT	First Word Fall Through
GUI	Graphical User Interface
HDL	Hardware Description Language
ID	Identification
IP	Intellectual Property
LUT	Look-Up Table
MC	Memory Controller
MI	Manager Interface
RAM	Random Access Memory
RDATA	Read Data Channel
RTL	Register Transfer Level
SAMD	Shared Address and Multiple Data Channels
SASD	Shared Address and Shared Data Channels
SI	Subordinate Interface
WDATA	Write Data Channel
XB	Crossbar

1. Introduction

This document provides information on the Unified Interconnect IP, essential for IP/system development, verification, integration, testing, and validation. In general, this document covers design specifications from RTL to IP packaging and details the procedures for IP generation and integration.

Note: This IP currently only supports AXI4 interconnection.

1.1. Overview of the IP

The unified interconnect is a high-performance and low-latency interconnect fabric for AXI4- and AXI4-Lite-based systems. Any AXI4- or AXI4-Lite-compliant IP can be integrated into the system. The IP connects one or more memory-mapped *manager* devices to one or more memory-mapped *subordinate* devices and supports optional clock domain crossing (CDC) between interfaces. Each manager can access different subordinates in parallel. When more than one initiator tries to reach the same target, access is arbitrated.

1.2. Quick Facts

Table 1.1. Summary of the Unified Interconnect IP

IP Requirements	Supported Devices	CrossLink™-NX, CertusPro™-NX, Certus™-NX, MachXO5™-NX, Lattice Avant™, Certus-N2
	IP Changes[1]	Refer to the Unified Interconnect IP Release Notes (FPGA-RN-02107).
Resource Utilization	Supported User Interface	Advanced eXtensible Interface 4 (AXI4), AXI4-Lite
	Resources	Refer to Appendix A. Resource Utilization.
Design Tool Support	Lattice Implementation	IP Core v1.0.0 – Lattice Radiant™ Software 2025.2 Lattice Propel™ Design Environment 2025.2
	Synthesis	Synopsys® Synplify Pro for Lattice, Lattice Synthesis Engine
	Simulation	Refer to the Lattice Radiant Software User Guide for the list of supported simulators.

Note:

1. In some instances, the IP may be updated without changes to the user guide. This user guide may reflect an earlier IP version but remains fully compatible with the later IP version. Refer to the IP Release Notes for the latest updates.

1.3. Features

Key features of the Unified Interconnect IP include:

- Each external manager (EM) or external subordinate (ES) can be configured to support various protocols.
  - AMBA 4 AXI4
  - AMBA 4 AXI4-Lite

  Note: ARM Ltd. *AMBA AXI and ACE Protocol Specification,* Issue E, ARM IHI 0022E, February 2013. This specification defines the AMBA AXI4 and AXI4-Lite protocols supported by the Unified Interconnect IP.
- Configurable interface data widths:
  - AXI4: 32, 64, 128, 256, 512, or 1,024 bits
  - AXI4-Lite: 32 or 64 bits
- Address widths:
  - AXI4: Up to 64-bits (13 to 64)
  - AXI4-Lite: Up to 64-bits (13 to 64)
- Supports AXI4 with the following characteristics:
  - User width: Up to 128 bits
  - ID width: Up to 6 bits
  - INCR and FIXED bursts.
    - Supports three types of responses:

    - AXI OKAY
    - AXI DECERR – when undefined external subordinate address region is accessed.
    - AXI SLVERR – for pass through from the external subordinate.
- Supports reduced resource optimization including
    - Read-only manager and subordinate
    - Write-only manager and subordinate
- Supports up to four external managers and/or four external subordinates.
- Options to enable streaming queue, first in first out (FIFO) with CDC, and FIFO without CDC for each EM or ES port.
- Supports fragmented address space of up to 16 fragments per external subordinate.
- Selectable arbitration scheme:
    - Round robin (default)
    - Strict priority (fixed priority)

1.4. Licensing and Ordering Information

The Unified Interconnect IP is provided at no additional cost with the Lattice Radiant software and Lattice Propel design environment.

1.5. Naming Conventions

1.5.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.5.2. Signal Names

Signal names that end with:

- *_n* are active low signals (asserted when value is logic 0)
- *_i* are input signals
- *_o* are output signals

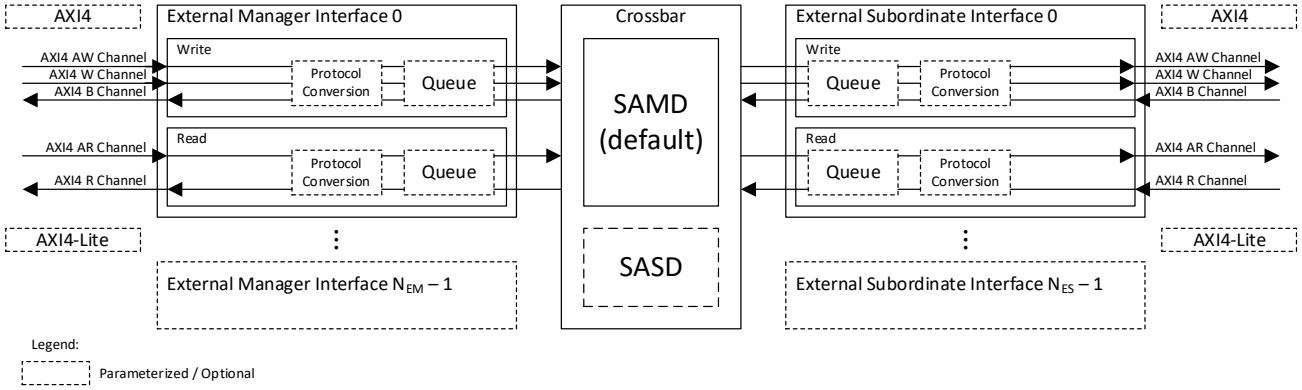
1.5.3. Attribute Names

Attribute names in this document are formatted in title case and italicized (*Attribute Name*).

2. Functional Description

2.1. IP Architecture Overview

The Unified Interconnect IP allows up to N_{EM} external manager devices to connect to N_{ES} external subordinate devices, subject to constraints of the supported protocols. The crossbar arbitrates and routes resource sharing.



Notes:
1. N_{EM} = *Total External Managers*. N_{ES} = *Total External Subordinates*.
2. The SASD crossbar architecture is only available for AXI4-Lite.

Figure 2.1. Lattice Unified Interconnect IP Block Diagram

The Unified Interconnect IP includes the following modules:

- External Manager (EM) Interface
- External Subordinate (ES) Interface
- Crossbar (XB)

2.2. Clocking and Reset

Table 2.1 summarizes the clock and reset domains according to interface and CDC enablement.

Table 2.1. Clocking and Reset Domains Summary

Module	Protocol Selection	CDC	Clock / Reset	Note
External manager interface	AXI4, AXI4-Lite	ENABLE	Sxx_aclk_i / Sxx_aresetn_i	CDC enables the EM interface to operate in the specific clock (Sxx_aclk_i) and reset (Sxx_aresetn_i) domain of the port.
	AXI4, AXI4-Lite	DISABLE	axi_aclk_i / axi_aresetn_i	Without CDC, the EM interface operates in the primary interconnect clock (axi_aclk_i) and reset (axi_aresetn_i) domain.
External subordinate interface	AXI4, AXI4-Lite	ENABLE	Myy_aclk_i / Myy_aresetn_i	CDC enables the ES interface to operate in the specific clock (Myy_aclk_i) and reset (Myy_aresetn_i) domain of the port.
	AXI4, AXI4-Lite	DISABLE	axi_aclk_i / axi_aresetn_i	Without CDC, the ES interface operates in the primary interconnect clock (axi_aclk_i) and reset (axi_aresetn_i) domain.

2.2.1. Reset Overview

The following are the interconnect reset requirements and limitations:

- When the primary *resetn_i signal asserts, the entire interconnect logic must be reset, regardless of CDC enablement in any EM or ES interface.
- Partial reset is not supported. When any EM or ES interface is reset, all EM and ES interfaces must assert their corresponding *resetn_i signals.
- The interconnect de-asserts all valid and ready outputs shortly after the *resetn_i signal asserts asynchronously.
- The assertion period of each *resetn_i signal must overlap across all relevant domains. It is recommended that each *resetn_i signal remains asserted for at least 20 clock cycles to ensure reliable reset synchronization.
- All *resetn_i signals do not need to be de-asserted in the same clock cycle. However, *resetn_i signals must be de-asserted synchronously with their corresponding EM or ES clock domains.

2.3. Other IP Specific Blocks/Layers/Interfaces

2.3.1. External Manager Interface

The external manager interface operates in the same clock and reset domain as the external manager. It connects to the external manager through protocol-specific interfaces. The following are characteristics of the EM interface:

- Supports CDC-capable queue.
- Supports AXI4 and AXI4-Lite protocol conversions.
- Supports configurable read ACCEPTANCE_LIMIT and write ACCEPTANCE_LIMIT to limit the number of outstanding transactions from each external manager.

Note: The external manager interface, also known as the subordinate interface (SI), connects to an AXI manager.

2.3.2. External Subordinate Interface

The external subordinate interface operates in the same clock and reset domain as the external subordinate. It connects to the external subordinate through protocol-specific interfaces. The following are characteristics of the ES interface:

- Supports CDC-capable queue.
- Supports AXI4 and AXI4-Lite protocol conversions.

Note: The external subordinate interface, also known as the manager interface (MI), connects to an AXI subordinate.

2.3.3. Crossbar

The crossbar arbitrates and routes the read or write requests from an external manager device to one or more memory-mapped external subordinate devices. The following are characteristics of the crossbar:

- Routes the write data from the external manager device to the target external subordinate device.
- Routes the response and read data returned from the external subordinate device to the external manager device.
- Supports two crossbar architectures: performance-optimized shared address and multiple data channel (SAMD), and area-optimized shared address and shared data channel (SASD).

2.3.3.1. Shared Address and Multiple Data Channels

The following are characteristics of the SAMD crossbar architecture:

- Regardless of the number of EM ports enabled, the following are present:
  - One shared read address phase processing unit.
  - One shared write address phase processing unit.
  - One shared write response channel.
- The parallel crossbar route for write and read data channels allows multiple write or read data sources to simultaneously target different destinations. This enables data transfers to proceed independently and concurrently, provided the AXI protocol ordering requirements are satisfied.
- Address phase arbitration latencies typically do not impact the data payload transfer throughput for burst transfers.

- Supports external manager devices with reordering depths of up to 2^n, where n represents the external manager *AXI ID width.*
- Configurable external manager read acceptance limit and external manager write acceptance limit to limit the number of outstanding read or write transactions from an external manager.
- Permits address request based on *single slave per active ID* mechanism to ensure protocol compliance in the response ordering.

2.3.3.2. Shared Address and Shared Data Channels

The following are characteristics of the SASD crossbar architecture:

- Regardless of the number of EM ports enabled, there is only one shared address phase processing unit to handle both read and write requests.
- Single access mode permits only one outstanding transaction at a time using the shared data and response channel.

2.3.3.3. Address Phase Processing Unit

The address phase processing unit decodes the address request from the EM to determine the route to an ES or internal default subordinate. The unit permits up to 2^n ID threads per EM, where n represents the external manager *AXI ID width*. After address arbitration, there is a two-clock bubble. Consequently, a minimum of three clock cycles is required between successive arbitrations for the same EM.

2.3.3.4. Single Slave per Active ID

For the *single slave per active ID* mechanism, each active ID thread initiated from an EM interface can have an outstanding transaction to only a single ES interface. Read access and write access are treated independently. ES interfaces are still permitted to issue multiple outstanding transactions initiated from multiple EM interfaces. In the case of external manager device access to different external subordinate devices (for example, A and B), using the same AXI ID, the request to B is permitted only after the outstanding transaction to A has completed. This mechanism supports up to 2^n ID threads per EM, where n represents the external manager *AXI ID width*.

2.3.3.5. Transaction Acceptance Limit

Transaction acceptance limits are configurable parameters to limit the number of outstanding transactions that the crossbar accepts from an EM interface. The following are the configurable parameters:

- External manager read acceptance limit
- External manager write acceptance limit

Each address phase processing unit tracks these limits and active ID threads to determine if a new transaction request from an EM will be temporarily disallowed.

2.3.3.6. Outstanding Transaction

An outstanding transaction is a transaction that has not been completed. A transaction is complete when the following occurs:

- AXI4 write with bvalid/bready handshake completed at XB.
- AXI4 read with rvalid/rready handshake completed at XB with rlast asserted.

2.3.4. Default Subordinate

There is one default subordinate per address phase processing unit. The following occurs when a request address cannot be mapped to a valid memory region for a memory-mapped external subordinate device:

1. The address phase processing unit stops granting new transaction requests from any EM.
2. The unit waits for all ongoing transactions to be completed, then hands execution over to the default subordinate.
3. Depending on the transaction, the following occurs:
    a. For read transaction: The default subordinate returns DECERR with Read Data = *don't care* to the EM until the final data transfer of the burst.
    b. For write transaction: The default subordinate accepts and discards all write data from the EM until the final data transfer of the burst. It then returns DECERR to the EM.

2.3.5. Infrastructure Modules

2.3.5.1. Queue

The queue block is part of a standard FIFO module. The following are characteristics of the block:

- When FIFO Depth = 0, the block is bypassed.
- Without CDC enabled, the single clock FIFO is instantiated.
- With CDC enabled, dual-clock FIFO is instantiated to handle the clock domain crossing between the external manager interface or external subordinate interface and the crossbar.

2.3.5.2. Protocol Conversion

AXI4-Lite to AXI4

For AXI4-Lite to AXI4 conversion, transactions from the AXI4-Lite EM port are mapped to a single-beat AXI4 transfer by setting the following:

- For read: arlen = 0
- For write: awlen = 0 and wlast = 1

AXI4 to AXI4-lite

For AXI4 to AXI4-Lite conversion, all AXI4 bursts (specifically INCR or FIXED burst types) targeting the AXI4-Lite ES port are sliced into multiple individual transfers matching the AXI4-Lite data width.

3. IP Parameter Description

The configurable attributes of the Unified Interconnect IP are shown in the following tables. You can configure the IP by setting the attributes accordingly in the IP Catalog Module/IP Block Wizard of the Lattice Radiant software.

Wherever applicable, default values are in bold.

3.1. General

Table 3.1. General Attributes

Attribute	Selectable Values	Description
General		
Total External Managers	1–4, **2**	Selects the total number of external managers. **Note:** *Total External Managers* and *Total External Subordinates* cannot be set to 1 at the same time.
Total External Subordinates	1–4, **2**	Selects the total number of external subordinates. **Note:** *Total External Managers* and *Total External Subordinates* cannot be set to 1 at the same time.
AXI User width	**1**–128	Specifies the AXI user width.
Memory Type of Large FIFOs	**LUT**, EBR	Selects the memory type for larger FIFOs.
Crossbar Optimization Strategy	**Maximize Performance**, Minimize Area	Selects crossbar mode. Maximize Performance – SAMD Minimize Area – SASD **Note:** The *Minimize Area* option appears only when the AXI4-Lite protocol is selected for all external managers and external subordinates.

3.2. External Manager Settings

Table 3.2. External Manager Settings Attributes

Attribute	Selectable Values	Description
General		
External Manager AXI ID width	1–6, **2**	External manager AXI ID width
Manager Max Address Width(bits)	13–64, **32**	External manager maximum address width Specifies the maximum address bus width of the available external manager.
Manager Max Data Width(bits)	8, 16, **32**, 64, 128, 256, 512,1024	External manager maximum data width Specifies the maximum data bus width of the available external manager.
External Manager Priority	**Round Robin**, Fixed Priority[1]	External manager priority
External Manager Access Type Settings		
External Manager AXI Access Type N	WO, RO, **WR**	External manager access type WO – Write only port RO – Read only port WR – Write/Read port **Note:** N ranges from 0 to (*Total External Managers* – 1).
External Manager Protocol Settings		
External Manager protocol N	**AXI4**, AXI4-Lite	AXI protocol supported by the external manager. **Note:** N ranges from 0 to (*Total External Managers* – 1).

Attribute	Selectable Values	Description
External Manager CDC Enable Settings		
External Manager CDC Enable N	**Unchecked**, Checked	External manager CDC enable Unchecked – CDC is disabled for external manager N. Checked – CDC is enabled for the connected external manager N, which is asynchronous to interconnect clock axi_aclk_i. **Note:** N ranges from 0 to (*Total External Managers* – 1).
External Manager Address Settings		
External Manager N Address width	13–64, **32**	External manager address width **Note:** N ranges from 0 to (*Total External Managers* – 1). **Note:** The *External Manager N Address width* setting must match the *External Subordinate M Address width* setting.
External Manager Data Settings		
External Manager Data width N	8, 16, **32**, 64, 128, 256, 512, 1024	External manager data width **Note:** N ranges from 0 to (*Total External Managers* – 1). **Note:** When *External Manager protocol N* = AXI4-Lite, the available options are only 32 and 64. **Note:** The *External Manager Data width N* setting must match the *External Subordinate Data width M* setting.
External Manager Write Acceptance Limit Settings		
External Manager Write Acceptance Limit N	1–32, **2**	External manager write acceptance limit Sets the limit for the number of outstanding write transactions from the external manager. **Note:** N ranges from 0 to (*Total External Managers* – 1).
External Manager Read Acceptance Limit Settings		
External Manager Read Acceptance Limit N	1–32, **2**	External manager read acceptance limit Sets the limit for the number of outstanding read transactions from the external manager. **Note:** N ranges from 0 to (*Total External Managers* – 1).
External Manager Write Address Buffer Depth Settings		
External Manager Write Address Buffer Depth N	**0**[2, 3], 2, 4, **8**[3], 16	Sets the number of outstanding write transactions that can be accepted by external manager N connected to the interconnect. This setting configures the internal FIFO depth for the Write Address channel. **Note:** N ranges from 0 to (*Total External Managers* – 1).
External Manager Read Address Buffer Depth Settings		
External Manager Read Address Buffer Depth N	**0**[2, 3], 2, 4, **8**[3], 16	Sets the number of outstanding read transactions that can be accepted by external manager N connected to the interconnect. This setting configures the internal FIFO depth for the Read Address channel. **Note:** N ranges from 0 to (*Total External Managers* – 1).
External Manager Write Buffer Settings		
External Manager Write Response Buffer Depth N	**0**[2, 3], 2, 4, **8**[3], 16	Sets the internal FIFO depth for the Write Response channel. **Note:** N ranges from 0 to (*Total External Managers* – 1).
External Manager Write Data Buffer Depth N	0[2], **2**[4], 4, **8**[4], 16, 32, 64, 128, 256, 512	Sets the internal FIFO depth for the Write Data channel. **Note:** N ranges from 0 to (*Total External Managers* – 1).
External Manager Read Buffer Settings		
External Manager Read Data Buffer Depth N	**0**[2, 3], 2, 4, **8**[3], 16, 32, 64, 128, 256, 512	Sets the internal FIFO depth for the Read Data channel. **Note:** N ranges from 0 to (*Total External Managers* – 1).
External Manager 0 Fixed Priority Settings		
Ext Manager N Fixed Priority	0 to (*Total External Subordinates* –1), **N**	External manager N fixed priority **Note:** N ranges from 0 to (*Total External Managers* – 1).

Notes:

1. Priority order 0, 1, 2, …, N, with 0 being the highest priority.
2. The selectable value 0 is only available when the external manager CDC is disabled.

3. The following default values apply depending on whether CDC is enabled or disabled:
   - 0 when external manager CDC is disabled.
   - 8 when external manager CDC is enabled.
4. The following default values apply depending on whether CDC is enabled or disabled:
   - 2 when external manager CDC is disabled.
   - 8 when external manager CDC is enabled.

3.3. External Subordinate Settings

Table 3.3. External Subordinate Settings Attributes

Attribute	Selectable Values	Description
General		
External Subordinate AXI ID width	1–8, **4**	External subordinate AXI ID width The setting must satisfy the following condition: *External Subordinate AXI ID width* ≥ *External Manager AXI ID width* + $\log_2$(*Total External Managers*)
Subordinate Max Address Width(bits)	13–64, **32**	External subordinate maximum address width Specifies the maximum address bus width of the available external subordinate.
Subordinate Max Data Width(bits)	8, 16, **32**, 64, 128, 256, 512,1024	External subordinate maximum data width Specifies the maximum data bus width of the available external subordinate.
Subordinate Max Fragment count	1–16, **8**	External subordinate maximum fragment count Specifies the maximum fragment count of the available external subordinate.
External Subordinate Access Type Settings		
External Subordinate AXI Access Type M	WO, RO, **WR**	External subordinate AXI access type WO – Write only port RO – Read only port WR – Write/Read port **Note:** M ranges from 0 to (*Total External Subordinates* – 1).
External Subordinate Protocol Type Settings		
External Subordinate Protocol type M	**AXI4**, AXI4-Lite	AXI protocol supported by the external subordinate. **Note:** M ranges from 0 to (*Total External Subordinates* – 1).
External Subordinate CDC Enable Settings		
External Subordinate CDC Enable M	**Unchecked**, Checked	External subordinate CDC enable Unchecked – CDC is disabled for external subordinate M. Checked – CDC is enabled for the connected external subordinate M, which is asynchronous to interconnect clock axi_aclk_i. **Note:** M ranges from 0 to (*Total External Subordinates* – 1).
External Subordinate Address Settings		
External Subordinate M Address width	13–64, **32**	External subordinate address width **Note:** M ranges from 0 to (*Total External Subordinates* – 1). **Note:** The *External Subordinate M Address width* setting must match the *External Manager N Address width* setting.
External Subordinate Data Settings		
External Subordinate Data width M	8, 16, **32**, 64, 128, 256, 512, 1024	External subordinate data width **Note:** M ranges from 0 to (*Total External Subordinates* – 1). **Note:** When *External Subordinate Protocol type M* = AXI4-Lite, the available options are only 32 and 64. **Note:** The *External Subordinate Data width M* setting must match the *External Manager Data width N* setting.

Attribute	Selectable Values	Description
External Subordinate Write Address Buffer Depth Settings		
External Subordinate Write Address Buffer Depth M	**0**[1, 2], 2, 4, **8**[2], 16	Sets the number of outstanding write transactions issued from external subordinate M connected to the interconnect. This setting configures the internal FIFO depth for the Write Address channel. **Note:** M ranges from 0 to (*Total External Subordinates* – 1).
External Subordinate Read Adress Buffer Depth Settings		
External Subordinate Read Address Buffer Depth M	**0**[1, 2], 2, 4, **8**[2], 16	Sets the number of outstanding read transactions issued from external subordinate M connected to the interconnect. This setting configures the internal FIFO depth for the Read Address channel. **Note:** M ranges from 0 to (*Total External Subordinates* – 1).
External Subordinate Write Buffer Settings		
External Subordinate Write Response Buffer Depth M	**0**[1, 2], 2, 4, **8**[2], 16	Sets the internal FIFO depth for the Write Response channel. **Note:** M ranges from 0 to (*Total External Subordinates* – 1).
External Subordinate Write Data Buffer Depth M	**0**[1, 2], 2, 4, **8**[2], 16, 32, 64, 128, 256, 512	Sets the internal FIFO depth for the Write Data channel. **Note:** M ranges from 0 to (*Total External Subordinates* – 1).
External Subordinate Read Buffer Settings		
External Subordinate Read Data Buffer Depth M	**0**[1, 3], **2**[3], 4, **8**[3], 16, 32, 64, 128, 256, 512	Sets the internal FIFO depth for the Read Data channel. **Note:** M ranges from 0 to (*Total External Subordinates* – 1).
External Subordinate Fragment Settings		
External Subordinate M Fragment Cnt	**1**–16	Sets the external subordinate fragment count. **Note:** M ranges from 0 to (*Total External Subordinates* – 1).
External Subordinate M Base Address Settings[4]		
Base address F	0 to (2^*External Subordinate M Address width*) – 'h1000	Base address for external subordinate M fragment F. **Note:** F ranges from 0 to (*External Subordinate M Fragment Cnt* – 1). **Note:** M = *Total External Subordinates* – 1
External Subordinate M End Address Settings[4]		
End address F[5]	'hFFF – (2^*External Subordinate M Address width*)	End address for external subordinate M fragment F. **Note:** F ranges from 0 to (*External Subordinate M Fragment Cnt* – 1). **Note:** M = *Total External Subordinates* – 1

Notes:

1. The selectable value 0 is only available when external subordinate CDC is disabled.
2. The following default values apply depending on whether CDC is enabled or disabled:
   - 0 when external subordinate CDC is disabled.
   - 8 when external subordinate CDC is enabled.
3. The following default values apply depending on whether CDC is enabled or disabled and the *Crossbar Optimization Strategy* setting:
   - 0 when external subordinate CDC is disabled with crossbar mode set to SASD.
   - 2 when external subordinate CDC is disabled with crossbar mode set to SAMD.
   - 8 when external subordinate CDC is enabled.
4. These attributes are hidden and automatically configured in the Lattice Propel Builder software.
5. The minimum size for each of the external subordinate fragments must be a multiple of 4 KB.
   Examples:
   - Subordinate 0 fragment 0 base address = 'h0000
   - Subordinate 0 fragment 0 end address = 'h0FFF
   - Subordinate 0 fragment 1 base address = 'h1000
   - Subordinate 0 fragment 1 end address = 'h1FFF

4. Signal Description

This section describes the Unified Interconnect IP ports. Figure 4.1 shows the interface diagram for the Unified Interconnect IP without CDC enabled. This diagram shows all the available ports for the IP except clock domain crossing clock and reset ports. Figure 4.2 shows the interface diagram for the Unified Interconnect IP with CDC enabled.

All AXI manager and subordinate interface signals are compliant with the AXI4 and AXI4-Lite protocols. All reset signals are asynchronously asserted but synchronously de-asserted. Refer to the AMBA AXI Protocol Specification web page for the timing diagrams and more information about the protocol.

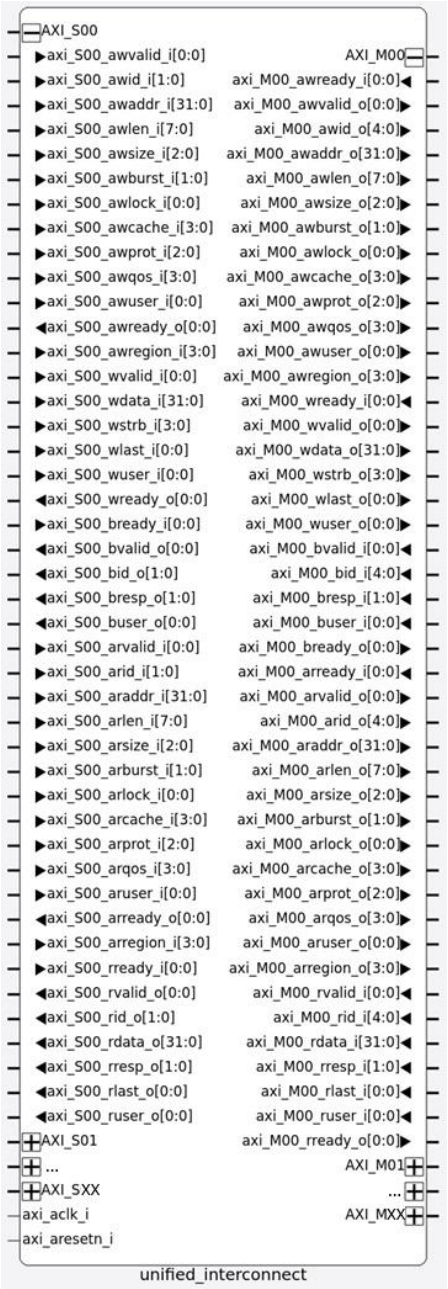


Figure 4.1. Unified Interconnect IP Interface Diagram without CDC

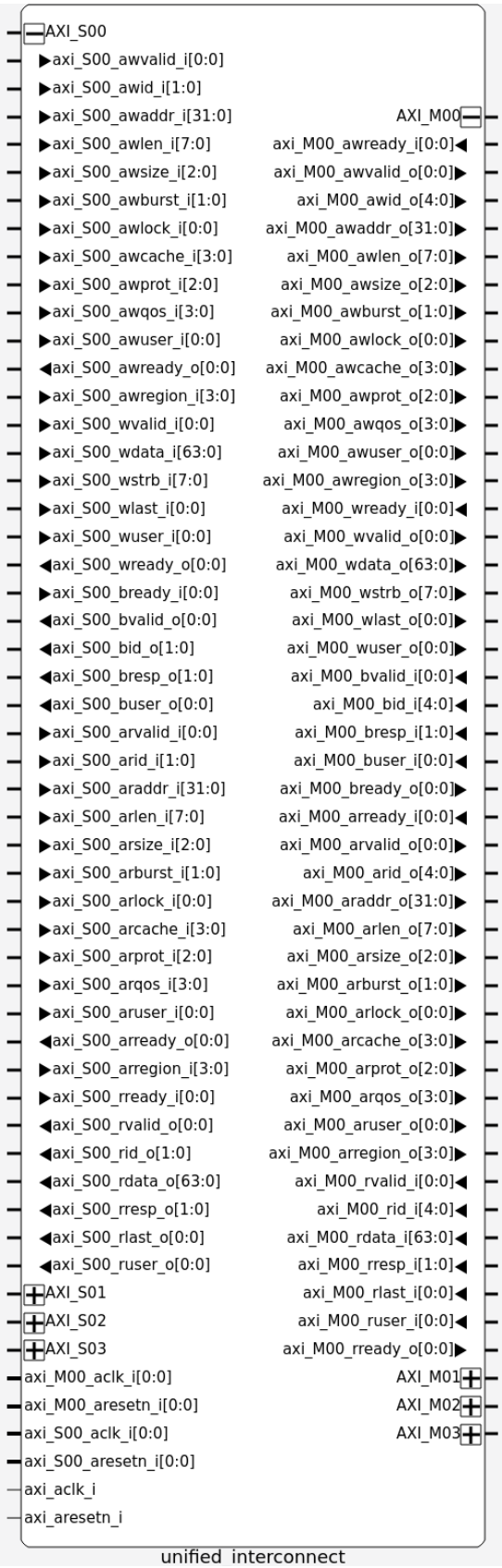


Figure 4.2. Unified Interconnect IP Interface Diagram with External Manager 0 and External Subordinate 0 CDC Enabled

4.1. AXI4 External Manager Interface

Table 4.1 AXI4 External Manager Interface Ports

Port[1]	Type	Description
AXI Interconnect Subordinate xx Clock and Reset (Available if CDC is Enabled for Port Sxx)		
axi_Sxx_aclk_i[2]	Input	Input clock to AXI interconnected subordinate xx port This signal is required only when CDC is enabled for the external manager xx port.
axi_Sxx_aresetn_i[2]	Input	Input AXI active low reset to AXI interconnected subordinate xx port This signal is required only when CDC is enabled for the external manager xx port.
AXI Interconnect xx Interface – Connected to External Manager xx[3]		
axi_Sxx_awvalid_i[2]	Input	Write address valid
axi_Sxx_awid_i[x:0][4]	Input	Write address ID **Note:** x = *External Manager AXI ID width* – 1
axi_Sxx_awaddr_i[x:0][2]	Input	Write address **Note:** x = *Manager Max Address Width(bits)* – 1
Axi_Sxx_awlen_i[7:0][4]	Input	Write address burst length The exact number of transfers in a burst.
axi_Sxx_awsize_i[2:0][4]	Input	Write address burst size The size of each transfer in the burst.
axi_Sxx_awburst_i[1:0][4]	Input	Write address burst type
axi_Sxx_awlock_i[4]	Input	Write address lock type
axi_Sxx_awcache_i[3:0][4]	Input	Write address memory type
axi_Sxx_awprot_i[2:0][2]	Input	Write address protection type
axi_Sxx_awqos_i[3:0][4]	Input	Write address quality of service
axi_Sxx_awregion_i[3:0]	Input	Write address region
axi_Sxx_awuser_i[x:0][4]	Input	Write address user signals **Note:** x = *AXI User width* – 1
axi_Sxx_awready_o[2]	Output	Write address ready
axi_Sxx_wvalid_i[2]	Input	Write valid
axi_Sxx_wdata_i[x:0][2]	Input	Write data **Note:** x = *Manager Max Data Width(bits)* – 1
axi_Sxx_wstrb_i[x:0][2]	Input	Write strobes **Note:** x = (*Manager Max Data Width(bits)*/8) – 1
axi_Sxx_wlast_i[4]	Input	AXI4 last write beat/burst
axi_Sxx_wuser_i[x:0][4]	Input	Write data user signal **Note:** x = *AXI User width* – 1
axi_Sxx_wready_o[2]	Output	Write ready
axi_Sxx_bvalid_o[2]	Output	Write response valid
axi_Sxx_bid_o[x:0]	Output	Write respond ID **Note:** x = *External Manager AXI ID width* – 1
axi_Sxx_bresp_o[1:0][2]	Output	Write response
axi_Sxx_buser_o[x:0][4]	Output	Write response user signal **Note:** x = *AXI User width* – 1
axi_Sxx_bready_i[2]	Input	Response ready
axi_Sxx_arvalid_i[2]	Input	Read address valid
axi_Sxx_arid_i[x:0][4]	Input	Read address ID **Note:** x = *External Manager AXI ID width* – 1
axi_Sxx_araddr_i[x:0][2]	Input	Read address **Note:** *Manager Max Address Width(bits)* – 1

Port[1]	Type	Description
axi_Sxx_arlen_i[7:0][4]	Input	Read address burst length
axi_Sxx_arsize_i[2:0][4]	Input	Read address burst size
axi_Sxx_arburst_i[1:0][4]	Input	Read address burst type
axi_Sxx_arlock_i[4]	Input	Read address lock type
axi_Sxx_arcache_i[3:0][4]	Input	Read address memory type
axi_Sxx_arprot_i[2:0][2]	Input	Read address protection type
axi_Sxx_arqos_i[3:0][4]	Input	Read address quality of service
axi_Sxx_arregion_i[3:0]	Input	Read address region
axi_Sxx_aruser_i[x:0][4]	Input	Read address user signal **Note:** x = *AXI User width* – 1
axi_Sxx_arready_o[2]	Output	Read address ready
axi_Sxx_rvalid_o[2]	Output	Read valid
axi_Sxx_rid_o[x:0]	Output	Read ID **Note:** x = *External Manager AXI ID width* – 1
axi_Sxx_rdata_o[x:0][2]	Output	Read data **Note:** x = *Manager Max Data Width(bits)* – 1
axi_Sxx_rresp_o[1:0][2]	Output	Read response
axi_Sxx_rlast_o	Output	Last read
axi_Sxx_ruser_o[x:0][4]	Output	Read response user signal **Note:** x = *AXI User width* – 1
axi_Sxx_rready_i[2]	Input	Read ready

Notes:

1. All ports are applicable or optional when the AXI4 protocol is selected. Only selected ports are applicable when the AXI4-Lite protocol is selected as indicated by Note 2. Optional ports for the AXI4 protocol are indicated by Note 4.
2. Applicable when the AXI4-Lite protocol is selected.
3. xx denotes the external manager port number ranging from 00 to 0N, where N = *Total External Managers* – 1.
4. Optional when the AXI4 protocol is selected.

4.2. AXI4 External Subordinate Interface

Table 4.2. AXI4 External Subordinate Interface Ports

Port[1]	Type	Description
AXI Interconnect Manager yy Clock and Reset (Available if CDC is Enabled for Port Myy)[2]		
axi_Myy_aclk_i[2]	Input	Input clock to AXI interconnected manager yy port. This signal is required only when CDC is enabled for the external subordinate yy port.
axi_Myy_aresetn_i[2]	Input	Input AXI active low reset to AXI interconnected manager yy port. This signal is required only when CDC is enabled for the external subordinate yy port.
AXI Interconnect Manager yy Interface – Connected to External Subordinate yy		
axi_Myy_awvalid_o[3]	Output	Write address valid
axi_Myy_awid_o[x:0]	Output	Write address ID **Note:** x = *External Subordinate AXI ID width* – 1
axi_Myy_awaddr_o[x:0][3]	Output	Write address **Note:** x = *Subordinate Max Address Width(bits)* – 1
axi_Myy_awlen_o[7:0]	Output	Write address burst length The exact number of transfers in a burst.
axi_Myy_awsize_o[2:0]	Output	Write address burst size The size of each transfer in the burst.
axi_Myy_awburst_o[1:0]	Output	Write address burst type
axi_Myy_awlock_o	Output	Write address lock type
axi_Myy_awcache_o[3:0]	Output	Write address memory type
axi_Myy_awprot_o[2:0][3]	Output	Write address protection type
axi_Myy_awqos_o[3:0]	Output	Write address quality of service
axi_Myy_awregion_o[3:0]	Output	Write address region
axi_Myy_awuser_o[x:0]	Output	Write address user signals **Note:** x = *AXI User width* – 1
axi_Myy_awready_i[3]	Input	Write address ready
Axi_Myy_wvalid_o[3]	Output	Write valid
Axi_Myy_wdata_o[x:0][3]	Output	Write data **Note:** x = *Subordinate Max Data Width(bits)* – 1
Axi_Myy_wstrb_o[x:0][3]	Output	Write strobes **Note:** x = (*Subordinate Max Data Width(bits)*/8) – 1
Axi_Myy_wlast_o[4]	Output	AXI4 last write beat/burst
axi_Myy_wuser_o[x:0]	Output	User signal **Note:** x = *AXI User width* – 1
axi_Myy_wready_i[3]	Input	Write ready
Axi_Myy_bvalid_i[3]	Input	Write response valid
Axi_Myy_bid_i[x:0]	Input	Write response ID **Note:** x = *External Subordinate AXI ID width* – 1
axi_Myy_bresp_i[1:0][3]	Input	Write response
axi_Myy_buser_i[x:0]	Input	User signal **Note:** x = *AXI User width* – 1
axi_Myy_bready_o[3]	Output	Response ready
axi_Myy_arvalid_o[3]	Output	Read address valid
axi_Myy_arid_o[x:0]	Output	Read address ID **Note:** x = *External Subordinate AXI ID width* – 1
axi_Myy_araddr_o[x:0][3]	Output	Read address **Note:** x = *Subordinate Max Address Width(bits)* – 1

Port[1]	Type	Description
axi_Myy_arlen_o[7:0]	Output	Read address burst length
axi_Myy_arsize_o[2:0]	Output	Read address burst size
axi_Myy_arburst_o[1:0]	Output	Read address burst type
axi_Myy_arlock_o	Output	Read address lock type
axi_Myy_arcache_o[3:0]	Output	Read address memory type
axi_Myy_arprot_o[2:0][3]	Output	Read address protection type
axi_Myy_arqos_o[3:0]	Output	Read address quality of service
axi_Myy_arregion_o[3:0]	Output	Read address region
axi_Myy_aruser_o[x:0]	Output	Read address user signal **Note:** x = *AXI User width* – 1
axi_Myy_arready_i[3]	Input	Read address ready
axi_Myy_rvalid_i[3]	Input	Read valid
axi_Myy_rid_i[x:0]	Input	Read ID **Note:** x = *External Subordinate AXI ID width* – 1
axi_Myy_rdata_i[x:0][3]	Input	Read data **Note:** x = *Subordinate Max Data Width(bits)* – 1
axi_Myy_rresp_i[1:0][3]	Input	Read response
axi_Myy_rlast_i	Input	Last read
axi_Myy_ruser_i[x:0][4]	Input	Read response user signal **Note:** x = *AXI User width* – 1
axi_Myy_rready_o[3]	Output	Read ready

Notes:

1. All ports are applicable or optional when the AXI4 protocol is selected. Only selected ports are applicable when the AXI4-Lite protocol is selected as indicated by Note 3. Optional ports for the AXI4 protocol are indicated by Note 4.
2. yy denotes the external subordinate port number ranging from 00 to 0M, where M = *Total External Subordinates* – 1.
3. Applicable when the AXI4-Lite protocol is selected.
4. Optional when the AXI4 protocol is selected.

4.3. AXI4 Crossbar Interface

Table 4.3. AXI4 Crossbar Interface Ports

Port	Type	Description
Clock and Reset		
axi_aclk_i	Input	AXI clock to AXI interconnect
axi_aresetn_i	Input	AXI active low reset

5. Designing with the IP

This section provides information on how to generate the IP core using the Lattice Radiant software. For more details on the Lattice Radiant software, refer to the Lattice Radiant Software User Guide.

Note: Similar information applies for the Lattice Propel design environment. For more information, refer to the Lattice Propel Builder User Guide.

Note: The screenshots provided are for reference only. Details may vary depending on the version of the IP or software being used. If there have been no significant changes to the GUI, a screenshot may reflect an earlier version of the IP.

5.1. Generating and Instantiating the IP

You can use the Lattice Radiant software to generate IP modules and integrate them into the device architecture. The steps below describe how to generate the Unified Interconnect IP in the Lattice Radiant software.

To generate the Unified Interconnect IP:

1. Create a new Lattice Radiant software project or open an existing project.
2. Click the **IP Catalog** button to view the **IP Catalog** pane.
3. On the **IP on Local** tab, double-click **Unified Interconnect** under **IP/…/Processors_Controllers_and_Peripherals** category. The **Module/IP Block Wizard** opens.
   Note: If the IP is not available on the **IP on Local** tab, download the IP from the **IP on Server** tab.

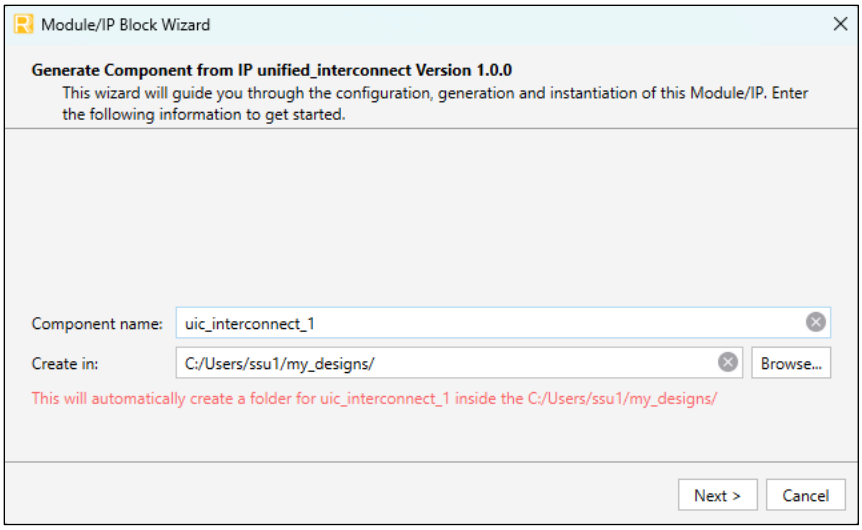


Figure 5.1. Module/IP Block Wizard

4. Enter values in the **Component name** and **Create in** fields, then click **Next**.
5. Customize the selected Unified Interconnect IP using drop-down lists and check boxes. Figure 5.2 shows an example configuration of the Unified Interconnect IP. For details on the configuration options, refer to the IP Parameter Description section.

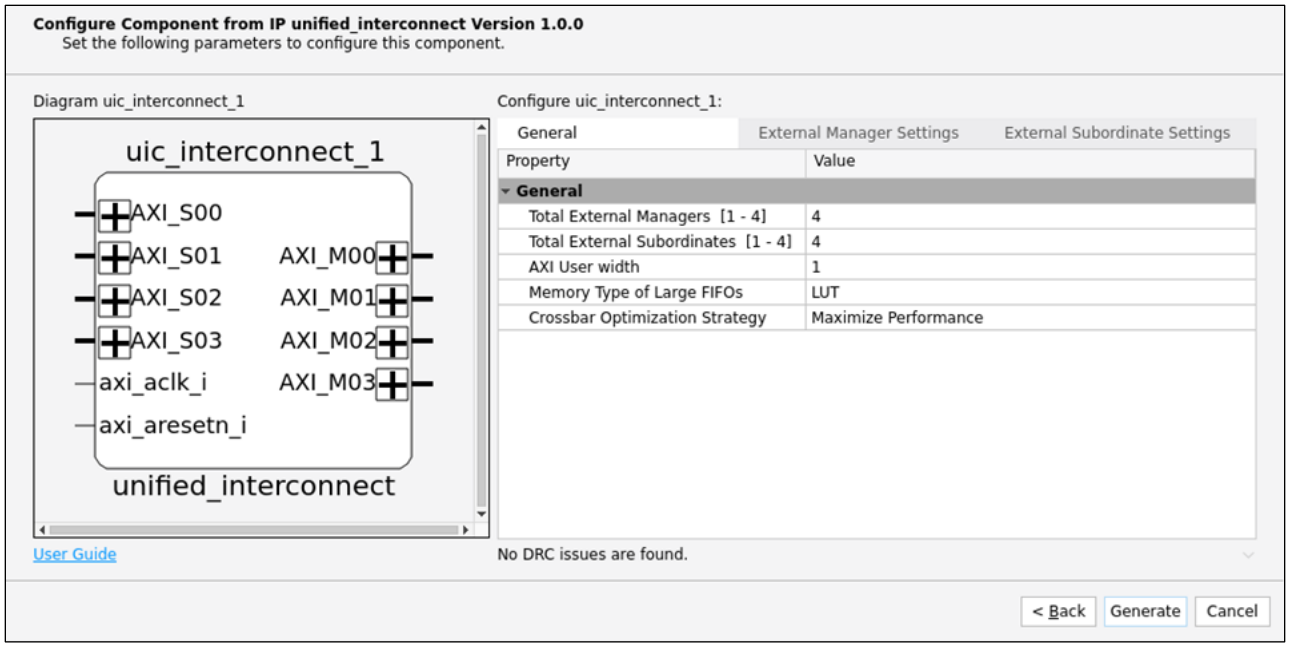


Figure 5.2. IP Configuration

6. Click **Generate**. The **Check Generated Result** window opens. This window shows design block messages and results.

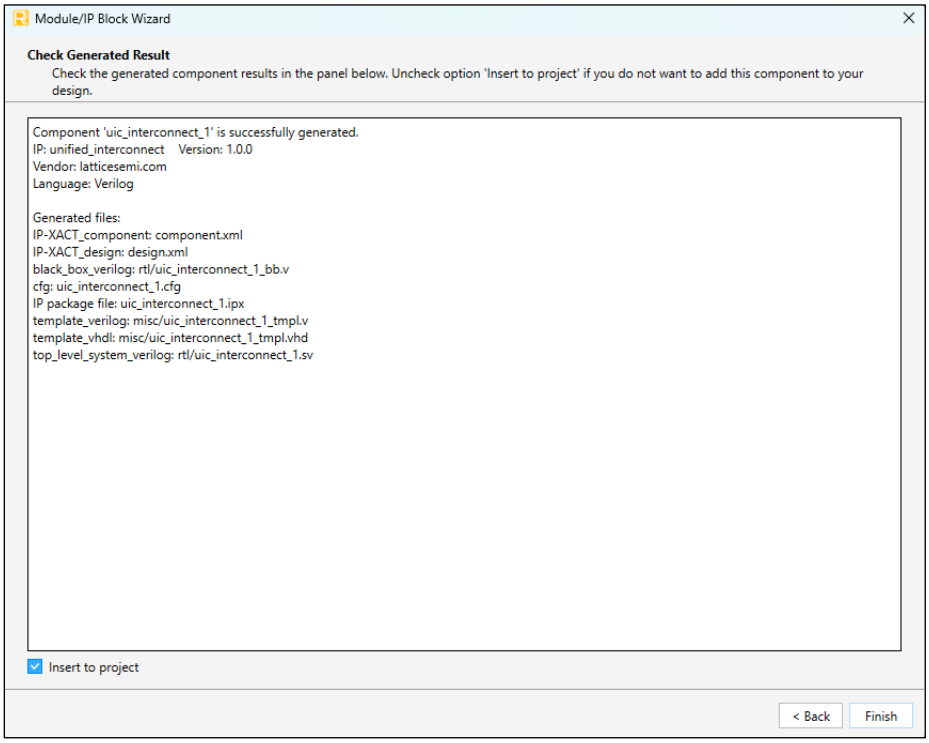


Figure 5.3. Check Generated Result

7. Click **Finish**. All generated files are placed in the directory specified by the **Component name** and **Create in** fields shown in Figure 5.1.

5.1.1. Generated Files and File Structure

The generated Unified Interconnect module package includes the closed-box (*<Component name>_bb.v*) and instance templates (*<Component name>_tmpl.v/vhd*) that can be used to instantiate the core in a top-level design. An example RTL top-level reference source file (*<Component name>.v*) that can be used as an instantiation template for the module is also provided. You may also use this example as the starting template for your top-level design. The generated files are listed in Table 5.1.

Table 5.1. Generated File List

Attribute	Description
<Component name>.ipx	Contains the information on the files associated with the generated IP.
<Component name>.cfg	Contains the parameter values used in IP configuration.
component.xml	Contains the ipxact: component information of the IP.
design.xml	Documents the configuration parameters of the IP in IP-XACT 2014 format.
rtl/<Component name>.v	Provides an example RTL top file that instantiates the module.
rtl/<Component name>_bb.v	Provides the synthesis closed-box.
misc/<Component name>_tmpl.v misc /<Component name>_tmpl.vhd	Provide instance templates for the module.

5.2. Design Implementation

Completing your design includes additional steps to specify analog properties, pin assignments, and timing and physical constraints. You can add and edit the constraints using the Device Constraint Editor or by manually creating a .pdc file.

Post-Synthesis constraint files (.pdc) contain both timing and non-timing *constraint.pdc* source files for storing logical timing/physical constraints. Constraints that are added using the Device Constraint Editor are saved to the active .pdc file. The active post-synthesis design constraint file is then used as input for post-synthesis processes.

Refer to the relevant sections in the Lattice Radiant Software User Guide for more information on how to create or edit constraints and how to use the Device Constraint Editor.

5.3. Timing Constraints

The timing constraints are based on the clock frequency used. The timing constraints for the IP are defined in relevant constraint files. There are three clock groups in the Unified Interconnect IP as follows:

- Interconnect primary clock (axi_aclk_i) – required by the IP

```
create_clock [get_ports {axi_aclk_i}] -name aclk -period <clock period in ns>
```

- Individual EM clock (axi_Sxx_aclk_i) – when external manager CDC is enabled

```
create_clock [get_ports {axi_Sxx_aclk_i[0]}] -name cdc_sxx_aclk -period
<master period in ns>
set_clock_groups -asynchronous -group aclk -group cdc_sxx_aclk
```

- Individual ES clock (axi_Myy_aclk_i) – when external subordinate CDC is enabled

```
create_clock [get_ports {axi_Myy_aclk_i[0]}] -name cdc_myy_aclk -period
<slave period in ns>
set_clock_groups -asynchronous -group aclk -group cdc_myy_aclk
```

Note: xx denotes the external manager port number ranging from 00 to 0N, where N = *Total External Managers* – 1. yy denotes the external subordinate port number ranging from 00 to 0M, where M = *Total External Subordinates* – 1

The example below shows the IP timing constraints generated for the Unified Interconnect IP for the following IP configuration:

- Crossbar clock = 125 MHz
- Two external managers
- External manager 0: CDC enabled, supplied clock = 120 MHz
- Two external subordinates
- External subordinate 0: CDC enabled, supplied clock = 80 MHz

For timing closure, add the following timing constraints in the .pdc file:

```
create_clock [get_ports {axi_aclk_i}] -name aclk -period 8.000
create_clock [get_ports {axi_S00_aclk_i}] -name cdc_s00_aclk -period 8.333
set_clock_groups -asynchronous -group aclk -group cdc_s00_aclk
create_clock [get_ports {axi_M00_aclk_i}] -name cdc_m00_aclk -period 12.500
set_clock_groups -asynchronous -group aclk -group cdc_m00_aclk
```

For more information on timing constraints, refer to the Lattice Radiant Timing Constraints Methodology (FPGA-AN-02059).

6. Design Considerations

6.1. Limitations

Limitations of the Unified Interconnect IP include the following:

- WRAP bursts are not supported.
  - For AXI4 to AXI4-Lite conversion, the AXI4-Lite ES araddr or awaddr will be incorrect.
  - For AXI4 transactions without data width conversion, arburst or awburst is passed through.
- During an AXI4 external manager request:
  - AxQOS, AxREGION, AxUSER, AxCACHE, and AxLOCK signals are ignored when transactions are forwarded to an external AXI4-Lite subordinate interface.
  - AxQOS, AxREGION, AxUSER, AxCACHE, AxLOCK, and AxPROT signals are preserved when transactions are forwarded to an external AXI4 subordinate interface.

6.2. Design Considerations for Throughput

6.2.1. Burst Transfer

The following are design considerations when implementing burst transfer:

- In the SAMD crossbar architecture, to prevent bubbles in the WDATA or RDATA channel during performance-critical AXI4 transfers, the burst length must be greater than or equal to the shared address channel grant and routing latency. This ensures that bubbles are not introduced in the WDATA or RDATA channel.
- You can optionally configure the queue depth at the EM or ES interface, through the *External Manager Write Address Buffer Depth N*, *External Manager Read Address Buffer N*, *External Subordinate Write Address Buffer Depth M*, or *External Subordinate Read Address Buffer Depth M* attributes as applicable, to reduce the impact of address grant bottlenecks. For example, EM1-to-ES1 transfers can be queued behind stalled EM0-to-ES0 transfers.
- With a shared write response channel, there is a small grant delay in the write response (B channel). You can optionally configure the external manager response FIFO, through the *External Manager Write Response Buffer Depth N* attribute, to minimize the impact of response path bottlenecks.

6.2.2. Pipelining Transfer

In pipelining transfer, a new transaction is accepted before the previous transaction is completed. The following sections describe design considerations when pipelining for write and read transactions and performing bottleneck clearance.

Note: The examples discussed in this section are based on the SAMD crossbar architecture with the Round Robin arbiter scheme setting for the *External Manager Priority* attribute.

6.2.2.1. Write Transaction

After the address phase grant for an EM, a two-clock bubble occurs. This results in a minimum of three clock cycles between successive arbitrations by the same EM due to internal tracking pipe stages. For example:

- With only one EM actively issuing transaction requests:
  - After granting an ES to the EM, the address phase processing unit will not grant to the same EM for two clock cycles.
  - If awlen ≥ 2, no bubble is introduced in WDATA.

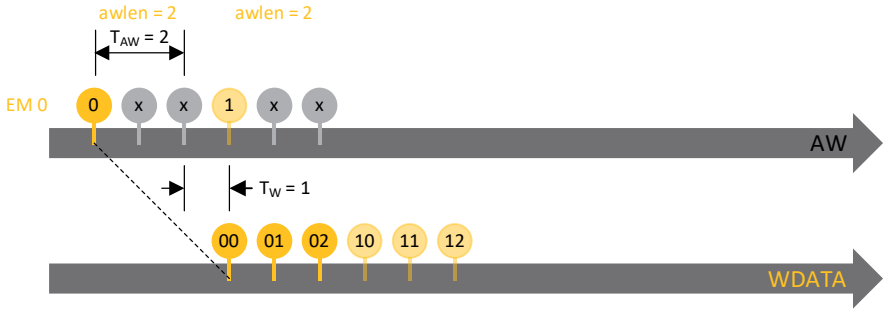


Figure 6.1. Write Transactions for One Active EM with awlen ≥ 2

- With up to four EMs actively issuing transaction requests:
  - The address phase processing unit grants to the EMs back-to-back.
  - When there are many EMs actively issuing transaction requests, a larger burst awlen might be required to avoid bubbles in WDATA.
    - If burst awlen = 2 for four EMs, a bubble is introduced in WDATA for each transaction.

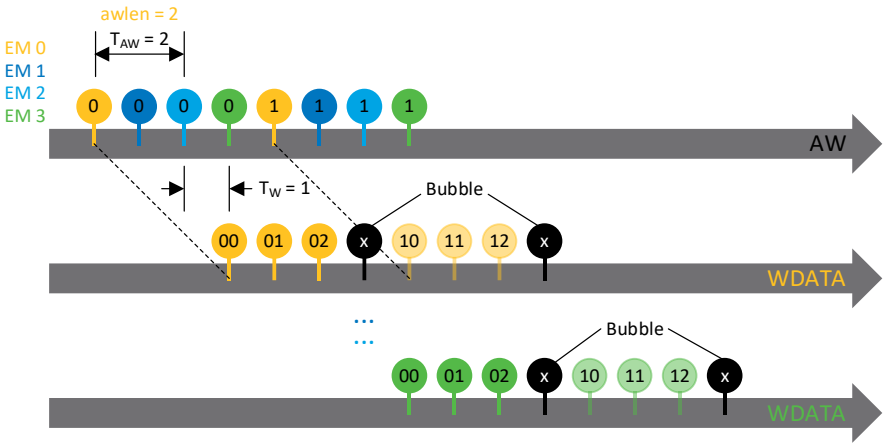


Figure 6.2. Write Transactions for Four Active EMs with awlen = 2

- If burst awlen ≥ 3 for four EMs, no bubble is introduced in WDATA.

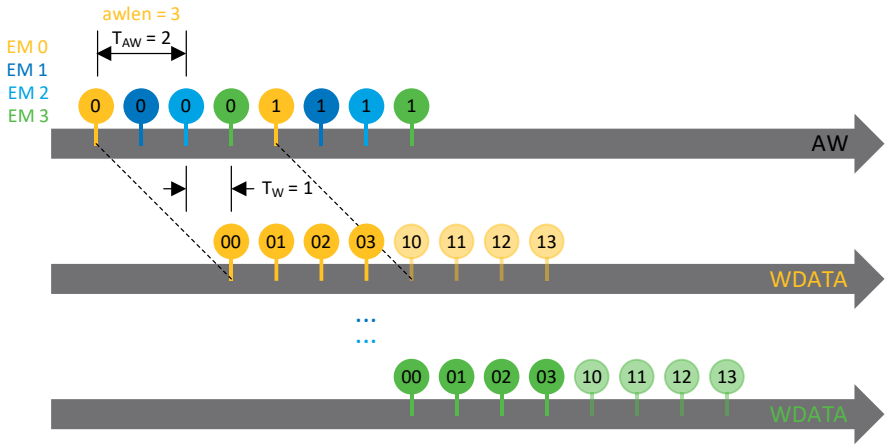


Figure 6.3. Write Transactions for Four Active EMs with awlen ≥ 3

6.2.2.2. Read Transaction

After the address phase grant for an EM, a two-clock bubble occurs. This results in a minimum of three clock cycles between successive arbitrations by the same EM due to internal tracking pipeline stages. For example:

- With only one EM actively issuing transaction requests:
  - After granting an ES to the EM, the address phase processing unit will not grant to the same EM for two clock cycles.
  - If the back-to-back read address request interval < burst arlen, no bubble is introduced in RDATA.

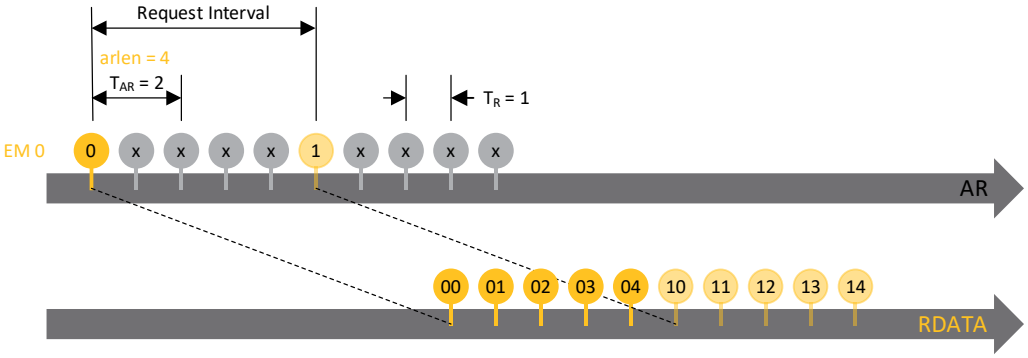


Figure 6.4. Read Transactions for One Active EM with Request Interval < arlen

- If the back-to-back AR request interval > burst arlen, bubbles are introduced in RDATA.

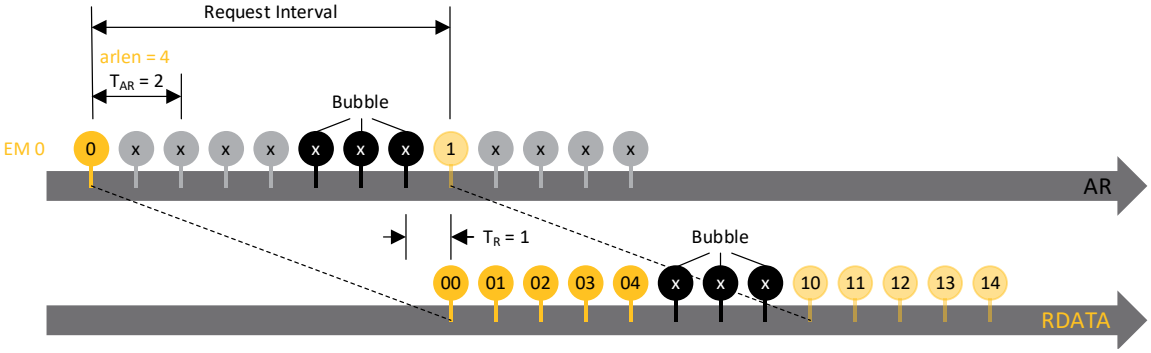


Figure 6.5. Read Transactions for One Active EM with arlen ≤ Request Interval

- To ensure back-to-back read data requests do not introduce bubbles in RDATA, the following condition must be met:
  External Manager Read Acceptance Limit N × [Time to transfer (arlen + 1) × arsize] ≥ Memory Read Round Trip Latency
  Note: Memory Read Round Trip Latency is defined as the time from the read address request to an external subordinate device until the first beat of read data return arrives at the external manager.

- With up to four EMs actively issuing transaction requests:
  - The address phase processing unit grants to the EMs back-to-back.
  - When there are many EMs actively issuing transaction requests, a larger burst arlen might be required to avoid bubbles in RDATA.
    - If burst arlen = 2 for four EMs, a bubble is introduced in RDATA for each transaction.

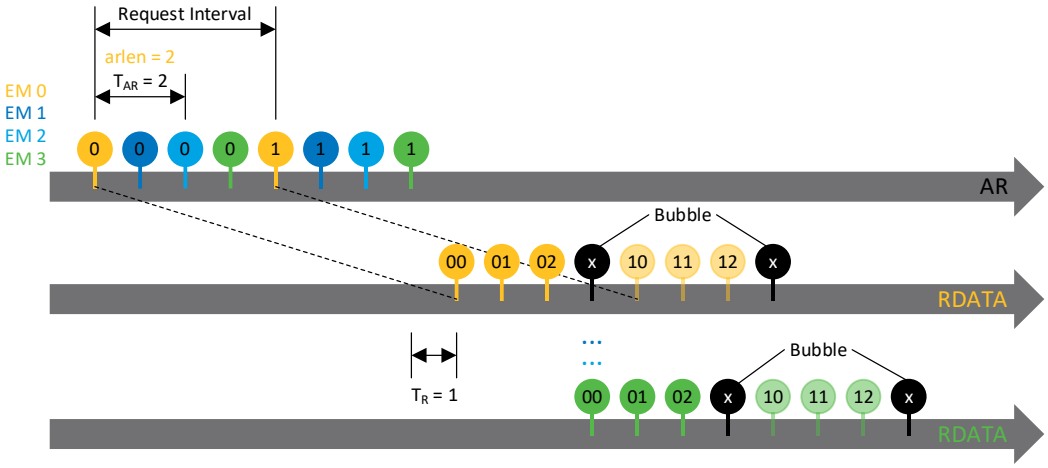


Figure 6.6. Read Transactions for Four Active EMs with arlen = 2

    - If burst arlen ≥ 3 for four EMs, no bubble is introduced in RDATA.

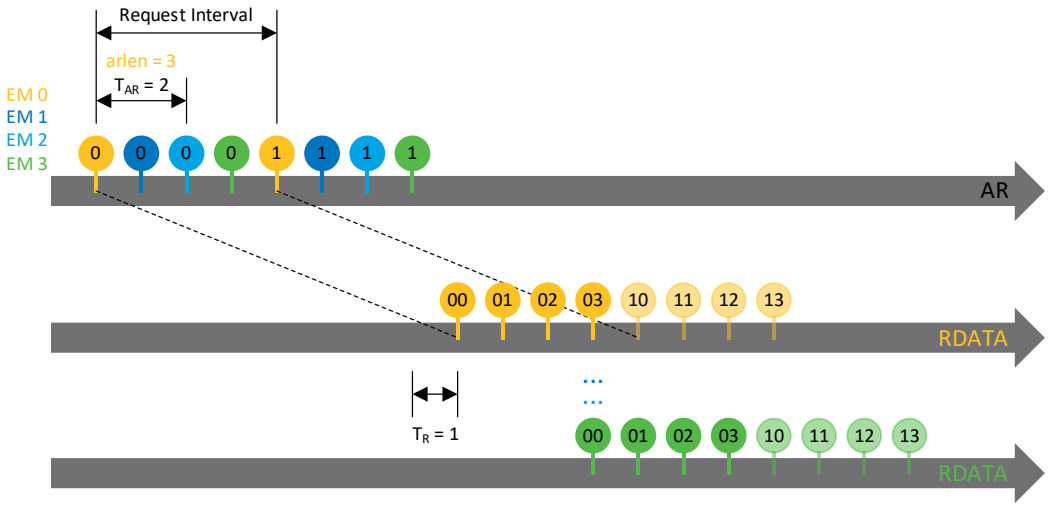


Figure 6.7. Read Transactions for Four Active EMs with arlen ≥ 3

6.2.3. Bottleneck Clearance

The following are design considerations to address various bottlenecks:

- Handling low-performance or slow external subordinate devices
  - To prevent back-pressure from propagating to the shared address processing unit, allocate the optional queue at the external subordinate. This queue acts as a buffer to temporarily store transactions and avoid stalling upstream components.
  - Similarly, allocate the read data channel queue at the external subordinate to handle incoming read data. This queue accumulates read data until the system is ready to route it back to the external manager. This ensures smooth data flow and prevents data delays.
- Handling slow external manager devices
  - Allocate the optional queue at the external manager. This queue accumulates write data until the path to the external subordinate is granted.

6.3. Design Considerations for Latency

6.3.1. Minimum Crossbar Latency

Table 6.1 shows the minimum crossbar latency for the SAMD and SASD crossbar architecture.

Table 6.1. Minimum Crossbar Latency

Channel	Latency (Clock Cycle)
Read Address	2
Write Address	2
Write Data	0
Write Response	1
Read Data	0

6.3.2. EM or ES Interface Latency

Table 6.2 shows additional latencies introduced by the EM or ES interface.

Table 6.2. Additional Latency Introduced by Optional Couplers at EM or ES Interface

Channel	Latency (Clock Cycle)			
	Queue without CDC		Queue with CDC	
	LUT	EBR	LUT	EBR
Address	1	3	7	7
Write Data	1	3	7	7
Write Response	1	3	7	7
Read Data	1	3	7	7

6.3.3. Default AXI4 Use Case without CDC

The following describes the latencies associated with the default AXI4 use case with CDC disabled:

- Address Phase (Read or Write)
  T_{AR} or T_{AW}: Two clock cycles for the forward propagation of awvalid or arvalid from EM port to ES port.
- Write Address Phase to Write Data Phase
  T_{WC}: One additional clock cycle required to push write address phase grant into the targeted write data channels to ensure in-order write. This is required for AXI4 write data.
- Write Data Phase
  T_{W}: One clock cycle without bubble for back-to-back write data.

- Write Response or Read Data Phase
  T_R: One clock cycle without bubble for back-to-back read data. The same latency applies for write response.

Table 6.3 shows the latencies associated with the SAMD crossbar architecture. Figure 6.8 illustrates the related transaction paths.

Table 6.3. Default AXI4 without CDC with SAMD Crossbar Architecture

Channel	Latency (Clock Cycle)				Note
	Crossbar	EM Interface Queue (LUT)	ES Interface Queue (LUT)	Total	
Read Address	2	0	0	2	T_{AR}
Write Address	2	0	0	2	T_{AW}
Write Data	0	1	0	1	T_W
Write Response	1	0	0	1	T_B
Read Data	0	0	1	1	T_R

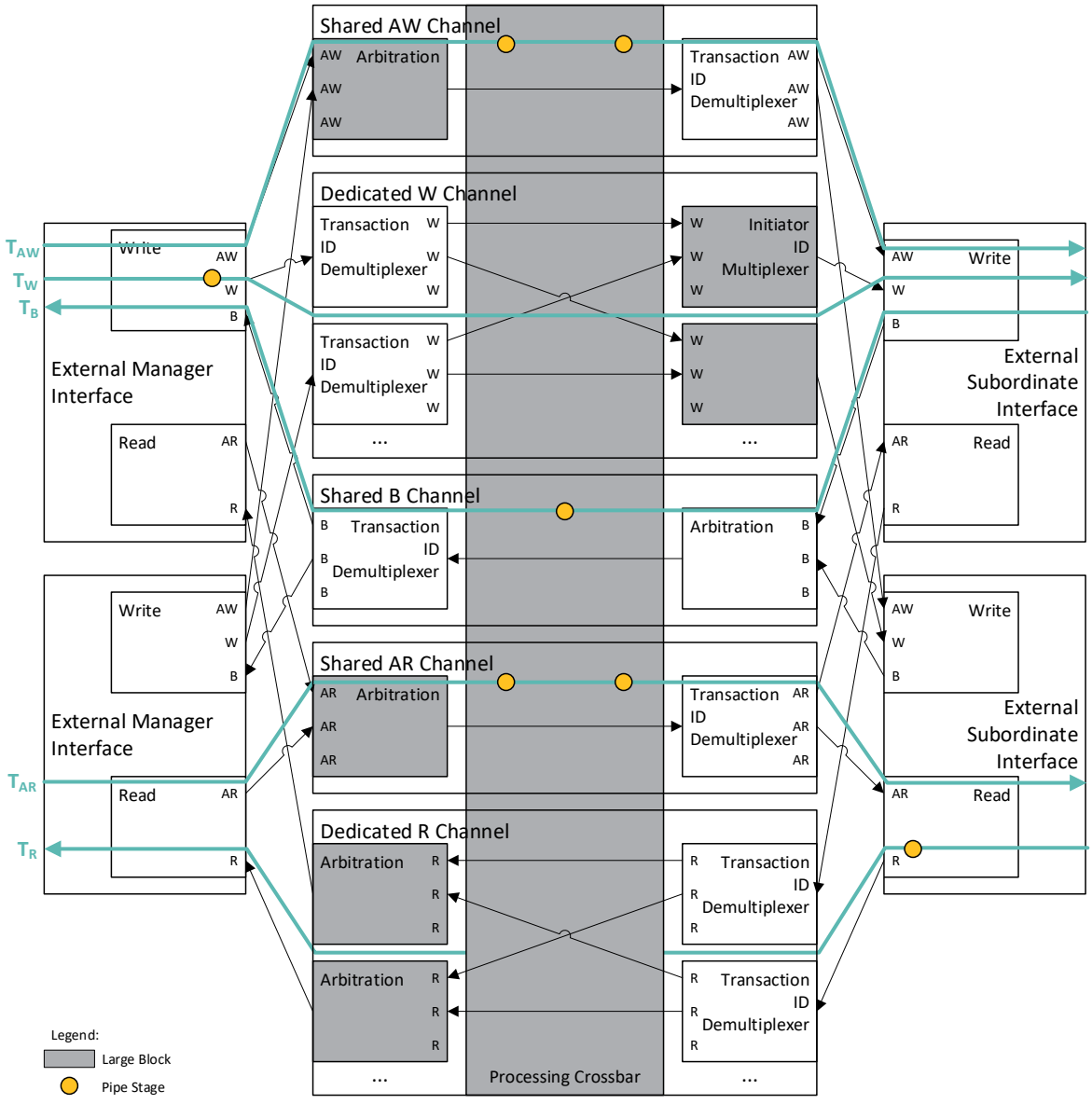


Figure 6.8. Default AXI4 with SAMD Crossbar Architecture Latencies

Table 6.4 shows the latencies associated with the SASD crossbar architecture. Figure 6.9 illustrates the related transaction paths.

Table 6.4. Default AXI4 without CDC with SASD Crossbar Architecture

Channel	Latency (Clock Cycle)				Note
	Crossbar	EM Interface Queue (LUT)	ES Interface Queue (LUT)	Total	
Address (Read/Write)	2	0	0	2	T_{AR} or T_{AW}
Write Data	0	1	0	1	T_W
Response (Write Resp/Read Data)	1	0	0	1	T_B or T_R

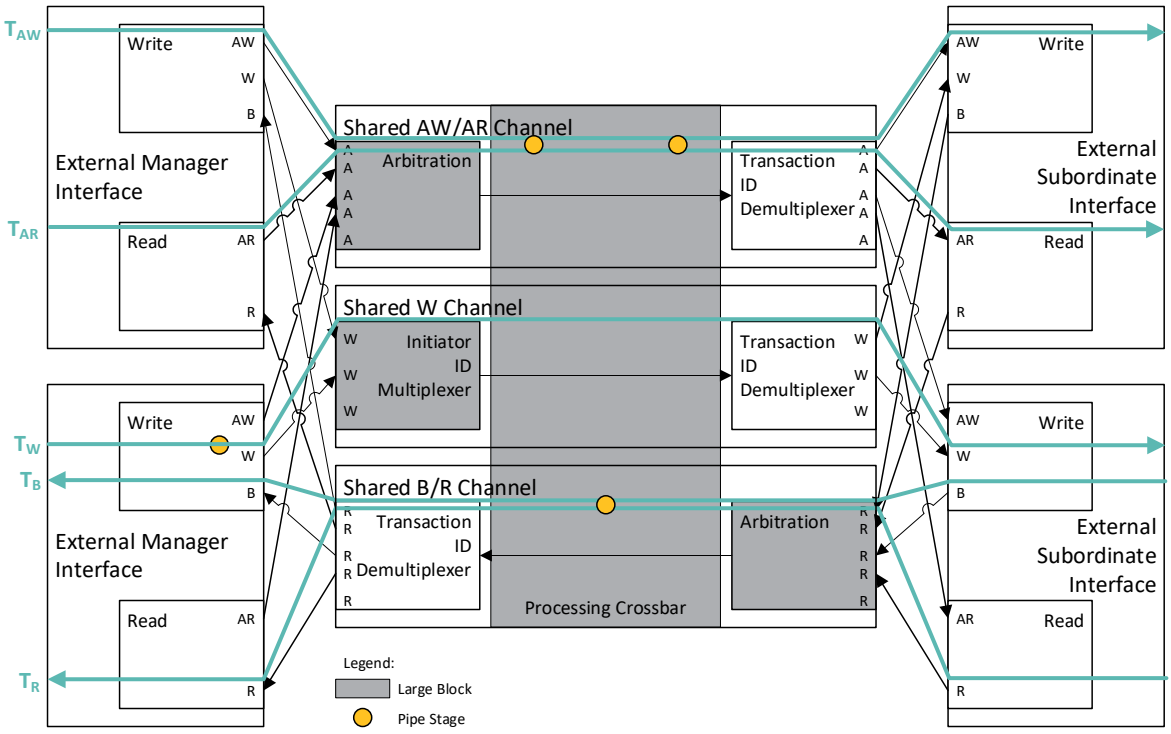


Figure 6.9. Default AXI4 with SASD Crossbar Architecture Latencies

Appendix A. Resource Utilization

Table A.1 through Table A.7 show sample resource utilizations of the Unified Interconnect IP core on CertusPro-NX (LFCPNX-100-8ASG256I) and Avant (LAV-AT-X70-1LFG1156C) devices, where applicable.

Note: The f_{MAX} values shown here are for reference only. f_{MAX} values might differ depending on factors such as the operating system and Radiant software version.

Maximize Performance Mode

For the sample resource utilizations shown in this section, the following IP configuration applies:

- *External Manager protocol N* = AXI4
- *External Subordinate Protocol type M* = AXI4
- *Crossbar Optimization Strategy* = Maximize Performance
- *External Manager Address N width* = 32 bits
- *External Subordinate M Address width* = 32 bits
- *External Manager AXI ID width* = 2 bits
- *External Subordinate M Fragment Cnt* = 1
- *External Manager Priority* = Round Robin
- *External Manager Write Acceptance Limit N* = 4
- *External Manager Read Acceptance Limit N* = 4
- No CDC unless otherwise specified

Table A.1. Resource Utilization for 32-bit Data Width without CDC in Maximize Performance Mode

Device	Total EMs	Total ESs	LUTs	Registers	f_{MAX} (MHz)
CertusPro-NX	1	2	460	616	200.000
	1	3	653	723	200.000
	1	4	778	828	174.459
	2	1	666	638	196.541
	2	2	959	779	190.440
	2	3	1301	908	167.168
	2	4	1561	1038	178.891
	3	1	1036	764	200.000
	3	2	1481	929	184.162
	3	3	1977	1078	180.799
	3	4	2288	1215	170.590
	4	1	1209	886	195.771
	4	2	1796	1070	186.463
	4	3	2283	1243	170.940
	4	4	2708	1409	167.729
Avant	1	2	474	617	250.000
	1	3	640	723	250.000
	1	4	792	826	250.000
	2	1	697	638	250.000
	2	2	981	781	250.000
	2	3	1296	911	250.000
	2	4	1595	1034	250.000
	3	1	1045	764	250.000

Device	Total EMs	Total ESs	LUTs	Registers	f_{MAX} (MHz)
	3	2	1530	936	250.000
	3	3	1934	1080	250.000
	3	4	2318	1223	250.000
	4	1	1240	885	250.000
	4	2	1885	1070	244.738
	4	3	2319	1247	237.135
	4	4	2795	1419	233.863

Table A.2. Resource Utilization for 64-bit Data Width without CDC in Maximize Performance Mode

Device	Total EMs	Total ESs	LUTs	Registers	f_{MAX} (MHz)
CertusPro-NX	1	2	606	816	200.000
	1	3	811	987	172.712
	1	4	1006	1154	175.039
	2	1	794	846	196.657
	2	2	1250	1051	177.462
	2	3	1791	1244	153.516
	2	4	2046	1433	168.663
	3	1	1264	1044	185.943
	3	2	1922	1273	174.216
	3	3	2514	1493	166.417
	3	4	2979	1691	164.636
	4	1	1460	1235	187.512
	4	2	2292	1486	173.040
	4	3	3005	1732	166.176
	4	4	3513	1950	163.773
Avant	1	2	618	816	250.000
	1	3	809	987	250.000
	1	4	1088	1154	250.000
	2	1	813	846	250.000
	2	2	1236	1060	250.000
	2	3	1709	1249	250.000
	2	4	2039	1434	249.128
	3	1	1250	1044	250.000
	3	2	1919	1275	250.000
	3	3	2577	1489	250.000
	3	4	3046	1709	231.054
	4	1	1469	1237	250.000
	4	2	2307	1494	250.000
	4	3	3078	1726	250.000
	4	4	3571	1956	245.218

Table A.3. Resource Utilization for 128-bit Data Width without CDC in Maximize Performance Mode

Device	Total EMs	Total ESs	LUTs	Registers	f_{MAX} (MHz)
CertusPro-NX	1	2	844	1216	162.575
	1	3	1250	1515	144.907
	1	4	1469	1810	133.761
	2	1	1082	1262	177.022
	2	2	1824	1595	165.893
	2	3	2506	1916	170.823
	2	4	3007	2229	158.755
	3	1	1690	1604	154.512
	3	2	2767	1961	147.471
	3	3	3775	2309	144.009
	3	4	4467	2646	141.123
	4	1	1944	1939	161.970
	4	2	3234	2318	155.618
	4	3	4472	2677	147.080
	4	4	5173	3037	125.392
Avant	1	2	854	1216	250.000
	1	3	1196	1515	250.000
	1	4	1477	1810	250.000
	2	1	1124	1263	250.000
	2	2	1788	1602	250.000
	2	3	2500	1920	246.914
	2	4	2939	2231	236.518
	3	1	1664	1606	250.000
	3	2	2767	1961	250.000
	3	3	3819	2311	223.614
	3	4	4455	2642	236.183
	4	1	1967	1941	250.000
	4	2	3308	2318	248.633
	4	3	4472	2689	225.124
	4	4	5194	3037	239.063

Table A.4. Resource Utilization for 32-bit Data Width with CDC in Maximize Performance Mode

Device	Total EMs	Total ESs	LUTs	Registers	f_{MAX} (MHz)
CertusPro-NX	4	4	6664	5807	134.048
Avant	4	4	6648	5808	202.758

Note: CDC is enabled for all external managers and external subordinates.

Minimize Area Mode

For the sample resource utilizations shown in this section, the following IP configuration applies:

- *External Manager protocol N* = AXI4-Lite
- *External Subordinate Protocol type M* = AXI4-Lite
- *Crossbar Optimization Strategy* = Minimize Area (Single Access Mode)
- *External Manager N Address width* = 32 bits
- *External Subordinate M Address width* = 32 bits
- *External Subordinate M Fragment Cnt* = 1
- *External Manager Priority* = Round Robin
- No CDC unless otherwise specified

Table A.5. Resource Utilization for 32-bit Data Width without CDC in Minimize Area Mode

Device	Total EMs	Total ESs	LUTs	Registers	f_{MAX} (MHz)
CertusPro-NX	1	2	316	269	192.345
	1	3	375	290	193.611
	1	4	452	305	197.824
	2	1	375	338	192.345
	2	2	476	357	182.017
	2	3	543	382	188.253
	2	4	625	401	200.000
	3	1	592	426	200.000
	3	2	670	445	178.317
	3	3	775	473	168.890
	3	4	853	489	175.747
	4	1	703	511	186.986
	4	2	794	530	189.322
	4	3	884	556	177.999
	4	4	925	579	163.747
Avant	1	2	330	269	250.000
	1	3	414	290	250.000
	1	4	512	305	250.000
	2	1	399	338	250.000
	2	2	499	357	250.000
	2	3	585	378	250.000
	2	4	645	393	250.000
	3	1	592	426	250.000
	3	2	697	451	250.000
	3	3	806	472	250.000
	3	4	846	485	250.000
	4	1	712	511	250.000
	4	2	817	530	250.000
	4	3	913	556	250.000
	4	4	986	577	250.000

Table A.6. Resource Utilization for 64-bit Data Width without CDC in Minimize Area Mode

Device	Total EMs	Total ESs	LUTs	Registers	f_{MAX} (MHz)
CertusPro-NX	1	2	387	373	200.000
	1	3	477	394	178.158
	1	4	544	409	200.000
	2	1	497	514	187.688
	2	2	614	533	188.466
	2	3	725	558	176.772
	2	4	772	577	187.617
	3	1	759	674	200.000
	3	2	897	693	152.648
	3	3	1006	714	174.611
	3	4	1070	738	190.223
	4	1	914	831	183.621
	4	2	1038	850	176.772
	4	3	1170	879	187.056
	4	4	1202	892	155.909
Avant	1	2	396	373	250.000
	1	3	518	394	250.000
	1	4	559	409	250.000
	2	1	511	514	250.000
	2	2	634	533	250.000
	2	3	753	554	250.000
	2	4	800	573	250.000
	3	1	775	674	250.000
	3	2	911	693	250.000
	3	3	1036	714	250.000
	3	4	1094	731	250.000
	4	1	909	831	250.000
	4	2	1043	850	250.000
	4	3	1175	874	250.000
	4	4	1240	889	250.000

Table A.7. Resource Utilization for 32-bit Data Width with CDC in Minimize Area Mode

Device	Total EMs	Total ESs	LUTs	Registers	f_{MAX} (MHz)
CertusPro-NX	4	4	4285	4243	145.328
Avant	4	4	4378	4243	244.499

Note: CDC is enabled for all external managers and external subordinates.

References

- Unified Interconnect IP Release Notes (FPGA-RN-02107)
- Lattice Radiant Timing Constraints Methodology (FPGA-AN-02059)
- AMBA AXI Protocol Specification web page
- Avant-E web page
- Avant-G web page
- Avant-X web page
- Certus-N2 web page
- Certus-NX web page
- CertusPro-NX web page
- CrossLink-NX web page
- MachXO5-NX web page
- Lattice Radiant Software web page
- Lattice Propel Design Environment web page
- Lattice Solutions IP Cores web page
- Lattice Solutions Reference Designs web page
- Lattice Insights for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Note: In some instances, the IP may be updated without changes to the user guide. The user guide may reflect an earlier IP version but remains fully compatible with the later IP version. Refer to the IP Release Notes for the latest updates.

Revision 1.0, IP v1.0.0, December 2025

Section	Change Summary
All	Initial release.

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