Lattice Propel 2025.2 Builder

User Guide

FPGA-UG-02243-1.0

December 2025

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Inclusive Language

This document was created consistent with Lattice Semiconductor’s inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice’s inclusive language FAQ 6878 for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

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Abbreviations in This Document

A list of abbreviations used in this document.

Glossary	Definition
BSP	Board Support Package, the layer of software containing hardware-specific drivers and libraries to function in a particular hardware environment.
CPU	Central Processing Unit
CSV	Comma Separated Values file
DGE	Design Generator Engine
DRC	Design Rule Check
DUT	Design Under Test
ESI	Previous name of Propel
FPGA	Field Programmable Gate Array
GUI	Graphic User Interface
HDL	Hardware Description Language
HSM	Hardware Security Module
IDE	Integrated Development Environment
IP-XACT	An XML format that defines and describes electronic components and their designs.
IPX	Internet Packet Exchange
LHS	Left Hand Side
LSB	Least Significant Bit
MSB	Most Significant Bit
OS	Operating System
Perspective	A group of views and editors in the Workbench window.
PGE	Package Generate Engine
Programmer	A tool can program Lattice FPGA SRAM and external SPI Flash through various interfaces, such as JTAG, SPI, and I^2C.
RHS	Right Hand Side.
RISC-V	A free and open instruction set architecture (ISA) enabling a new era of processor innovation through open standard collaboration.
SBX	The files that store the spatial index of the features
SDK	Embedded System Design and Develop Kit. A set of software development tools that allows the creation of applications for software package on the Lattice embedded platform.
SGE	Software Generator Engine
SoC	System on Chip. An integrated circuit that integrates all components of a computer or other electronic systems.
SRAM	Static Random Access Memory
TCL	Tool Command Language
UFM	User Flash Memory
VIP	Verification IP
Workspace	The directory where stores your work, which is used as the default content area for your projects as well as for holding any required metadata.
Workbench	The desktop development environment in Eclipse IDE platform.

1. Introduction

Lattice Propel™ 2025.2 Builder is a graphical tool used to assemble complex System-on-Chip (SoC) modules which can be used in the supported Lattice FPGA devices. These modules and/or IP can be assembled and connected easily by simply dragging and dropping the modules and/or IP into the Schematic Window.

1.1. Purpose

Embedded system solutions play an important role in FPGA system design allowing you to develop the software for a processor in an FPGA device. It provides flexibility for you to control various peripherals from a system bus.

To develop an embedded system on an FPGA, you need to design the System on Chip (SoC) with an embedded processor. Lattice Propel Builder helps you develop your system with a RISC-V processor, peripheral IP, and a set of tools by a simple drag-and-drop.

The purpose of this document is to introduce Lattice Propel 2025.2 Builder tool and design flow to help you quickly get started to build a small demo system. You can also find the recommended flows of using Lattice Propel Builder in this document.

1.2. Audience

The intended audience for this document includes embedded system designs and embedded software developers using Lattice FPGA devices. For a complete list of supported devices, refer to the Lattice Propel 2025.2 Release Notes (FPGA-AN-02104). The technical guidelines assume readers have expertise in the embedded system area and FPGA technologies.

2. Lattice Propel Builder Design

The Propel Builder design includes creating a SoC project design, and a verification design. The workflow is described below, and the details are explained in the following sections.

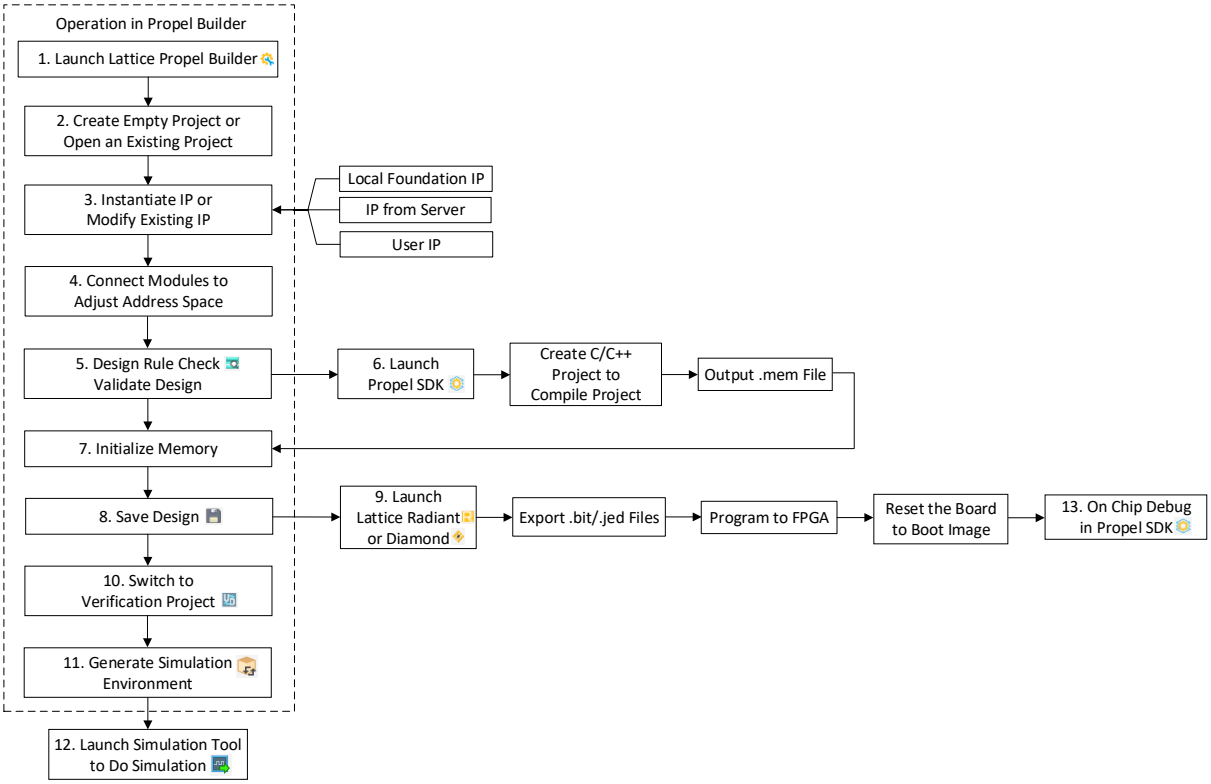


Figure 2.1. Propel Builder Workflow

2.1. Builder Environment

After Propel 2025.2 is installed, you can launch the stand-alone Propel Builder by double-clicking the **Run Propel Builder** icon ( ) from the toolbar.

You can also invoke the Propel Builder from the command line

- GUI mode:
  ```
  Windows: <propel_install_directory>\builder\rtf\bin\nt64\propelbld.exe <tcl_path_file>
  Linux:< propel_installation_directory>/builder/rtf/bin/lin64/propelbld
  ```
- Console mode:
  ```
  Windows: <propel_installation_directory>\builder\rtf\bin\nt64\propelbldc <tcl_path_file>
  Linux: <propel_installation_directory>/builder/rtf/bin/lin64/propelbldc
  ```

tcl_path_file is optional in both scenarios.

Refer to the Lattice Propel 2025.2 Installation for Windows User Guide (FPGA-AN-02106) and Lattice Propel 2025.2 Installation for Linux User Guide (FPGA-AN-02105) for details on the installation.

Notes:

- When you create a Propel SoC project, a linked verification project is always generated as well. Refer to the section for more information on verification project.

- It is recommended to use the same version of Radiant and Propel for best compatibility. To check Radiant installation version, choose **Tools** > **Options** > **Directories** from Propel Builder menu bar to see if the version of Radiant is set. If no Radiant is set, Propel Builder uses the latest Radiant it detects. Refer to the Tools section for more details. To check Propel installation version, choose **Help** > **About Lattice Propel Builder**.

After the Propel Builder is launched, a single workbench window is displayed. The workbench contains Menu, Toolbar, Design View, IP catalog, Schematic view, address mapping, Start Page, and TCL console. Figure 2.2 shows the workbench after opening a project.

1. Menu bar
2. Toolbar
3. IP Catalog and Design View
4. Schematic View, Address Mapping, and Start Page
5. TCL Console

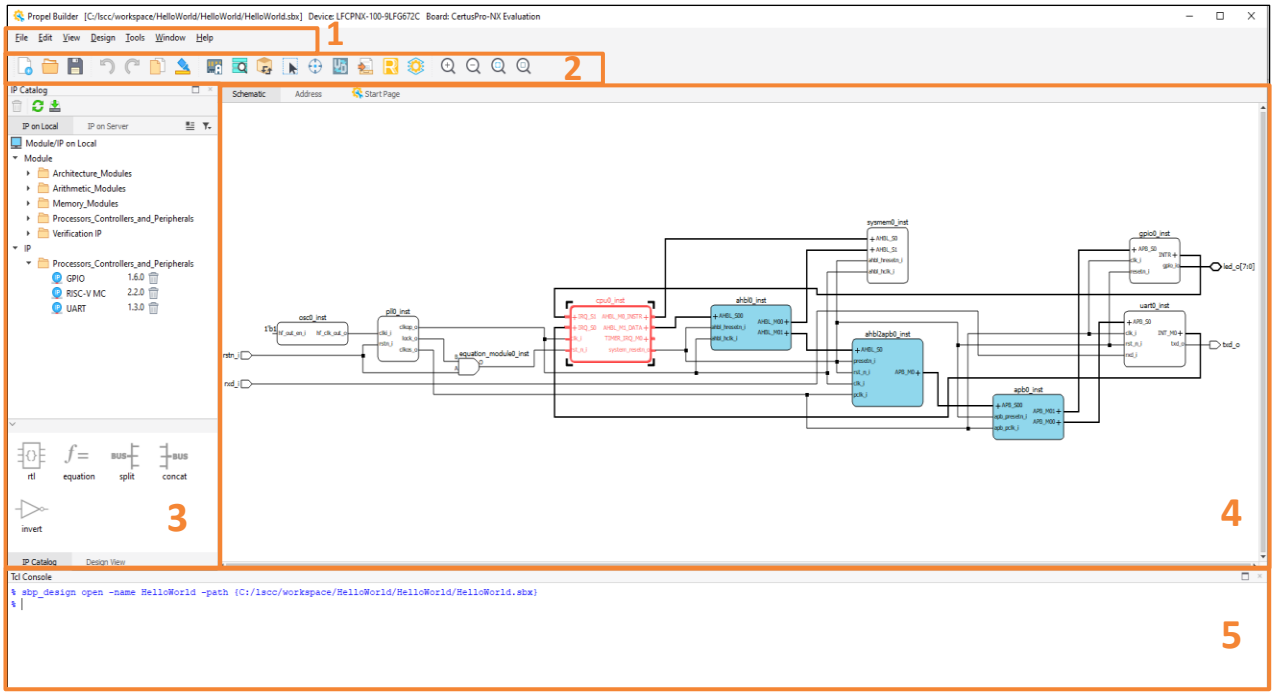


Figure 2.2. Propel Builder Workbench Window

2.2. Check Out What's New

When you install a new Propel Builder, and launch it for the first time, a dialog pops up demonstrating all the new features in GIF, which enables you to have a quick glance at the new features in the current Propel Builder release (see Figure 2.3). Release Notes can be accessed from this dialog as well.

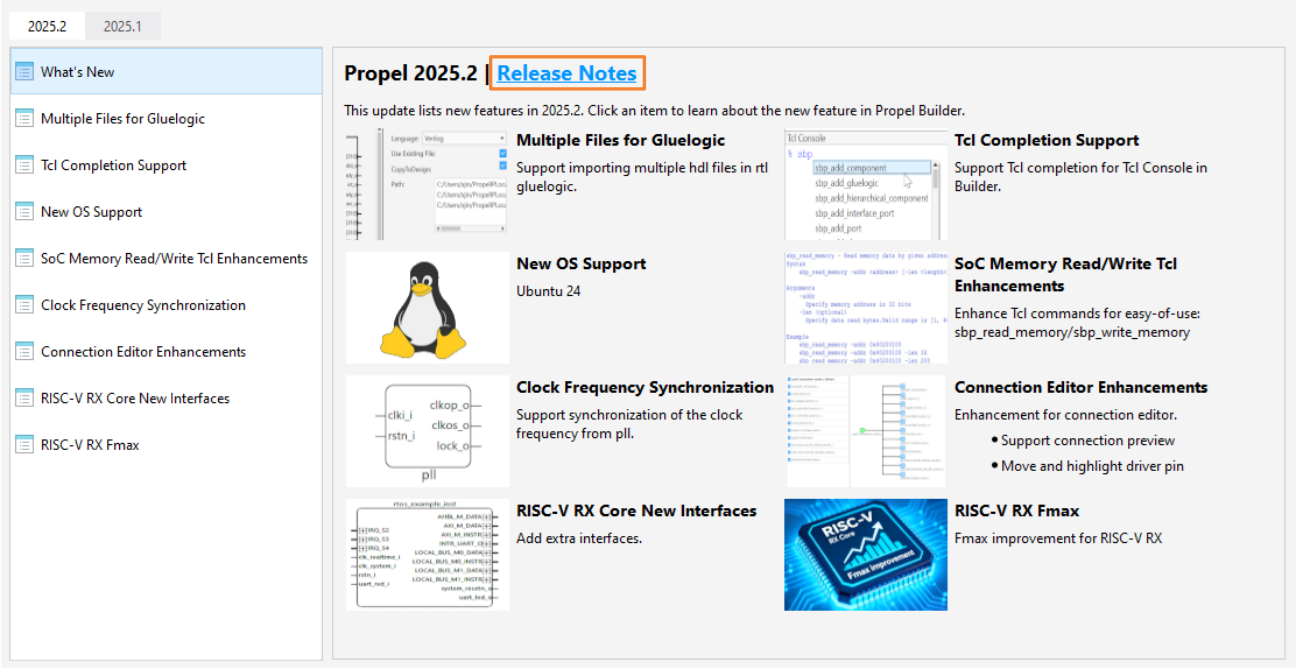


Figure 2.3. What's New in the Welcome Page

You can also check out the new feature information by clicking **What's New** in Propel Builder (Figure 2.4).

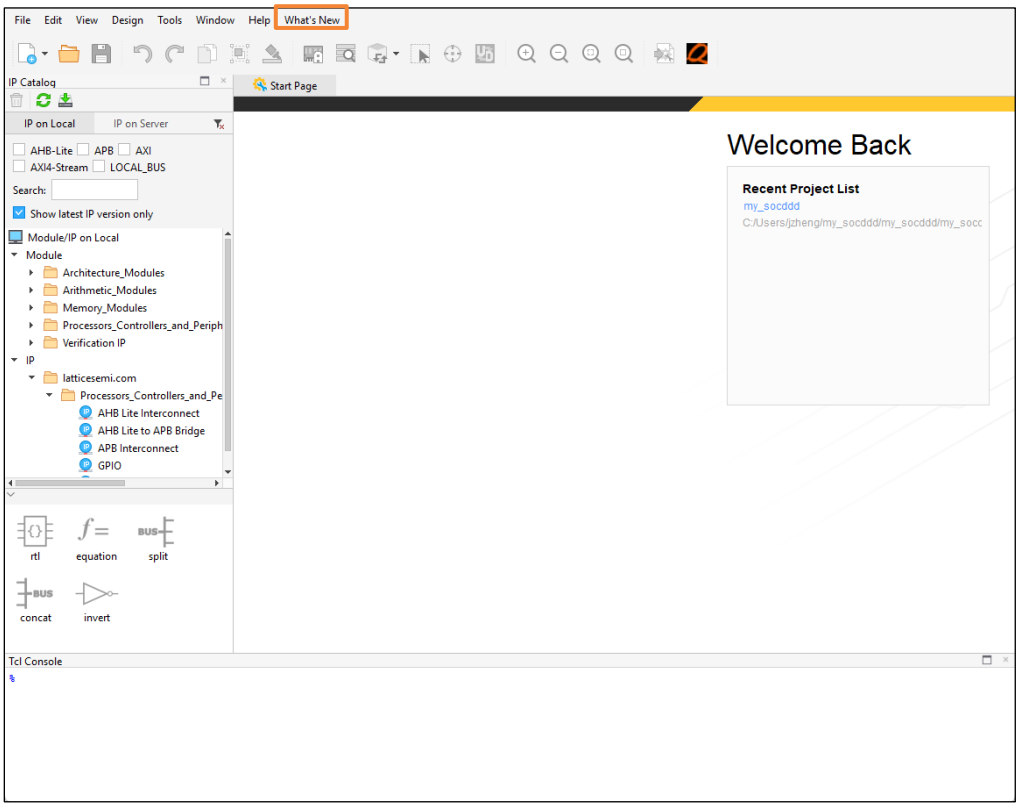


Figure 2.4. What's New in Help Menu

2.3. Project Design Flow

2.3.1. Creating SoC Project

2.3.1.1. New SoC Design Entry

Choose **File** > **New SoC Design** from the Lattice Propel Builder Menu bar (Figure 2.5), the Create System Design wizard opens (Figure 2.6). If you want to use an empty project, a scalable RISC-V SoC design, a pre-defined SoC template, or a user custom template, you can use this entry.

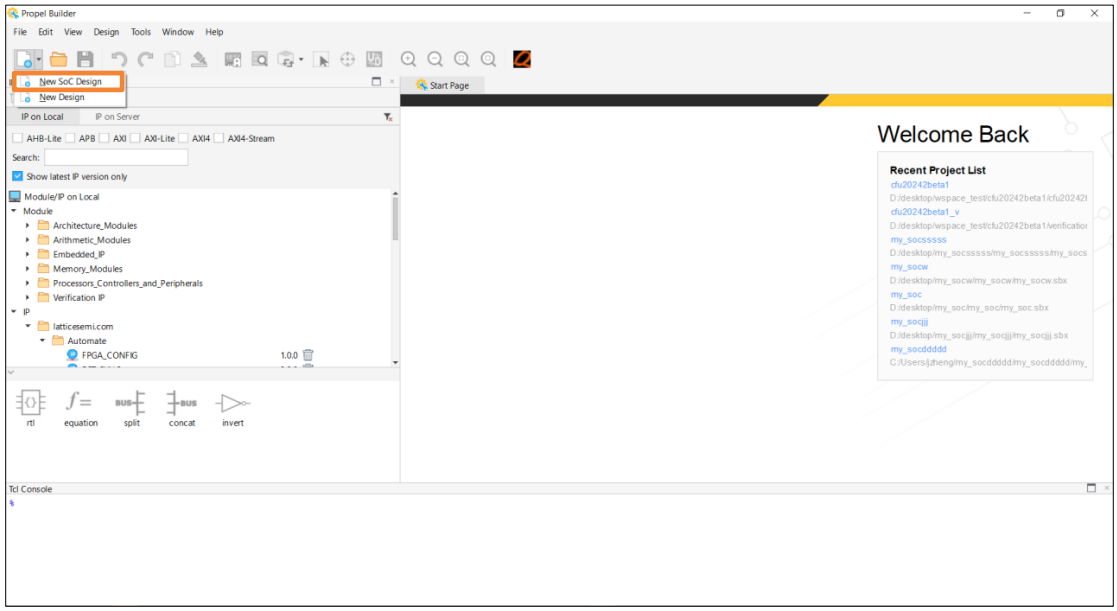


Figure 2.5. New SoC Project

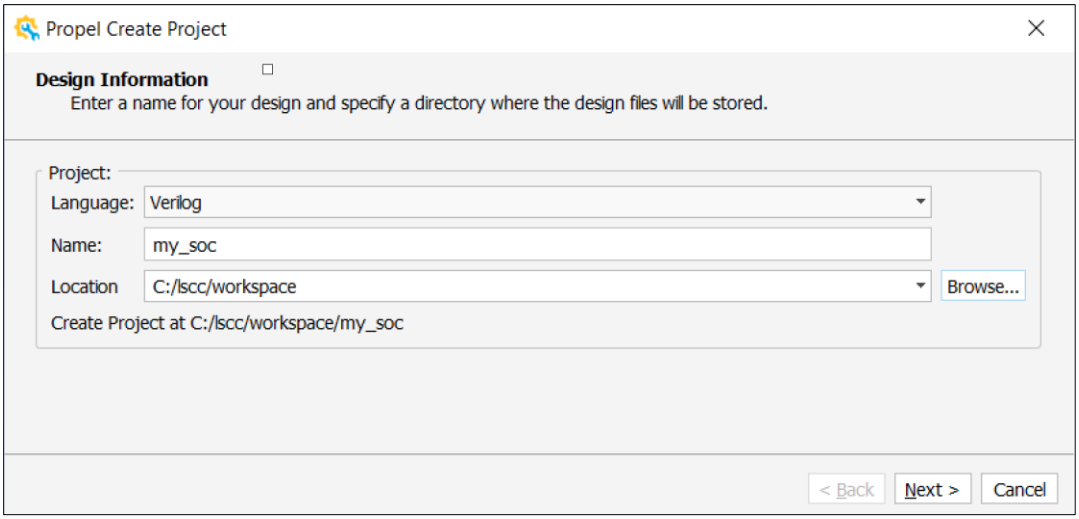


Figure 2.6. Create System Design – Design Information Wizard

1. The default Project Language is displayed in the **Language** field.
2. Enter a project name in the **Name** field, such as my_soc.
3. (Optional) The default location is shown in the **Location** field. Use the **Browse…** option to change the project workspace location.

Note: Long path is not well supported in Windows OS. If a file exists under the path but you get a prompt of No such file, try moving this file to a directory with a shorter path.

4. Click **Next**. You can get detailed information on Template in this flow (Figure 2.7).

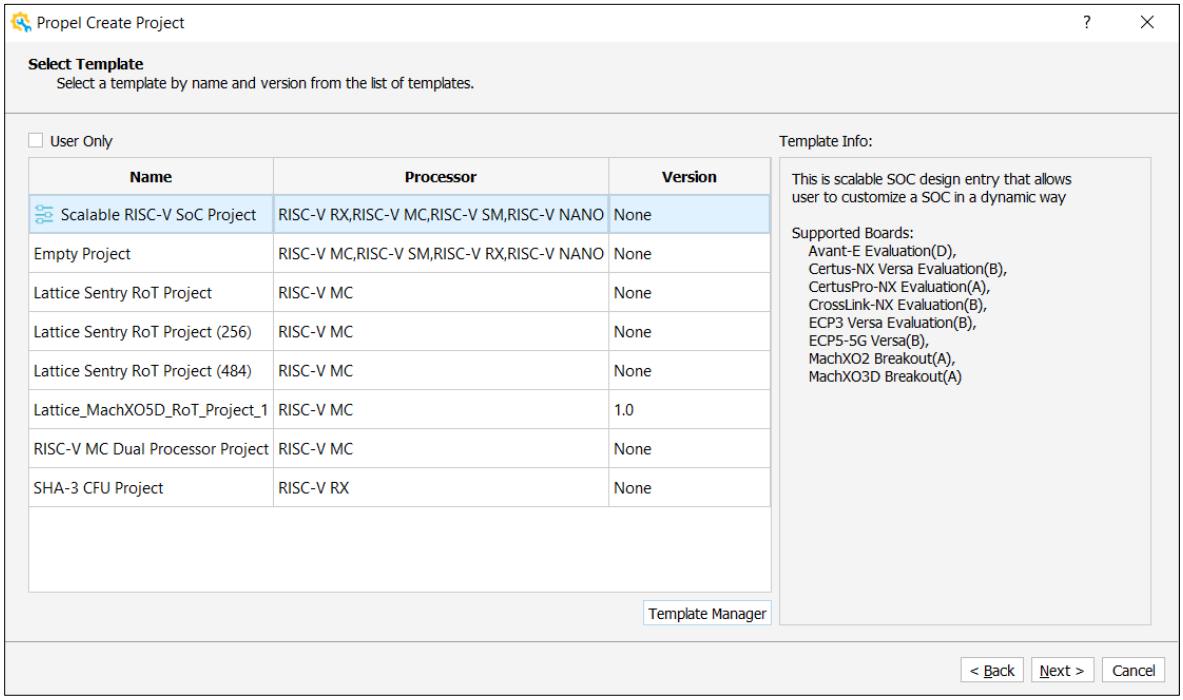


Figure 2.7. New SoC Project – Select Template

Notes:

- The Hello World SoC project for all RISC-V cores are in **Scalable RISC-V SoC Project**.
- You can see both empty project and some predefined templates listed in **Templates** field.
- Templates usually have been validated on board and some of them may have certain constraints. Check Lattice Propel 2025.2 Release Notes (FPGA-AN-02104) for more information on constraints.

5. (Optional) Click **User Only** to see user custom template (Figure 2.8). Refer to the Define Custom Template section for how to use **Template Manager**.

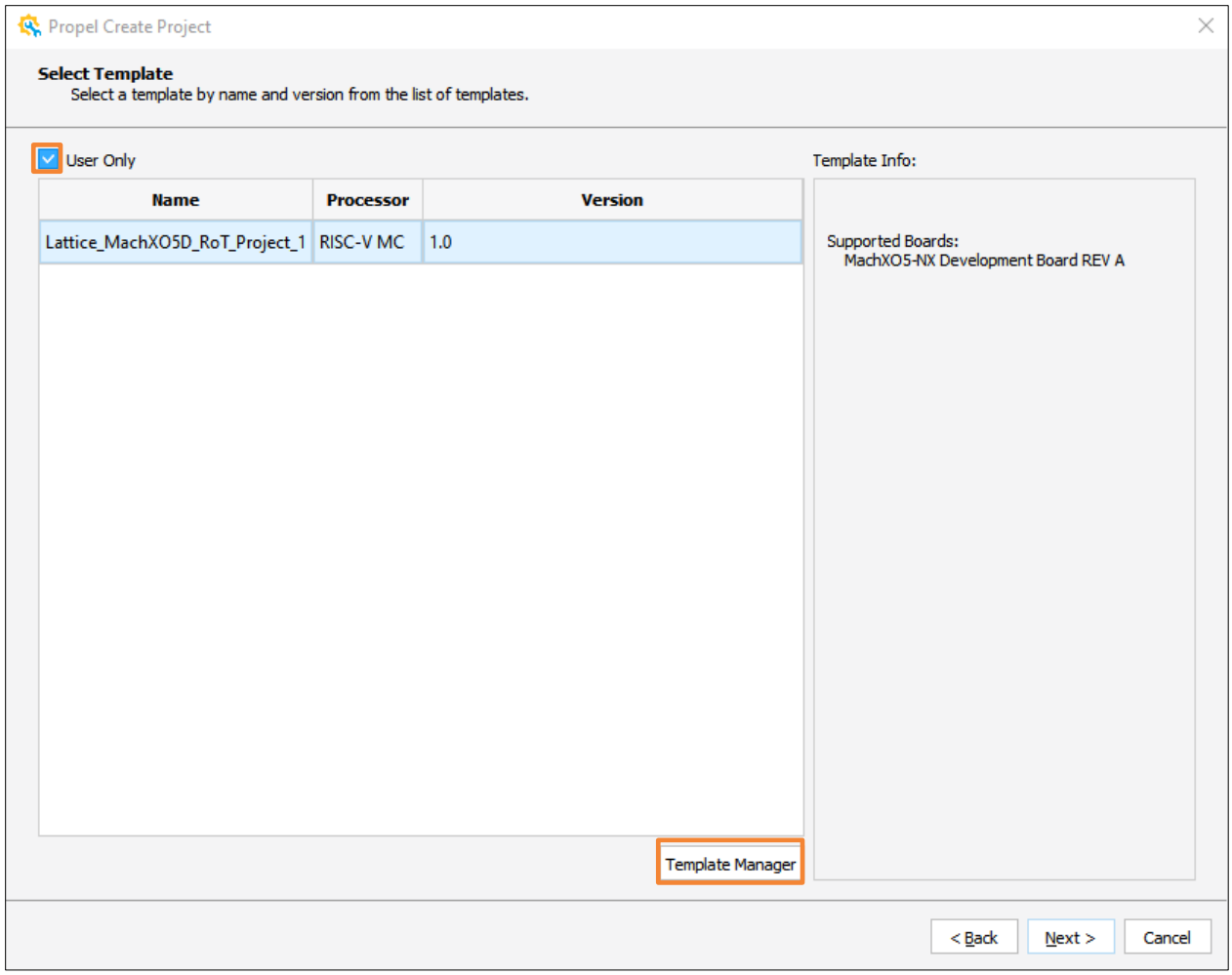


Figure 2.8. New SoC Project – Select Custom Template

6. You can choose **Device/Board** from the following view (Figure 2.9):

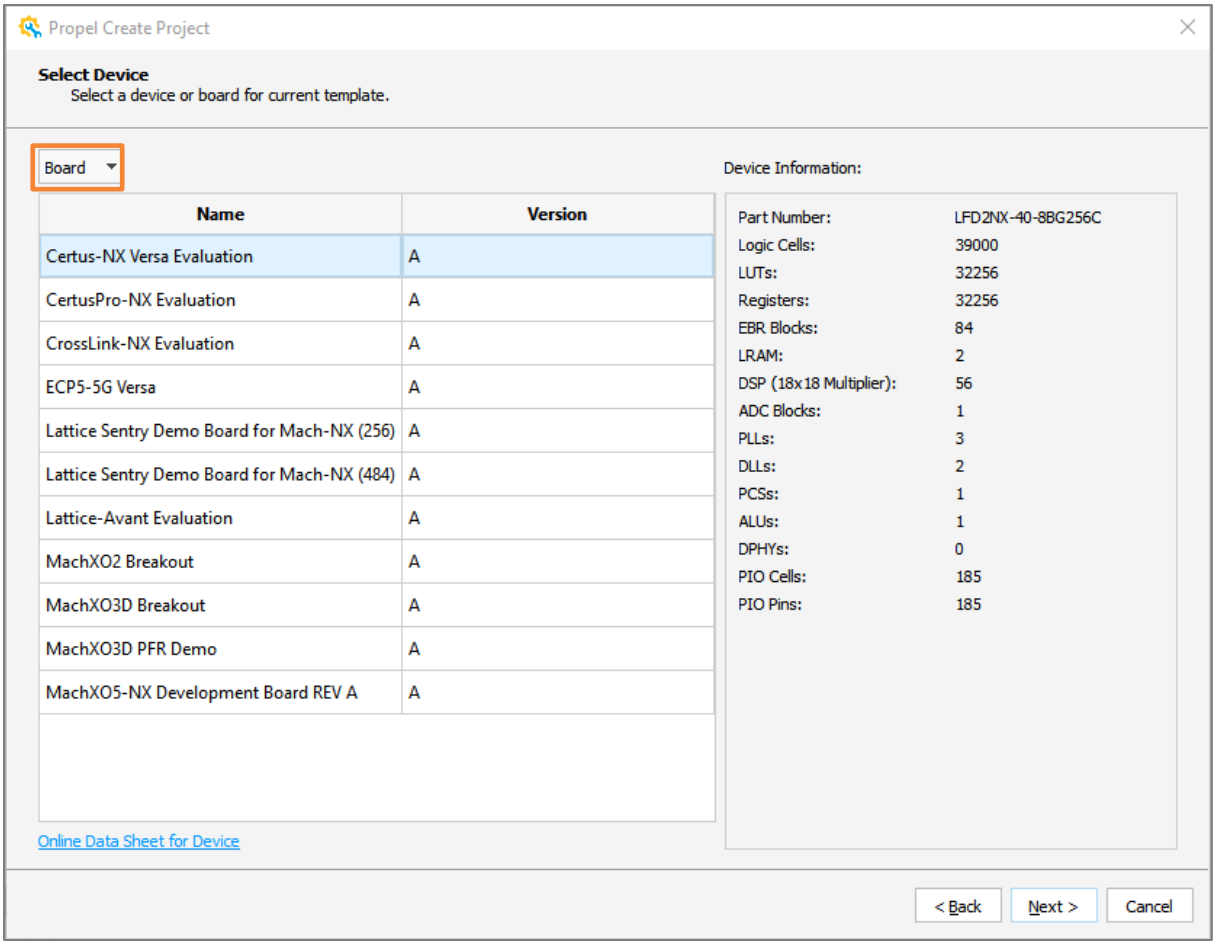


Figure 2.9. New SoC Project – Select Device

7. Click **Next**. The Project Information wizard opens. Check and confirm the project information (Figure 2.10).

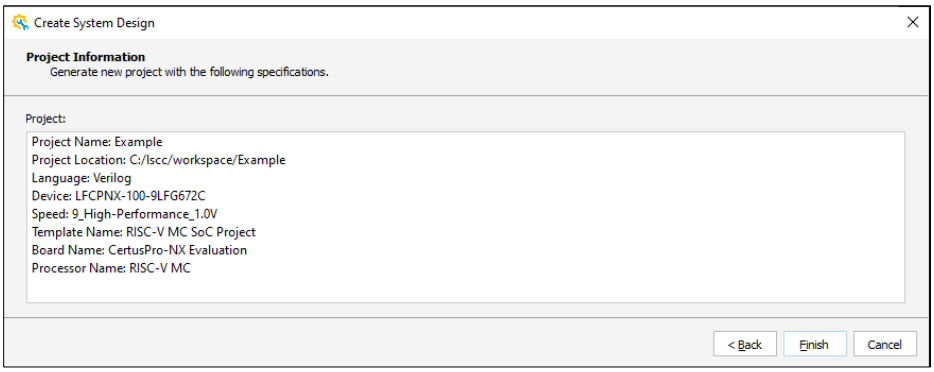


Figure 2.10. Project Information Wizard

8. Click **Finish**. The Propel Builder GUI opens (Figure 2.11).

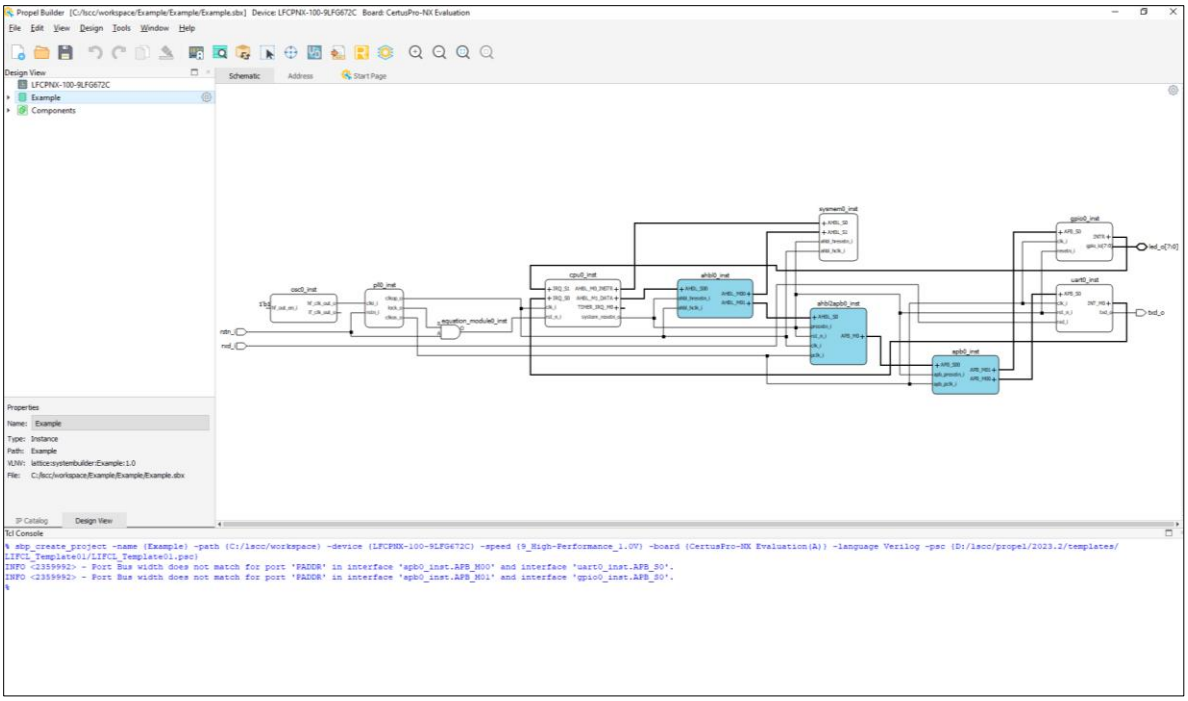


Figure 2.11. Propel Builder GUI showing Template SoC Project

9. Below is the basic information about this project. Click **Summary** (Figure 2.12). You can see the general information and IP summary information of the SoC project.

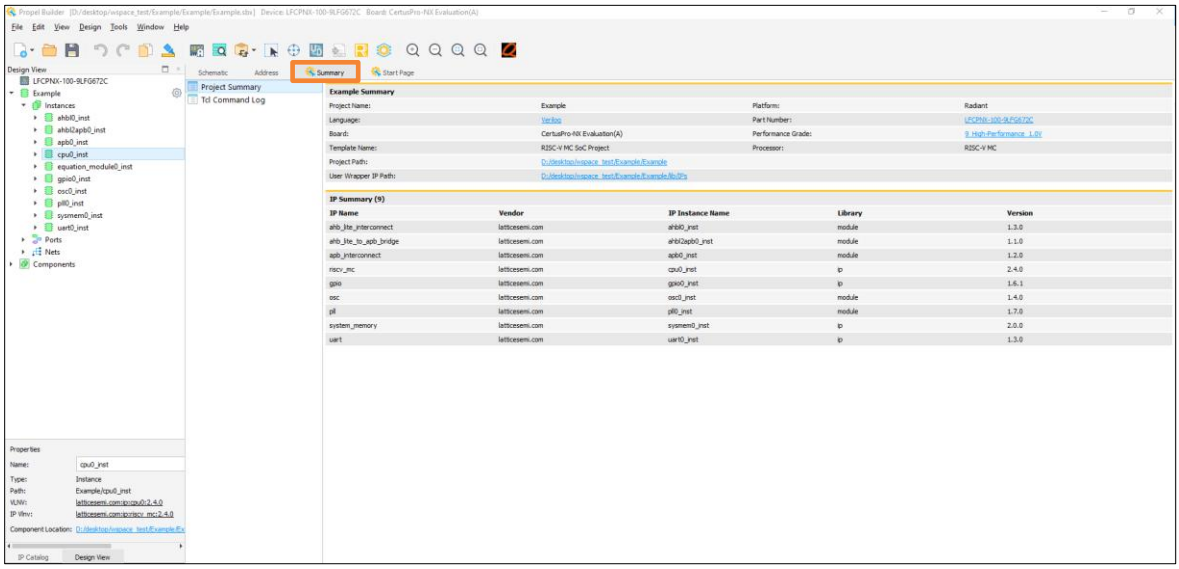


Figure 2.12. Propel Builder GUI showing SoC Project Summary

10. Click the **Language** link in **Summary** (Figure 2.13) to change the project setting for language.

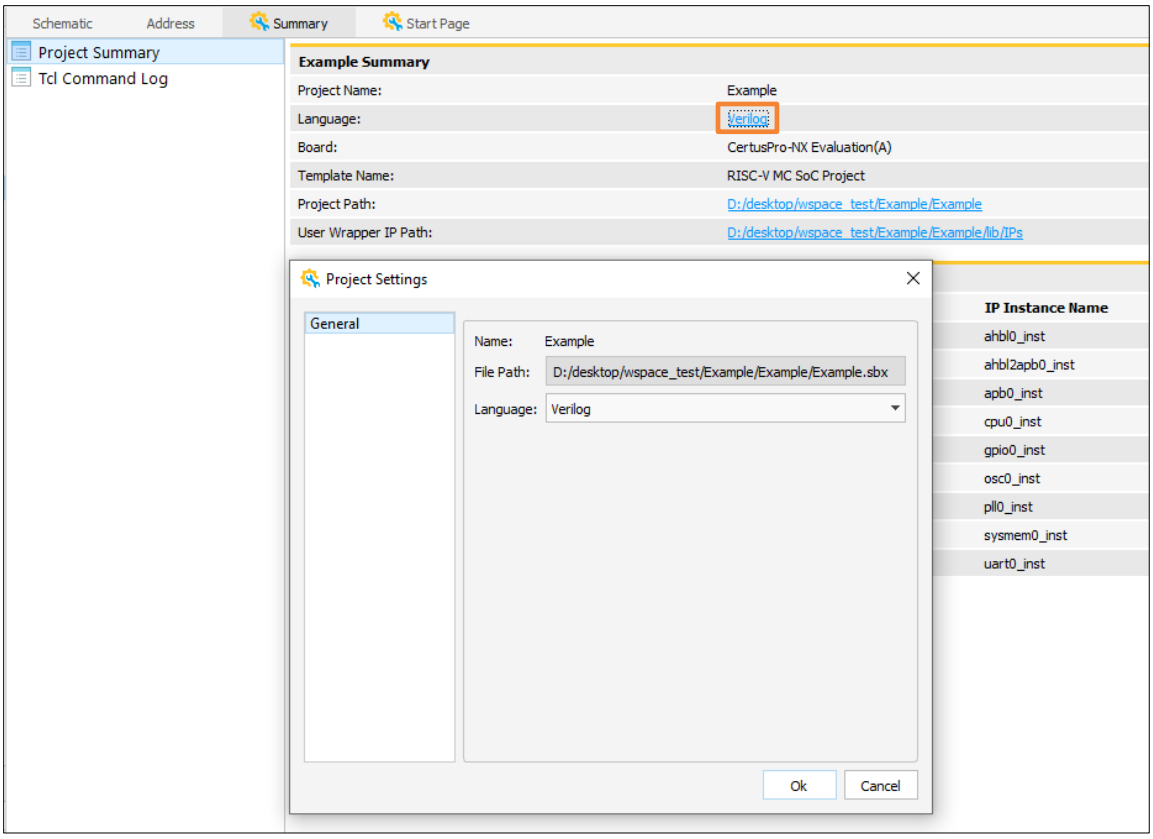


Figure 2.13. SoC Project Summary – Language

11. Click **Part Number** or **Performance Grade** link in **Summary** (Figure 2.14) to modify the device info.

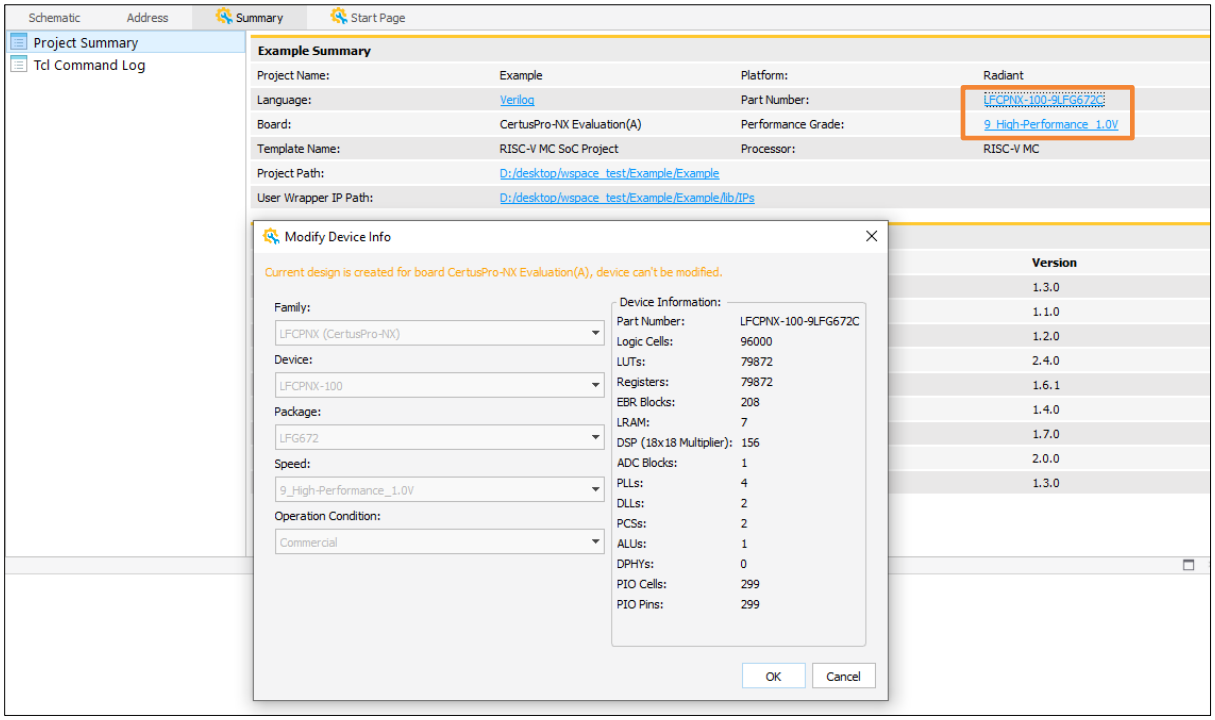


Figure 2.14. SoC Project Summary – Part Number or Performance Grade

12. Click **Project Path** or **User Wrapper IP Path link** in **Summary** (Figure 2.15) to open the project folder or open the user wrapper IP folder in library.

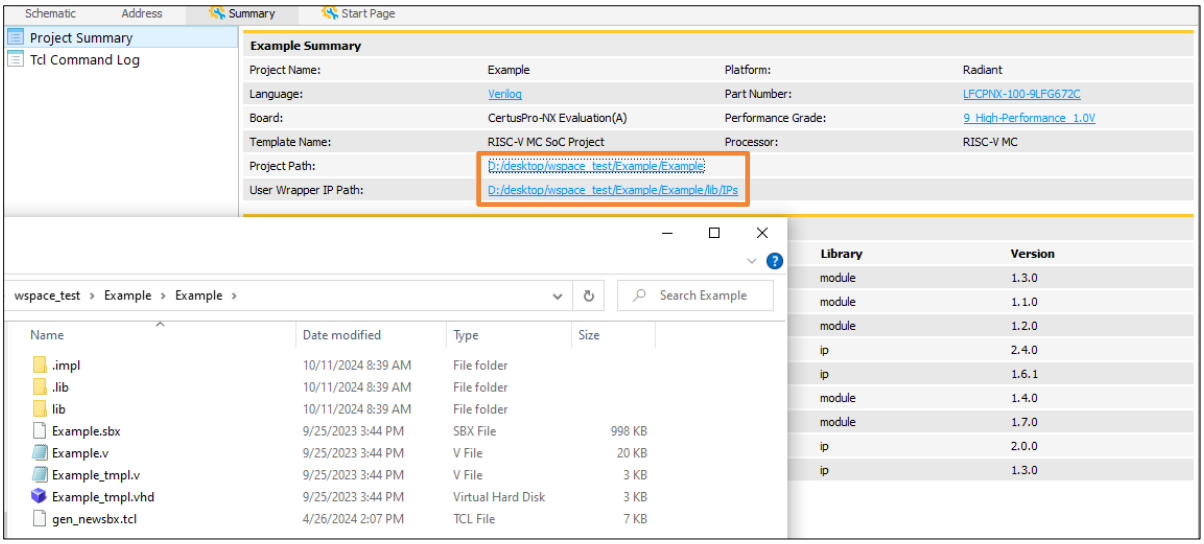


Figure 2.15. SoC Project Summary – Project Path or User Wrapper IP Path

13. Click **Tcl Command Log** in **Summary** (Figure 2.16) to see all history Tcl command of this SoC project.

    The Tcl Command Log page records all tcl commands that you have executed successfully, and logs are divided by date, such as 240917095148: year_month_day_hour_min_sec. You can also click on the right combo box to check specific log on some date.

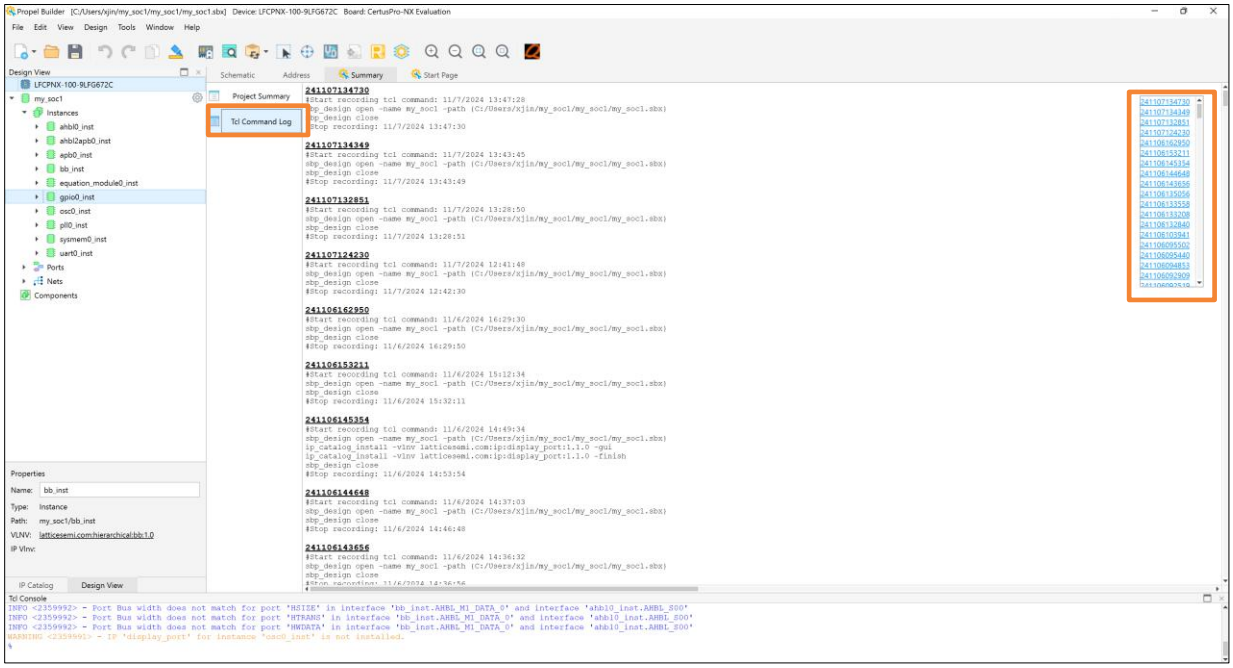


Figure 2.16. SoC Project Summary – Tcl Command Log

2.3.1.2. Scalable RISC-V SoC Design Flow

Lattice Propel Builder provides a Scalable RISC-V SoC Design Flow to enable high-level customized SoC creation.

All templates based on this workflow are application-oriented and contain following parts:

- Non-Configurable infrastructure (must-have components): User CPU, system memory/TCM and some other components to build a minimum functioning SoC project.
- User-Configurable peripheral : What peripherals are needed and their quantity.

Instead of starting from a fixed SoC template, Scalable Design encourages you to choose from a certain application level, such as RTOS, Bare Metal, and then choose the target board/device, and finally choose the kind and the amount of peripherals , such as UART, GPIO, I2C, SPI.

After user inputs, there is a layout preview for you to confirm before generating SoC on fly.

The functional diagram is shown below (Figure 2.17). Detailed steps are shown below.

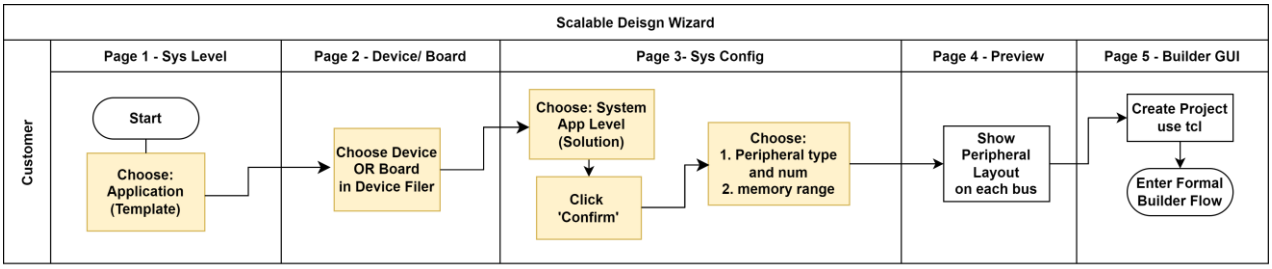


Figure 2.17 Scalable Design Functional Diagram

1. In the Propel Builder GUI, choose **New SoC Design** (Figure 2.18) to open the **Propel Create Project** page. Choose **Scalable RISC-V SoC project**. Click **Next** (Figure 2.19).

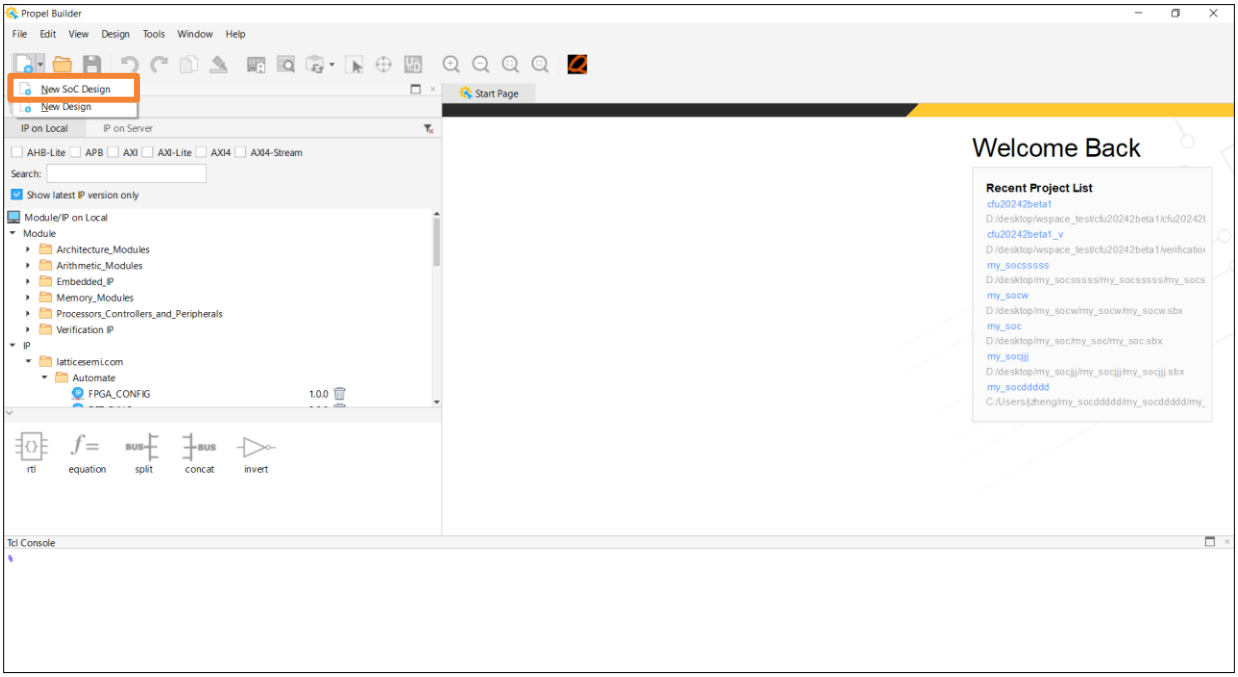


Figure 2.18. New Soc Design

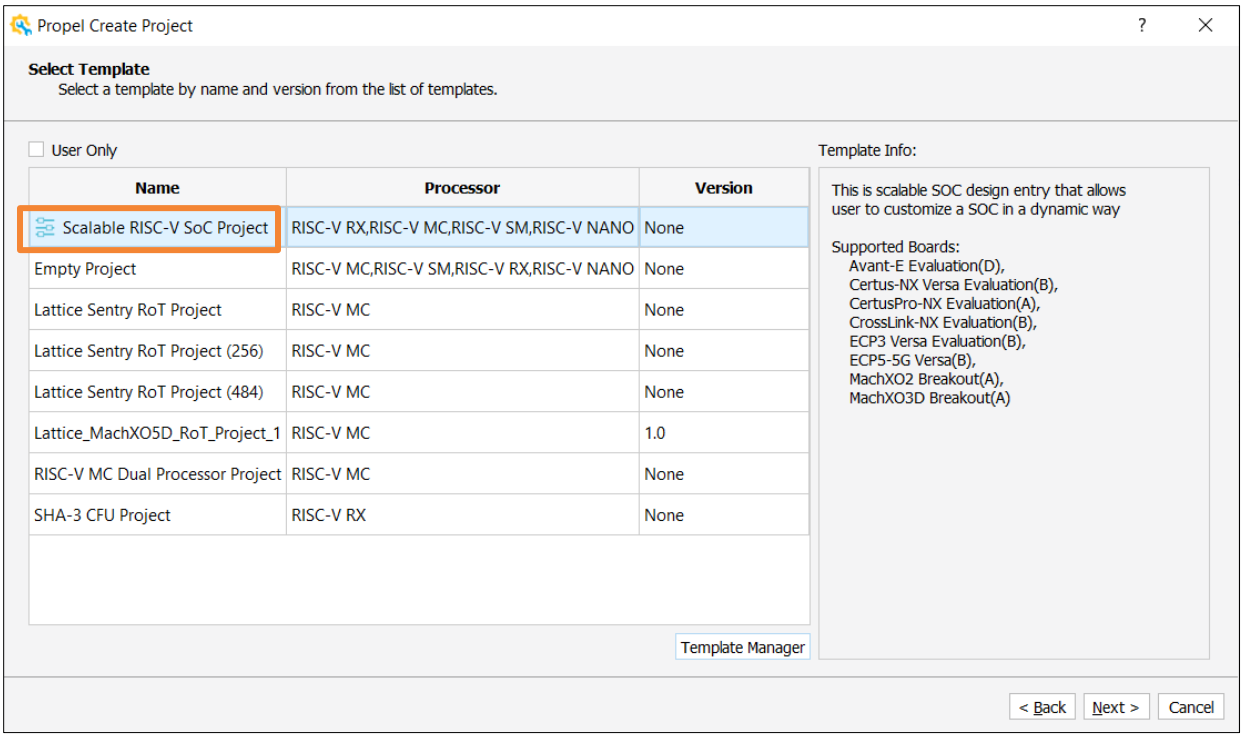


Figure 2.19. Choose Scalable RISC-V SoC Project

2. Enter the **Propel Create Project** wizard. From the **System Application Level** dialog, choose a template and click **Next** (Figure 2.20)**.**

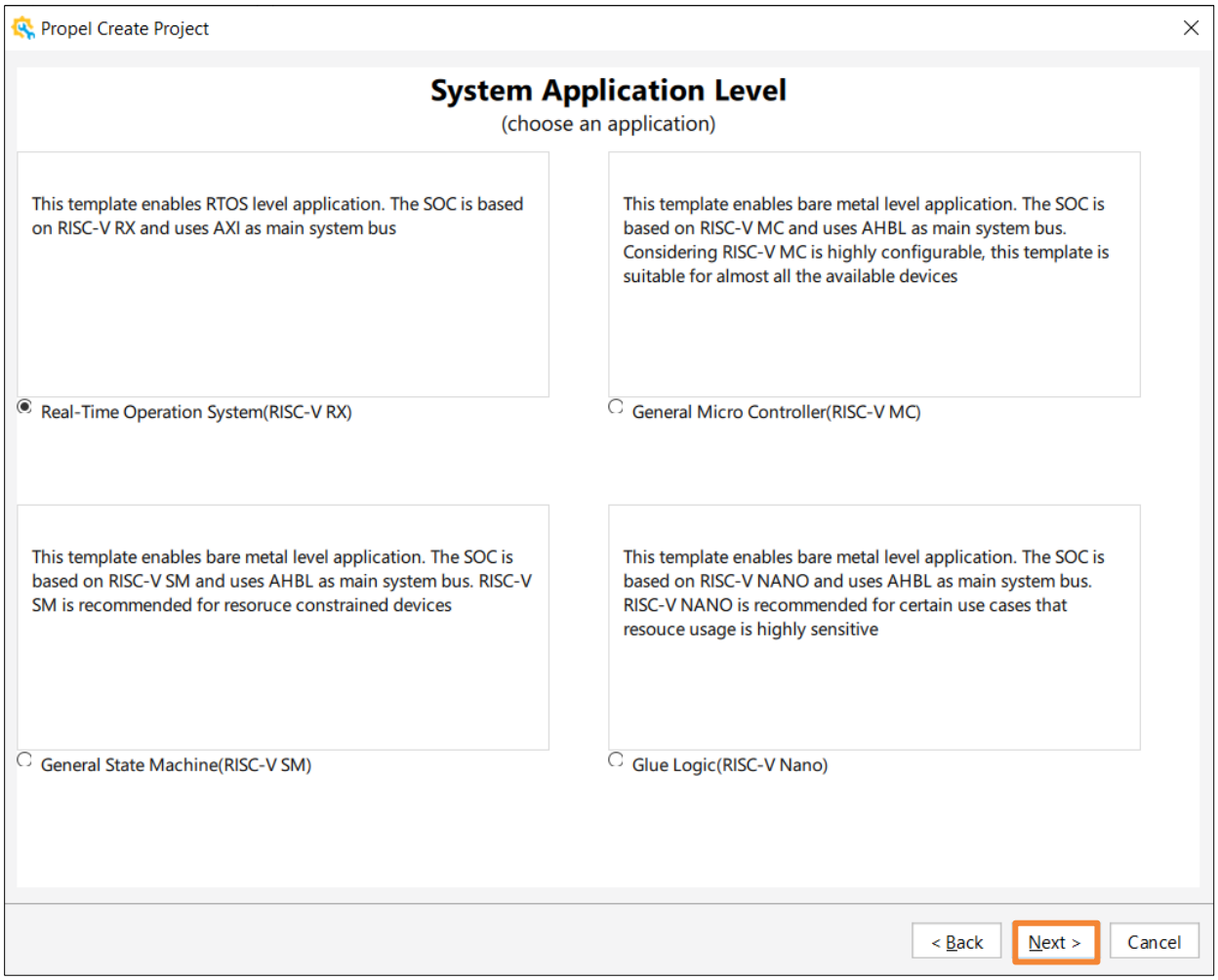


Figure 2.20. Scalable Wizard – System Application Level

3. From the **Select** Device Page, choose **Board** (Figure 2.21) or **Device** (Figure 2.22) that is supported for this template, click **Next**.

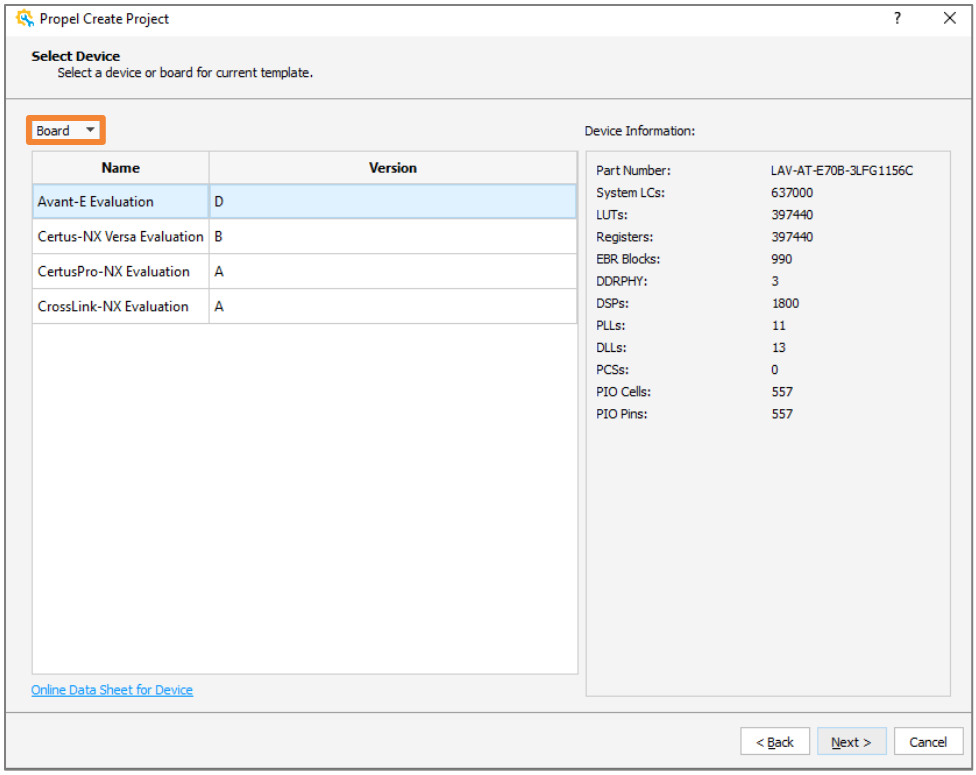


Figure 2.21. Scalable Wizard – Choose Board

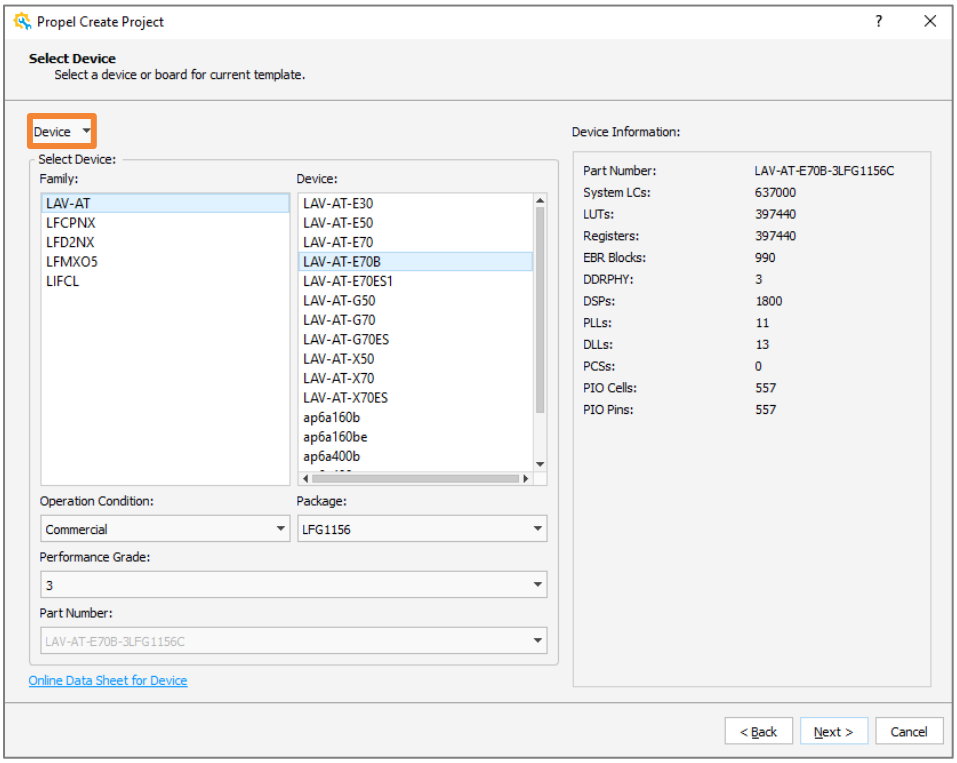


Figure 2.22. Scalable Wizard – Choose Device

4. From the System Configuration page, there are two steps (Figure 2.23):

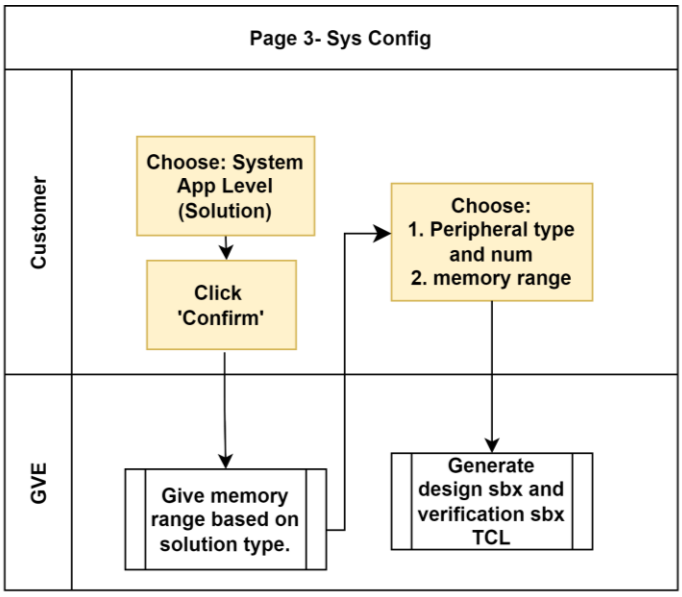


Figure 2.23. Scalable Wizard – System Configuration Page

Step1: First, choose a specific System App Level Solution based on this template via making choice in **System App Level** combo box (Figure 2.24) and then clicking **Confirm**.

At present, Propel Builder only supports one solution for each template and will scale them later if needed.

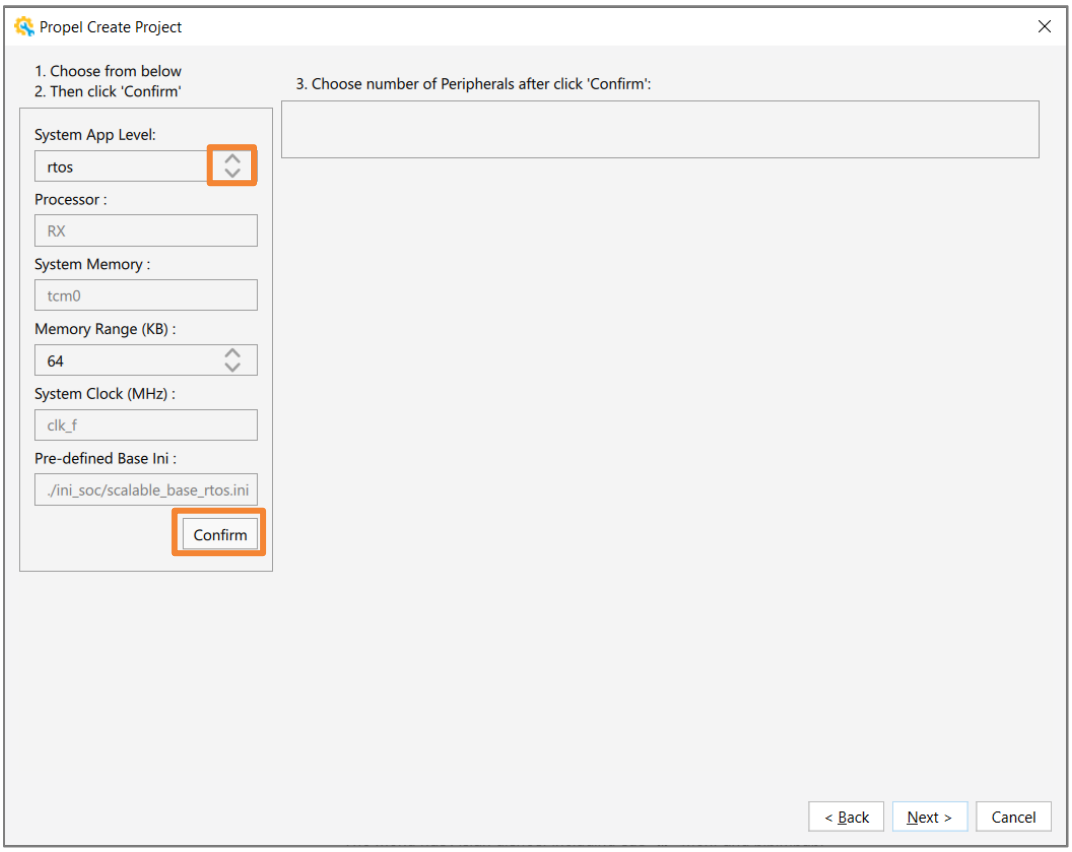


Figure 2.24. Scalable Wizard – System Configuration

After you click Confirm, Propel Builder does a preliminary check on all the IPs required in this solution. If there is any IP missing, an error message shows on the page. You can click on Install IPs to install missing IPs in bunch (Figure 2.25).

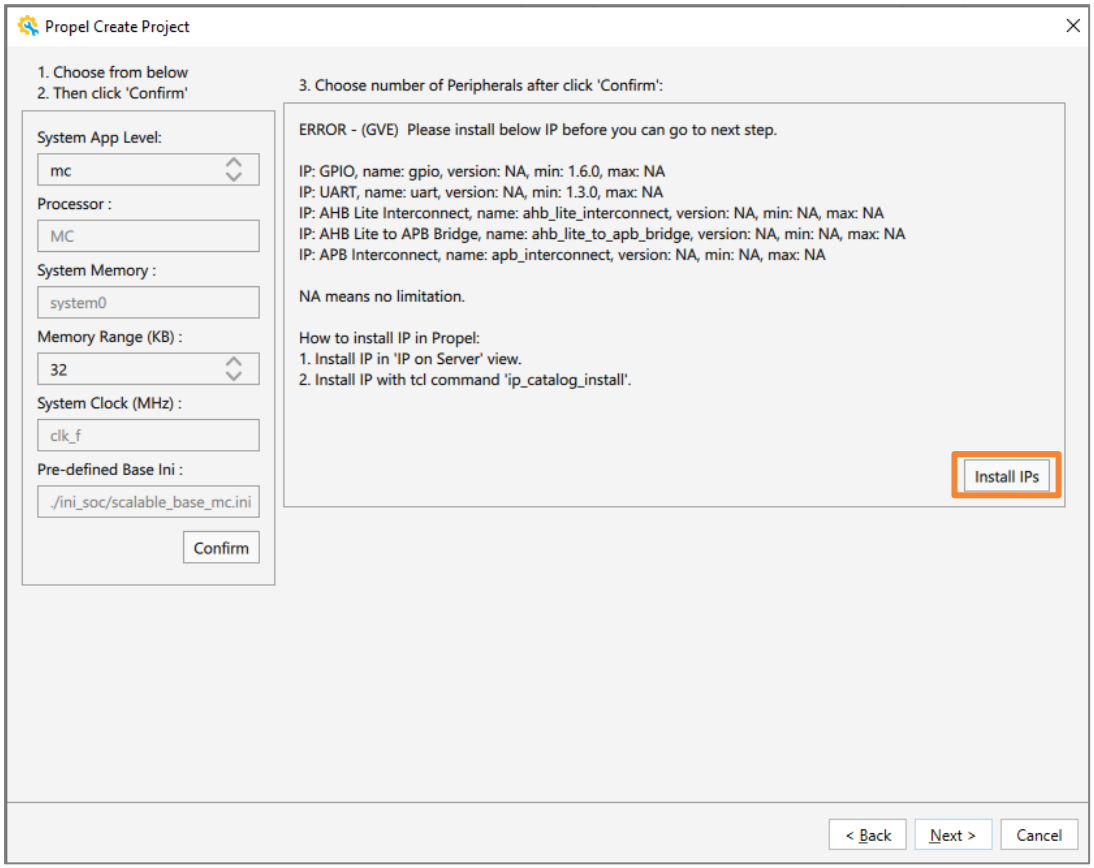


Figure 2.25. Scalable Wizard – Error Message when Missing IP

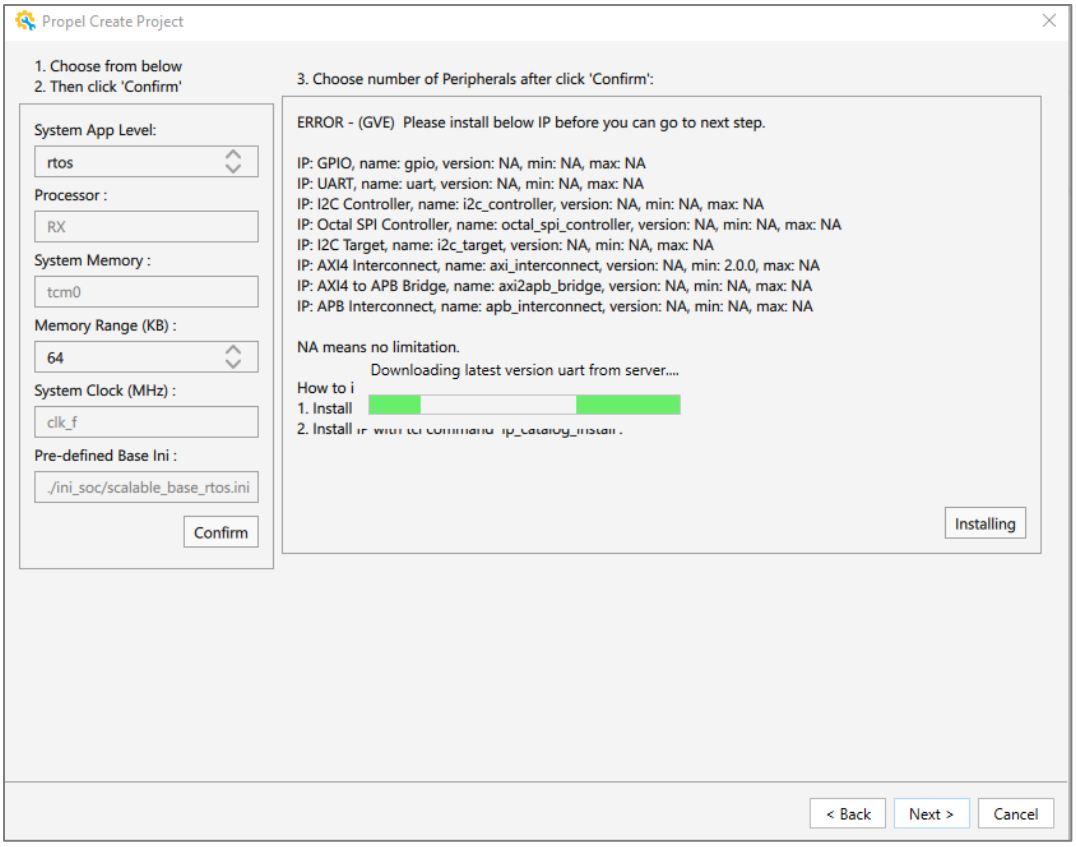


Figure 2.26. Scalable Wizard – Install IPs

Step2: After installing missing IPs, click **Confirm again**.

In the right column, you can see all the peripherals that are configurable in this solution. You can choose the number of each peripheral in its combo box.

In the left column, you can review the basic system information for this solution and select **Memory Range** of the system.

After all the selections are done, click **Next** (Figure 2.27).

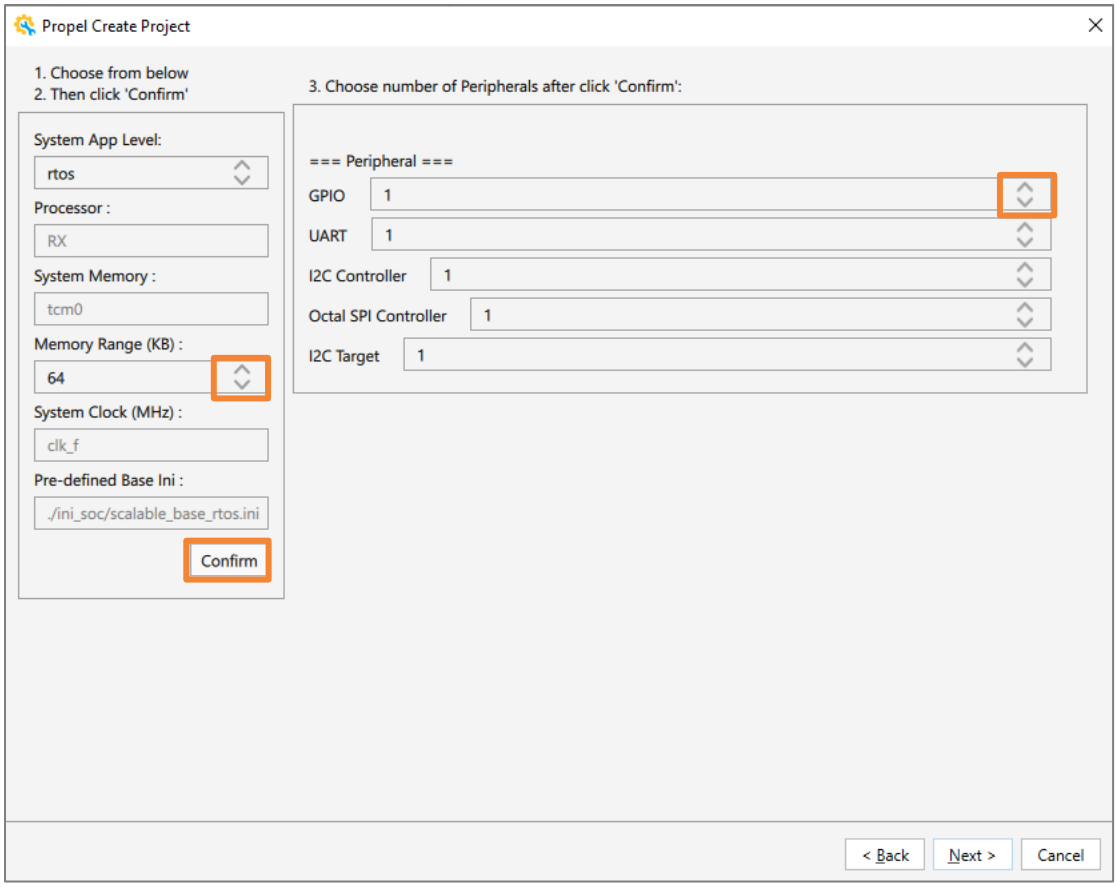


Figure 2.27. Scalable Wizard – System Configuration – Choose Peripherals

5. Now you can see a straight-forward layout preview about the current system structure(Figure 2.28). After confirming the system preview, click **Next**.

   This preview demonstrates the system bus type, frequency, the bus connection for each component, component type, number and their base address.

   Meanwhile, the TCL for launching the design project/verification project for this system design is generated at the background. The verification project is optional, meaning it depends on whether this solution defines the verification project beforehand.

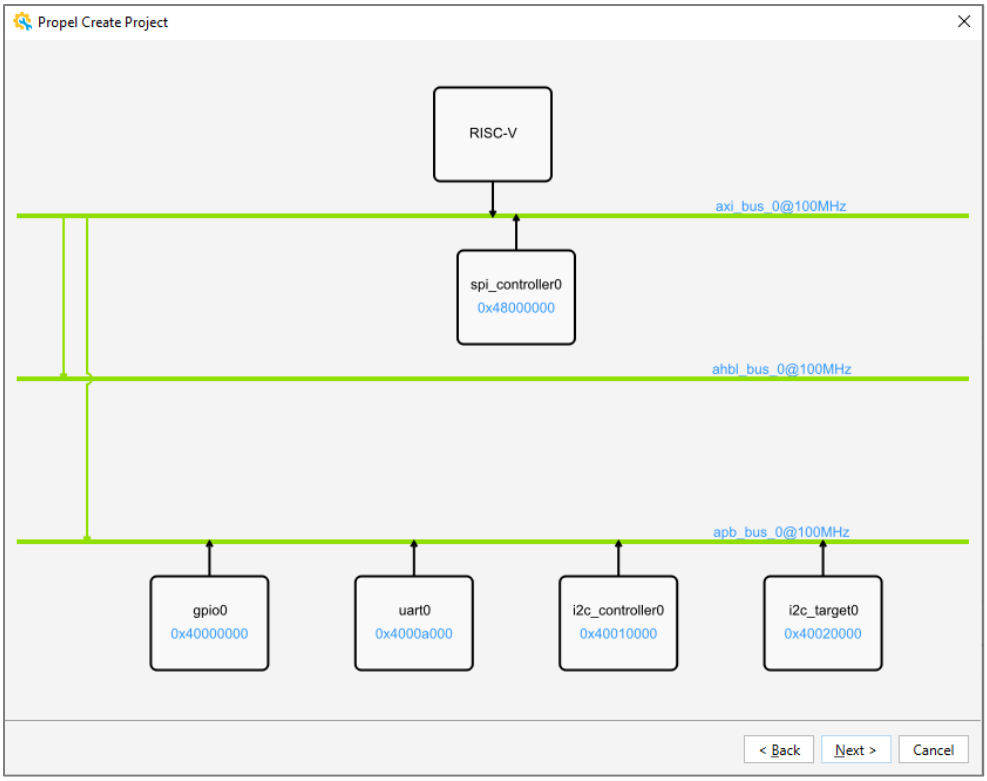


Figure 2.28. Scalable Wizard – System Preview

6. In **Project Information** Page, review the info for this project (Figure 2.29). Click **Next**.

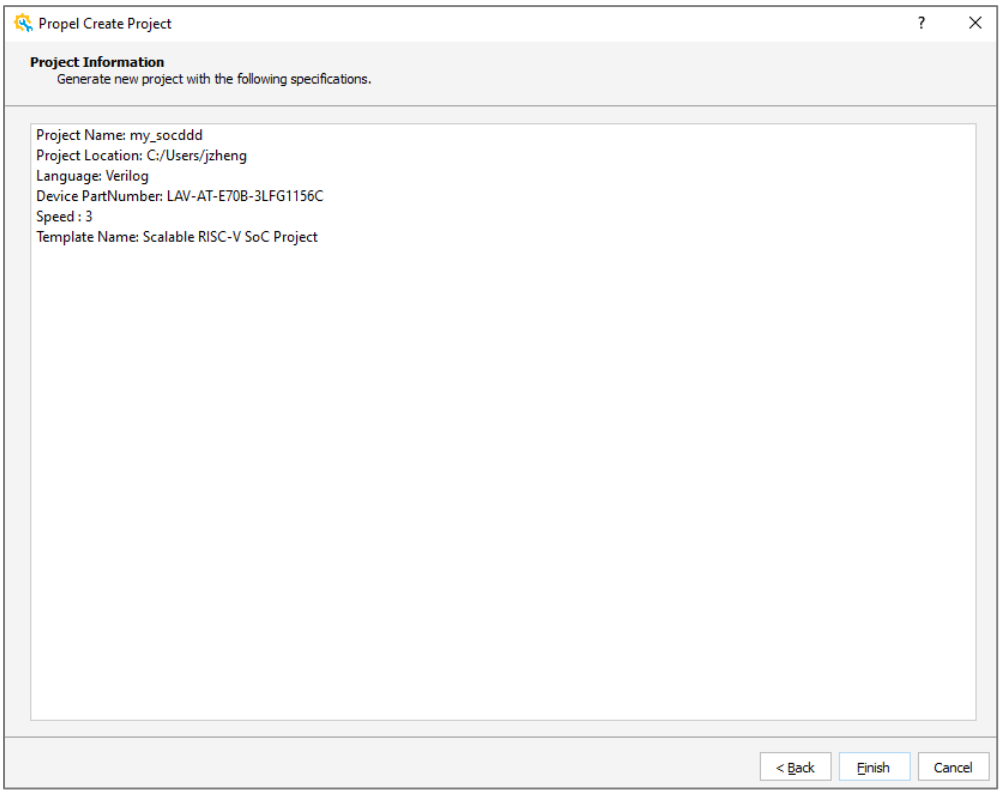


Figure 2.29. Scalable Wizard – Project Preview

7. The SoC design project is successfully created for Scalable Design (Figure 2.30).

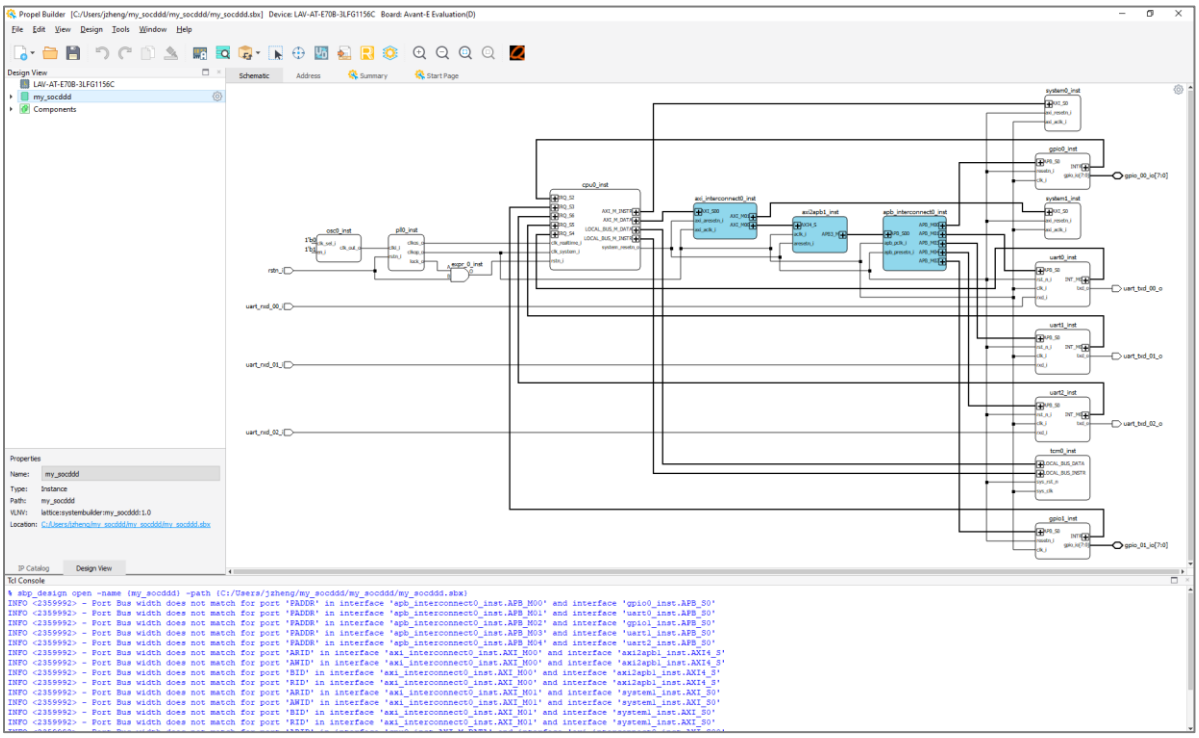


Figure 2.30. Scalable Wizard – Project Create Success

2.3.1.3. New Design Entry

1. Choose **File** >  **New Design** from the Lattice Propel Builder Menu bar. The Create System Design wizard (Figure 2.31) opens.

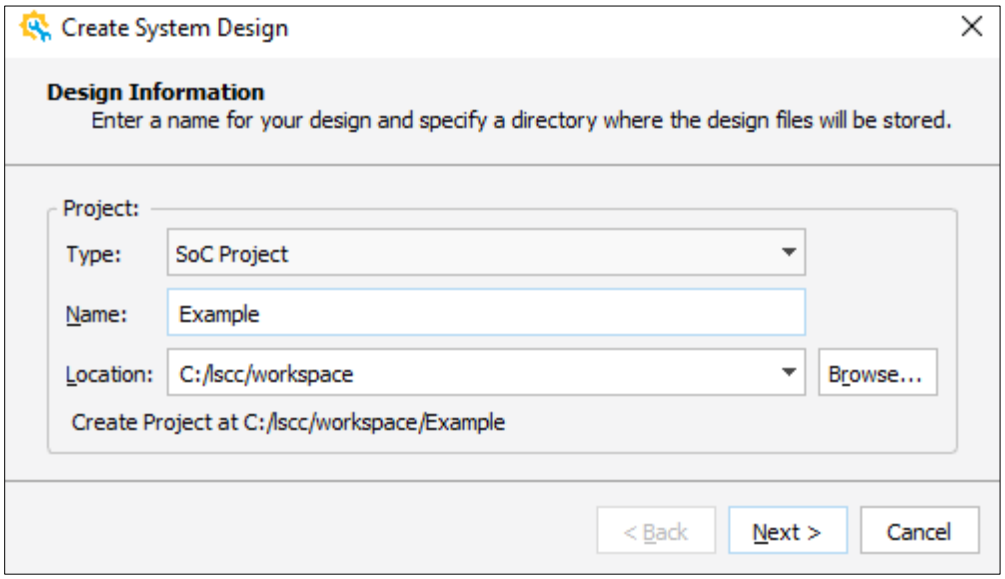


Figure 2.31. Create System Design – Design Information Wizard

2. The default Project Type is displayed in the **Type** field. Select **SoC Project** from the drop-down menu.
3. Enter a project name in the **Name** field, such as Example.

4. (Optional) The default location is shown in the **Location** field. Use the **Browse…** option to change the project workspace location.

   Note: Long path is not well supported in Windows OS. If a file exists under the path but you get a prompt of No such file, try moving this file to a directory with a shorter path.

5. Click **Next**. In the Configure Propel Project wizard, you can specify a device or a board for an SoC project.
   To specify a device for your new SoC project, use the **drop-down** menu to select the desired device information: Family, Device, Package, and Speed.

6. Select **Empty Project** in the **Templates** field (Figure 2.32).

   Templates are customized with commonly used programs as well as pre-defined family, device, package, speed, and operating condition. There are several templates here, which are programmed to run demo. You can make changes based on these templates.

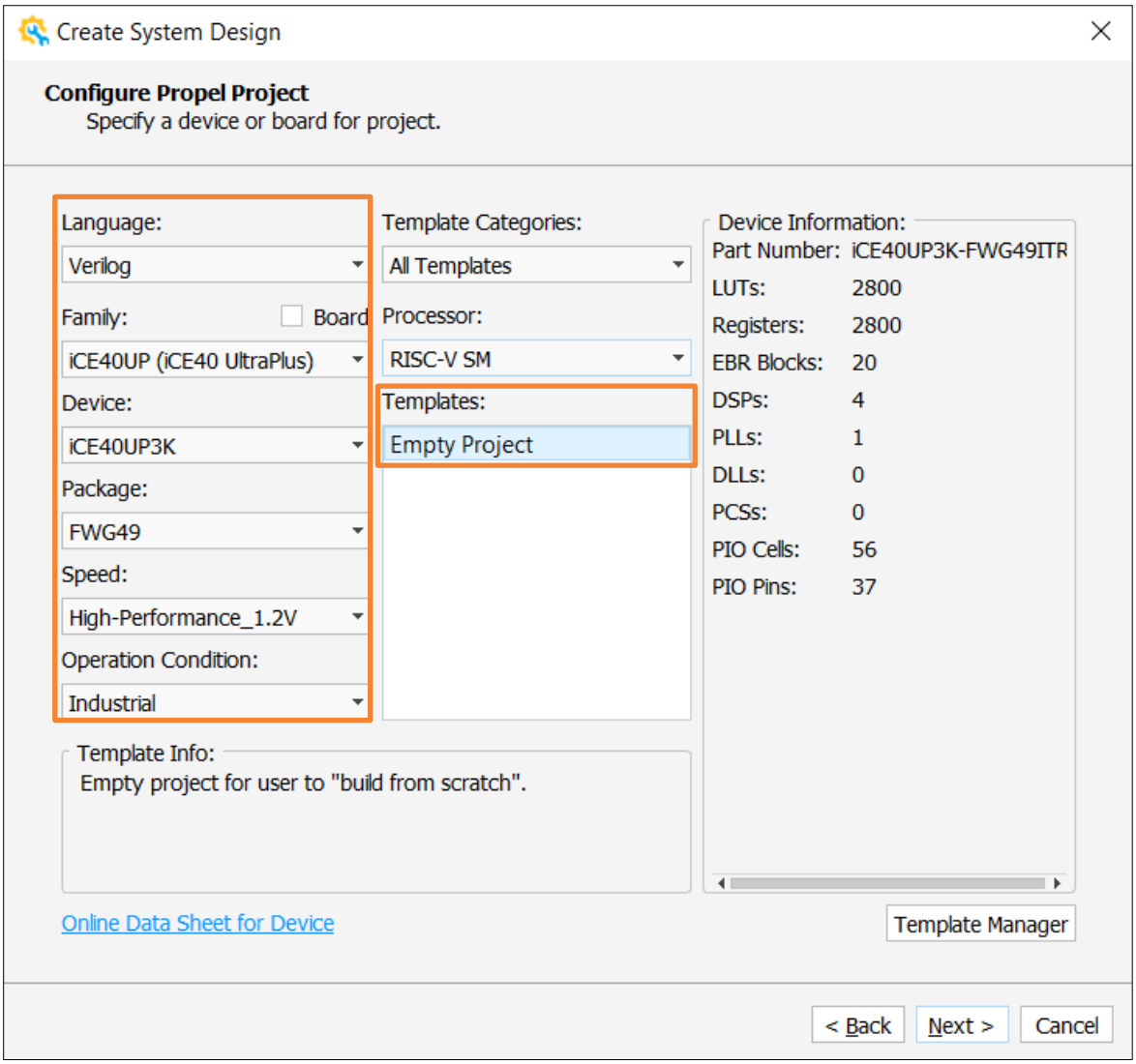


Figure 2.32. Specify a Device for Template SoC Project

Or, to specify a board for a new Template SoC project, check the **Board** box (Figure 2.33).

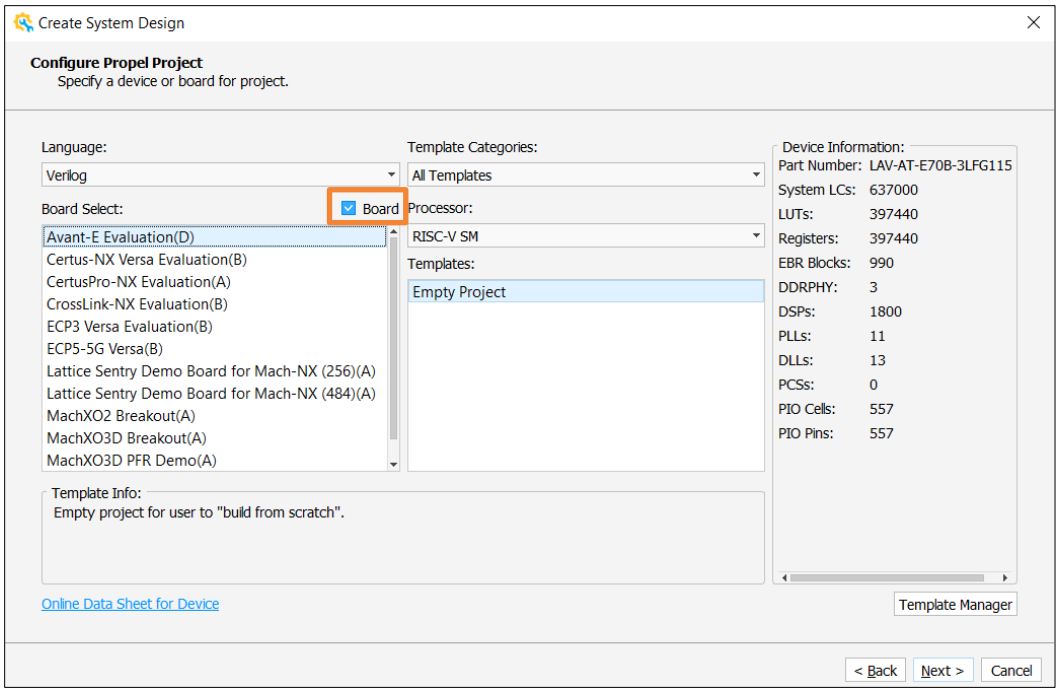


Figure 2.33. Specify a Board for Template SoC Project (1)

7. The Configure Propel Project wizard is shown in Figure 2.34. From the **Board Select** area, select the desired board.

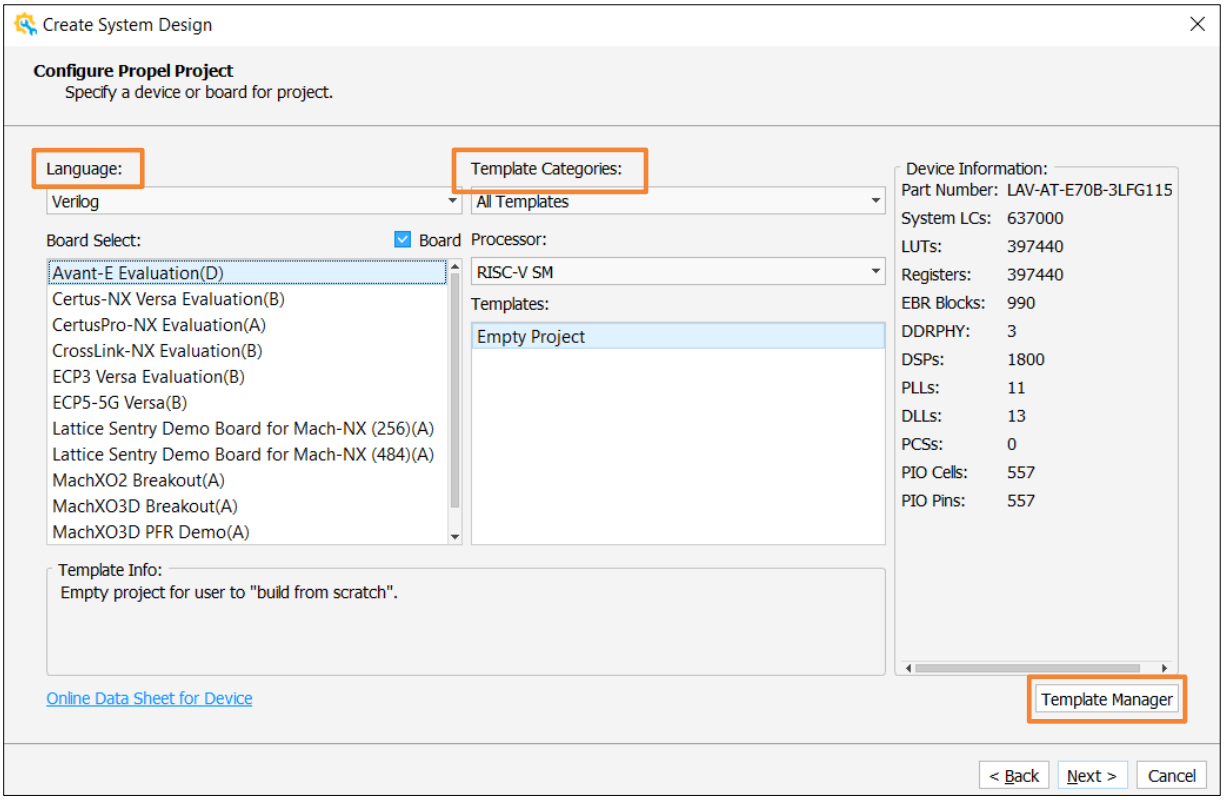


Figure 2.34. Specify a Board for Template SoC Project (2)

Notes:

- You can choose VHDL/Verilog in Language filed. The top wrapper is to be generated in your selected language. All other IP and modules are generated in their default language.
- Template Manager is for you to customize your own template that can be imported later. Refer to the Define Custom Template section for more information.
- Custom templates (User Templates) can also be selected from this page, from the drop-down menu of Template Categories.

8. (Optional) About the Processor section (Figure 2.35):
   - If you create an empty project, you do not need to make any selection.
   - If you want a template with a specific processor type, you need to select the correct processor.
   - Different processors are with different templates. For example, RISC-V RX processor is with different templates from those for RISC-V MC processor.

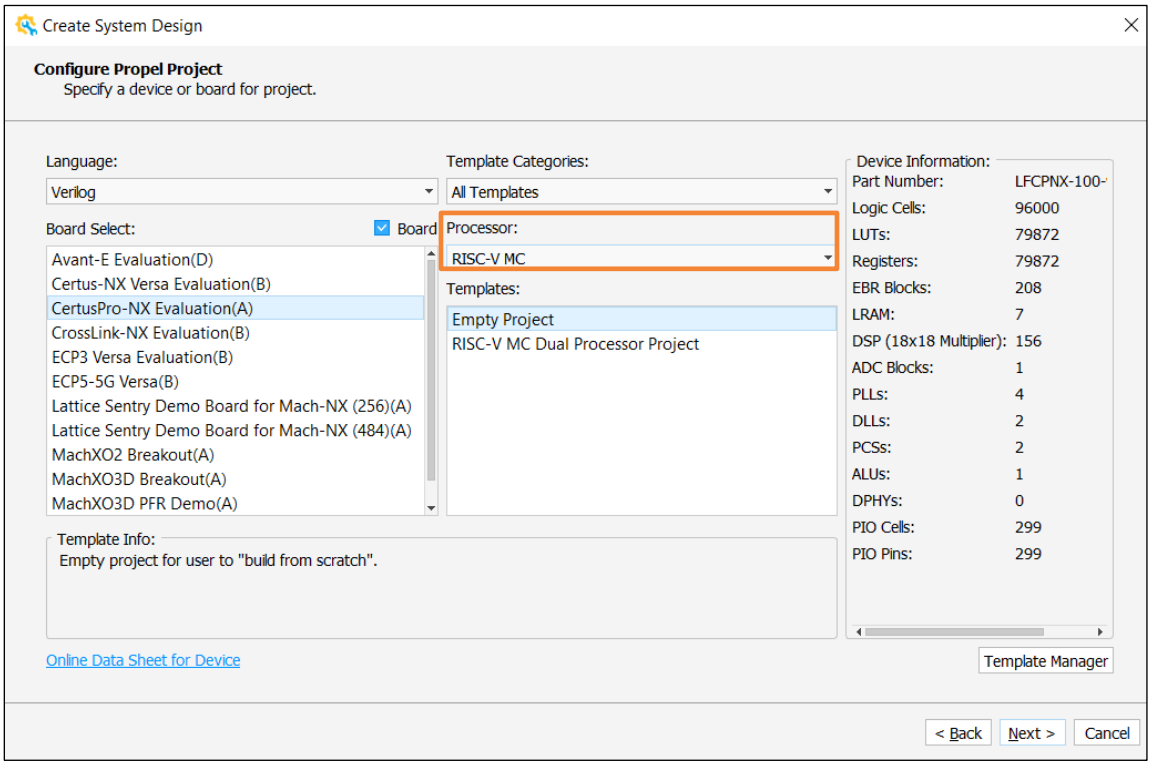


Figure 2.35. Specify a Board for Template SoC Project (3)

2.3.2. Opening an Existing SoC Project

To open an existing SoC project, choose **File** > **Open Design** from Propel Builder GUI menu or click **Open Design** icon from Propel Builder Toolbar (Figure 2.36).

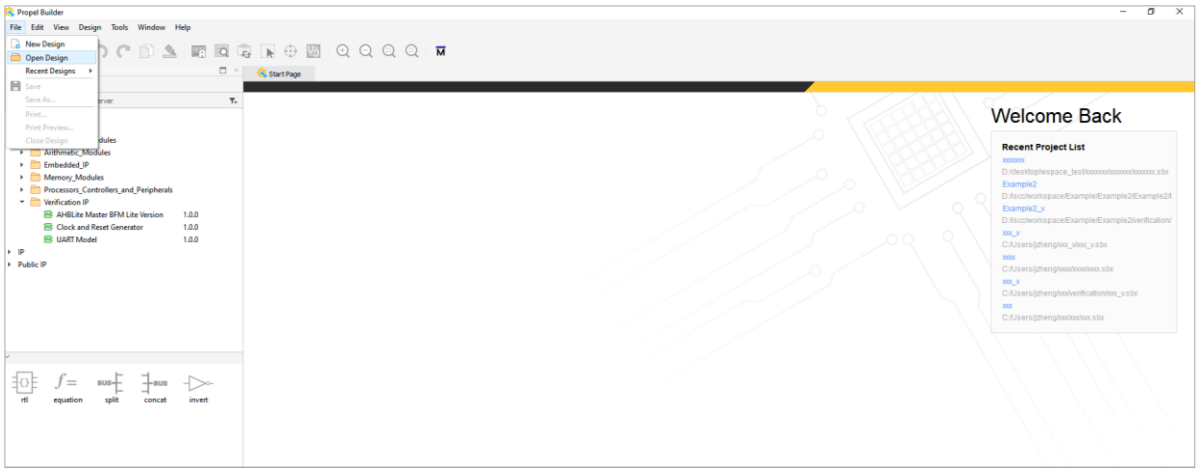


Figure 2.36. Open Design

1. Browse to find the default project workspace folder or your own project workspace folder. Choose the sbx file, such as HelloWorld.sbx (Figure 2.37).

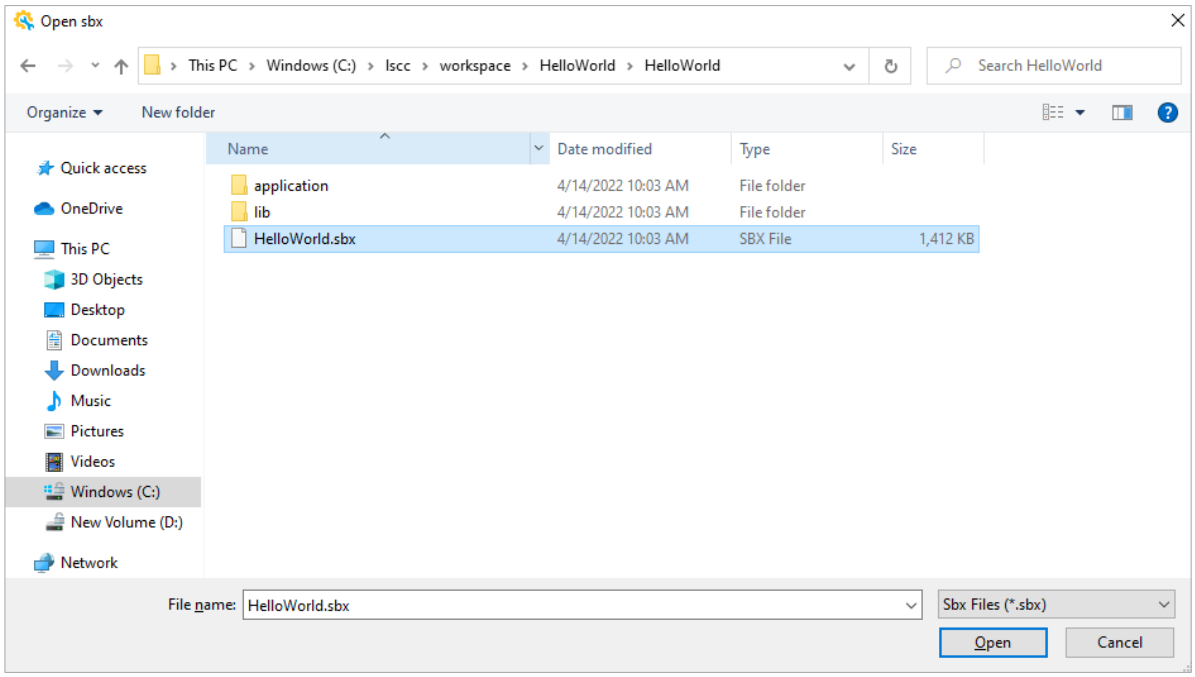


Figure 2.37. Open Existing Project

2. Click **Open**. The Builder GUI shows the SoC design.

   When opening a project, Propel Builder checks the uninstalled IPs based on name, library and vendor. Version check was skipped because IP can be updated to different versions. If IPs are not installed, warning messages are issued.

3. You can also use **File** > **Recent Designs** from Propel Builder Menu (Figure 2.38) to quickly open a recently closed project.

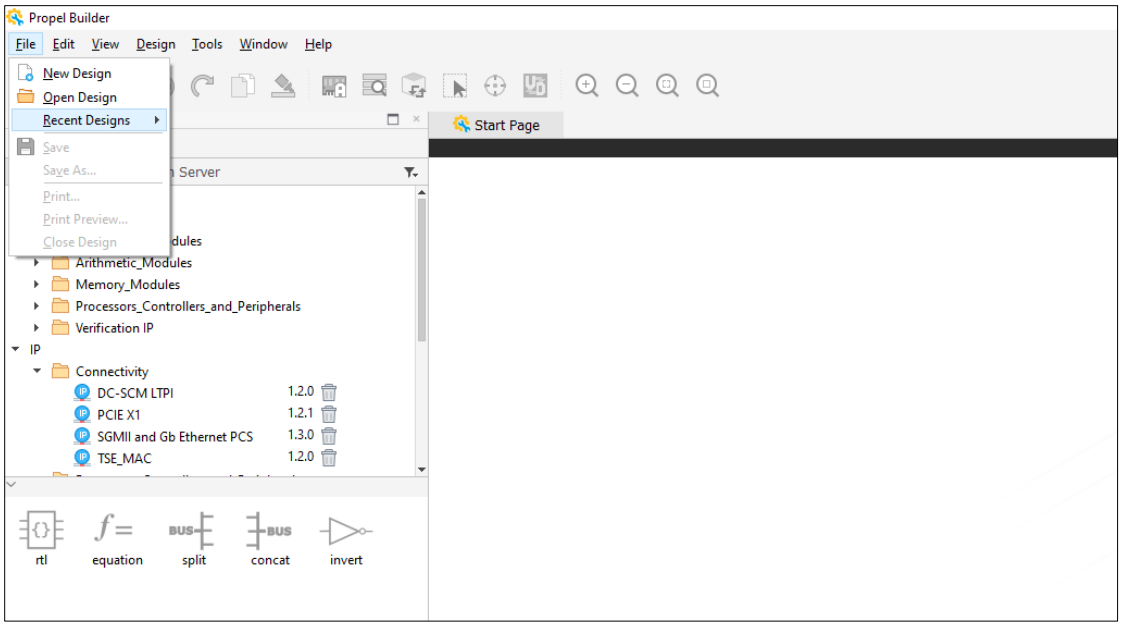


Figure 2.38. Open Recent Project

2.3.3. Generating and Instantiating IP/Module

After starting a Propel Builder project, you can add modules by dragging them from the IP Catalog view to the Schematic view. The IP Catalog view comes with a large variety of modules for common use and some glue logic modules, which can be found from the **IP on Local** tab. You can also click the **IP on Server** tab to find and download more modules for specialized use (Figure 2.39).

(Optional) From the Propel Builder GUI **IP Catalog** area (Figure 2.39), choose the **IP on Server** tab. Select a desired IP. IP version is displayed along with the IP name. For downloadable IP, a **Install** button is shown. indicates this IP is not compatible with the current version of Propel or the current device. You can hover the mouse over the to see the warning message details about why the IP is not supported (Figure 2.40). If the IP is already installed, Installed is shown (Figure 2.39).

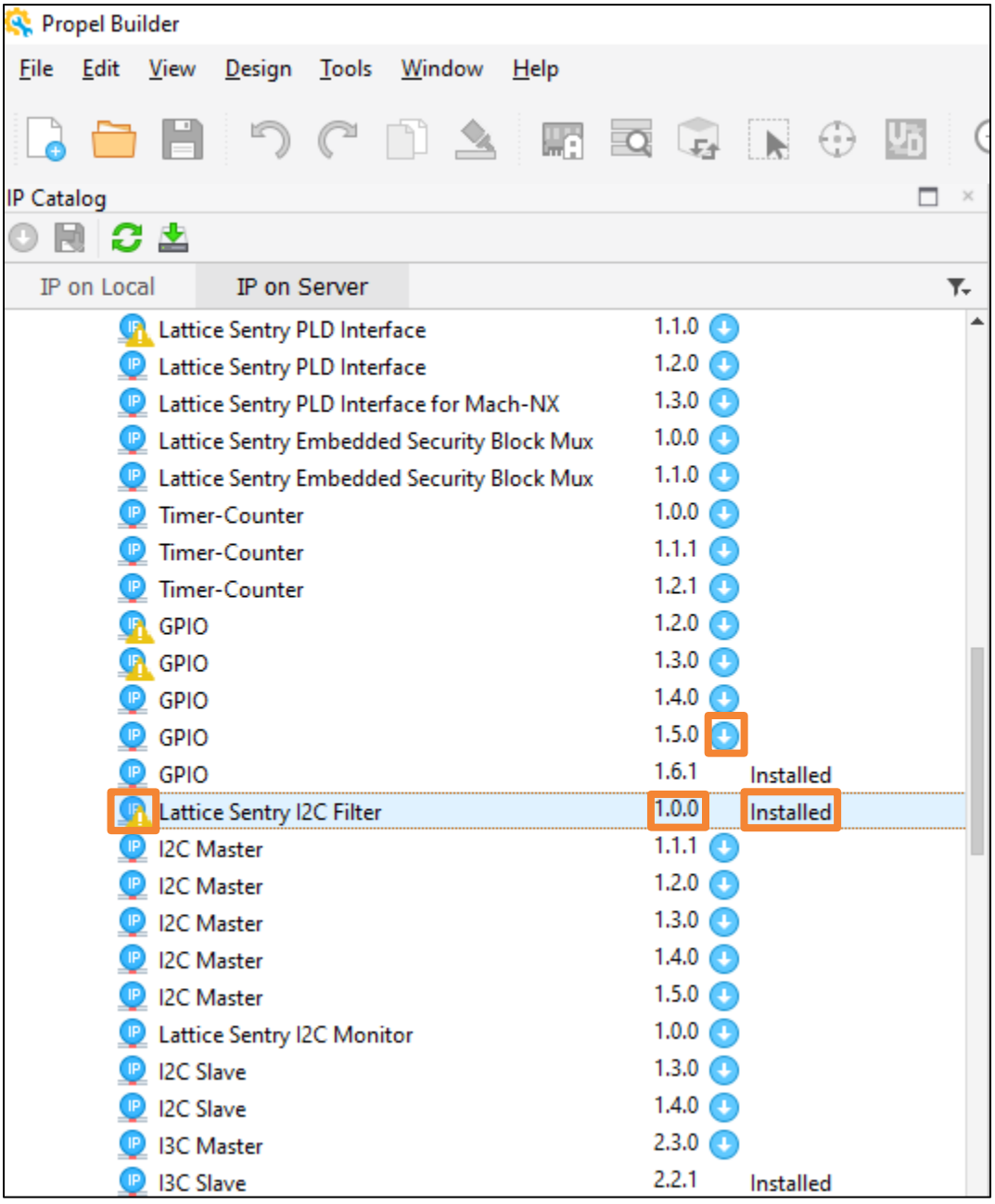


Figure 2.39. IP on Server

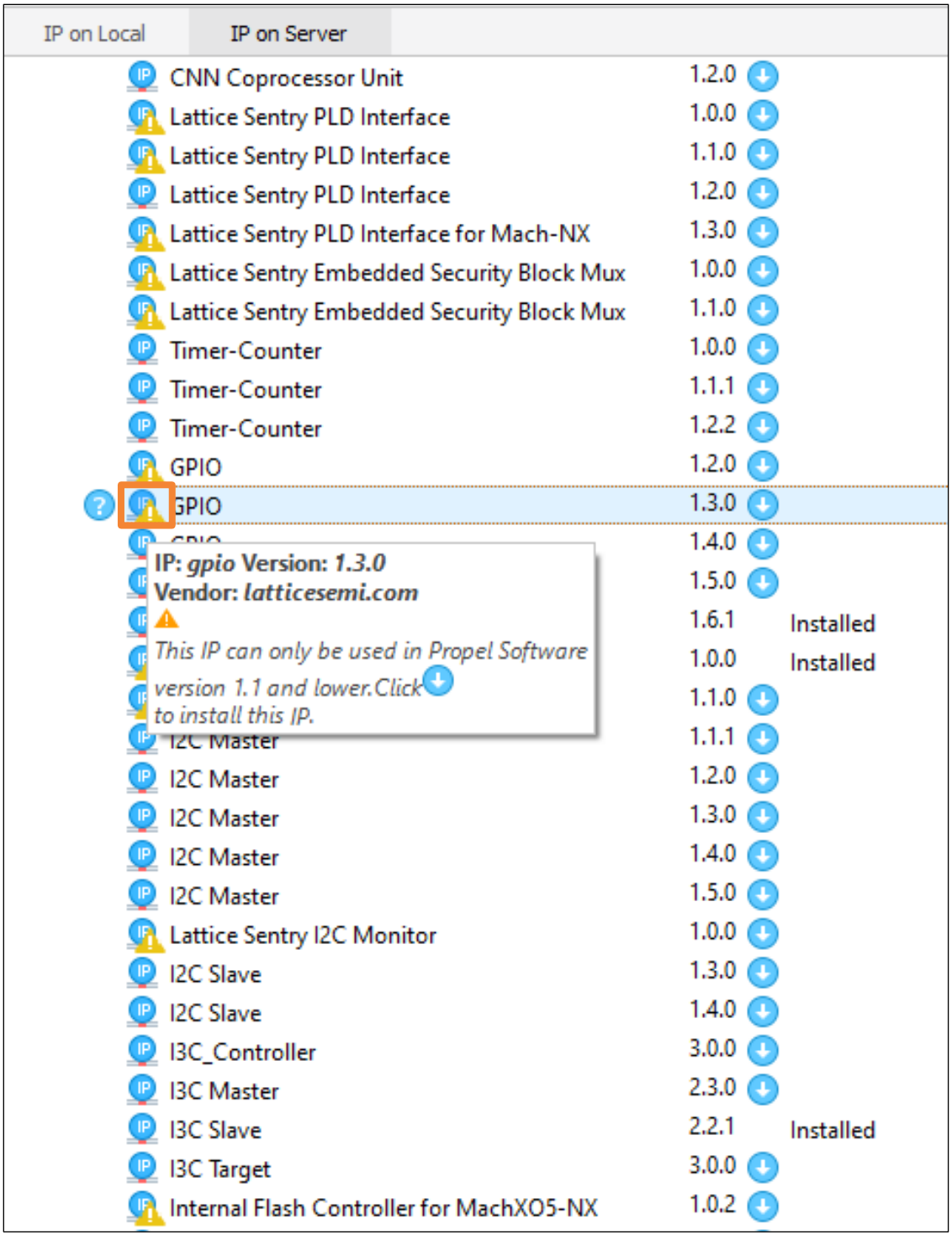


Figure 2.40. Hover Mouse over the Icon

You can use the filter and search function in IP catalog to find the IP you desire (Figure 2.41).

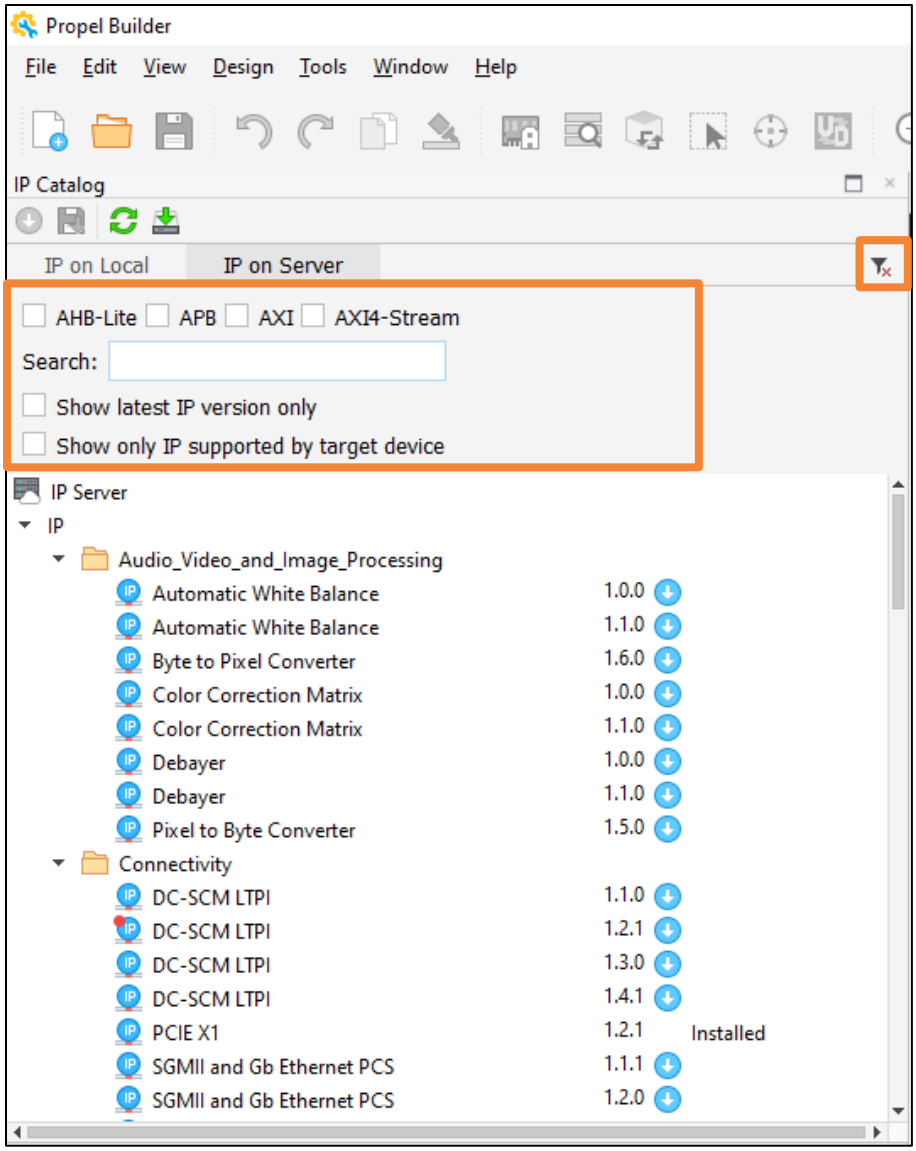


Figure 2.41. IP Filter and Search

1. Being installed successfully, the new IP is shown in the **IP on Local** tab (Figure 2.42).

   Note: Only IP that are compatible with the current device can appear under **IP on Local**.

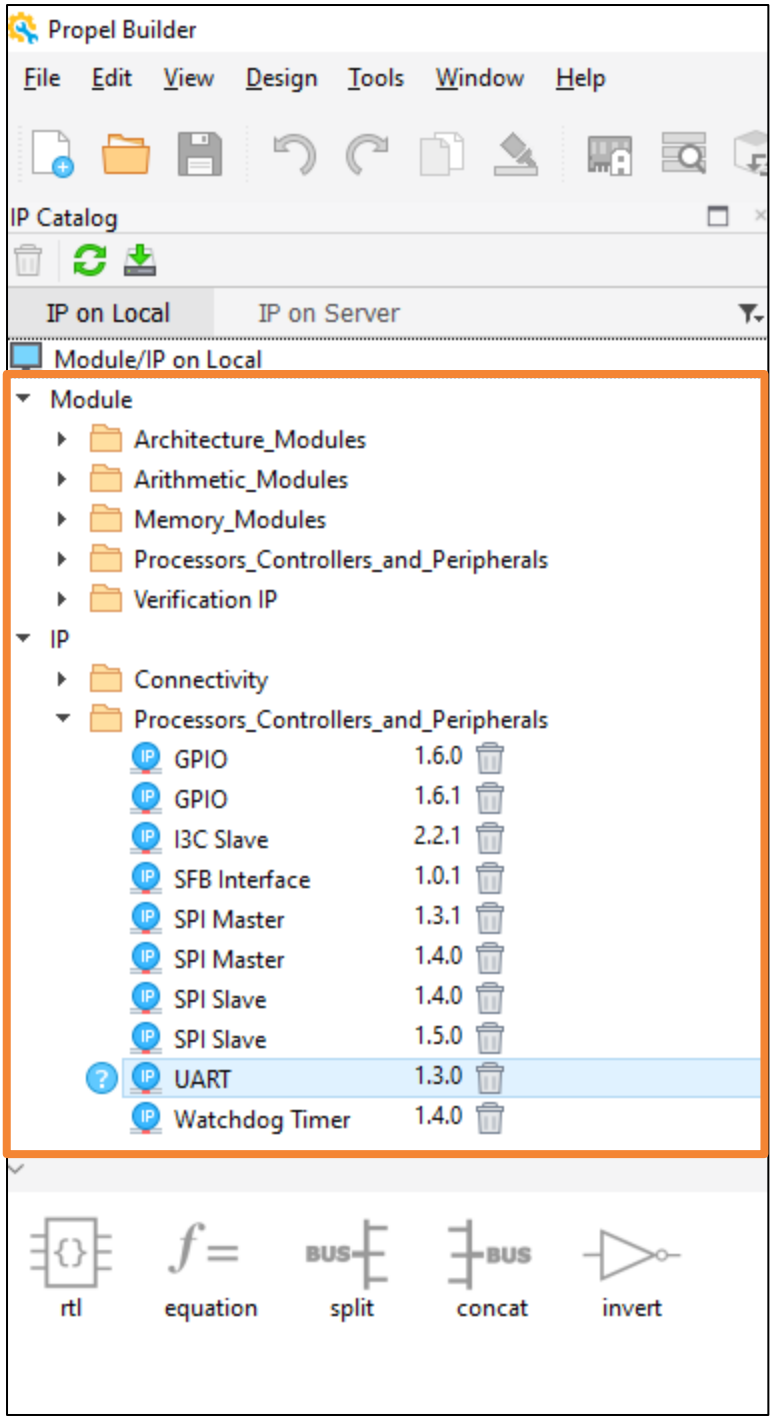


Figure 2.42. IP Catalog

2. From the **IP on Local** tab, select a desired IP, such as GPIO. Double-click the IP module, or drag and drop the IP module to the **Schematic** view. A Module/IP Block wizard pops up (Figure 2.43).

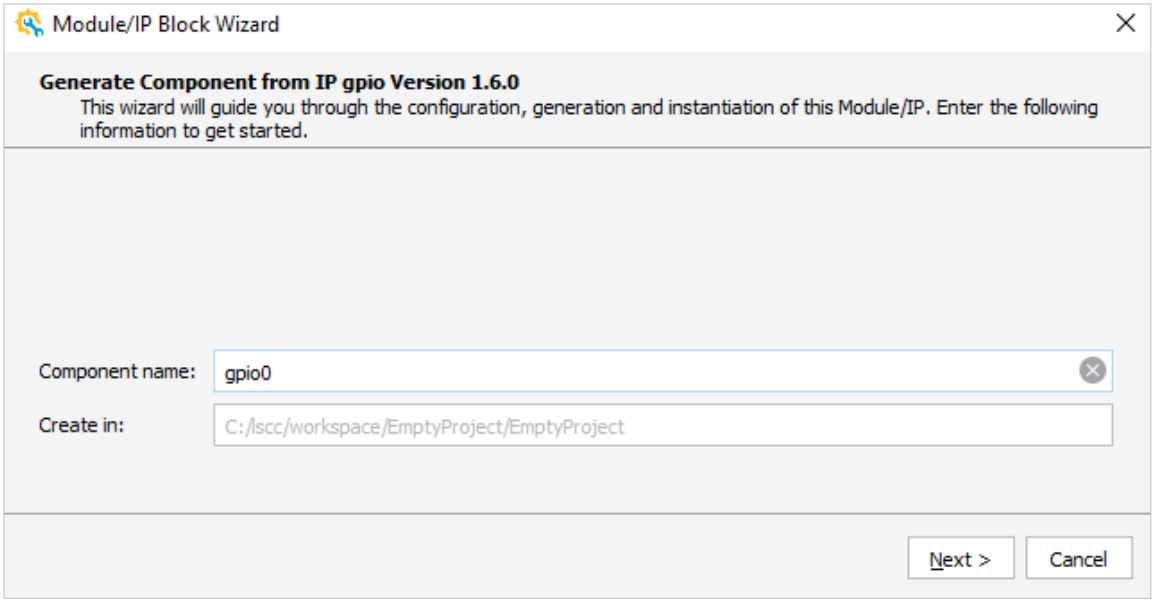


Figure 2.43. Module/IP Block Wizard – Generate Component from Module gpio Version 1.6.0

3. Enter a component name in the **Component name** area, such as gpio0. Click **Next**. Module/IP Block Wizard shows the **Configure Component from IP gpio Version 1.6.0** page (Figure 2.44).

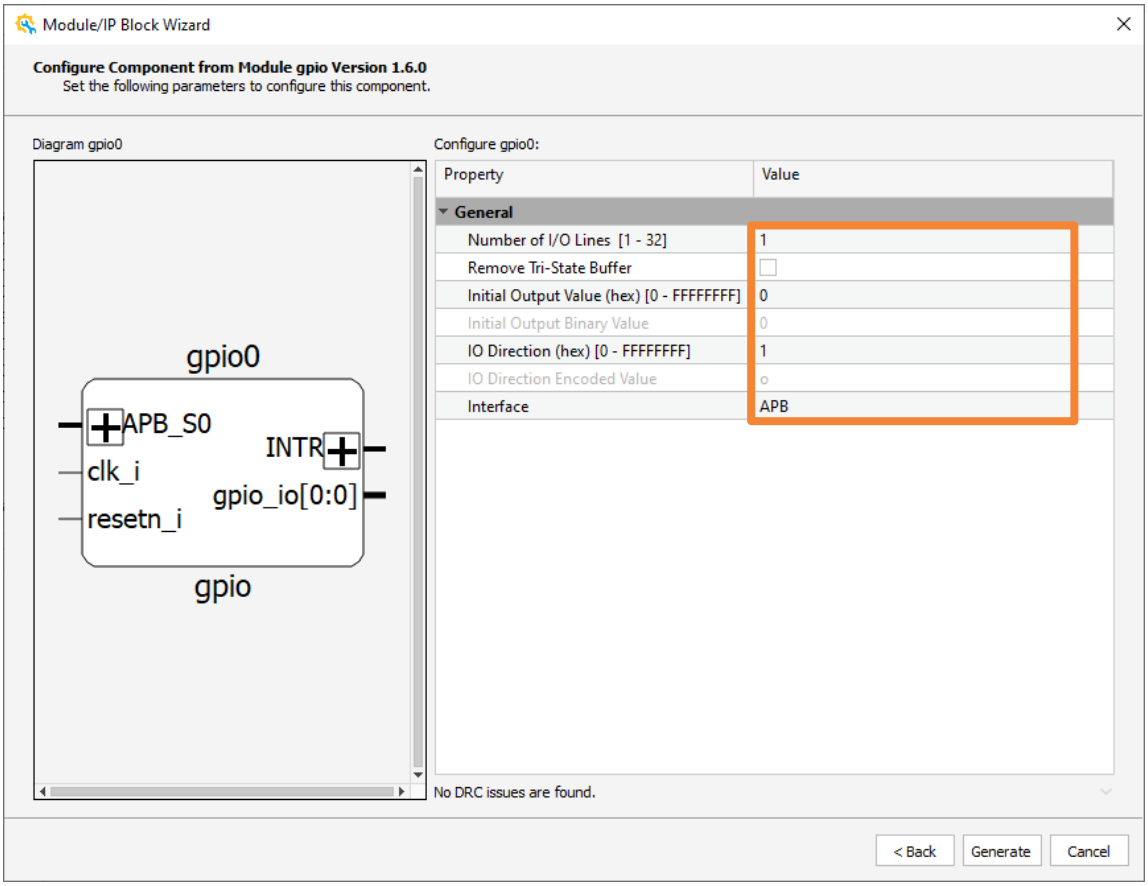


Figure 2.44. Module/IP Block Wizard – Configure Component from IP Gpio Version 1.6.0

4. (Optional) Reconfigure IP. Click the **Value** field. Enter a desired value for a property. Or check the checkbox to enable a property. You can also select a desired value from the dropdown menu for a property in the **Value** area. The property in gray is not configurable. By changing the value, the property is thus configured.

   Note: You need to generate the overall project for the IP to be generated or for any changes to take effect. Refer to Generating the Propel Design section for more info on how to do this.

5. Click **Generate**. Module/IP Block wizard shows the Check Generated Result page (Figure 2.45).

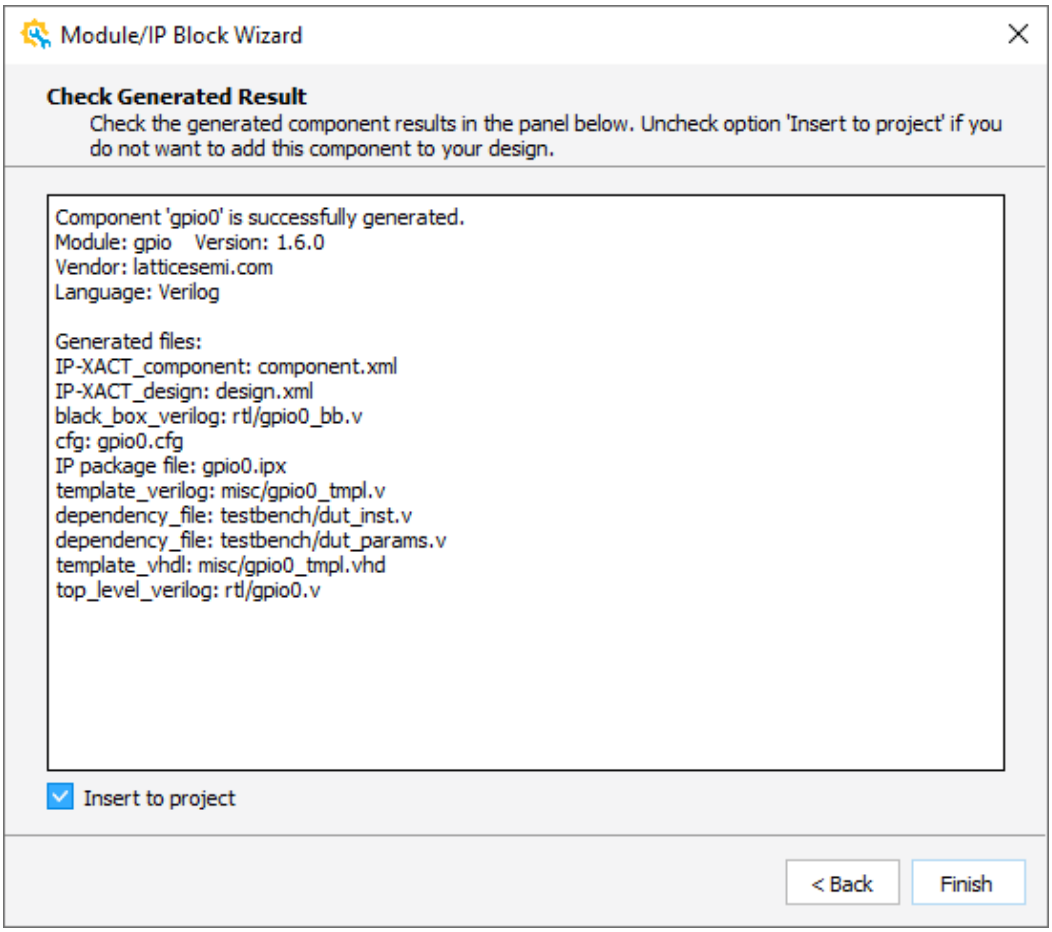


Figure 2.45. Module/IP Block Wizard – Check Generated Result

6. Select **Insert to project** (Figure 2.45) at the bottom of the Check Generate Result wizard, so that a **Define Instance** dialog box pops up as shown in next step. Or, this dialog box does not appear.
7. After selecting **Insert to project**, click **Finish** (Figure 2.45). The **Define Instance** dialog box opens (Figure 2.46).

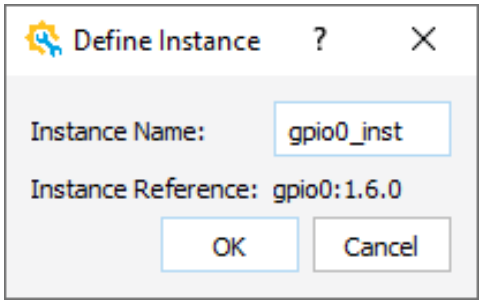


Figure 2.46. Design Instance Dialog Box

8. (Optional) Change the instance name, if desired. Space and special characters are not allowed.
9. Click **OK**. The schematic block for the module appears in the **Schematic** view (Figure 2.47).

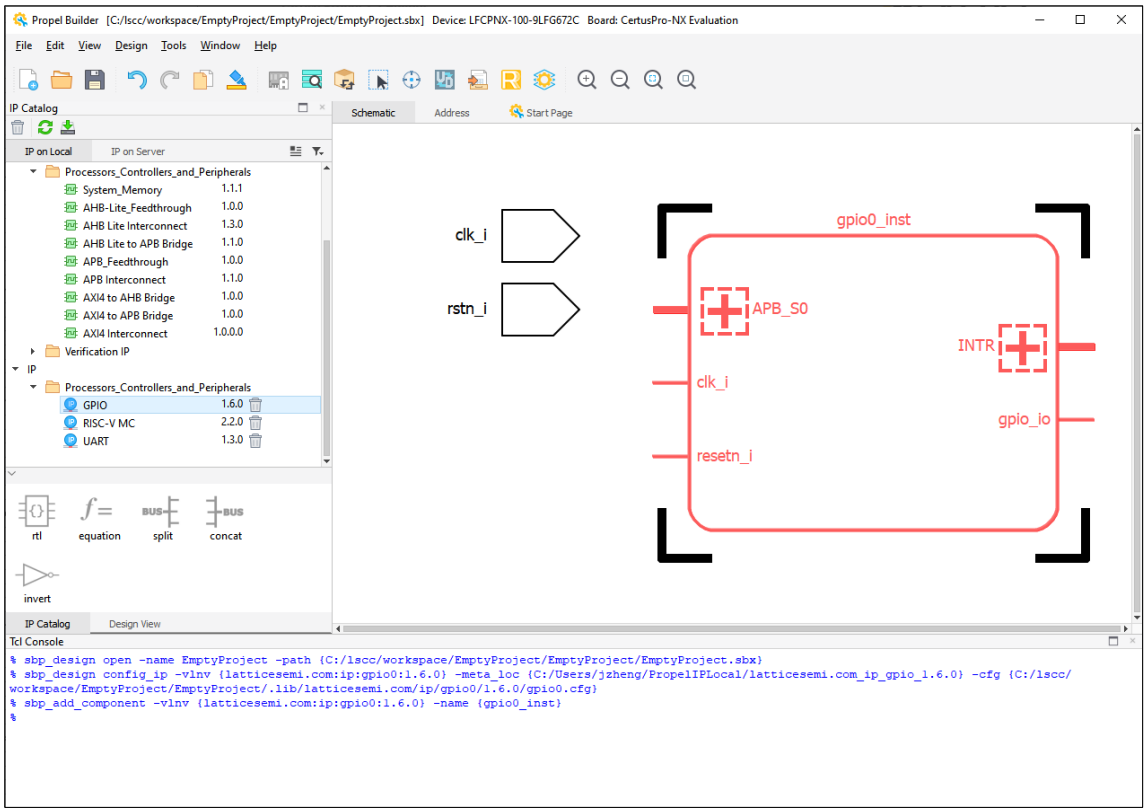


Figure 2.47. Propel Builder Schematic View Shows the Module Instance

10. (Optional) To re-generate this IP, double click on the instance. A Module/IP Block wizard pops up (Figure 2.48).

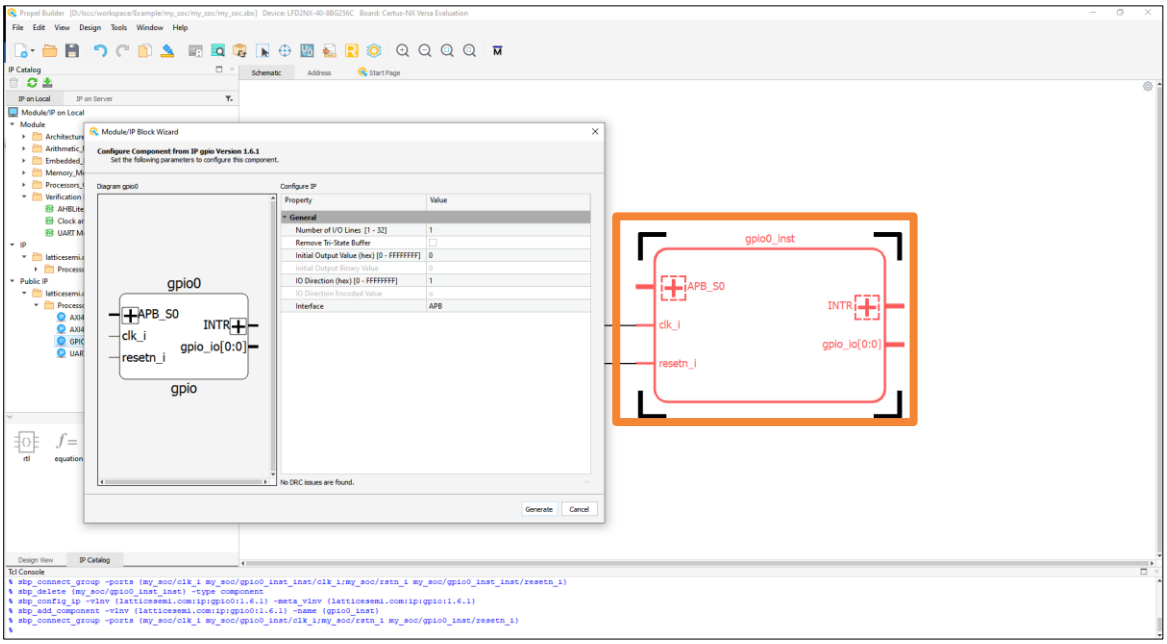


Figure 2.48. Regenerate Module/IP

11. (Optional) Propel Builder also supports to update all IPs. Choose **Edit > Upgrade ALL Ips**. Wait a few seconds, depending on how sophisticated the design is, to see the result (Figure 2.49).

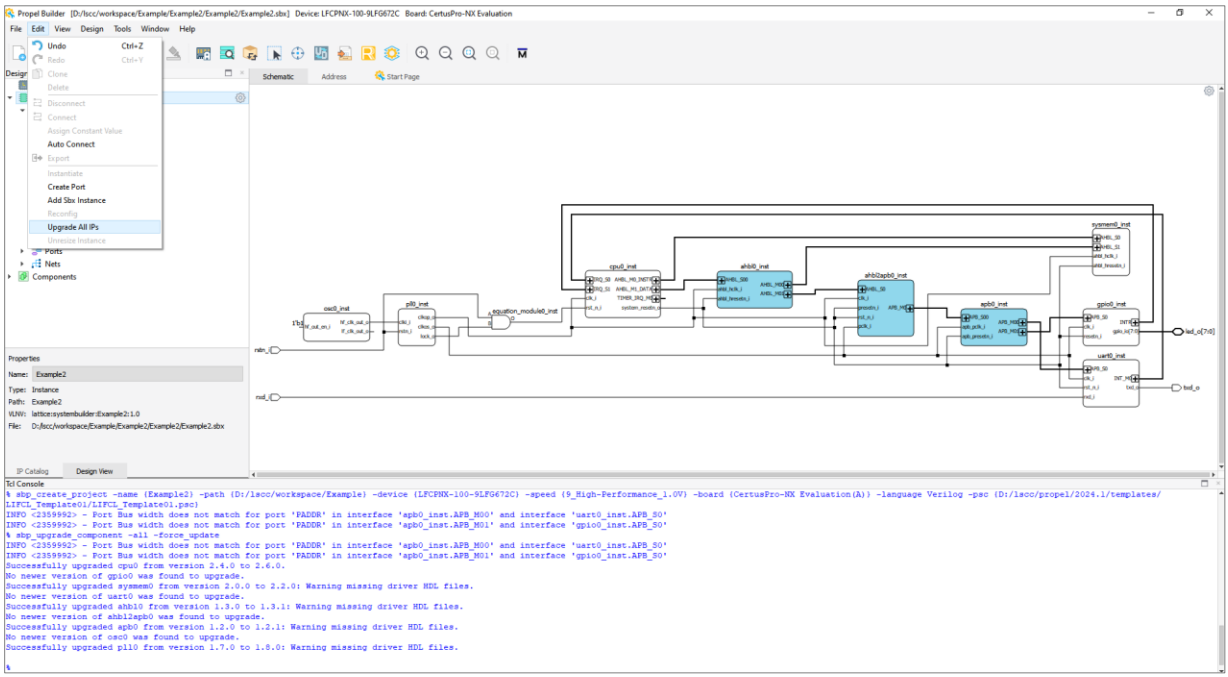


Figure 2.49. Upgrade All IPs

2.3.4. Adding Glue Logic

Propel 2025.2 builder supports glue logic modules as well as IP modules. You can add glue logic modules by dragging them from the IP Catalog view (Figure 2.50) to the Schematic view.

Glue logics is modified afterwards by double-clicking the module.

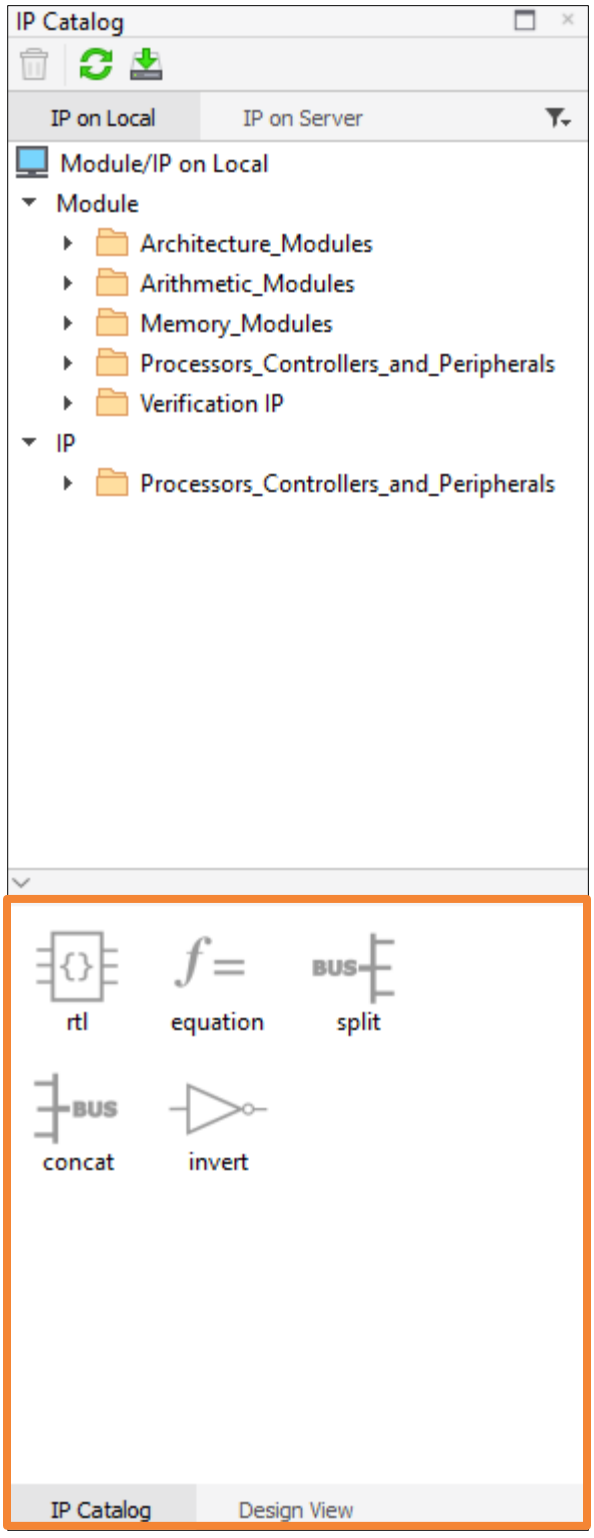


Figure 2.50. Glue Logic Section of the IP Catalog

2.3.4.1. Concat

1. From the IP Catalog, select the **concat** module. Double-click the concat module or drag and drop concat module to the Schematic view. A Glue Logic wizard (Figure 2.51) pops up.

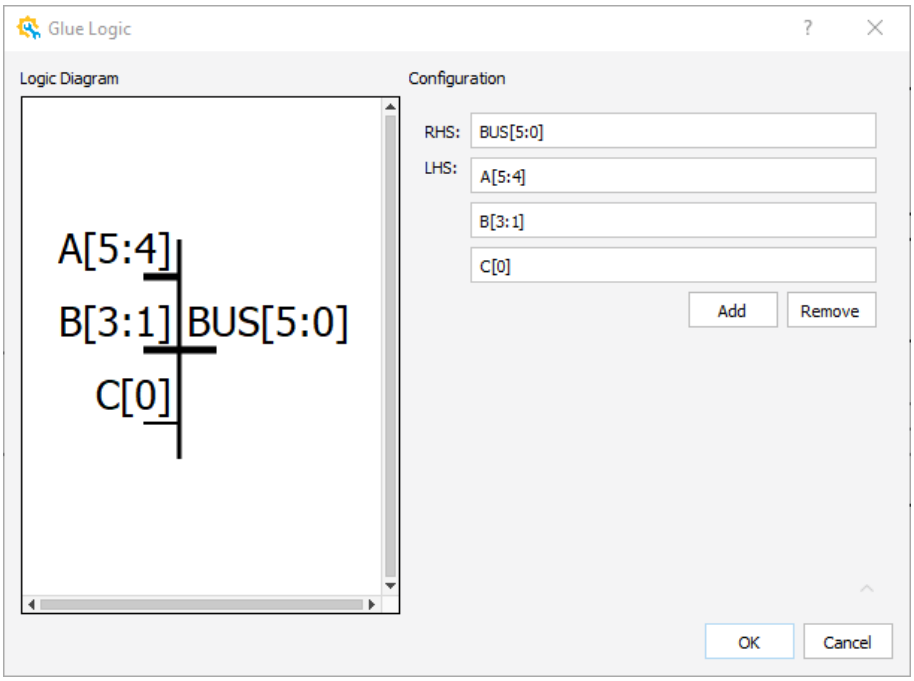


Figure 2.51. Glue Logic for Concat Module

Click the **RHS (right-hand side)** field to change the default right-hand side bus width to a desired one. Click the **LHS (left-hand side)** field to change the default left-hand side bus width to a desired one. Click the Add button to add LHS (Left-hand Side). Click the Remove button to remove LHS (Left-hand Side). You can only add or remove LHS but not RHS. LHS and RHS are thus configured.

2. Click **OK**. The schematic block for the concat module in red appears in the Schematic view (Figure 2.52). you can drag and connect them with the rest of design.

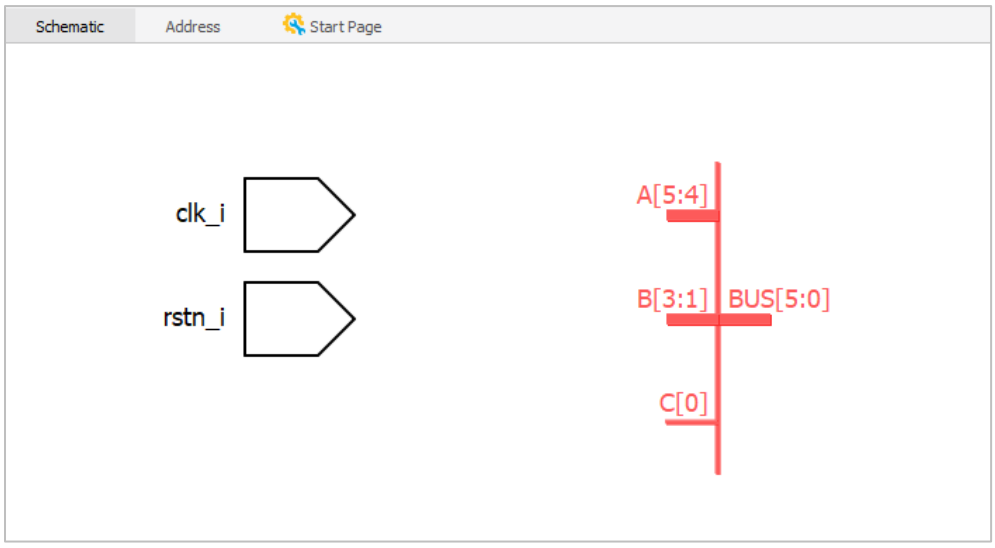


Figure 2.52. Schematic View Shows a Concat Module

2.3.4.2. Equation

1. From the IP Catalog, select the **equation** module. Double-click the equation module, or drag and drop the equation module to the Schematic view. A Glue Logic wizard (Figure 2.53) pops up.

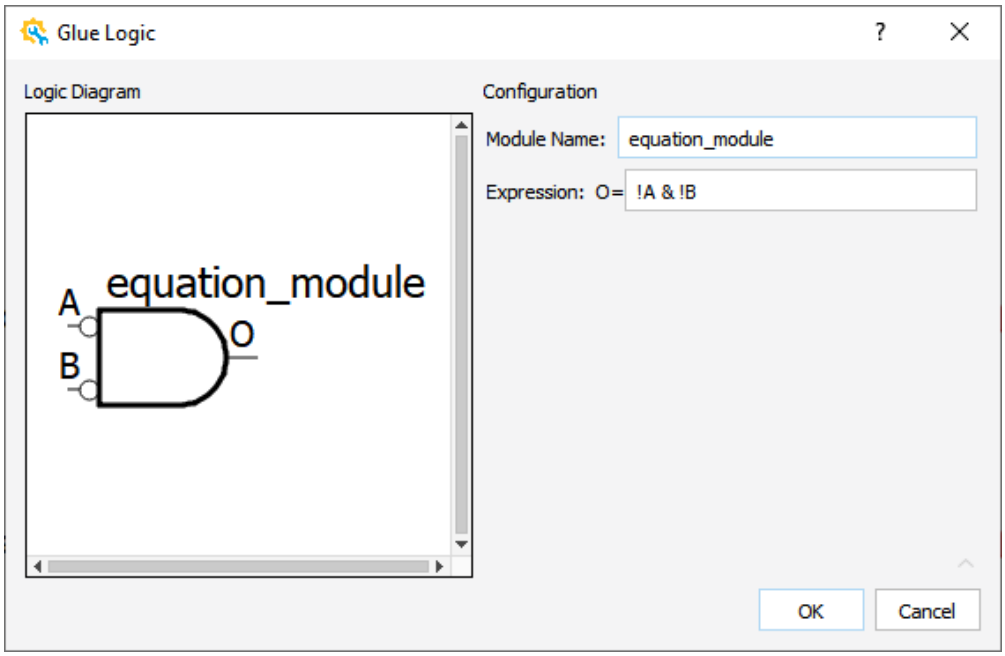


Figure 2.53. Glue Logic Wizard for Equation Module

2. Click the **Module Name** field to change the default value to a desired name. Click the **Expression** field to change the default expression to a desired one. The expression supports and (&), or (|), negation (!), caret (^). The module name and expression are thus configured. Expression supports parentheses, as it complies with Verilog-HDL grammar.
3. Click **OK.** The schematic block for the equation module in red appears in the Schematic view (Figure 2.54).

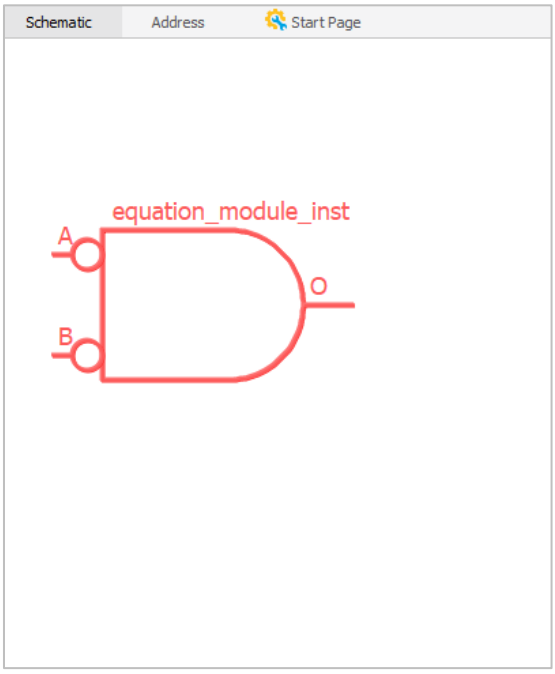


Figure 2.54. Schematic View Shows an Equation Module

2.3.4.3. Invert

1. From the IP Catalog, select the **invert** module. Double-click the invert module or drag and drop invert module to the Schematic view. The schematic block for the invert module in red appears in the Schematic view (Figure 2.55).

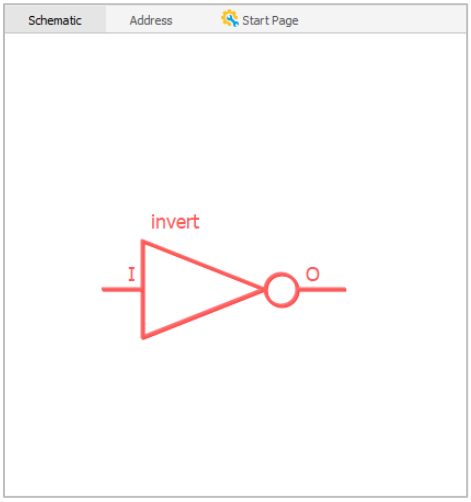


Figure 2.55. Schematic View Shows the Invert Module

2.3.4.4. RTL

1. From the IP Catalog, select the RTL module. Double-click the RTL module or drag and drop the RTL module to the Schematic view. A Glue Logic wizard pops up (Figure 2.56). Glue Logic supports both Verilog HDL and VHDL. You can use the drop-down menu to choose a desired language.

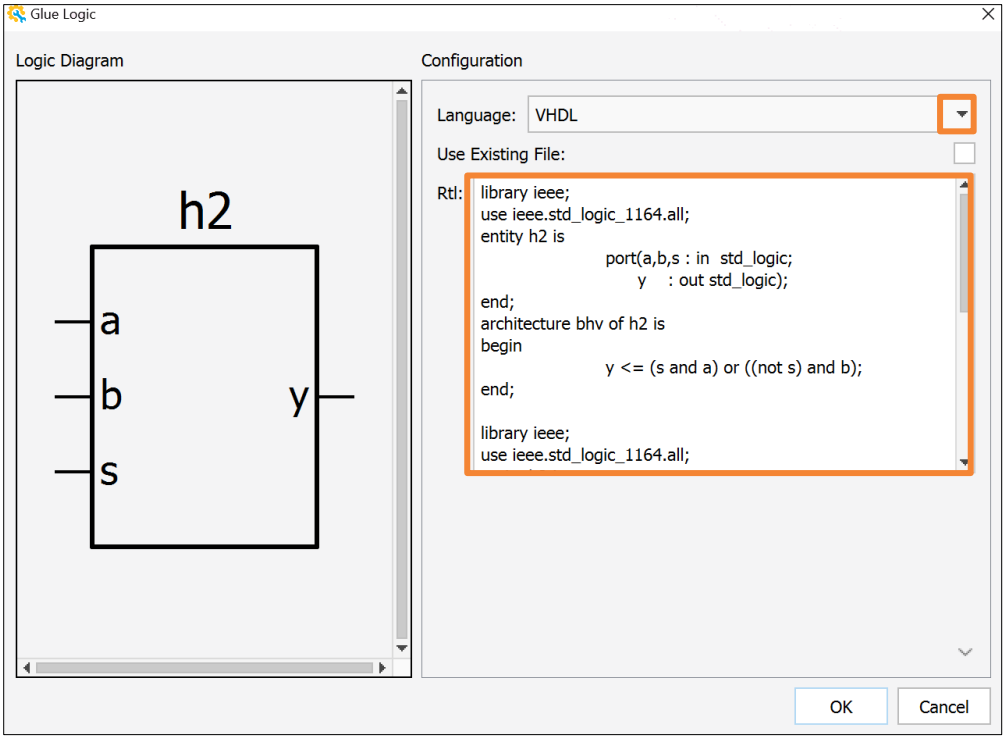


Figure 2.56. Glue Logic Wizard for RTL Module

2. You can edit your own RTL module in the **RTL** area by entering the RTL module function (Figure 2.56).

3. Or, you can use an existing RTL module by checking the **Use Existing File** checkbox. After checking the Use Existing File checkbox (Figure 2.57), browse to find the existing RTL module file path from the **Path** filed. If you use an existing file, RTL references that file from the source. If you do not use an existing file, RTL creates a new file called <*module name*>.v. If **CopyToDesign** is enabled, a copy of the original source is created in the Propel project under <project>/lib/gluelogics/, if not enabled, it is referenced from its current location (default is CopyToDesign).

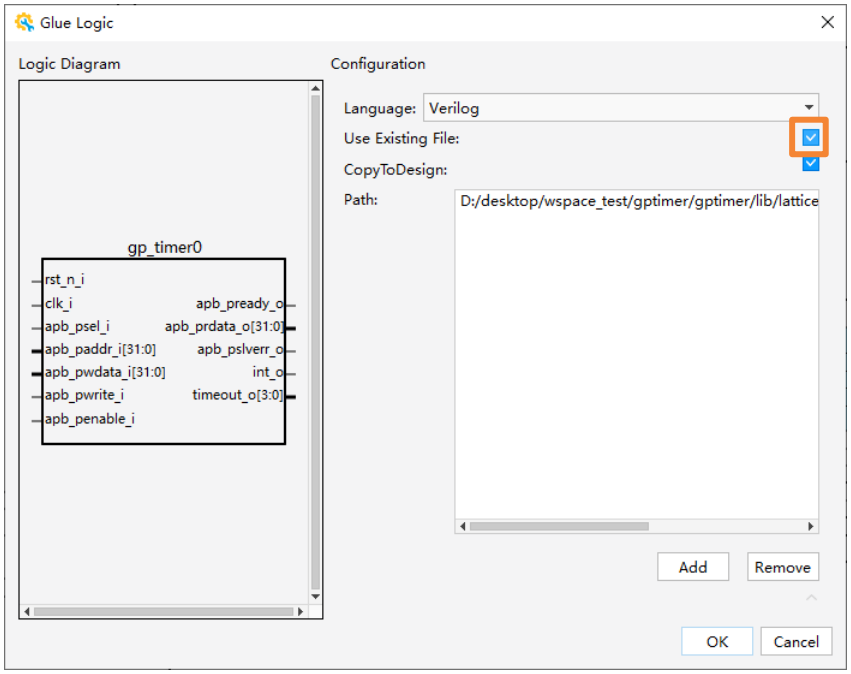


Figure 2.57. Existing RTL Module Configuration

Propel Builder now support **multiple** HDL files in RTL module. You can select multiple files in GUI when *Use Existing File* is checked. (Figure 2.58)

Note: You cannot set VHDL files in the RTL module.

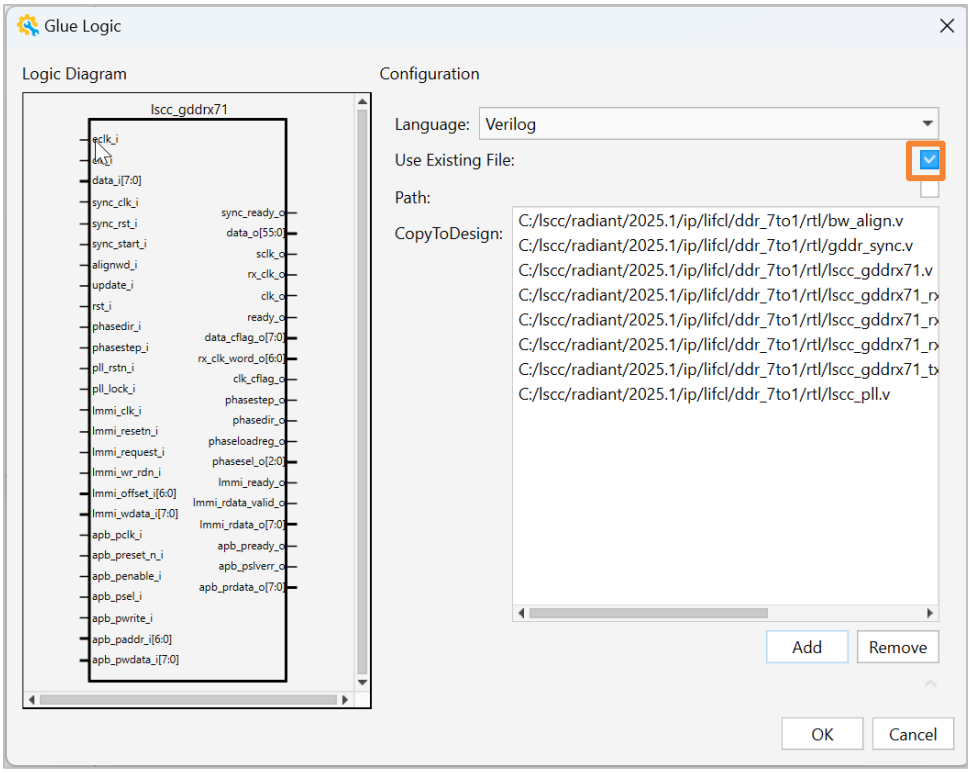


Figure 2.58. Use Existing File

4. Click **OK**. The schematic block for the RTL module in red appears in the Schematic view (Figure 2.59).

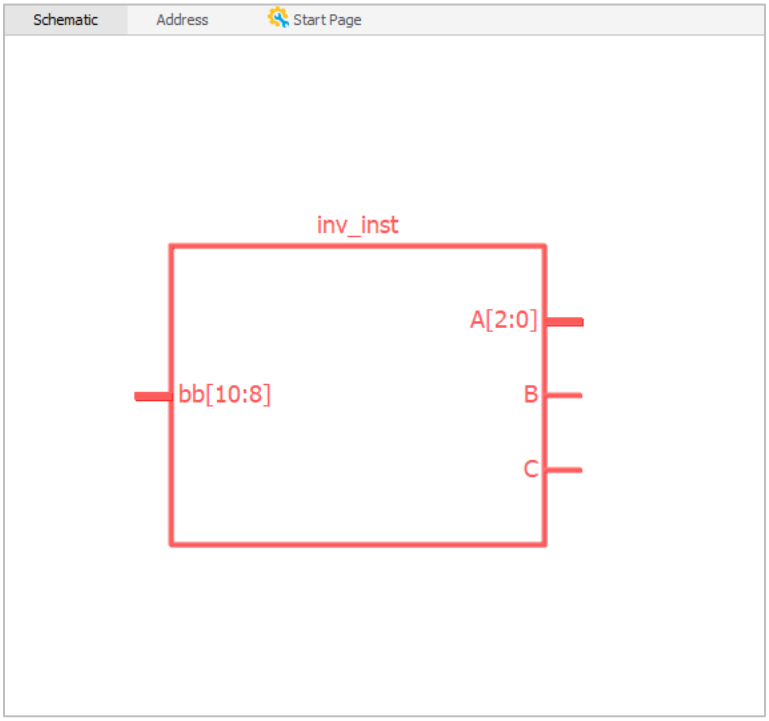


Figure 2.59. Schematic View Shows the Custom RTL Module

2.3.4.5. Split

1. From the IP Catalog, select the **split** module. Double-click the split module or drag and drop the split module to the Schematic view. A Glue Logic wizard (Figure 2.60) pops up.

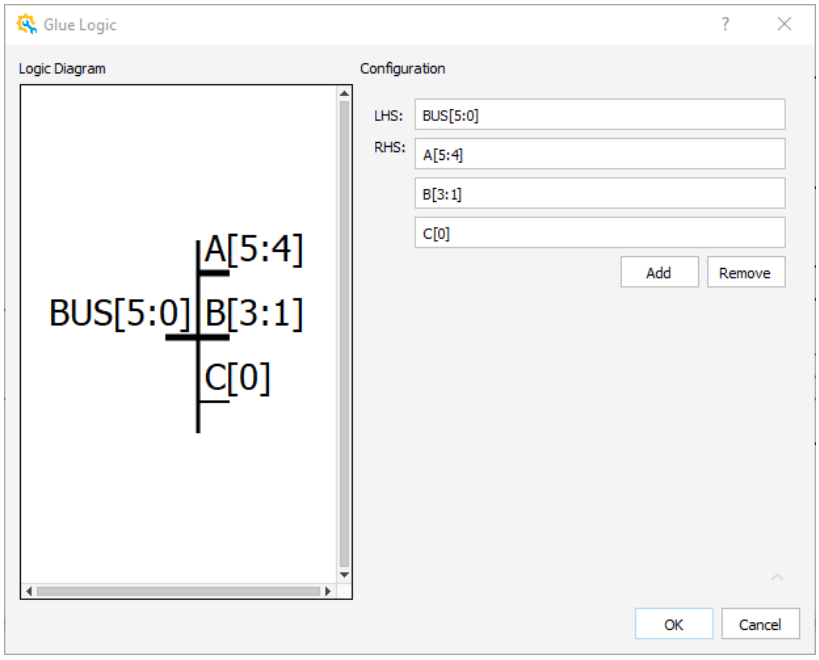


Figure 2.60. Glue Logic Wizard for Split Module

Click **LHS (left-hand side)** field to change the default left-hand side bus widths to a desired one. Click **RHS (right-hand side)** field to change the default right-hand side bit width to a desired one. Click the Add button to add an RHS. Click the Remove button to remove an RHS. You can only add or remove RHS but not LHS. LHS and RHS are thus configured.

2. Click **OK**. The schematic block for the split module in red appears in the Schematic view (Figure 2.61).

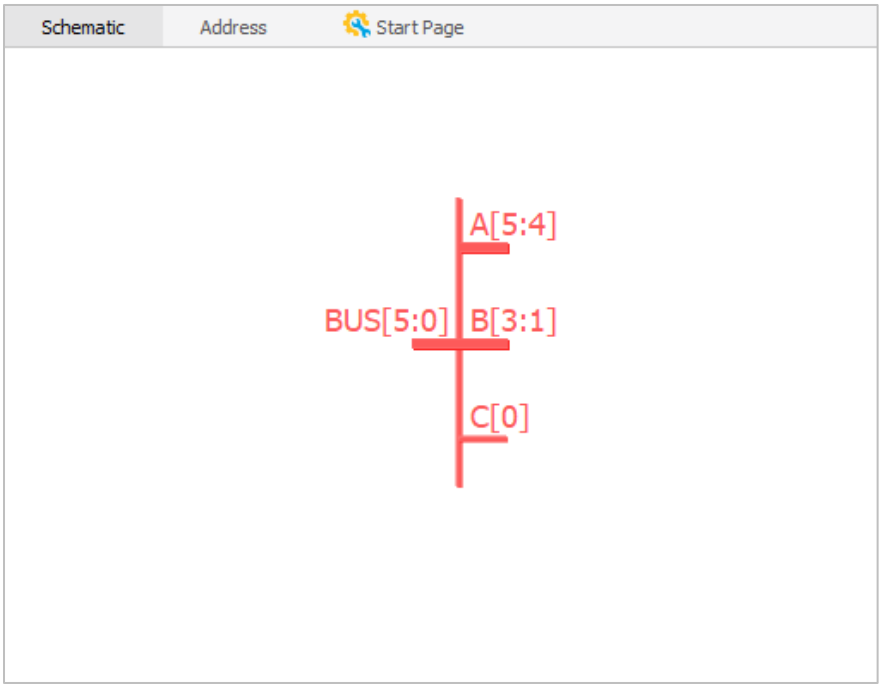


Figure 2.61. Schematic View Shows Split Module

2.3.5. Working with the Schematic View

You can make changes in the Schematic view including automatic layout to clean up the display, moving, resizing, renaming blocks manually, highlighting objects and zooming the display in and out.

2.3.5.1. View Signal List of Block

Click the plus sign of the desired block to see the signals it contains. The plus sign changes to a negative sign and shows the signal list as shown in Figure 2.62. Click the negative sign to close the expanded bus. The schematic returns to the previous form.

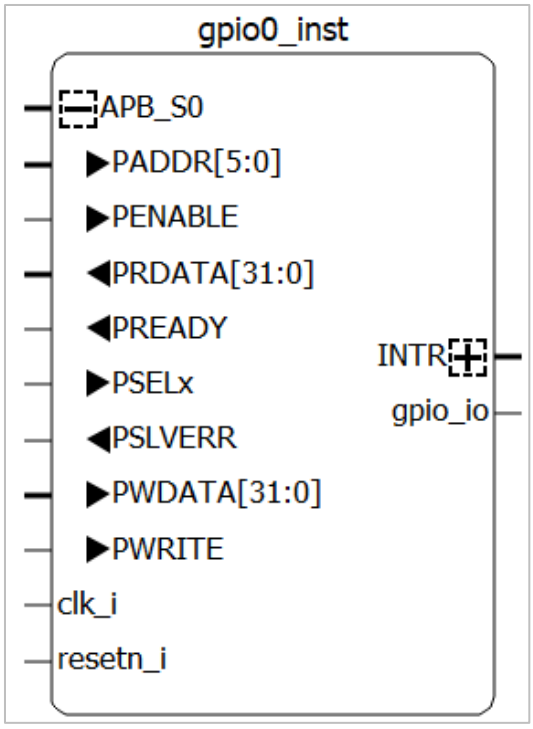


Figure 2.62. Signal List of Modules

2.3.5.2. Select One or More Objects

Select one object or more objects in one of the following ways:

- Click on the object in the Schematic view. The selected object turns to red (Figure 2.63).

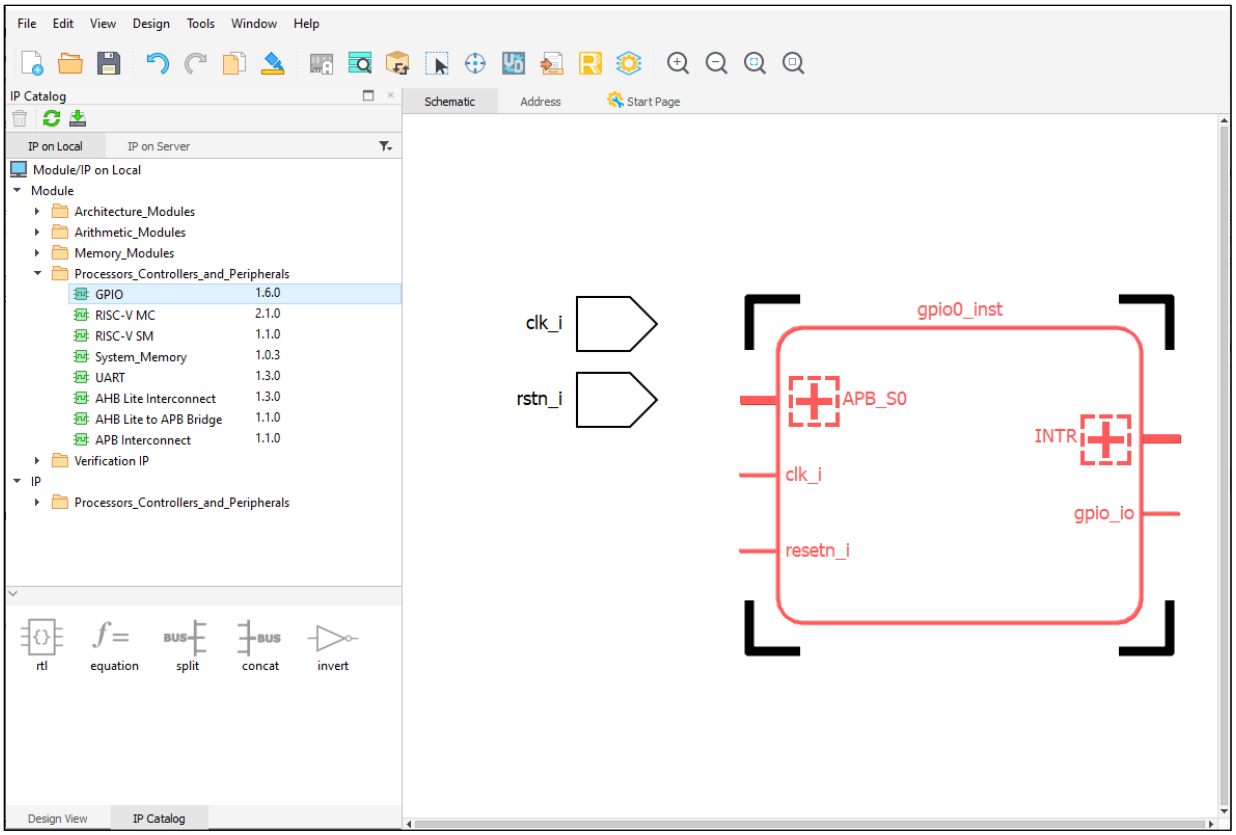


Figure 2.63. Select Object

- Ctrl-click or Shift-click in the Schematic view to select more than one objects.
- Click the Area_select icon from the Propel Builder Toolbar. Click and drag to draw a selection rectangle around the modules and ports in the Schematic view. Click the icon again to turn off the Area_select mode.
- From the Schematic view, right-click and choose Select All or press Ctrl-A to select all the objects.

Note: Ctrl-click or Shift-click on the object in the Schematic view can also de-select the object while leaving the others selected.

2.3.5.3. Re-arrange the Schematic

Propel Builder allows re-arranging the objects in the schematic view. You can re-arrange modules and ports. Drag objects to re-arrange the schematic. Propel Builder has rules for placing objects to adjust the schematic in an organized arrangement.

1. Select the desired modules (one or more modules can be dragged at the same time) or ports (one or more ports can be dragged at the same time).
2. Click on the selected items and drag it/them to the desired location.
3. Release the mouse button.

Note: The selected objects can be moved to a specified location, or near the existing object (as near as the rules allow). Other objects in the schematic can also be moved to accommodate the new location of the selected objects.

To bring selected objects to the center of the Schematic view using the Locate Object mode:

1. Click the **Locate Object** icon from the Propel Builder Toolbar. The background turns to dark gray.
2. Select the object in the List view of the Design View. The selected object is in the center of the Schematic View (Figure 2.64).

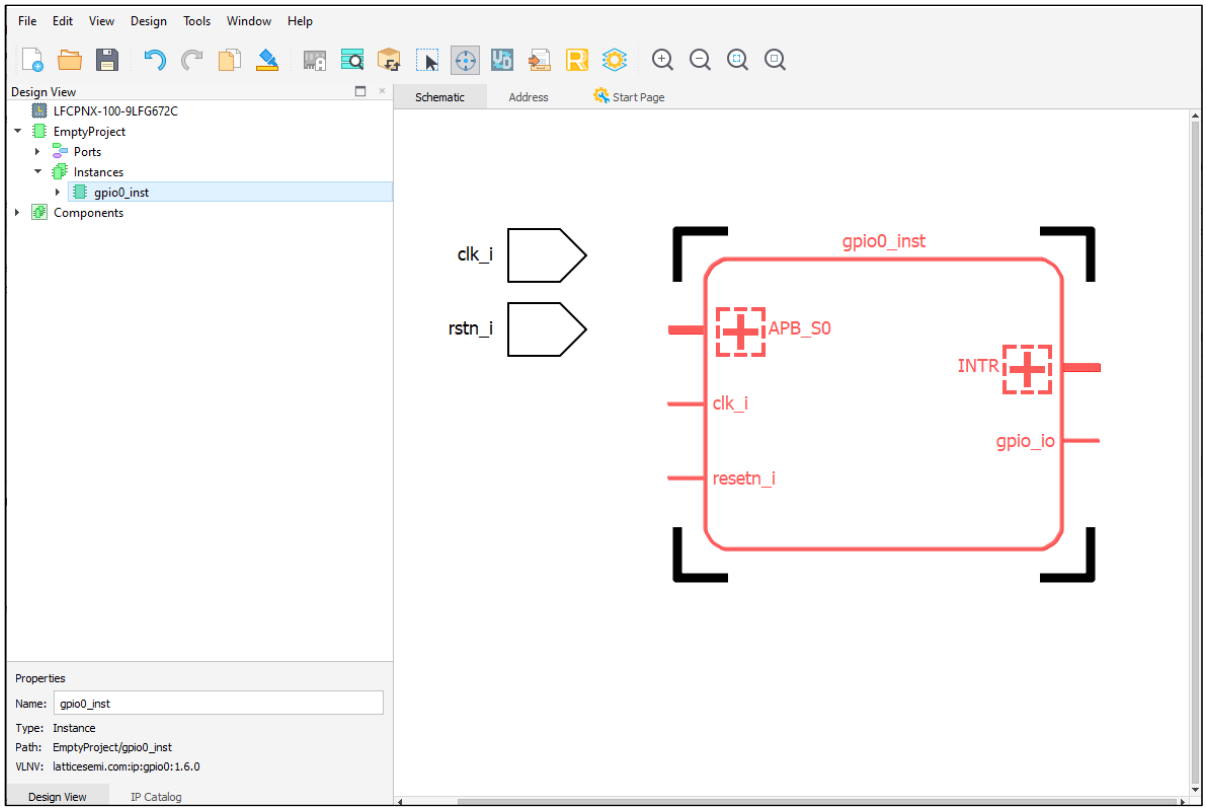


Figure 2.64. Locate Objects

To automatically simplify the layout:

1. Right-click anywhere in the Schematic view and choose **Relayout**.

2.3.5.4. Duplicate a Module

Select the desired module and click **Clone**  . Or right-click on the module and choose **Clone**  . A copy of the schematic block appears with a new instance name (Figure 2.65). It creates a separate copy of the original module using all the same settings and is essentially its own component which can be modified and managed separately.

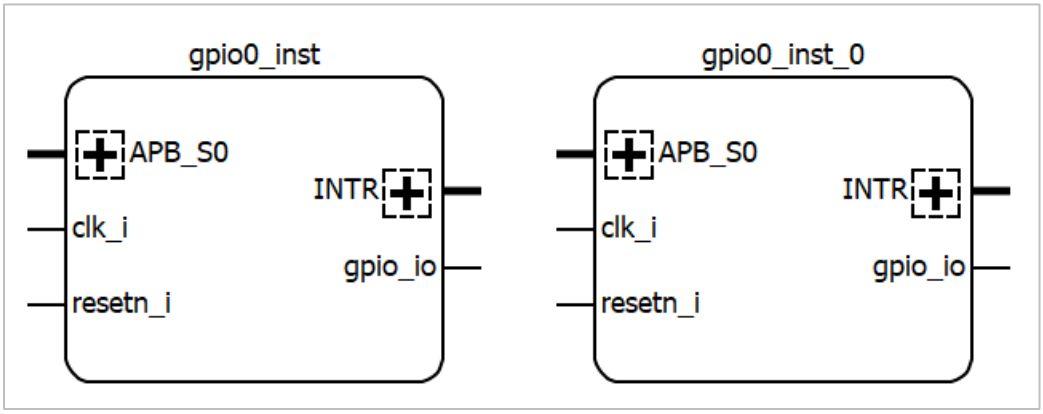


Figure 2.65. Duplicate a Module

2.3.5.5. Restore a Deleted Module

1. In the List view of the Design View (Figure 2.66), go to the Components folder. The deleted module can still be found in the List view in plain text. Those not deleted are shown in bold-faced text.

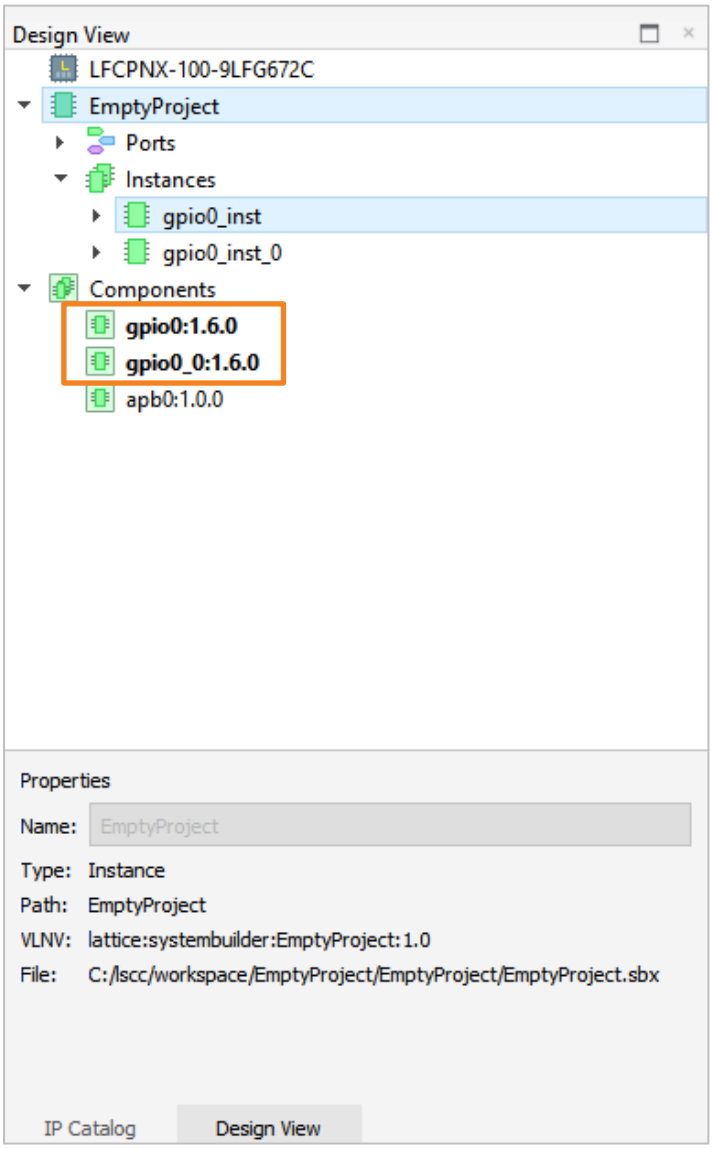


Figure 2.66. Design View

2. Right-click on the component you want to restore, and choose **Instantiate**. The Define Instance dialog box (Figure 2.67) open.

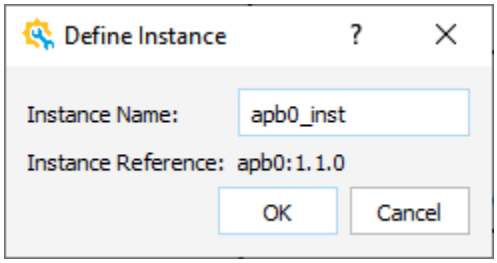


Figure 2.67. Define Instance Dialog Box

3. Enter a name for the new instance.
4. Click **OK**. The module appears in the Schematic view and the List view of Design Info, and the component name is bold-faced.

2.3.5.6. Reconfigure a Module

1. Double-click the module, or right-click the module you want to reconfigure. Choose **Reconfig**. The Module/IP Block wizard (Figure 2.68) opens.

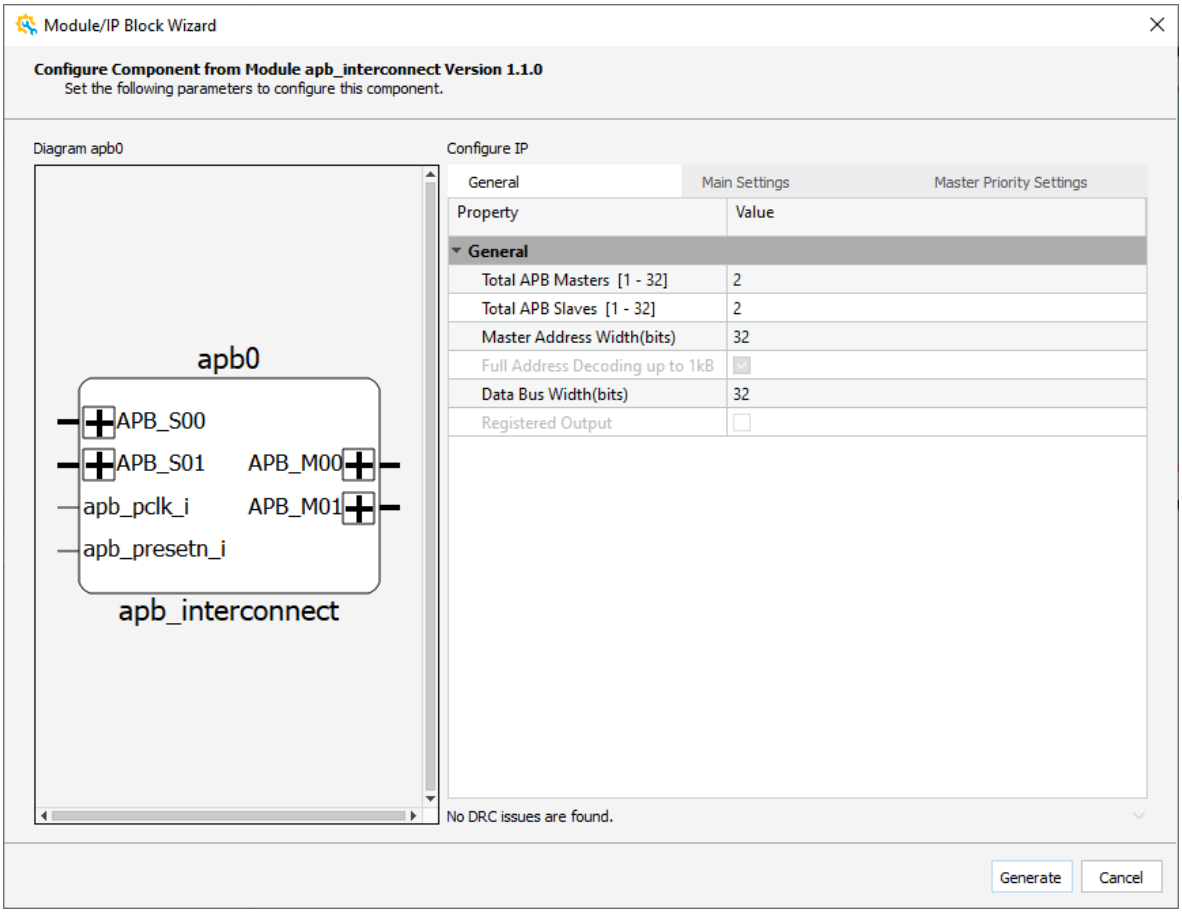


Figure 2.68. Module/IP Block Wizard – Configure Component

2. Configure component (including General property, Main Settings and Mater Priority Settings) at Configure IP table in the Module/IP Block Wizard. Click **Generate** to generate the module as usual. The schematic block for the module changes to match the new configuration.

2.3.5.7. Resize Module Blocks

1. Select the desired module block. The block is highlighted in red with black corners (Figure 2.69).

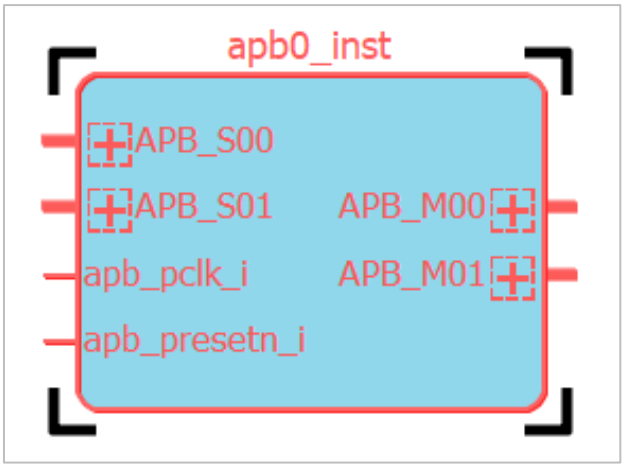


Figure 2.69. Select Module

2. Click and drag one of the corners to change the size and to shape of the block.
3. Release the mouse button. All the other objects move to make room for this block.

   Note: Right-click the module block and choose **Unresize Instance** to restore the size of the module block.

2.3.5.8. Methods to Zoom

There are a variety of methods to zoom within the Schematic view including toolbar commands and dragging in the Schematic view.

The following commands are available from the Propel Builder Toolbar.

Zoom In (Ctrl++) — enlarges the view of the entire layout.

Zoom Out (Ctrl+-) — reduces the view of the entire layout.

Zoom Fit — reduces or enlarges the entire layout so that it fits inside the window.

Zoom To — enlarges the size of one or more selected objects on the layout and fills the window with selection.

Note: The mouse wheel provides a finer zoom control by rolling the mouse wheel forward to zoom in and backward to zoom out while pressing the Ctrl key.

- To zoom by holding the mouse button and dragging.
- To zoom to fit the window, drag up and to the left. The image adjusts to fill the window.
- To zoom out, drag up and to the right. The dragging distance determines the amount of zoom. The image is reduced and centered in the window.
- To zoom in, drag down and to the left. The dragging distance determines the amount of zoom. The image is enlarged and centered in the window.
- To zoom in in a specific area, start at the upper-left corner of the area and drag to the lower-right corner of the area. The area that dragging across is adjusted to fill the window.

Note: Make sure that the **Area_select** icon is not selected in the Toolbar. If you need to use Area_select and zoom by dragging frequently, choose **Tools** > **Options** from Propel Builder menu bar. The Options Dialog opens (Figure 2.70). Select **Use right mouse button for zooming actions** and click **OK**. Then you can select an instance using the left mouse button, zoom in or zoom out using the right mouse button, and the **Area_select** icon disappears from the Propel Builder Toolbar.

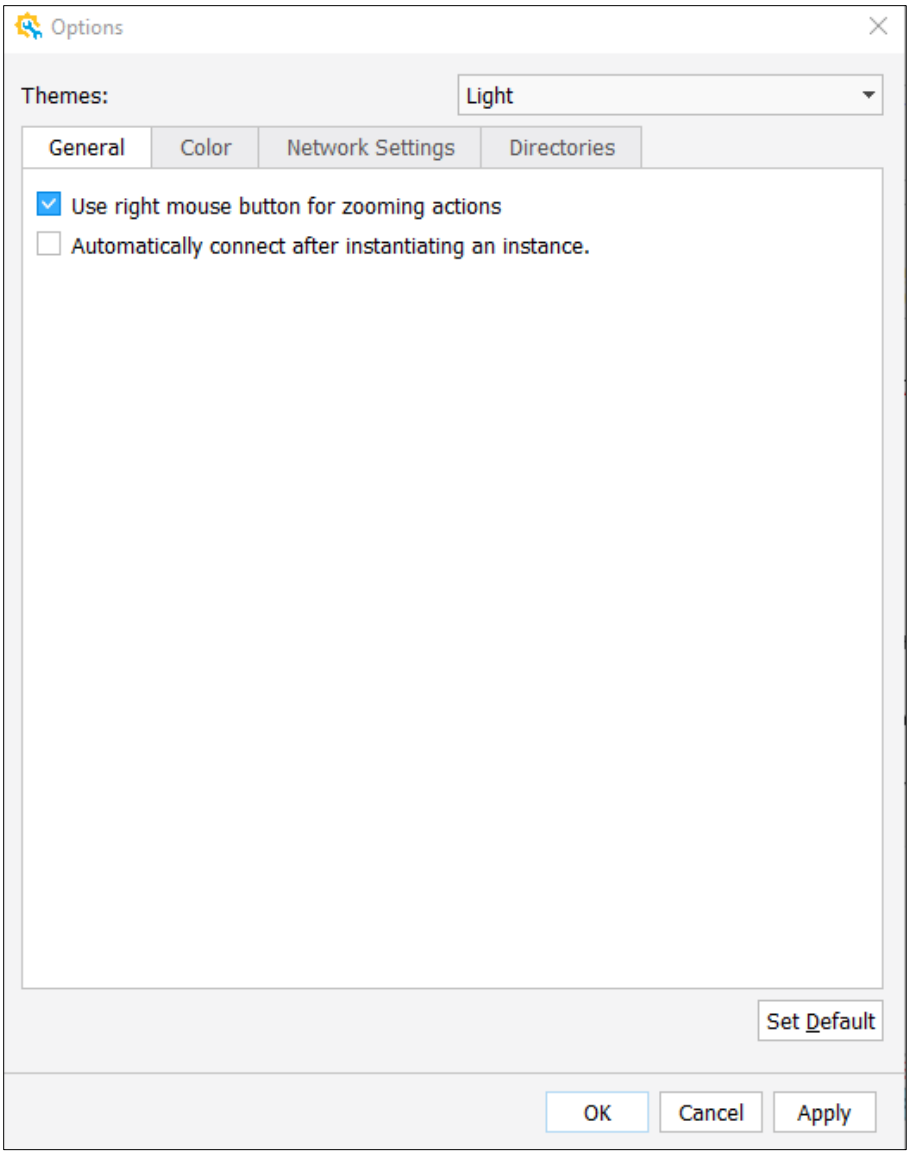


Figure 2.70. Options Dialog

2.3.5.9. Group

In the Schematic View, you can group the component as needed. Group does not introduce any RTL level change.

- Support creating group with selected instances. Click on the instances you want to group, and right-click on them, choose **Create Group** (Figure 2.71)**.** You can deselect/select the instances in the dialog. (Figure 2.72)

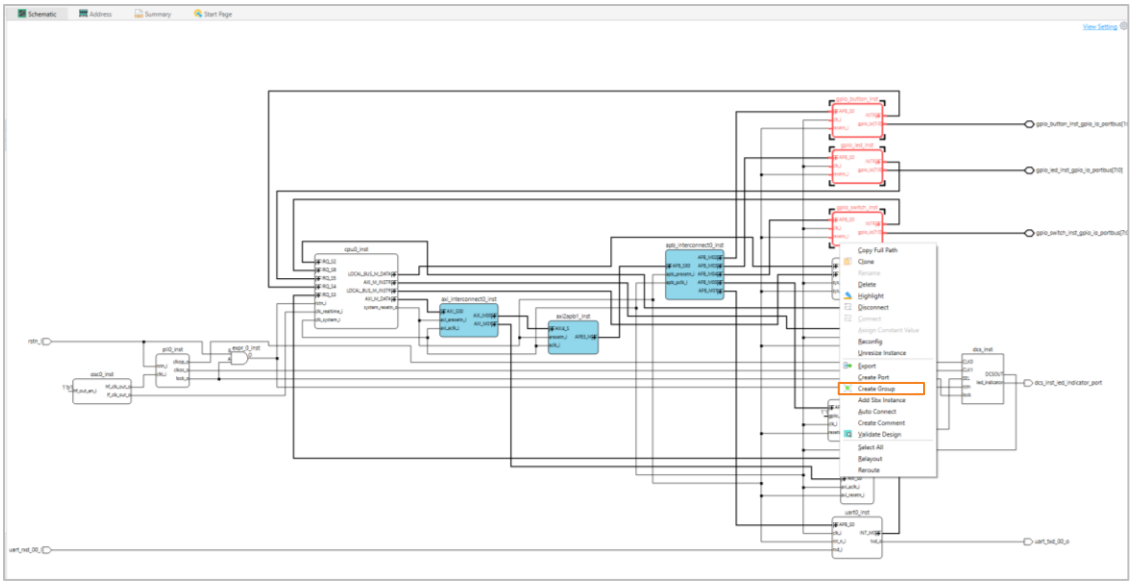


Figure 2.71. Create Group Right-Click Menu

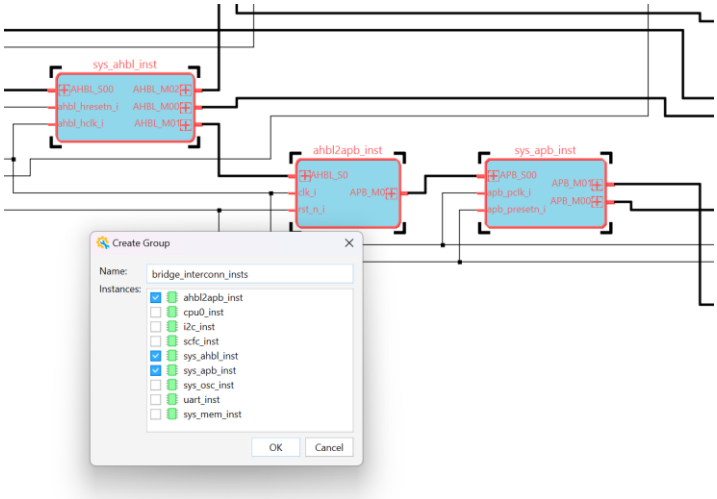


Figure 2.72. Create Group Dialog: Select/Deselect

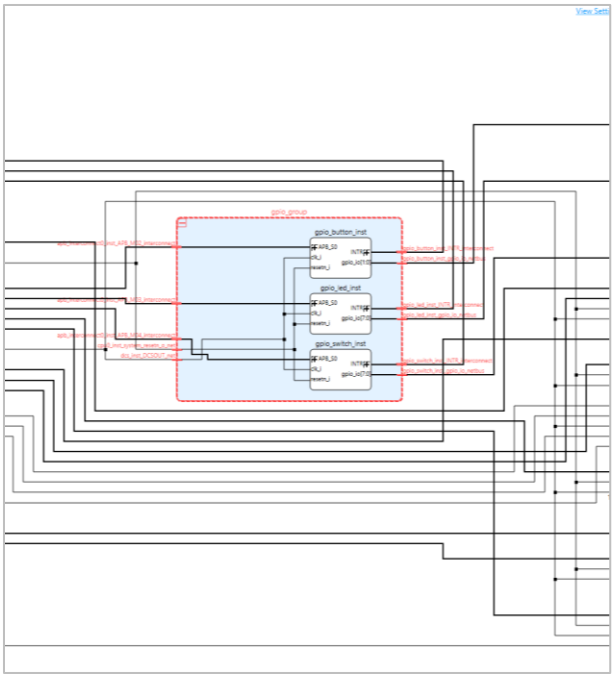


Figure 2.73. Create Group Effect

- Support dragging in/out instance from group by mouse.

  To ungroup, click on the component (gpio_button_inst), drag it outside the group area and then release the mouse over the blank space (Figure 2.74).

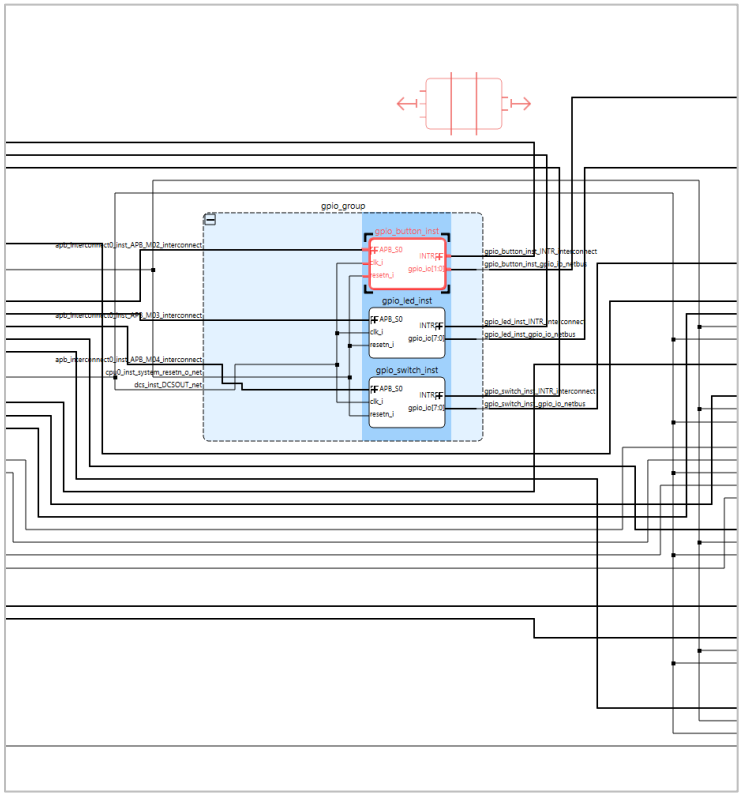


Figure 2.74. Ungroup

- Support creating empty groups.
- Only support soc project, group function will be hidden in the verification project view.

2.3.5.10. Move a Schematic Image

You can move a schematic image within the Schematic view by panning and scrolling:

- To pan the image: Hold down the **Ctrl** key and the left mouse button while dragging the image.
- To scroll vertically: Rotate the mouse wheel. Or click in the vertical scroll bar.
- To scroll horizontally: Hold down the Shift key and rotate the mouse wheel. Or click in the horizontal scroll bar.

2.3.5.11. Show the Connectivity of a Module

Right-click the module and choose **Show Connectivity**. All nets connected to the module, all pins and ports connected to the nets are highlighted (Figure 2.75).

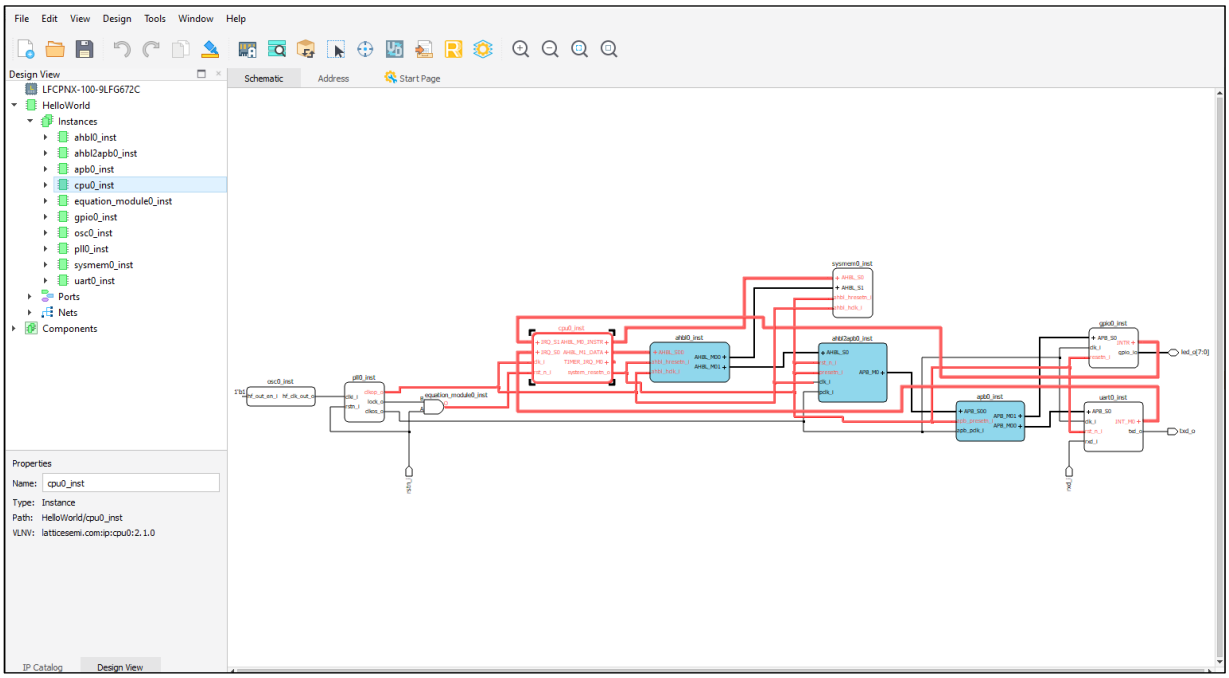


Figure 2.75. Show Connectivity of the Module

2.3.5.12. Highlight an Object

Select an object and click **Highlight** , or, right-click the object and choose **Highlight** . The object is highlighted in blue (Figure 2.76). Click **Highlight** again. You can remove highlighting. In the Tools section, you can change the highlight color.

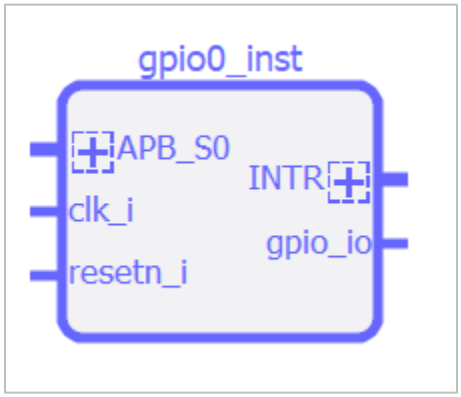


Figure 2.76. Highlight an Object

2.3.5.13. Change the Name of an Object

1. Select the object from List view of the Design View. Information of the selected object is shown in the **Properties** area (Figure 2.77).

Figure 2.77. Object Properties

2. Change the name and click **Enter.** The name changes in the Schematic view and List view of Design Info.

2.3.5.14. Print a Schematic

1. Choose **File** > **Print Preview**. The Print Preview window (Figure 2.78) opens.

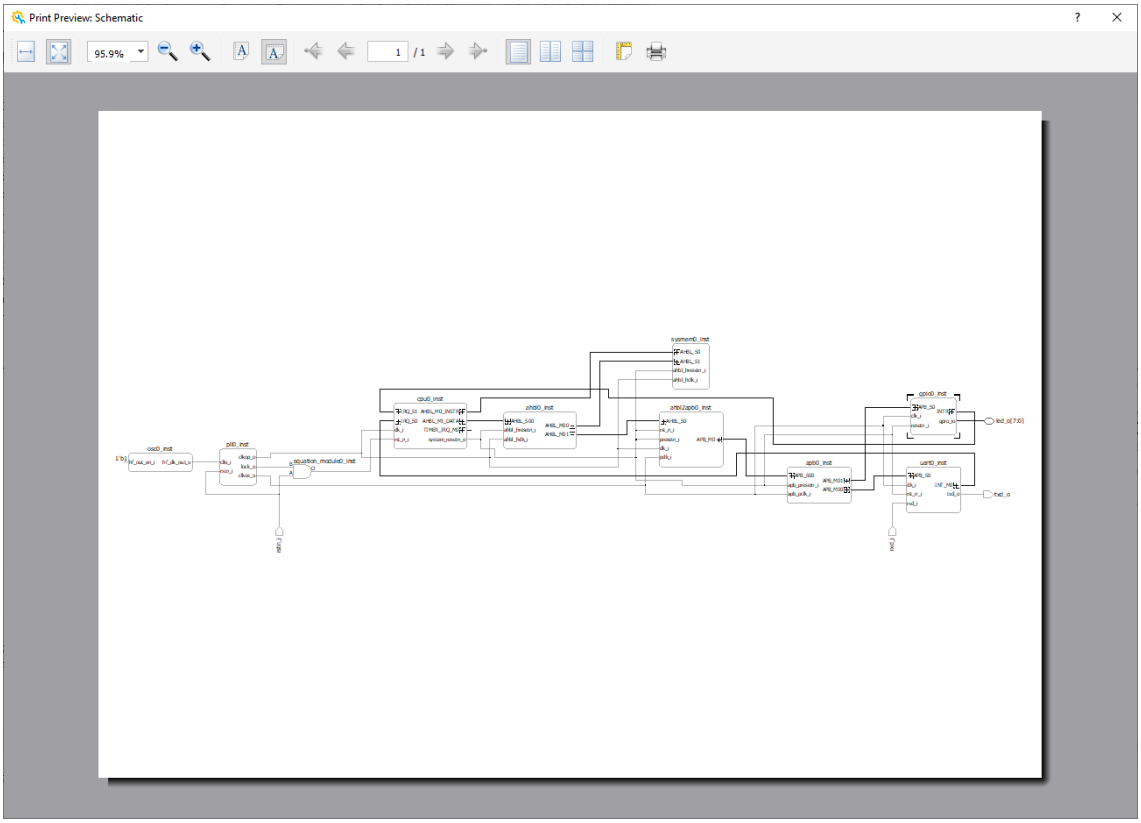


Figure 2.78. Print Preview

2. Expand the Print Preview window to the desired size.
3. Click the **Page Setup** button and adjust the paper size and margins, if necessary.

4. Click the **Print** button .
5. Adjust the printer settings, if necessary. Click **Print**.

2.3.6. Connecting Modules

You can connect the pins of modules to other modules or to top-level ports by dragging a line between them or by selecting connection points, or by assigning a constant value to an input pin or bus. Propel Builder does not allow obvious inappropriate connections, such as a connection between two output pins or mismatched buses.

2.3.6.1. Connect Modules by Drawing

1. Move the cursor to a pin or port. The cursor changes to a pencil icon . Click and hold while dragging to another pin, port, or net. An allowed pin or port shows a green checkmark when you hover over it (Figure 2.79). An allowed net becomes bold when you hover over it (Figure 2.80).

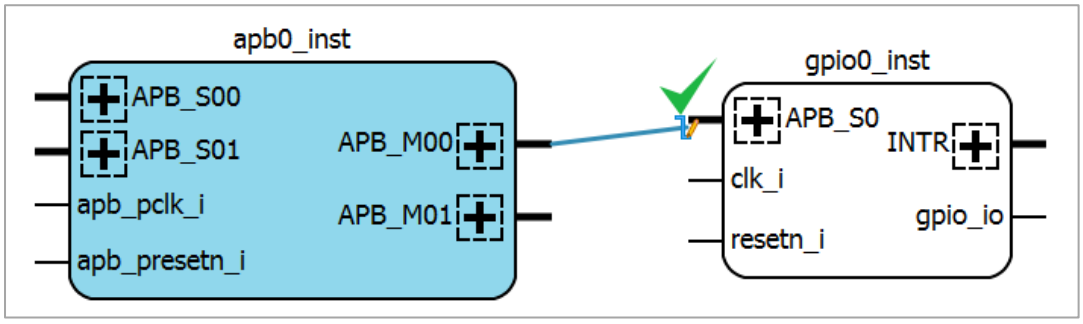


Figure 2.79. Draw a Pin or a Port

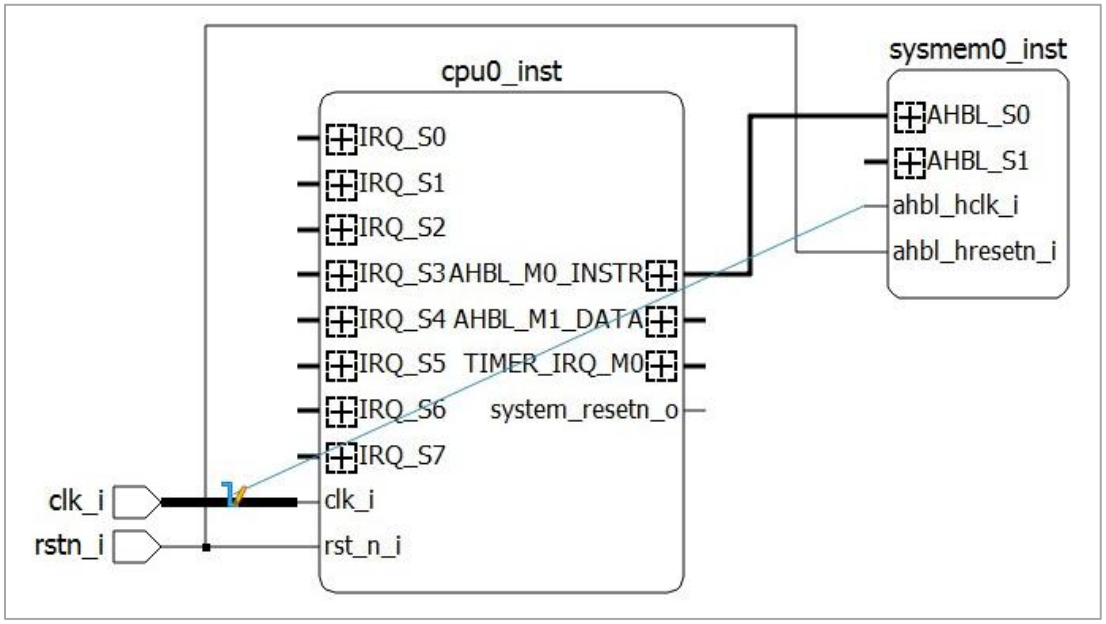


Figure 2.80. Draw Nets

2. Click on the pin, port, or net that you want to connect to. If the connection is allowed, a line appears connecting the two objects. Propel Builder creates a path around other objects.
3. You can connect multiple ports once. When more than one port is selected (Figure 2.81), click **connect** from the right-click menu to implement it.

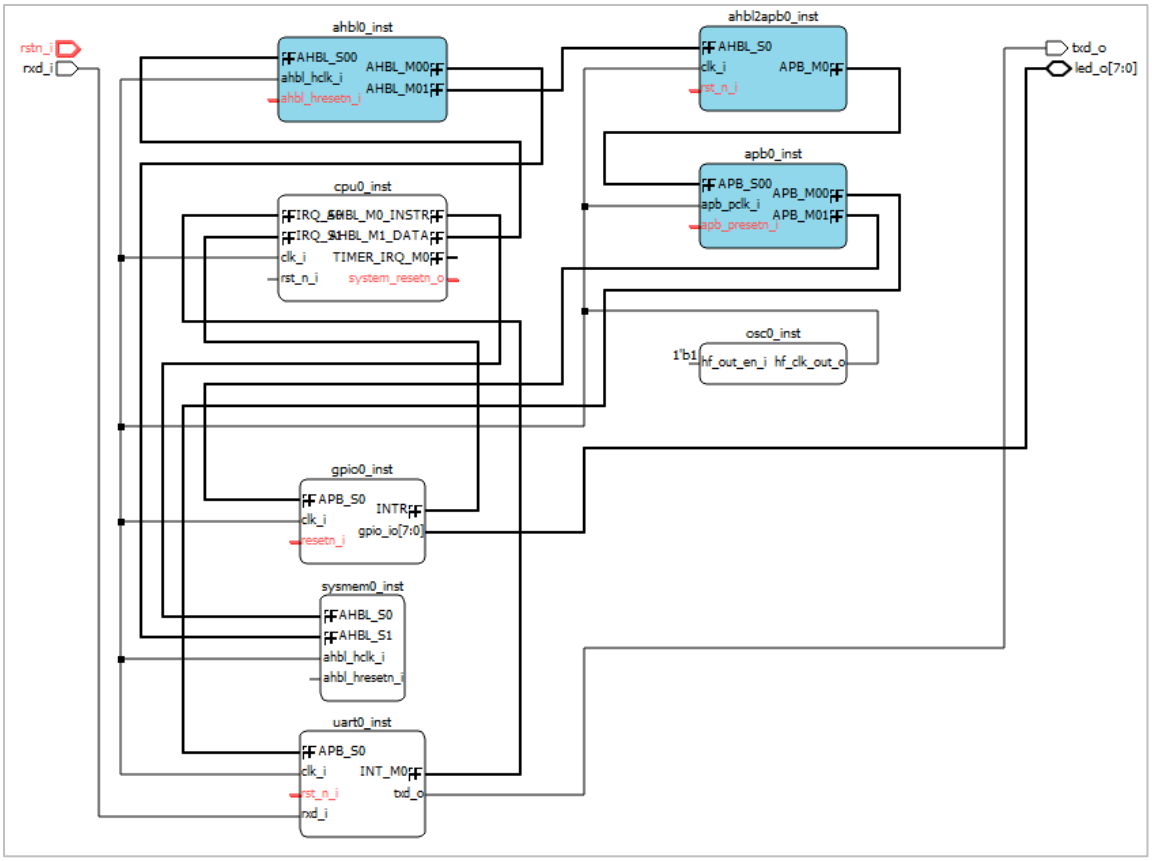


Figure 2.81. Select More than One Ports

4. When the connection is completed, right-click to leave the drawing mode.
   Pin/Net/PinIface/NetIface display filter:
5. Click the  icon on Schematic view, the filter shows. By clicking it again, filter hides.

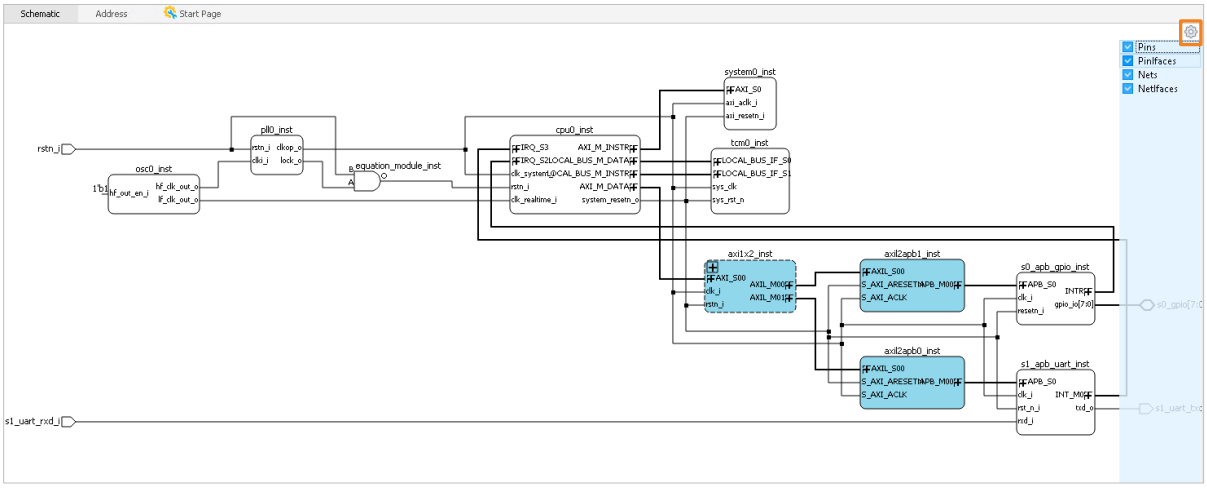


Figure 2.82. Pin/Net/PinIface/NetIface Display Filter

When Pin/PinIface is hidden, the connection is hidden. The hidden status is not to be saved in design. It is only used to view design easily.

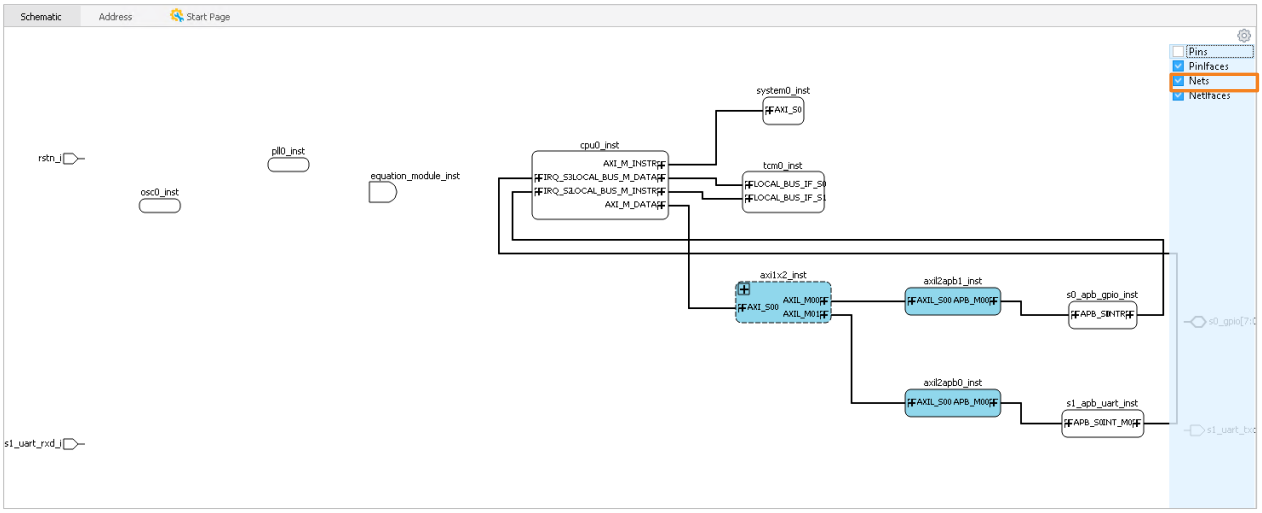


Figure 2.83. Pin/PinIface is Hidden

6. Individual ports are allowed to connect within bus interface (Figure 2.84 and Figure 2.85).

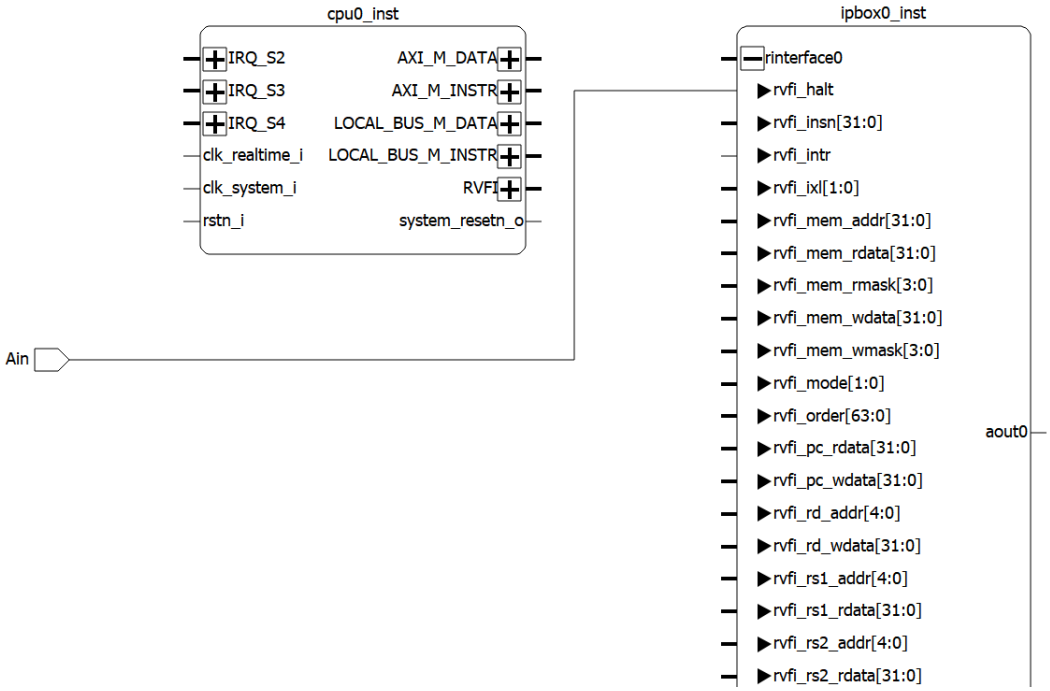


Figure 2.84. Individual Port Connection within Bus Interface (1)

- If the bus interface is already connected, individual port connection overrides the existing connection inside the bus interface.
- If the individual port connection exists, bus connection is still allowed for other signals.

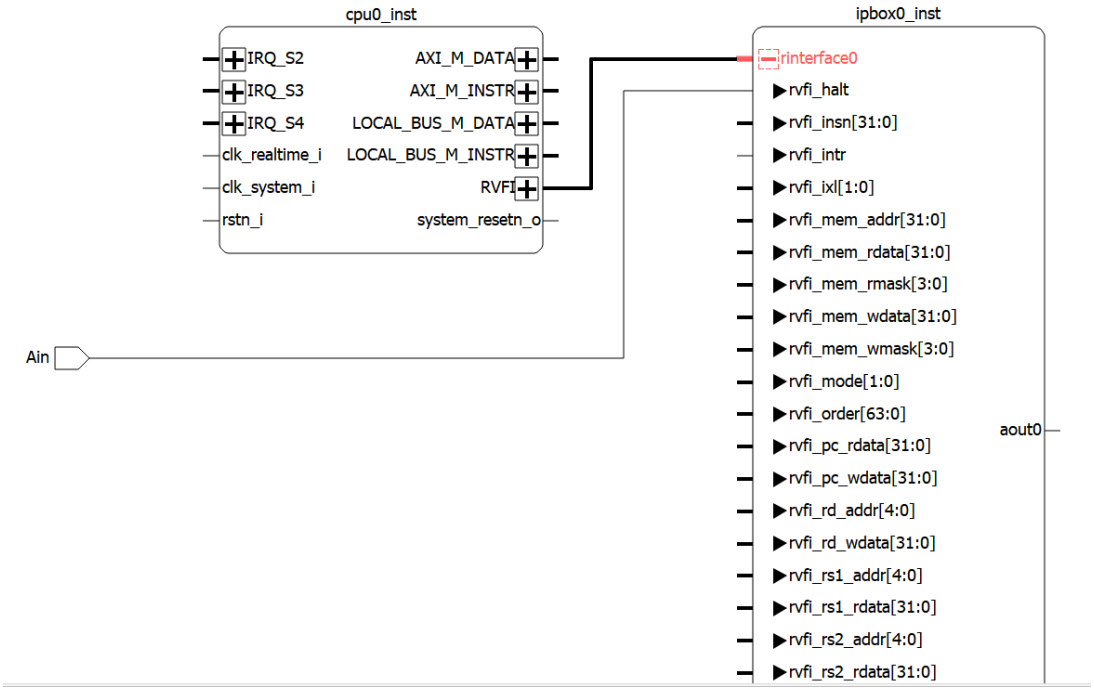


Figure 2.85. Individual Port Connection within Bus Interface (2)

Warning message are issued on individual port connection when doing the connection or generating the SoC design.

The following bus interface are supported for this feature:

- flash_ext
- gpio_ext
- Uart
- i2c_ext/i2c_int
- JTAG
- SPI,Interrupt
- Other customer-defined interfaces

Standard interfaces connection are still not allowed to ensure connection integrity.

- AMBA
- ICC
- CFU
- LPDDR4
- local bus
- local memory interface

2.3.6.2. Connect Modules by Selecting Points

1. Select the pins, ports, and nets you want to connect, using Ctrl + Left click.
2. Right-click one of the selected objects. Choose **Connect** from the menu. The objects are connected.

2.3.6.3. Connect Pins by Auto Connect

1. Right-click on Schematic view and choose **Auto Connect** (Figure 2.86). The Connect Ports dialog appears (Figure 2.87).

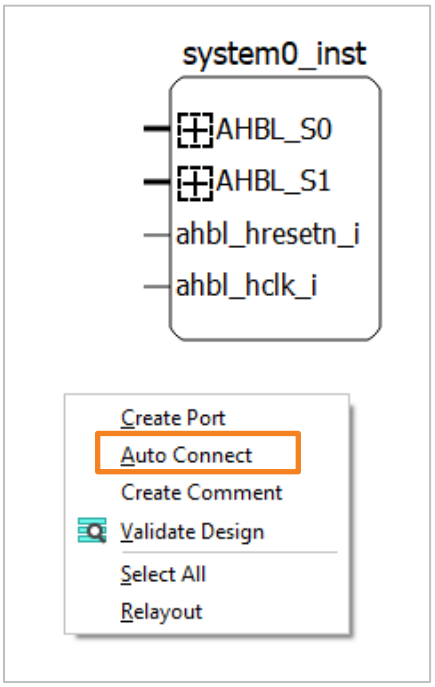


Figure 2.86. Action Menu of Right-clicking on a Blank

2. By default, **Auto Connect** selects all ports. You can also deselect the interface/clock/rest pins that you do not want to auto-connect (Figure 2.87).
3. Auto Connect can only connect one of its suggested sources at a time. For example, for PLL connections, you can only select clkos_o or clkop_o to connect to multiple destination ports, but you cannot make those connections at the same time.

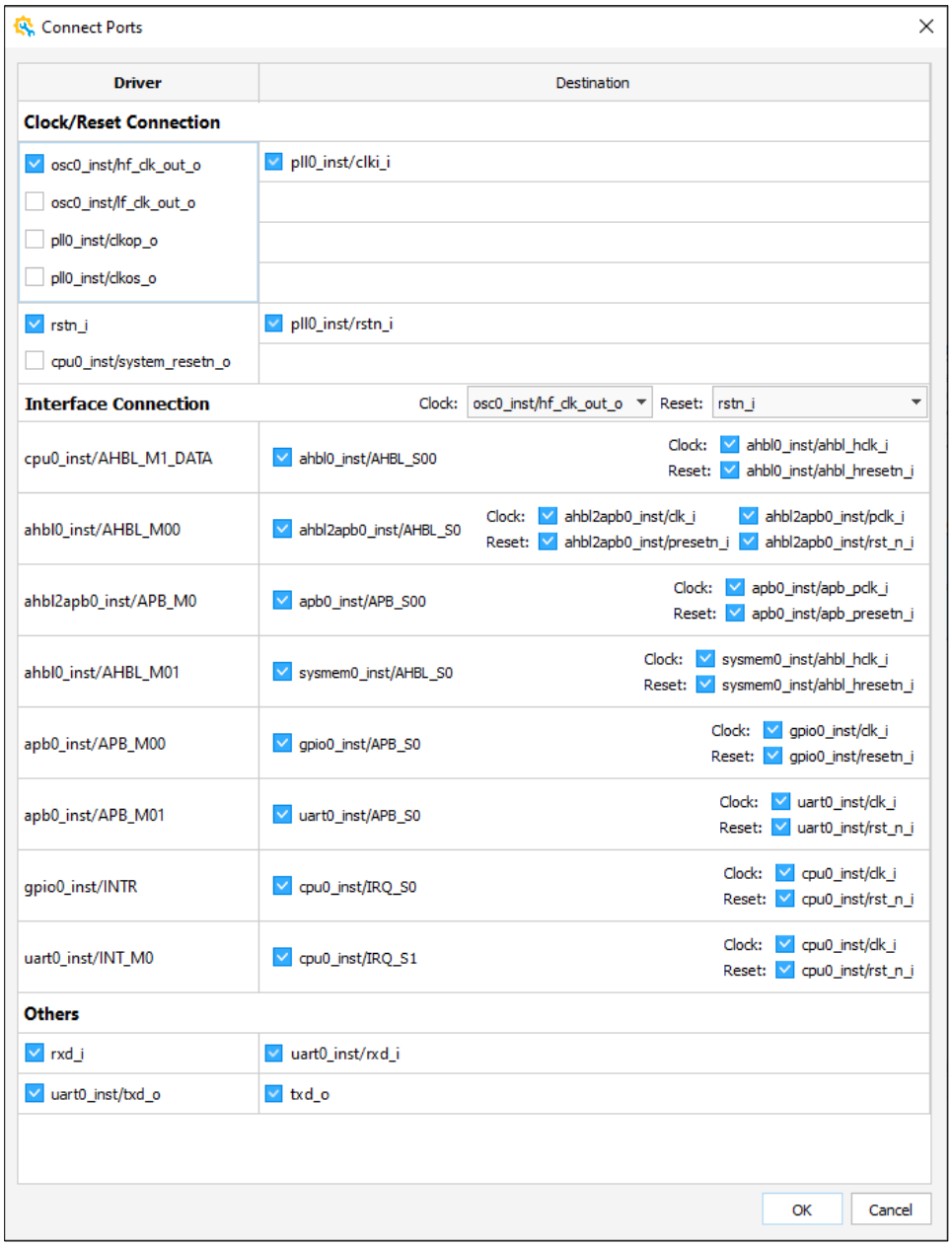


Figure 2.87. Action Menu of Connecting Ports

Auto Connect Rules

Auto Connect can initialize three types of connections: Clock/Reset connection, Interface connection, and other connection.

A. Clock/Reset Connection

For clock/reset connection, you can choose only one clock port and one reset port in the Driver selection area. In the example below, you can choose only one clock port from osc0_inst.hf_clk_out_o, pll0_inst.clkop_o, or pll0_inst.clkos_o, and one reset port from cpu0_inst.system_reset_n_0 or rstn_i (Figure 2.88).

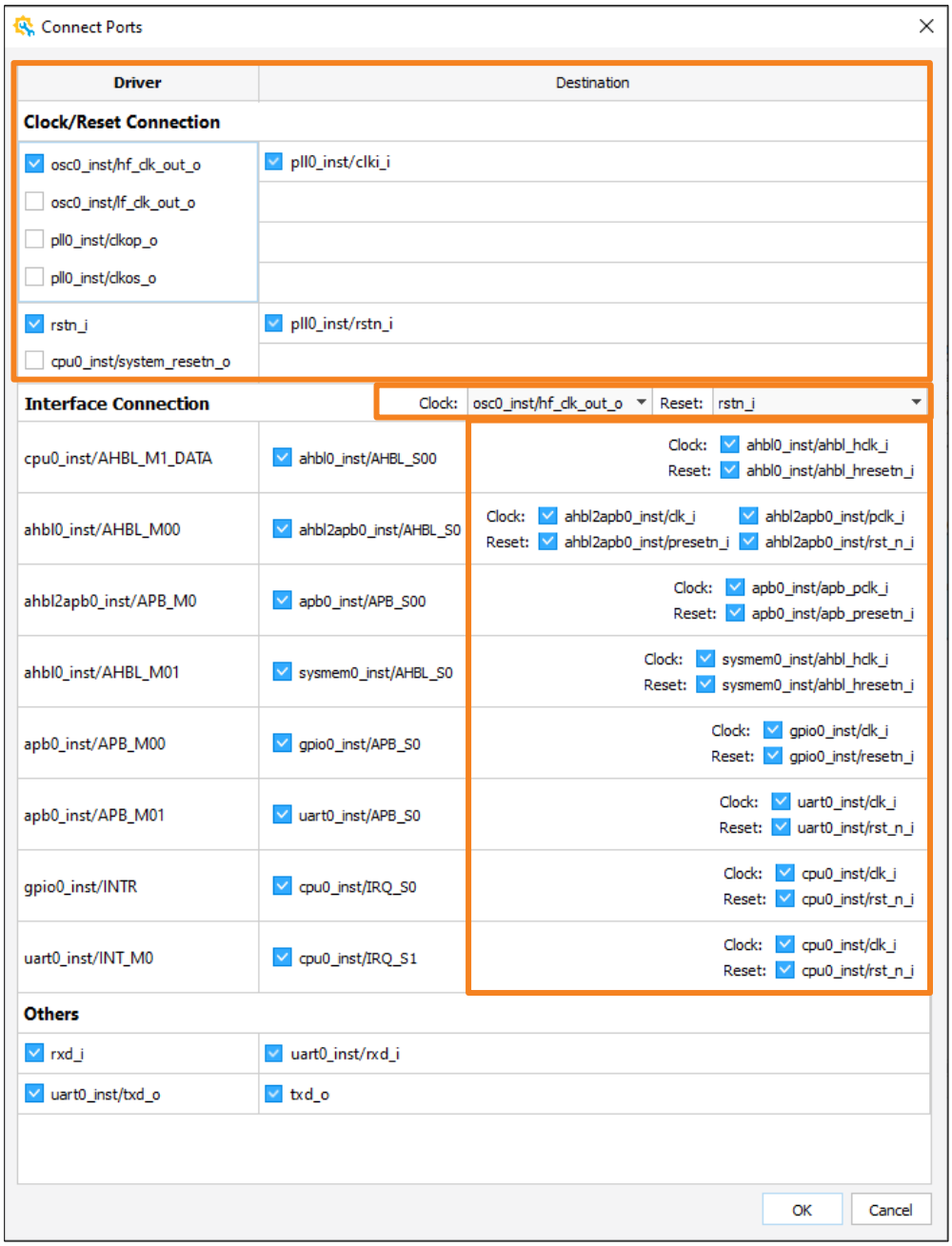


Figure 2.88. Select One Clock/Reset Port

Following are rules of how clock/reset driver port auto connects to the destination:

a. Whether or not the SoC project contains a CPU instance.

- If the SoC project contains a CPU instance, and the CPU instance has an output clock/reset port, such as cpu0_inst.system_resetn_o (Figure 2.89), the clock/reset of other instances are thus connected to the clock/reset port of the CPU Instance (Figure 2.89).

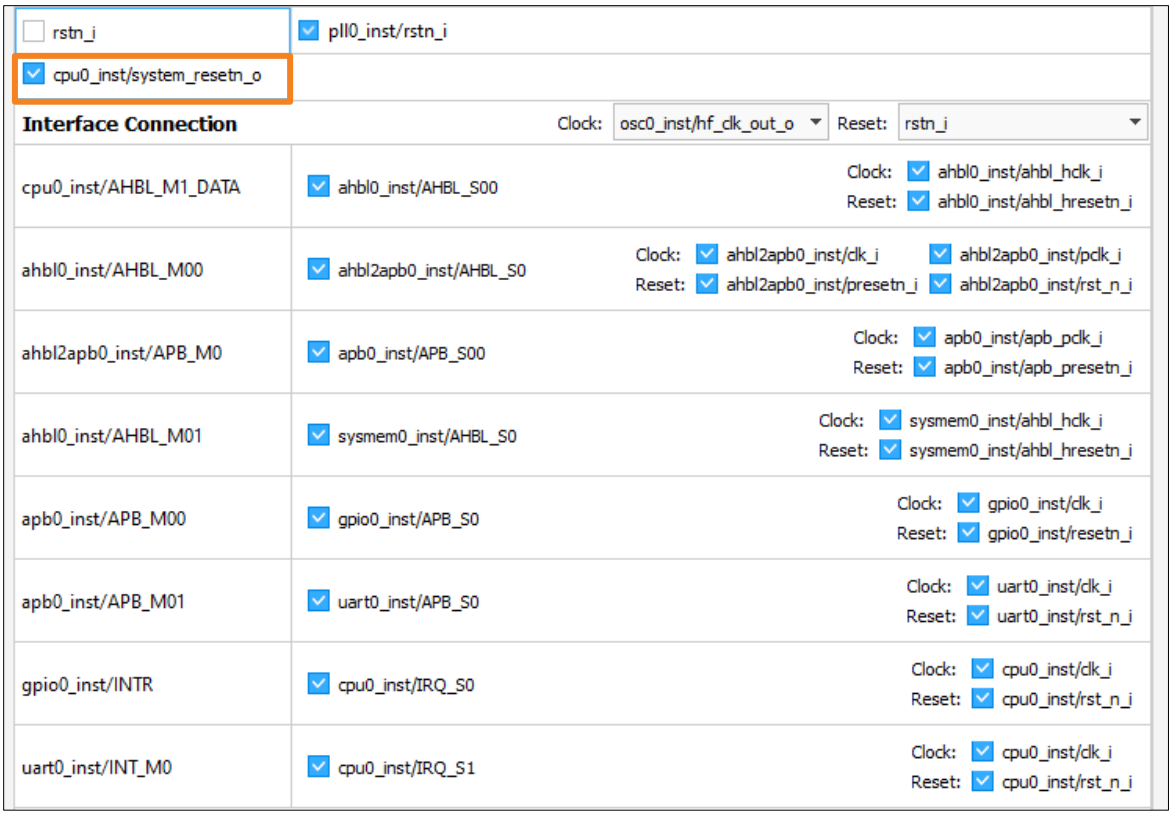


Figure 2.89. Connecting CPU Instance Reset Output Port

- If the SoC project does not contain a CPU instance, clock/reset on all instances connect to the top clock/reset port. Top clock/reset port is the port such as rstn_i in Figure 2.89.

b. The output clock/reset port on one instance should not be connected to its own clock/reset input port. For example, cpu0_inst.system_resetn_o should not connect to cpu0_inst.rst_n_i in Figure 2.89.

B. Interface Connection

Bus interfaces can only connect from one interface to another. It is a one-to-one relation, not a one-to-multiple relation. And the interfaces must have the same interface type.

In the example below (Figure 2.90), cpu0_inst.AHBL_M1_DATA is a bus interface. It can only connect to one destination, ahbl0_inst.AHBL_S00, because they have the same interface type AHBLite. To know the interface type, you can check the **Bus Type** in **Design View** (Figure 2.90).

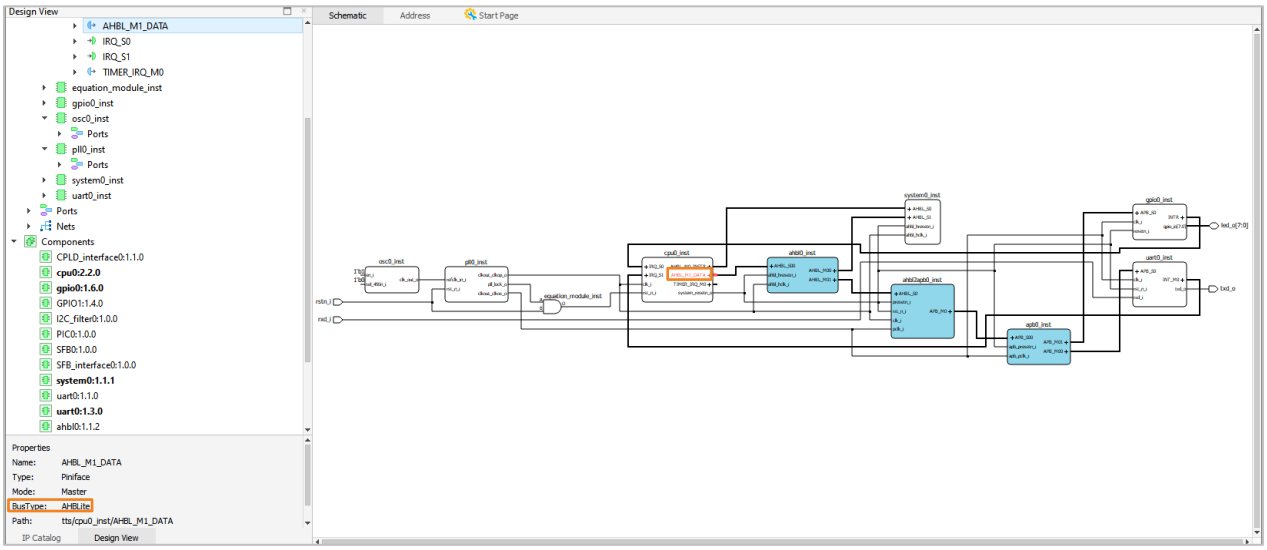


Figure 2.90. Interface Type of cpu0_inst.AHBL_M1_DATA

Interface Connects Rules

If a project contains a CPU instance, the interface connection starts from the CPU instance, then to one bus/bridge instance, and then to another bus/bridge instance. After connecting all bus/bridge instances one by one (cpu0 > ahbl0 > ahbl2apb0 > apb0), finally connects to other instances (gpio0, uart0). See Figure 2.91 and Figure 2.92.

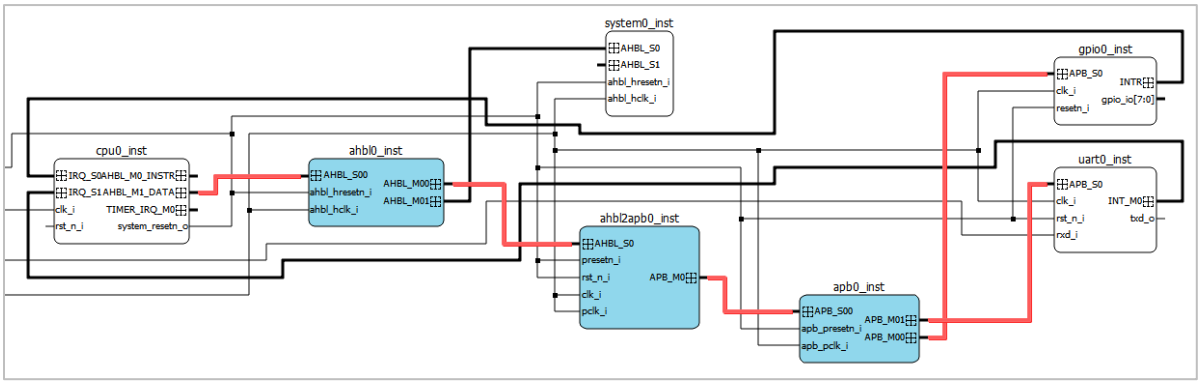


Figure 2.91. Interface Connection on from CPU to Bus/Bridge instances in Schematic View

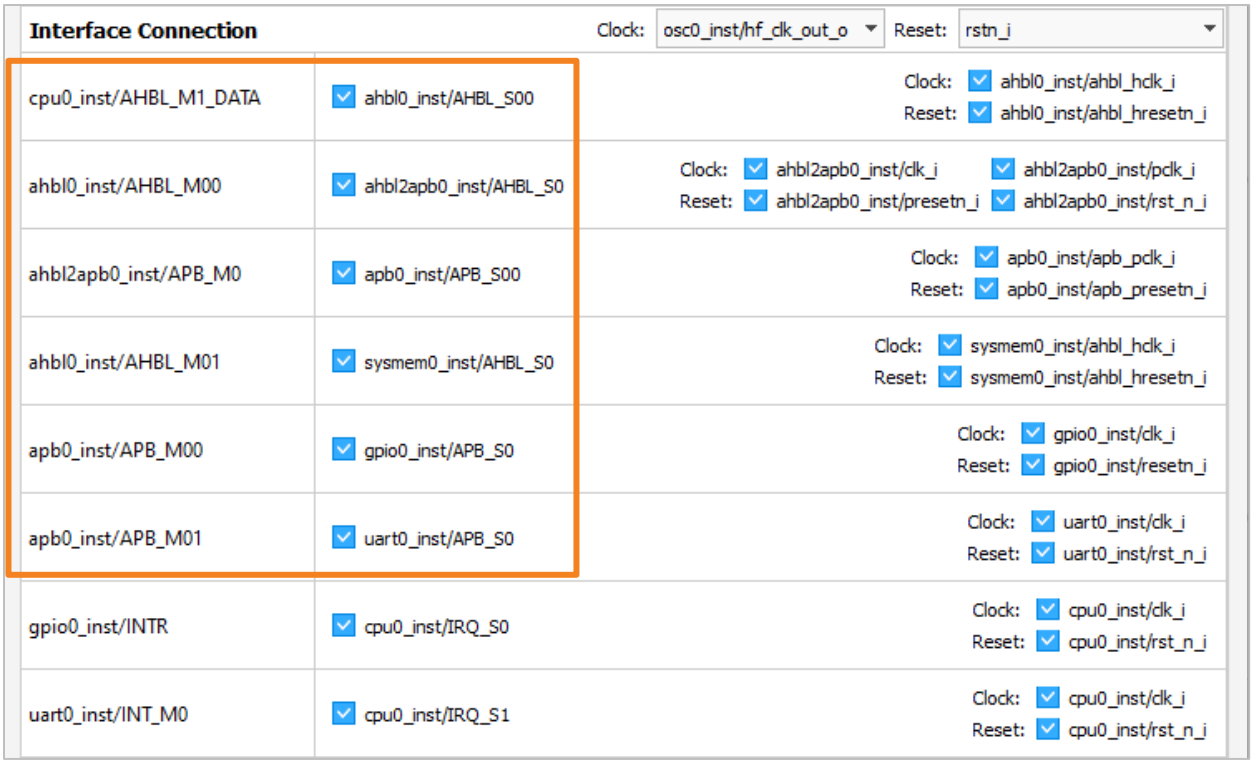


Figure 2.92. Interface Connection from CPU to Bus/Bridge Instances in Connect Port View

If the last instance connected has the same bus interface type as that of the CPU instance, then it connects back to CPU instance (see Figure 2.93 and Figure 2.94). In Figure 2.95 and Figure 2.96, you can see gpio0_inst.INTR and cpu0_inst.IRQ_S0 have the bus type: Interrupt.

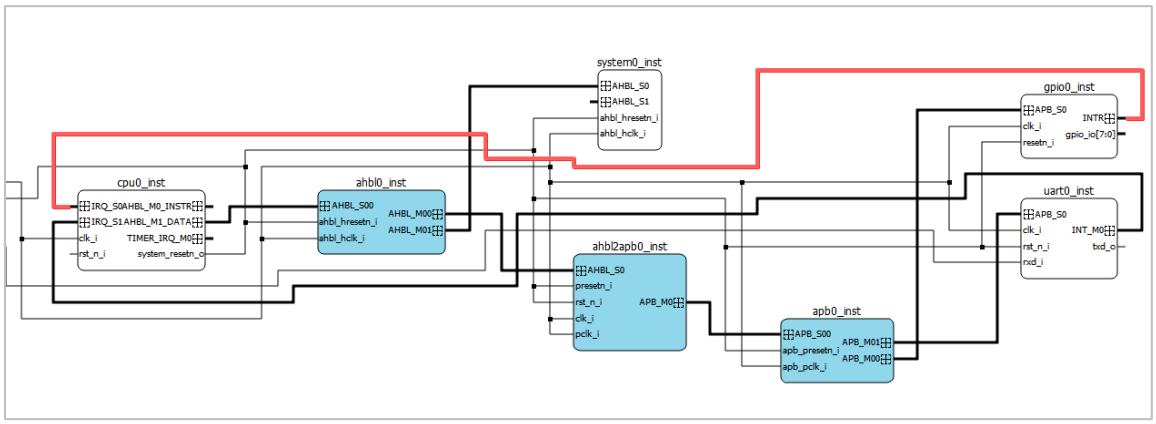


Figure 2.93. Interface Connection on Other Instances Connecting back to CPU in Schematic View

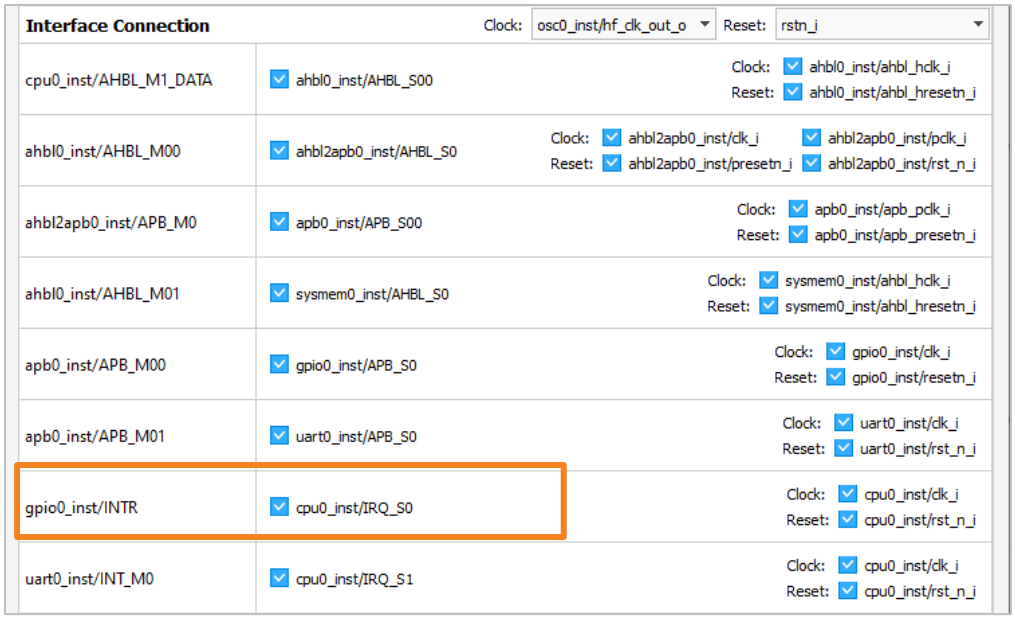


Figure 2.94. Interface Connection on Other Instances Connecting back to CPU in Connect Port View

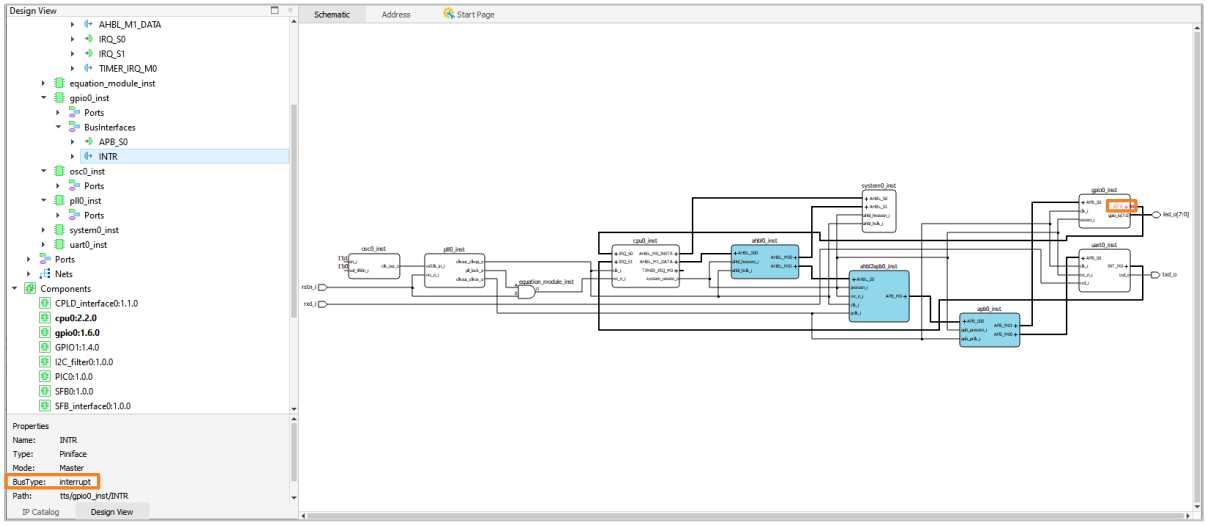


Figure 2.95. Interface Type of gpio0_inst.INTR

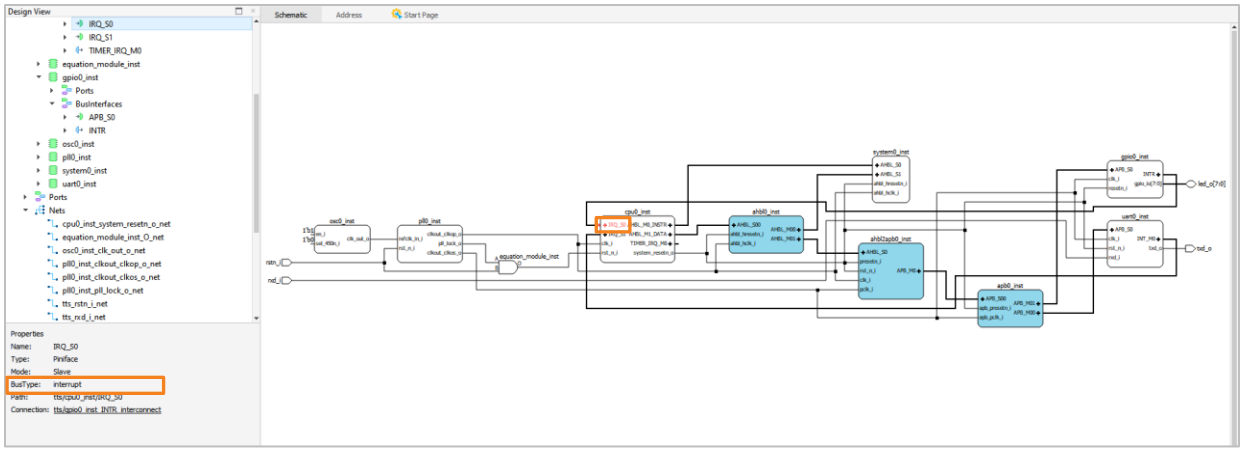


Figure 2.96. Interface Type of cpu0_inst.IRQ_S0

If the project does not contain CPU instance, the interface connection starts from the bus/bridge instance, and then to each bus/bridge instance one by one, and finally connects to the other instances.
Note: If the bus interface is an instruction set, such as CPU0_inst.AHBL_M0_INSTR, it does not perform auto-connect.

C. Other Connection
If ports have the same port name, for example, rxd_i and uart0_ins.rdx_i, they are auto connected.

2.3.6.4. Assign a Constant Value to an Input Pin

1. Select the desired pin and right-click the pin. Choose **Assign Constant Value** (Figure 2.97).

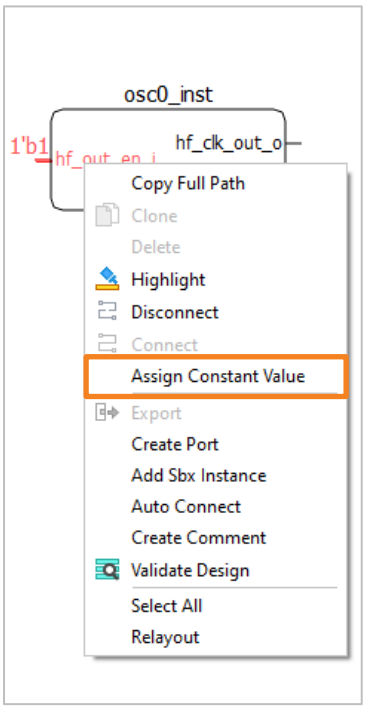


Figure 2.97. Right-click Menu of an Input Pin

2. A small dialog box appears (Figure 2.98). Enter the desired value. To erase the value and start over, click X. For all buses (more than one pin), the format is hexadecimal. Make sure the value fits the number of pins in the bus. For example, a 3-pin bus can accept 0-7, but not 8.

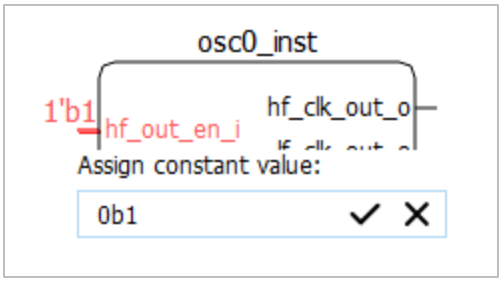


Figure 2.98. Dialog Box of Assigning Constant Value to an Input Pin

2.3.6.5. Disconnect Modules

Usually, disconnecting modules means deleting a net. If the net has multiple branches, just delete one branch, leaving the rest of the nets intact.

- To disconnect one branch of a net, right-click the pin of that branch and choose **Disconnect**. The branch going to that pin disappears.
- To disconnect a whole net, right-click the net and choose **Delete**. The whole net is deleted.
- **Double Click on net connection** (Figure 2.99) or **Right Click to** choose **Disconnect**. to trigger a preview diagram to help user edit the net connection (Figure 2.100)

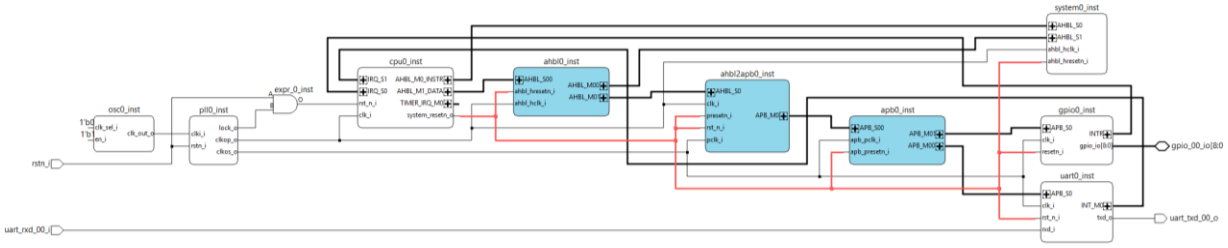


Figure 2.99. Double Click Net to Trigger a Preview Diagram

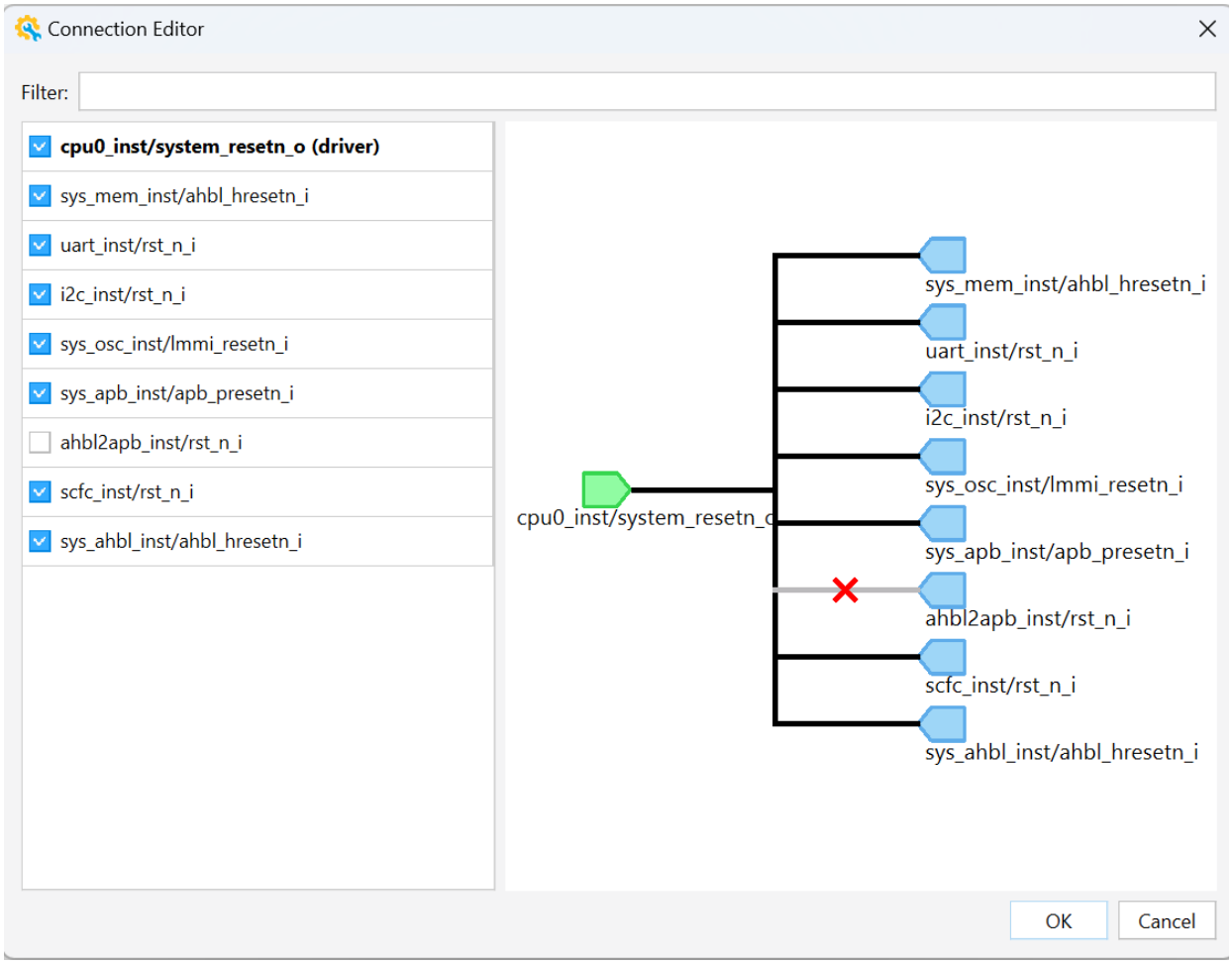


Figure 2.100. Preview Diagram to Help User Edit the Net Connection

2.3.6.6. Auto Set default value to interface dangling port

Dangling interface port is automatically set to a default value when the design is saved (Figure 2.101).

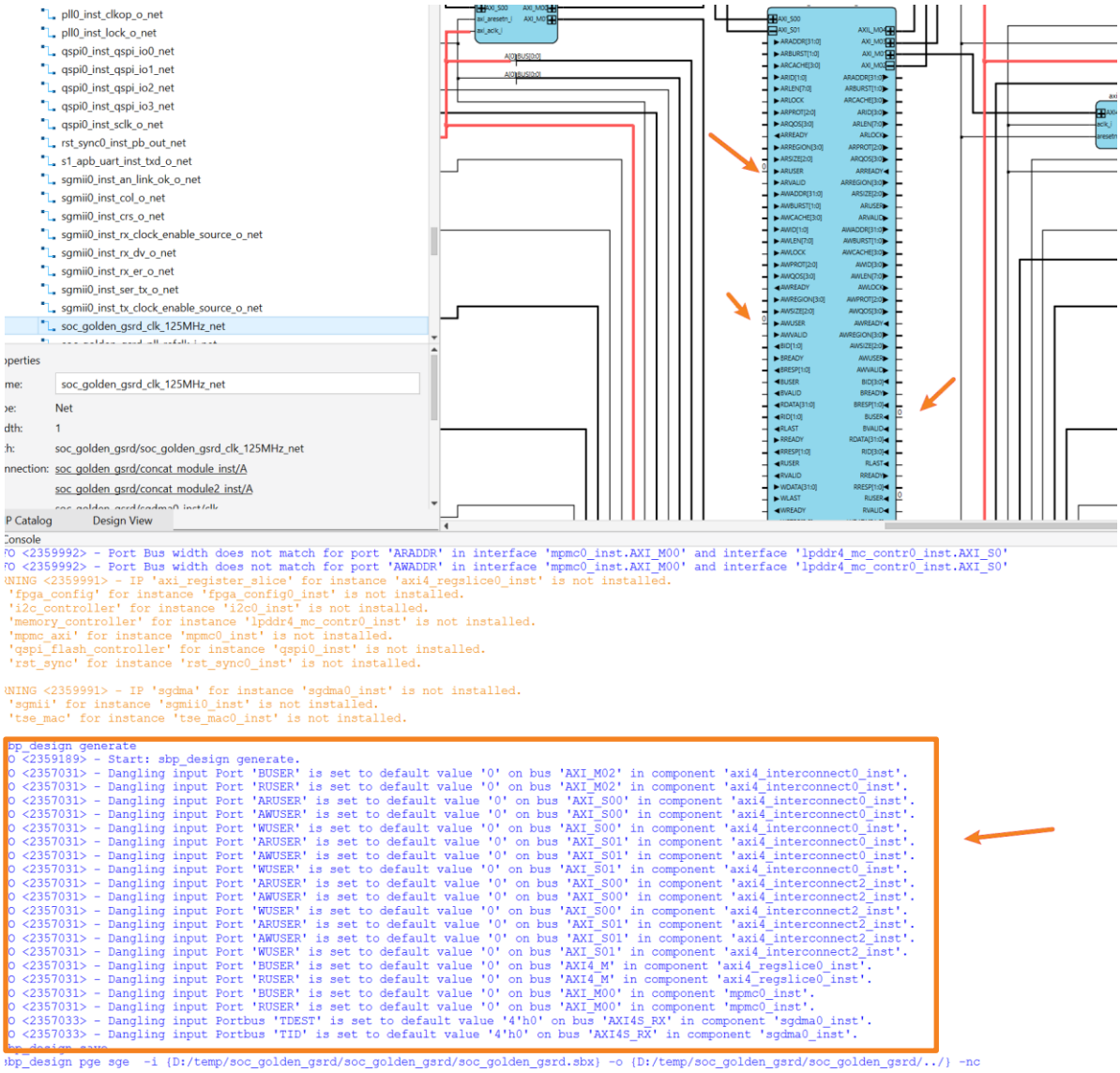


Figure 2.101. Auto Set Default Value to Dangling Interface Port

2.3.7. Creating Top-level Ports

With multiple modules in a Propel Builder project, top-level ports need to be created for a complete Propel Builder module. You can create a top-level port either manually or automatically.

For input ports that connect to more than one pin, such as for clock and reset signals, the manual way is more convenient than the automatic way. If the port names automatically-generated need to be changed, the manual way is better.

For other pins, the automatic way is usually preferred. The automatic way enables you to create the appropriate port type and connect net simultaneously. The automatic way can also create multiple ports at the same time.

The automatic way of creating ports is the most effective. If all the modules are selected, Propel Builder can automatically create ports for all the remaining unconnected pins for selected modules in one step.

- To create a port for a pin or bus manually:
  a. Right-click in the Schematic view and choose **Create Port**. The Create Port dialog box pops up (Figure 2.102).

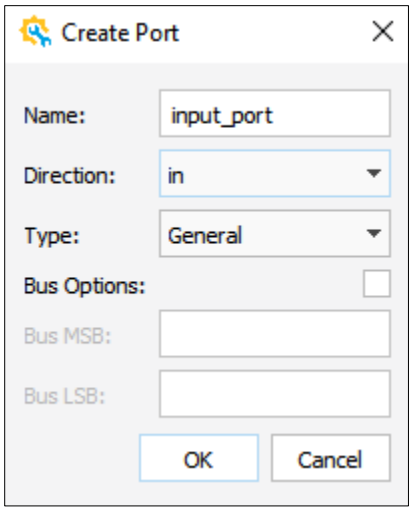


Figure 2.102. Create Port Dialog Box

b. Enter a name for the port in the **Name** field.
c. Choose a direction for the port, such as Input in the **Direction** field.
d. Choose the port type from the **Type** field. The default type is General.
e. (Optional) Select the **Bus Options**. Enter the number for the most significant bit (MSB) and the least significant bit (LSB). These two options define the bus width.
f. Click **OK**. The port appears. Figure 2.103 shows an input port, port name of which is on the left. Figure 2.104 shows an output port and an inout port, port names of which are on the right.

Figure 2.103. Input Port

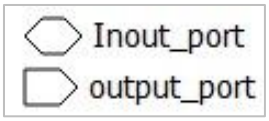


Figure 2.104. Output Port and Inout Port

g. Connect the port to the module pins. Refer to the Connecting Modules section for more details.
h. (Optional) Double click on the Port/Portbus in schematic view, the port edit dialog opens (Figure 2.105).

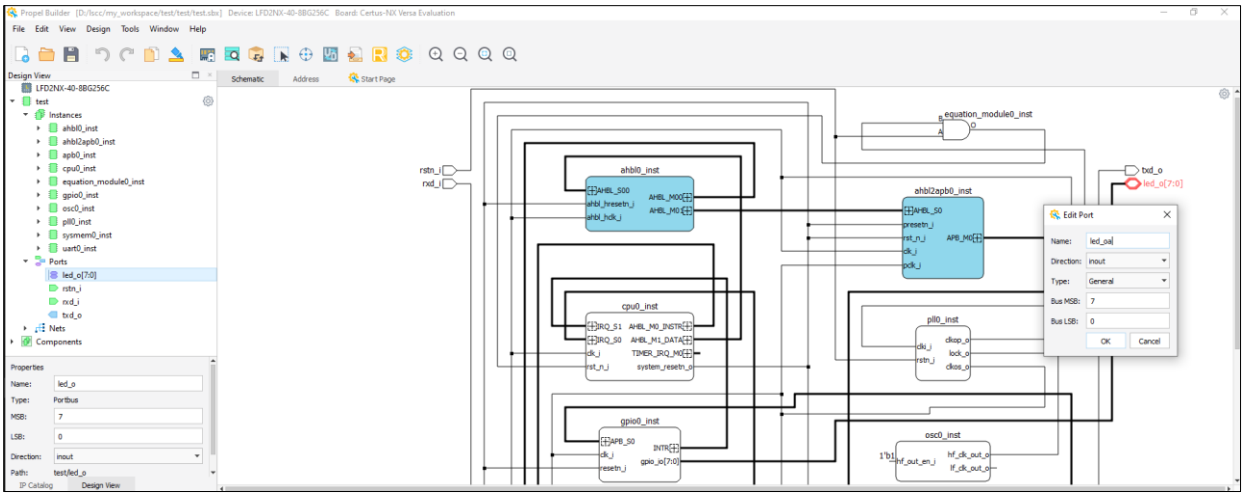


Figure 2.105. Port Edit Dialog

- To create ports automatically:
  a. Select the pins that are to be connected to the top-level ports. All the pins in a module can be selected by clicking its block. Any pins that are already connected to a net or a constant value are skipped.
  b. Right-click on one of the selected pins, interfaces or modules, and choose **Export**. The selected pins are extended by lines to new top-level port symbols. The names of the ports and nets are added to the List view. Zoom out or scroll the image in the Schematic view to see the new ports.
  c. Port or net names can be changed, if needed.
- To modify a port:
  a. Click on a port, **Properties** window open (Figure 2.106).

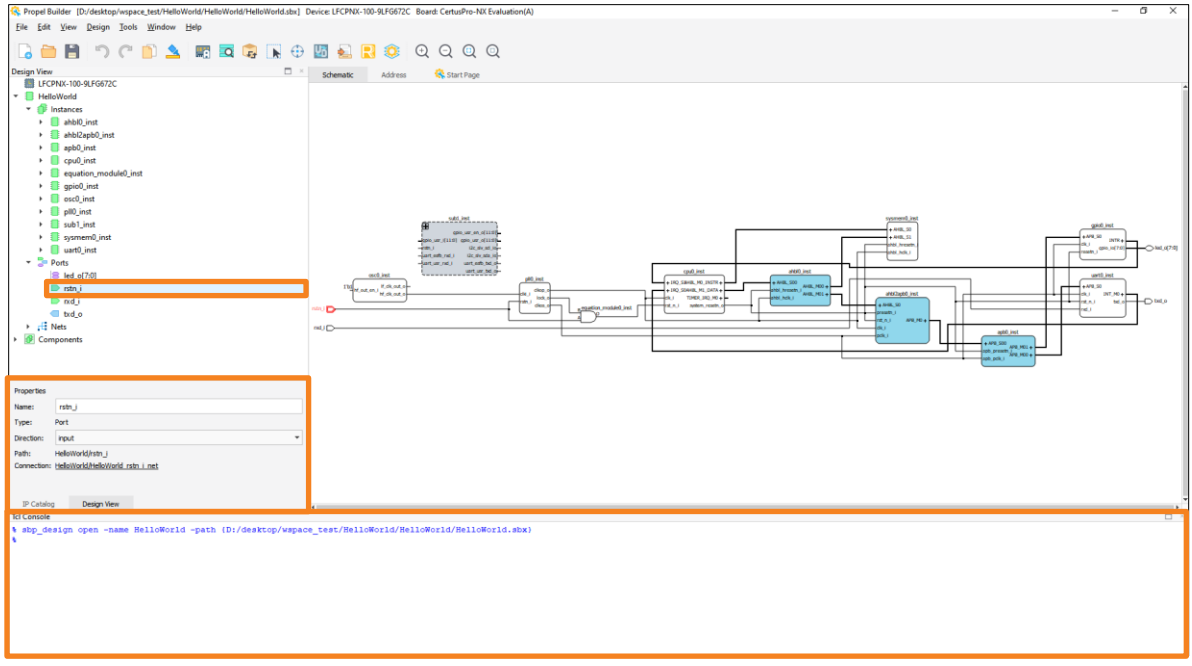


Figure 2.106. Properties of Port

  b. Port direction can be modified. You can use the drop-down menu to choose the desired port direction. TCL command is shown in **Design View** (Figure 2.107).

c. Port width can only be modified if it is already multi-bit. An error message is prompted out or shown in TCL Console, if the input value does not meet rules (Figure 2.107).

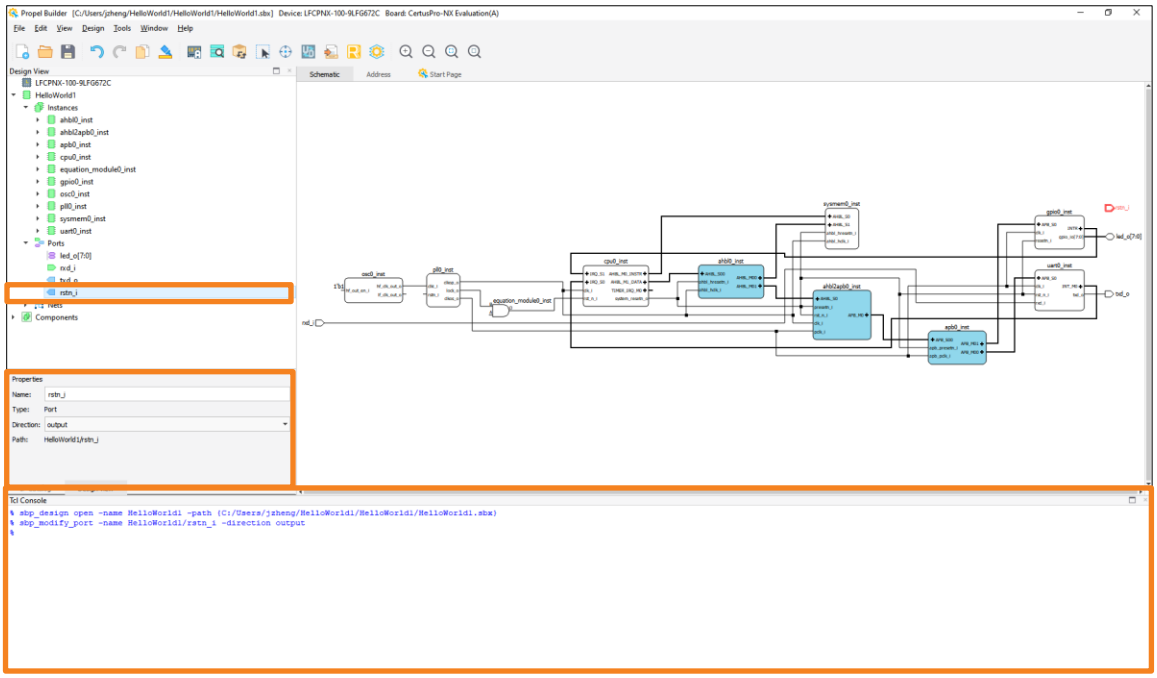


Figure 2.107. Port Direction

d. TCL history can be viewed in TCL History window (Figure 2.109) by choosing **Design** > **TCL History** (Figure 2.108).

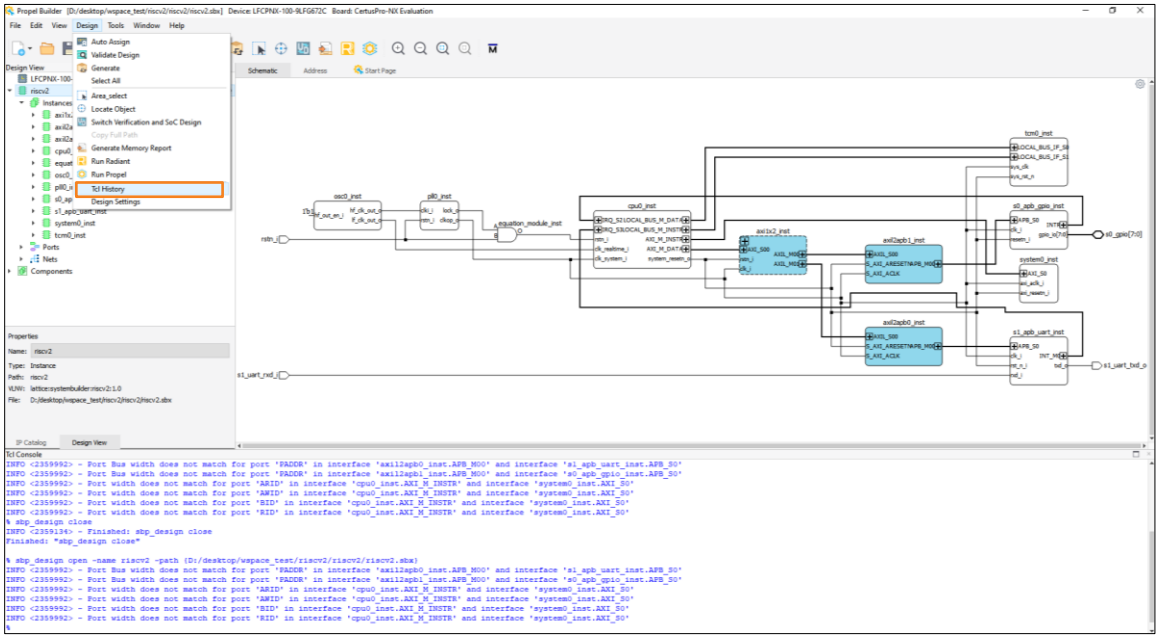


Figure 2.108. Open TCL History

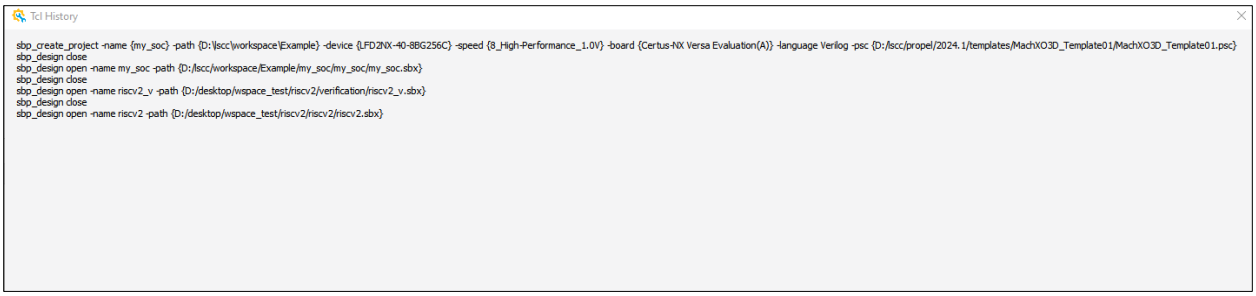


Figure 2.109. TCL History Window

e. PortBus MSB, LSB and direction can be modified. Click on PortBus and then use the drop-down menu to choose the desired direction (Figure 2.110).

Note: If the input value does not meet rules, an error message prompts out or shows the in TCL Console.

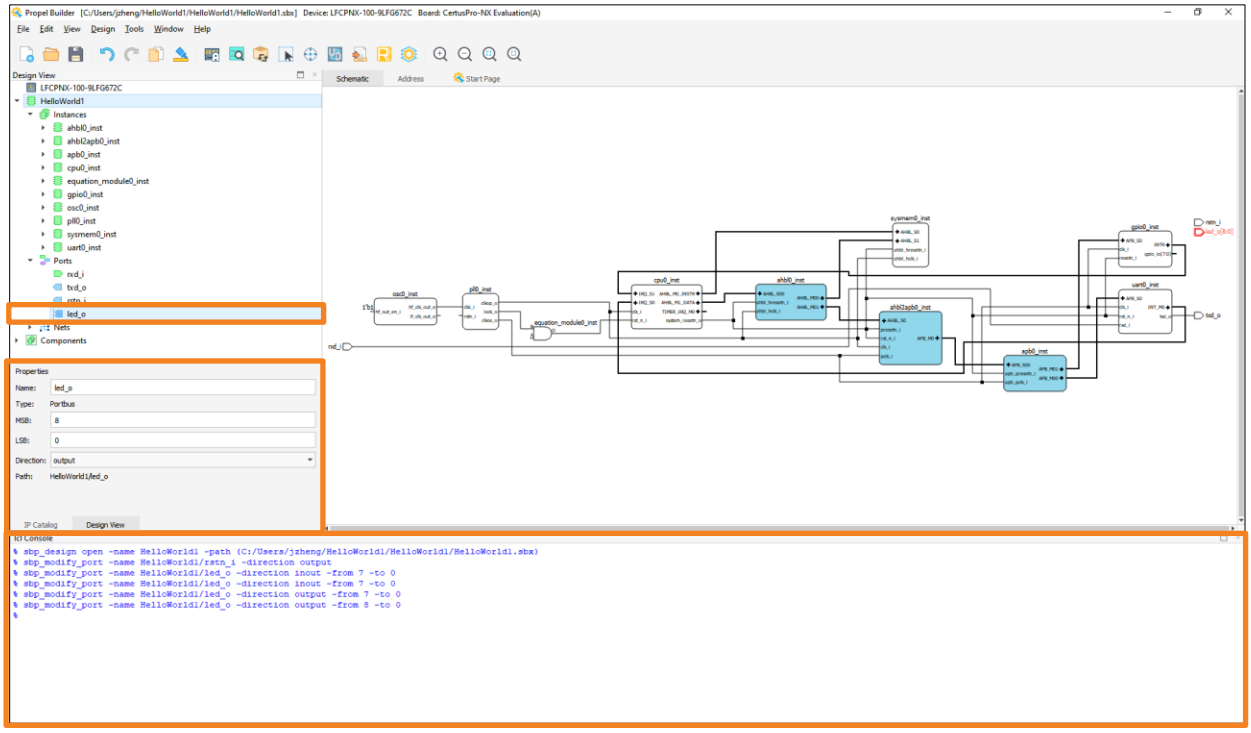


Figure 2.110. PortBus Direction

2.3.8. Adjusting Address Spaces

The Address view shows the base address, size of the address segment, and the end address for each leaf memory-mapped subordinate connection in the Propel Builder project. Propel Builder can automatically assign address values, while the base address value can be changed manually. The addresses are automatically assigned when major and subordinate components were connected. The ranges are set when the modules are configured. The end addresses are calculated.

The Lock option on each address space prevents Auto Assign from changing the base address value. The Lock option is selected automatically when you manually change the address value. To reset the address space, clear the Lock option before clicking the Auto Assign icon.

Note: There is no Lock option on Local Memory. The value of the base address can always be changed, while Auto Assign does not reset it to its original value.

1. In the Propel Builder main window, click the Address tab. The Address view (Figure 2.111) shows.

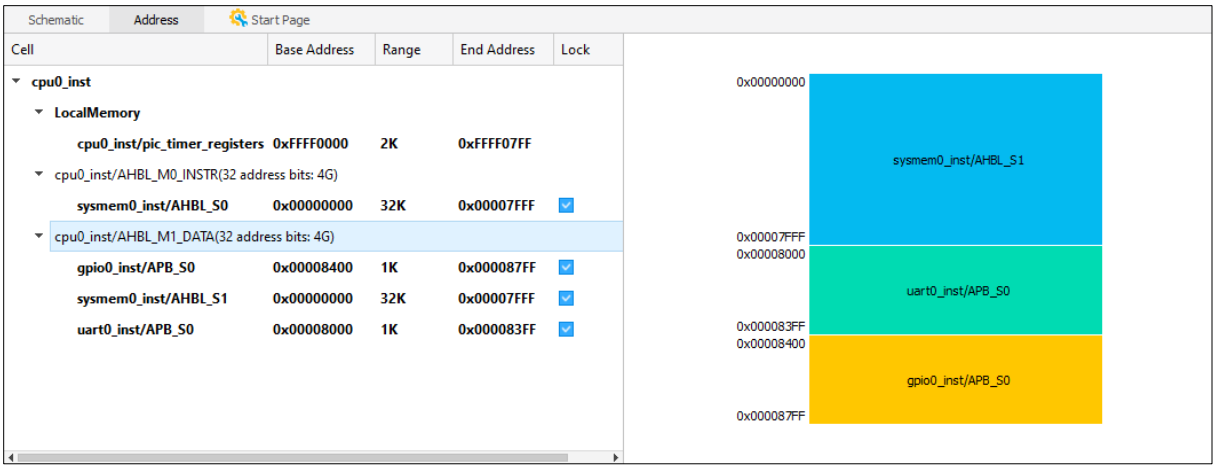


Figure 2.111. Address View

2. (Optional) Set or clear the Lock options as desired in Address view.
3. (Optional) Double-click the base address in Address view (Figure 2.112). Type the new value and press **Enter**.

   Note: Values must align with 1K boundaries, such as 0x00000400, 0x00000800, or 0x00000C00. The end address value changes based on the new value. The Lock option is selected automatically at this time.

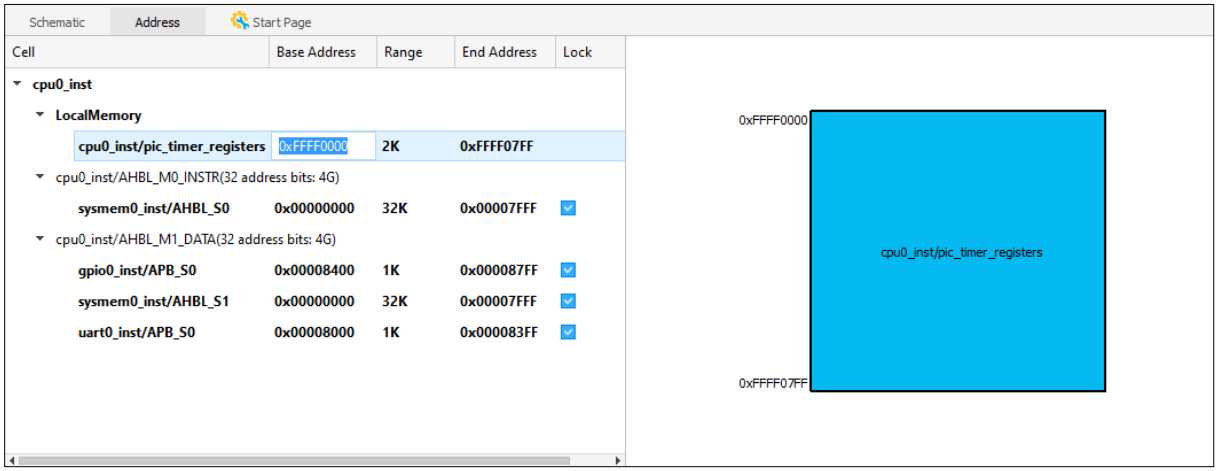


Figure 2.112. Edit Base Address

Note: If there is a conflict of a related address space, it is shown in red in the graphic.

2.3.9. Validating the Design

The design rule check (DRC) can be run at any time. It can check if there is any illegal connection, incorrect bus interface definition, overlapping address space, or non-cacheable components in CPU cache area. Clock frequency consistency check is also done between PLL output clock and peripheral IPs (UART). When a peripheral IP, such as UART, is installed and its configured SYS_CLOCK_FREQ does not match the output frequency of the connected PLL (pll0_inst.clkos_o), Propel automatically updates the peripheral frequency to match the PLL.

If the peripheral IP is not installed, and a mismatch is detected between the expected and actual clock frequencies, Propel reports an error, ensuring that invalid configurations are caught early.

To perform the design rule check, click the **Validate Design** icon on the toolbar of the Propel Builder main window. The DRC results appear in the TCL Console.

Note: Optional bus ports handling

Optional input ports on Propel IP bus interface, such as AXI4 Stream, are left dangling when the driver side connected bus do not support these ports. This may be IP dependent if the dangling input signals affect the functionality.

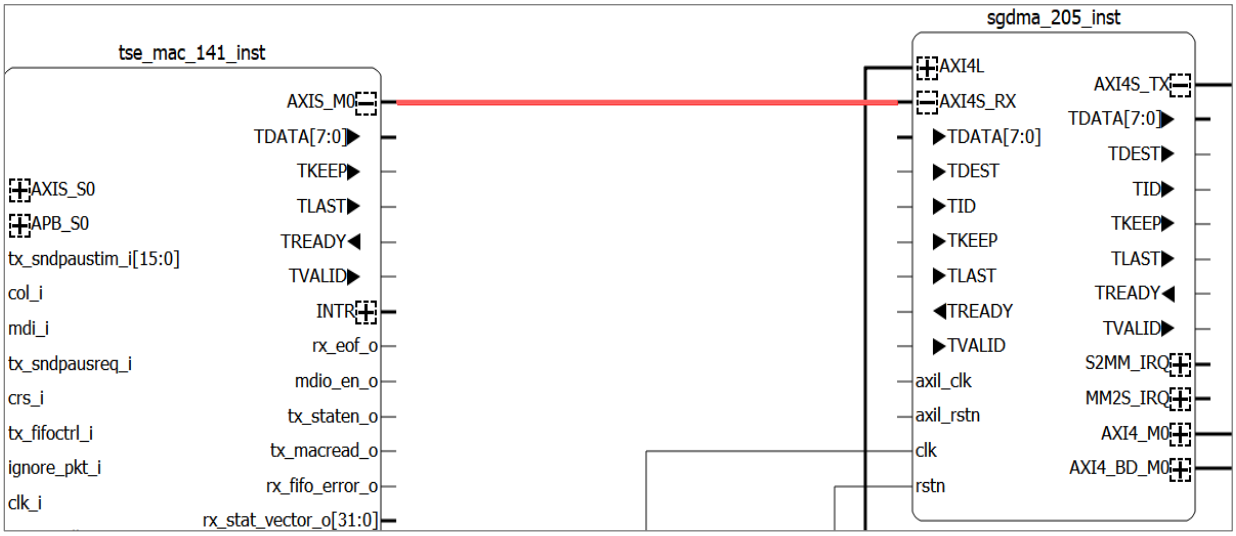


Figure 2.113. Optional Bus Ports Handling

The default values of these ports are defined in abstraction Definition of AMBA Bus. Builder can detect the dangling ports and then tie the default values to them. (Figure 2.113)

2.3.10. Generating the Propel Design

To create a Propel Builder module is to generate a .sbx file, which defines a Propel Builder project, RTL files, and the instantiation templates. The instantiation templates have Verilog and VHDL code to help instantiate the Propel Builder module in a design.

To generate Propel design:

From the toolbar of the Propel Builder main window, click the **Generate** icon . This saves the Propel Builder design and runs the design rules check (DRC) and can generate some RTL files. The RTL files include a top RTL file that is the top module for the entire Propel design. The RTL files for IPs are regenerated when you click this button.

Note: If any change is made on an IP, you need to use this icon to finish updating that IP.

Lattice Propel Builder only updates those modules that have changed since the last time the propel project files were generated. If there is no real modification on the design, that is, there is no change on components/ports/connections, no memory assignments and so on, the Generate operation does not regenerate the sbx and top-level RTL file and IP. So it does not trigger re-compilation in Lattice Radiant or Diamond Software. If regeneration is desired, the action Force Generate can force regeneration of the top-level RTL file.

2.3.11. Generating the Memory Report

From the toolbar of the Propel Builder main window, click the **Generate Memory Report** icon  . The SoC design memory information is generated. The memory report folder (mem_report) is generated. All design memory information is shown in detail in the memory report files. The Memory Report files are in HTML format (Figure 2.114). To see more about address space, refer to the Adjusting Address Spaces section.

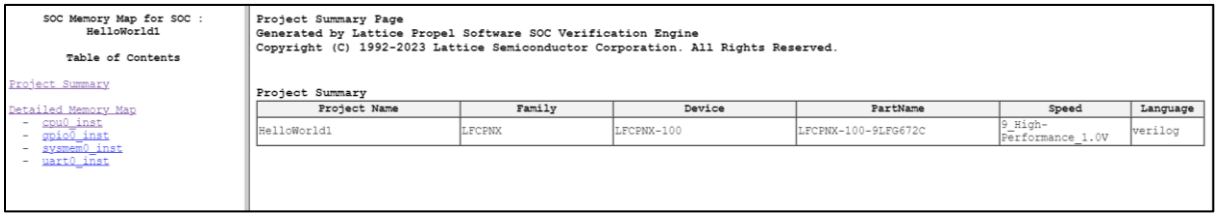


Figure 2.114. Memory Report

Click on the links in the left side pane, you can see more information on Detailed Memory Map (Figure 2.115) and each of the instances (Figure 2.116).

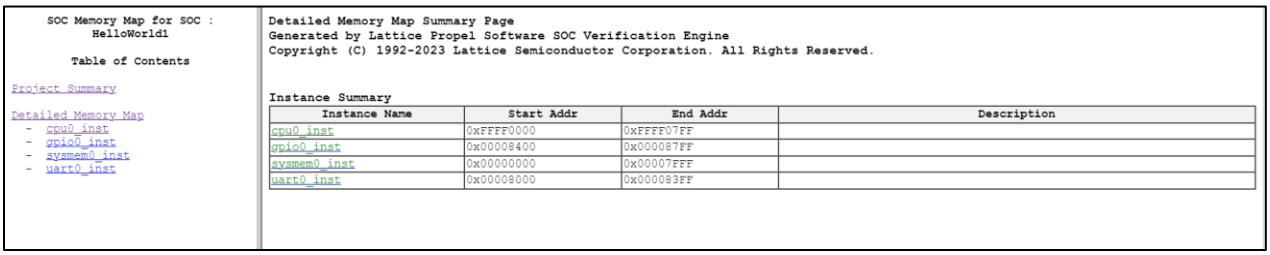
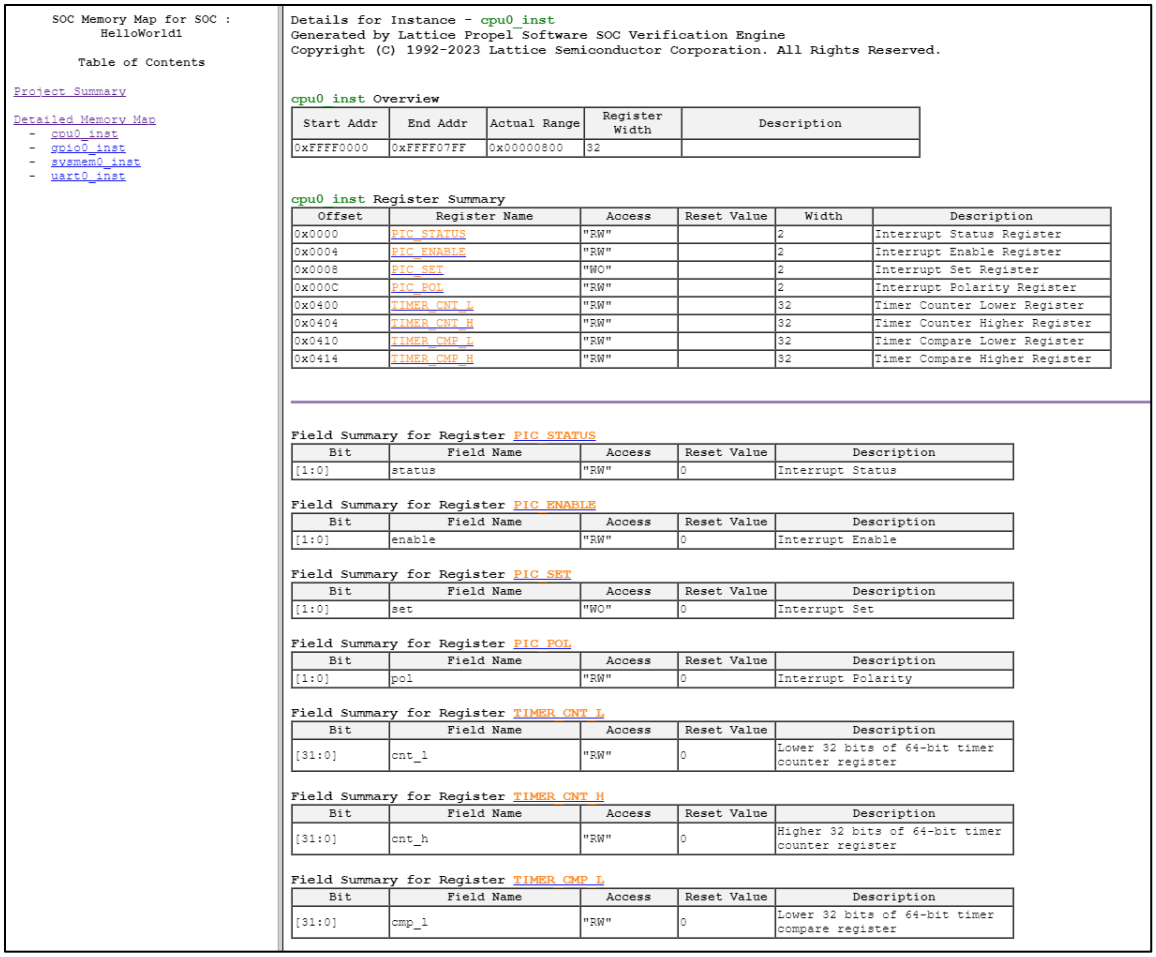


Figure 2.115. Memory Report



SOC Memory Map for SOC : HelloWorld1

Table of Contents

Project Summary

Detailed Memory Map
- cpu0_inst
- gpio0_inst
- sysmem0_inst
- uart0_inst

Details for Instance - cpu0_inst
Generated by Lattice Propel Software SOC Verification Engine
Copyright (C) 1992-2023 Lattice Semiconductor Corporation. All Rights Reserved.

cpu0_inst Overview

Start Addr	End Addr	Actual Range	Register Width	Description
0xFFFF0000	0xFFFF07FF	0x00000800	32	

cpu0_inst Register Summary

Offset	Register Name	Access	Reset Value	Width	Description
0x0000	PIC_STATUS	"RW"		2	Interrupt Status Register
0x0004	PIC_ENABLE	"RW"		2	Interrupt Enable Register
0x0008	PIC_SET	"WO"		2	Interrupt Set Register
0x000C	PIC_POL	"RW"		2	Interrupt Polarity Register
0x0400	TIMER_CNT_L	"RW"		32	Timer Counter Lower Register
0x0404	TIMER_CNT_H	"RW"		32	Timer Counter Higher Register
0x0410	TIMER_CMP_L	"RW"		32	Timer Compare Lower Register
0x0414	TIMER_CMP_H	"RW"		32	Timer Compare Higher Register

Field Summary for Register PIC_STATUS

Bit	Field Name	Access	Reset Value	Description
[1:0]	status	"RW"	0	Interrupt Status

Field Summary for Register PIC_ENABLE

Bit	Field Name	Access	Reset Value	Description
[1:0]	enable	"RW"	0	Interrupt Enable

Field Summary for Register PIC_SET

Bit	Field Name	Access	Reset Value	Description
[1:0]	set	"WO"	0	Interrupt Set

Field Summary for Register PIC_POL

Bit	Field Name	Access	Reset Value	Description
[1:0]	pol	"RW"	0	Interrupt Polarity

Field Summary for Register TIMER_CNT_L

Bit	Field Name	Access	Reset Value	Description
[31:0]	cnt_l	"RW"	0	Lower 32 bits of 64-bit timer counter register

Field Summary for Register TIMER_CNT_H

Bit	Field Name	Access	Reset Value	Description
[31:0]	cnt_h	"RW"	0	Higher 32 bits of 64-bit timer counter register

Field Summary for Register TIMER_CMP_L

Bit	Field Name	Access	Reset Value	Description
[31:0]	cmp_l	"RW"	0	Lower 32 bits of 64-bit timer compare register

Figure 2.116. Memory Report of Each Instance

2.3.12. Launching Project in Diamond or Radiant Software

In a complete SoC project, a Diamond or Radiant project can be created upon a Propel Builder design. After that, the SoC project can be launched in Diamond or Radiant software.

According to the device in the SoC project, Propel Builder can launch Diamond or Radiant software accordingly.

For Diamond support device, the **Diamond** software icon shows in the Builder GUI Toolbar.

For Radiant support device, the **Radiant** software icon shows in the Builder GUI Toolbar.

Notes:

- Different device families are supported and available in Radiant/Diamond software, as shown in Table 2.1.

Table 2.1. Different Device Families Supported in Radiant or Diamond

Software	Project Name	Part Number
Radiant	CertusPro-NX	LFCPNX
	Certus-NX	LFD2NX
	MachXO5-NX	LFMXO5
	CrossLink-NX	LIFCL
	LAV-AT Evaluation	LAV-AT

Software	Project Name	Part Number
Diamond	MachXO2	LCMXO2
	MachXO3D	LCMXO3D
	MachXO3L	LCMXO3DL
	MachXO3LF	LCMXO3DLF
	Mach-NX	LFMNX

- The installation path of Diamond or Radiant should be set using **Tools > Options > Directories**. See the Tools section for more details. Or, Diamond or Radiant software cannot be invoked.

2.3.12.1. Launch Diamond Software

1. Click the Diamond icon  from the Propel Builder toolbar. Diamond software is launched.

   A diamond_setup_template.tcl is generated in project path when you click the icon and is automatically invoked in Diamond. Refer to the Lattice Diamond Help for the meaning and usage of the TCL commands.

   In the meantime, there are also some files exported in project path, such as all RTL from IP, as well as the top-level module.

   IP encryption is converted to blowfish when exported to Diamond software. There are two sets of files generated for each IP for Diamond. You can use the blowfish file in case you need to add it again later.
2. Lattice Diamond is launched with a Diamond project generated for SoC at the background (Figure 2.117).

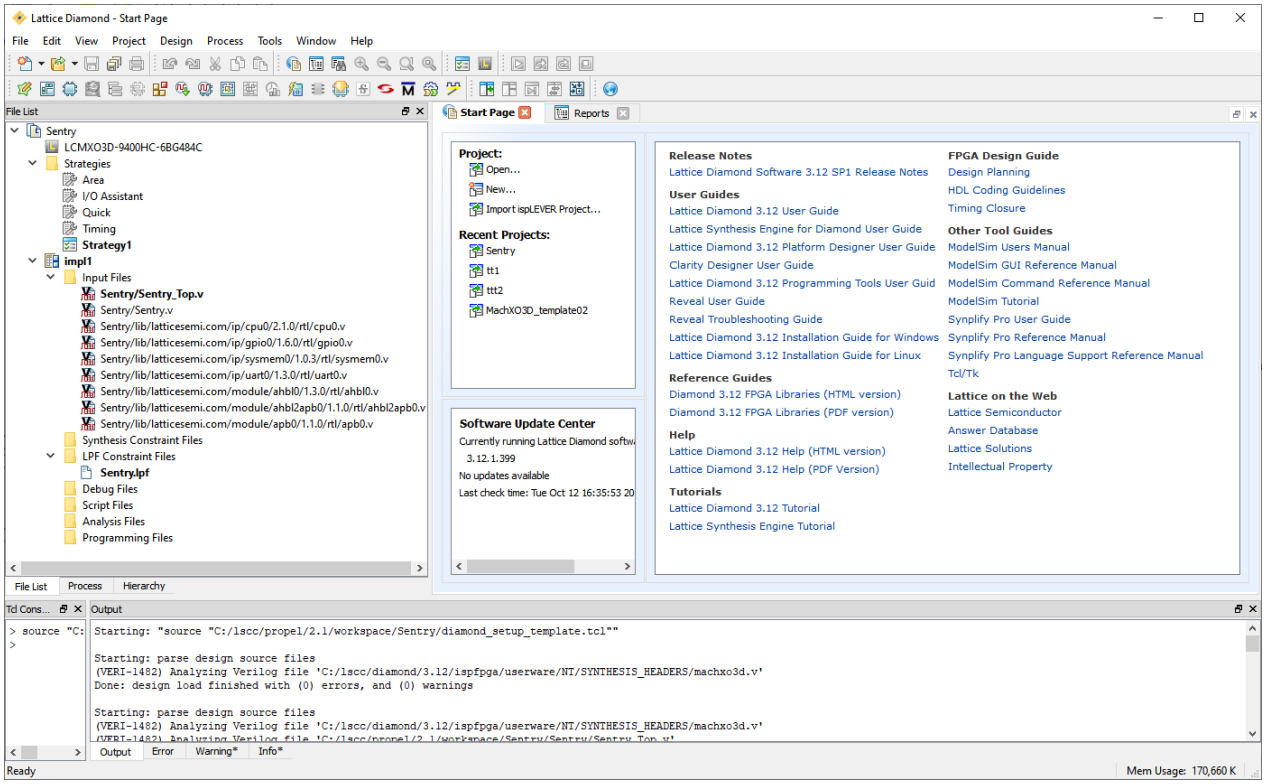


Figure 2.117. Diamond Project

3. (Optional) From the **File List** view of Diamond:
   - Modify the top-level RTL file (<*proj_name*>_Top.v) to match the SoC design, presupposition of which is that there is a top-level RTL file in your SoC design.

- Create a top-level RTL file (<*proj_name*>_Top.v) to match the SoC design, if the SoC design is created from an Empty Project template and there is no top-level RTL file in your SoC design.
  a. (Optional) Modify LPF constraint file (<*proj_name*>.lpf) to match the SoC design, if you have modified the SoC design. This step is a must to the SoC design that is created from Empty Project template.
  b. Switch to **Process** view of the Diamond project (Figure 2.118). Make sure at least one programming file (bitstream File or JEDEC file) is selected in the **Export Files** section. Available programming files can be different upon specific device included.

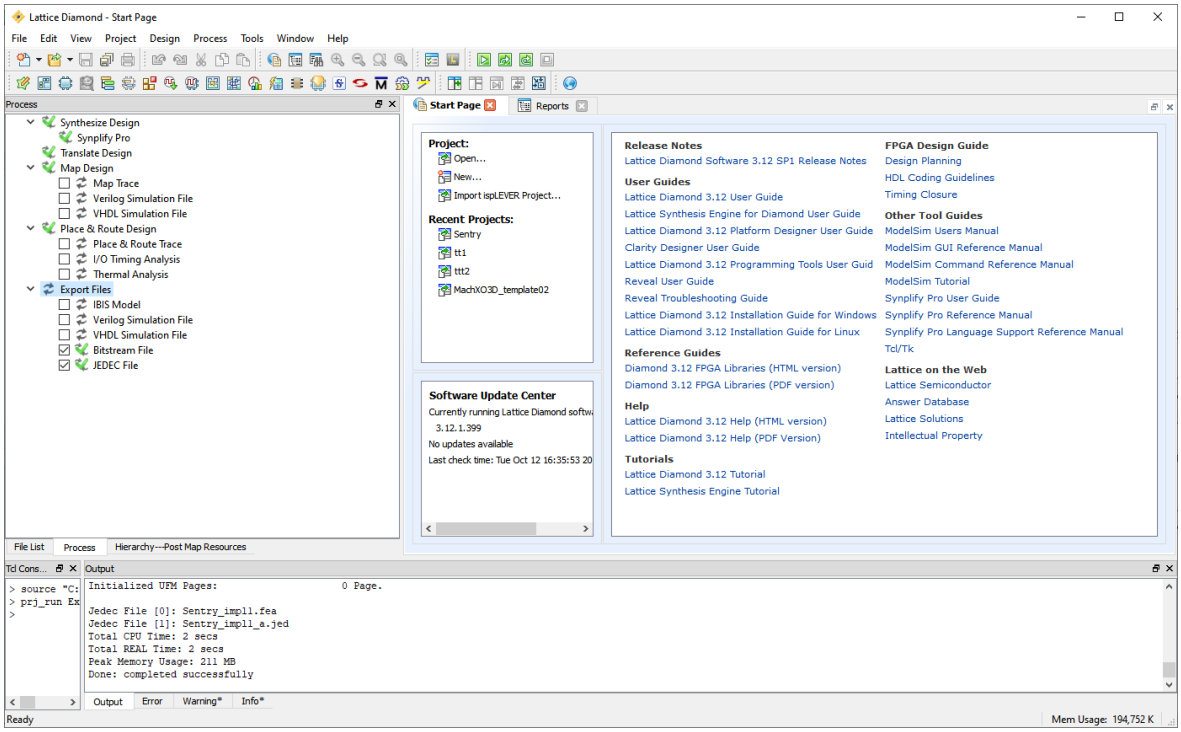


Figure 2.118. Generate Programming Files

  c. Right-click **Export Files** and choose **Run**  . The programming file is generated. The programming file can be used in the Diamond Programmer.

Note: Refer to the Lattice Diamond Help for more details of the Diamond project. Re-launch the Diamond project, if the project settings are modified in Propel 2025.2 Builder.

If there is encrypted RTL in diamond project, it is automatically detected in Diamond.

Board template may have some constraint files. Constraint files are different per each type of the board. The constraint files are also exported to Diamond.

2.3.12.2. Launch Radiant Software

1. Click the **Radiant** icon  from the Propel Builder toolbar. Radiant software is launched.

   A radiant_setup_template.tcl is generated in project path when you click this icon and is automatically invoked in **Radiant**. Refer to the Lattice Radiant Help for meaning and usage of the TCL commands.

   In the meantime, there are also some files exported in project path, like all RTL from IP, as well as the top-level module, and all files are listed in flist_design.f.
2. Lattice Radiant is launched with a Radiant project generated for SoC at the background (Figure 2.119).

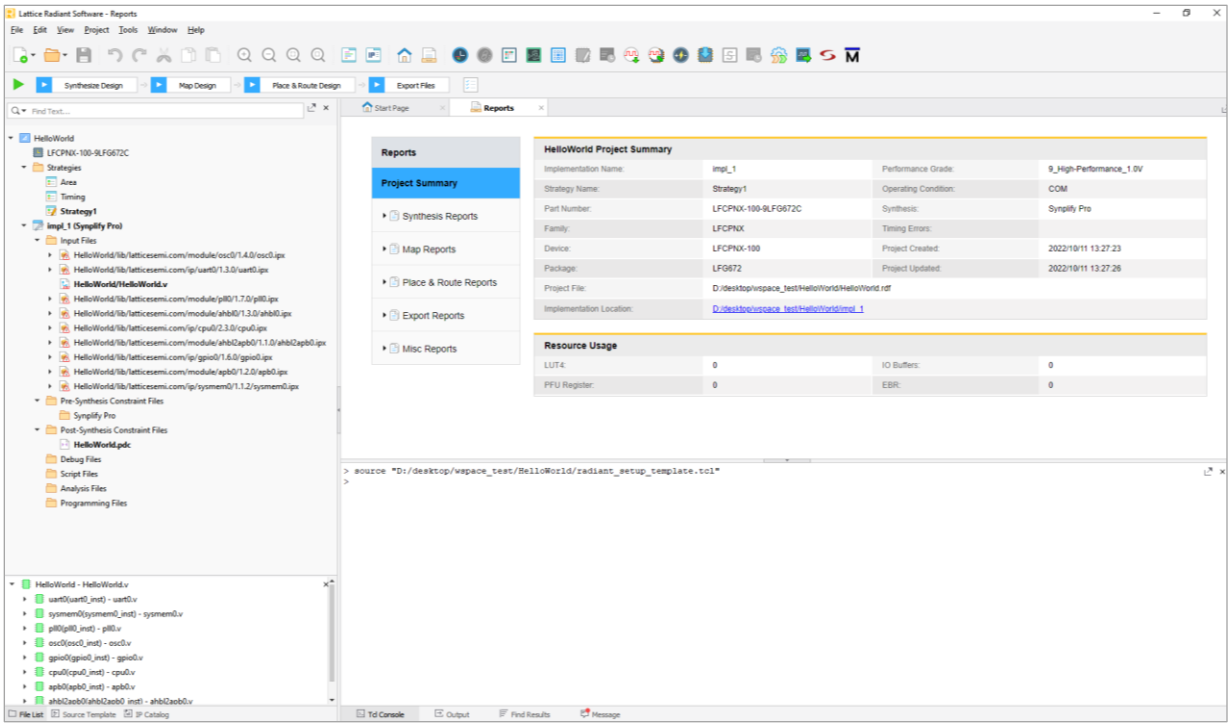


Figure 2.119. Radiant Project

a. (Optional) From the File **List** view of Radiant:
   - modify the top-level RTL file (<*proj_name*>_Top.v) to match the SoC design, presupposition of which is that there is a top-level RTL file in your SoC design; or
   - create a top-level RTL file (<*proj_name*>_Top.v) to match the SoC design, if the SoC design is created from an Empty Project template and there is no top-level RTL file in your SoC design.

b. (Optional) Modify pdc constraint file (<*proj_name*>.pdc) to match the SoC design, if you have modified the SoC design. This step is a must to the SoC design that is created from Empty Project template.

Click **Run all**. The Programming file is generated. It can be used in the Radiant Programmer.

Notes:

- Refer to the Lattice Radiant Help for more details of the Radiant project.
- Board template may have some constraint files. Constraint files are different per each type of board. The constraint files are also exported to Radiant.

2.3.12.3. Ipx Based Implementation Flow in Radiant

To enable Radiant constraint propagation flow, the design source files need to be switched from original HDL files to the .ipx file when generating the Radiant project.

Ipx based Radiant implementation flow is for project created in later than Propel Builder 2025.2. For project created before Propel Builder 2025.2, use a different method for exporting files (Figure 2.120). If you want to use ipx flow in these old projects, open them in Propel Builder 2025.2 and regenerate, then export to Radiant to change how it is exported to Radiant (Figure 2.121).

Considering some IPs are available at both Propel and Radiant side, you should only update IP through ipx in Propel Builder side.

Note: You must avoid IP update (through ipx) in Radiant side. The potential out-of-sync of updating IP in Radiant side may cause unexpected issues.

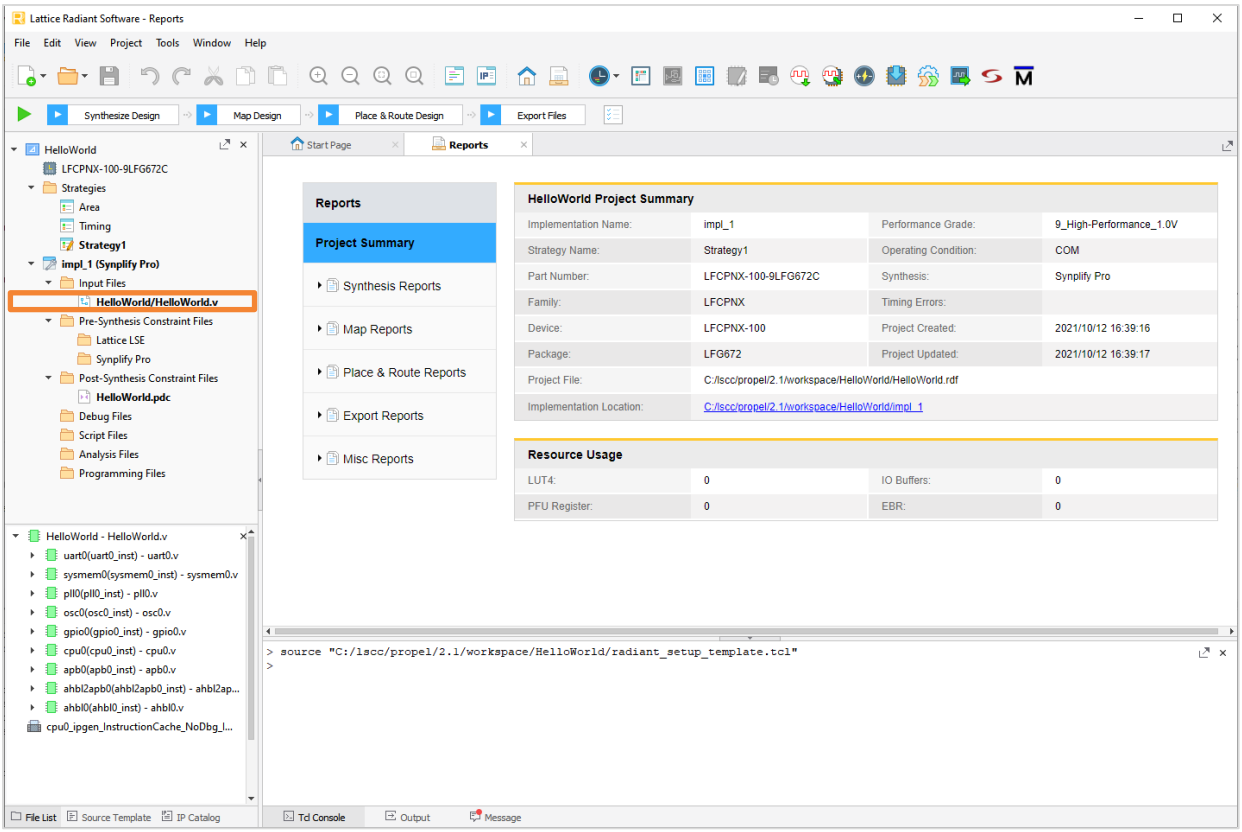


Figure 2.120. Radiant Project for Project before Propel Builder 2025.2

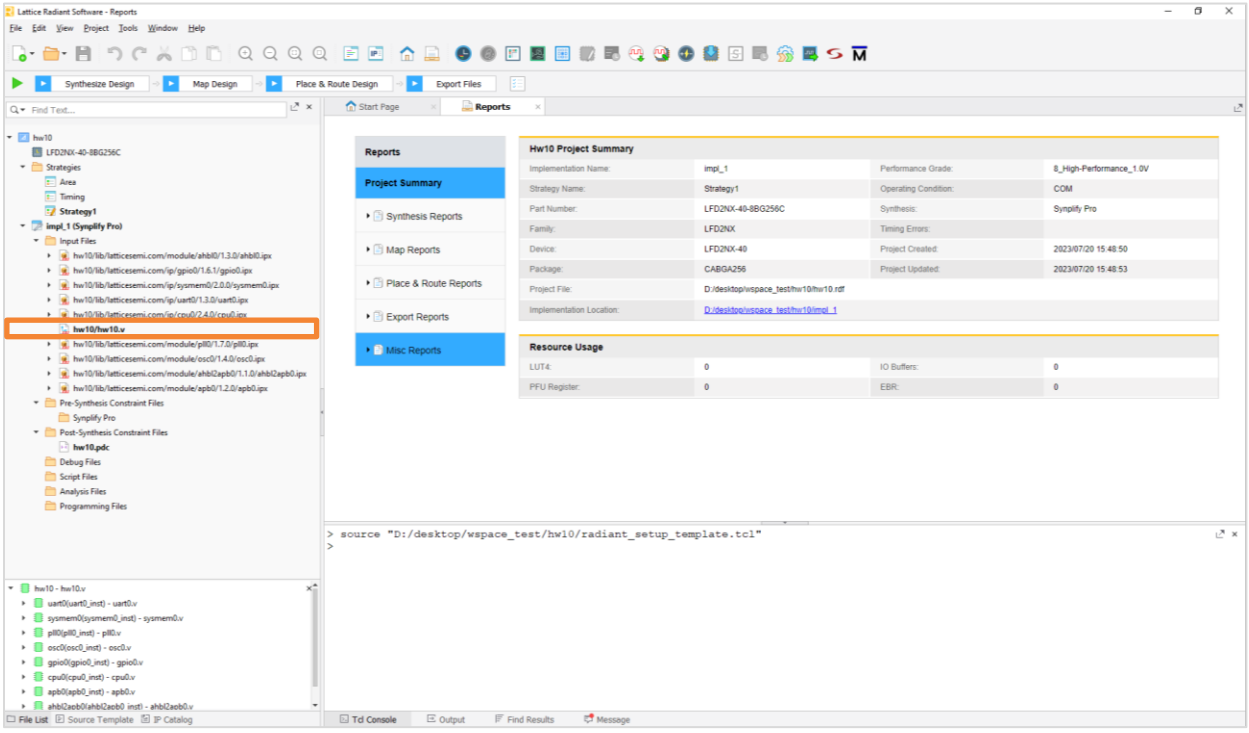


Figure 2.121. Radiant Project for Project since Propel Builder 2025.2

2.3.13. Launching SDK and Generate Mem File

After a SoC design is completed, Propel SDK can be launched in Propel Builder GUI for further software development in C project. For information about Propel SDK, refer to Lattice Propel 2025.2 SDK User Guide (FPGA-UG-02244).

Here is an example on how to generate a C project memory in Propel SDK for simulation use in verification project of Propel Builder. See Generating Simulation Environment section for more details on simulation.

For a template SoC project, you can launch SDK directly by clicking **Run Propel** icon from Propel Builder toolbar if a template SoC project is created.

1. Click the **Run Propel** icon  from Propel Builder GUI Toolbar. Lattice Propel Launcher (Figure 2.122) opens.

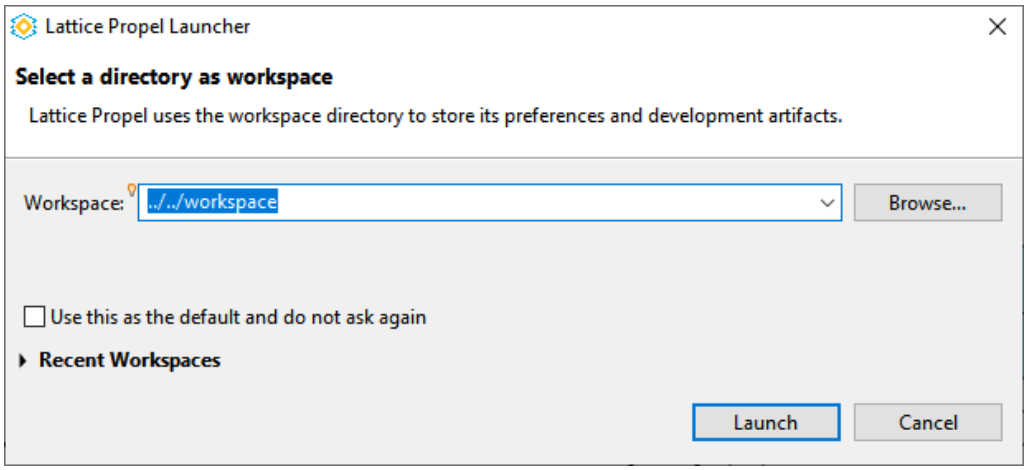


Figure 2.122. Lattice Propel Launcher Wizard

2. Click **Launch**. Propel SDK GUI opens. This C Project wizard is for loading the system and the board support package (BSP) to create a C/C++ project (Figure 2.123).

   Enter project name in the **Project Name** field, and then Click **Next**.

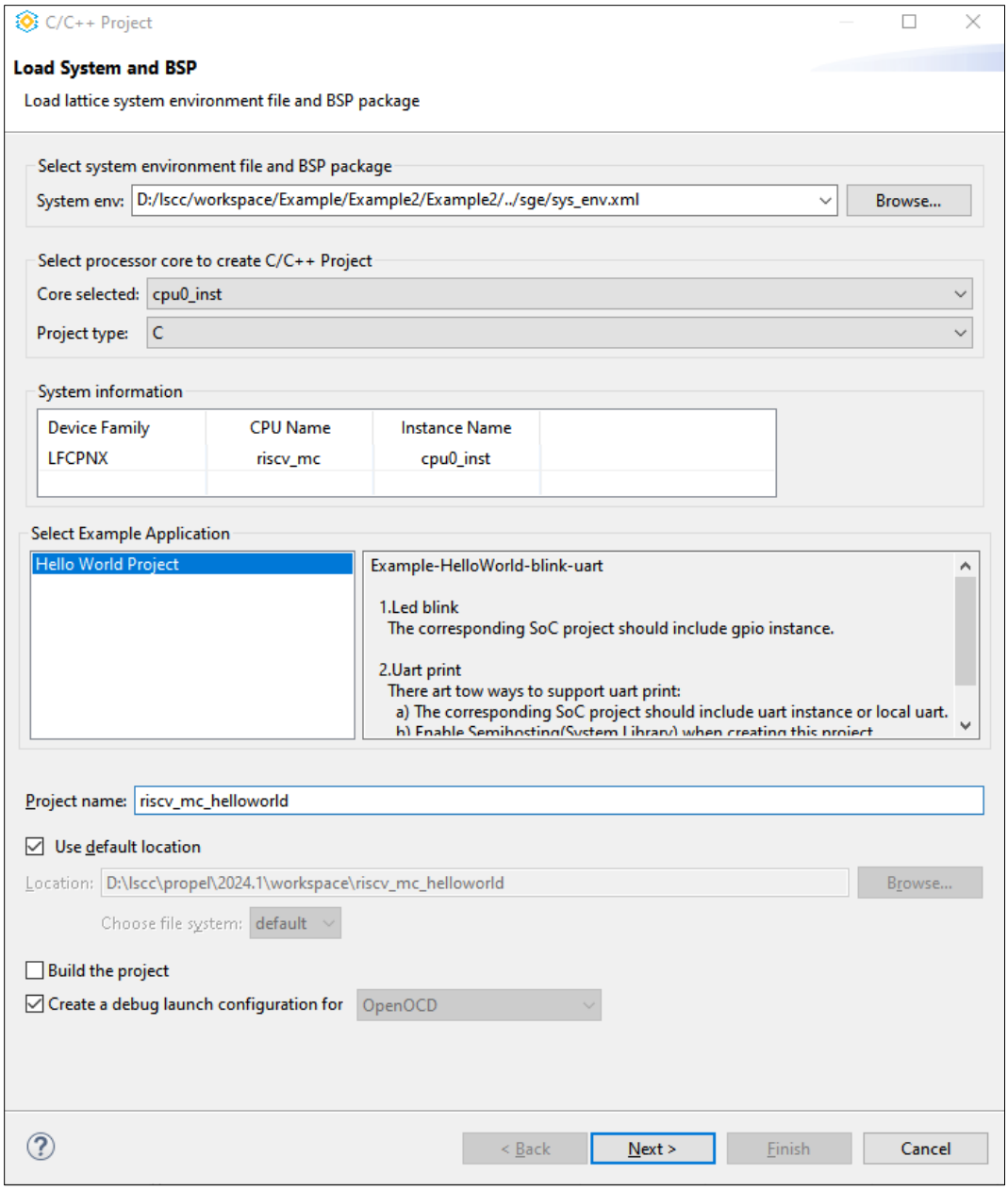


Figure 2.123. Propel SDK GUI and C/C++ Project Wizard

3. Click **Next**. The C/C++ project dialog (Figure 2.124) opens.

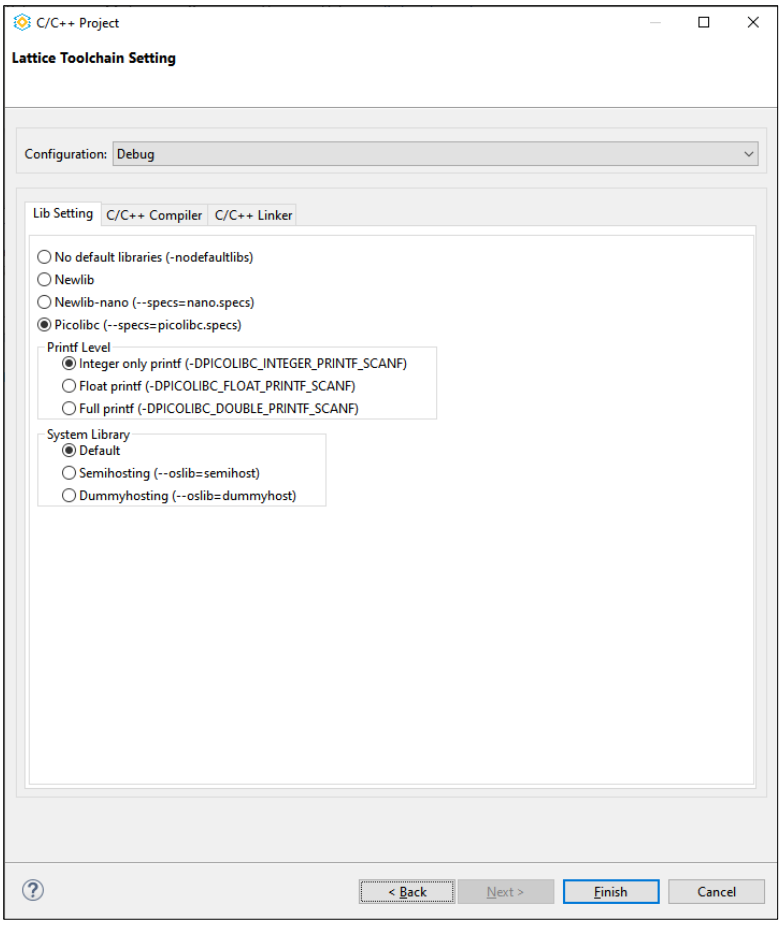


Figure 2.124. Create C/C++ Project

4. Click **Finish**. The C/C++ project is created and is displayed using the C/C++ perspective. A perspective is a collection of tool views for a particular purpose. The C/C++ perspective is for creating C/C++ programs.
5. Generate mem file in Propel SDK for simulation use:

   To use simulation, first we need to generate the initialization file of System Memory instance (mem file) in Propel SDK for simulation program to run on in verification project of Propel Builder.
6. In Propel SDK, right click on Project and then click **Build Project** (Figure 2.125). A mem file is generated in **Debug** folder (Figure 2.126).

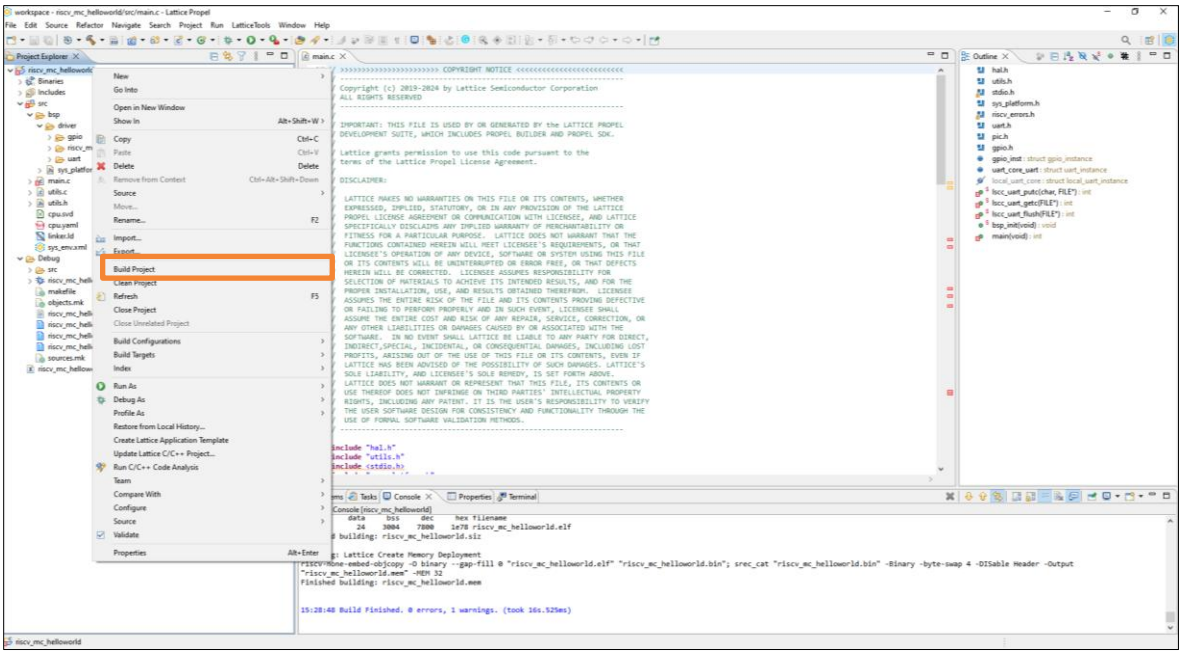


Figure 2.125. Build C/C++ Project

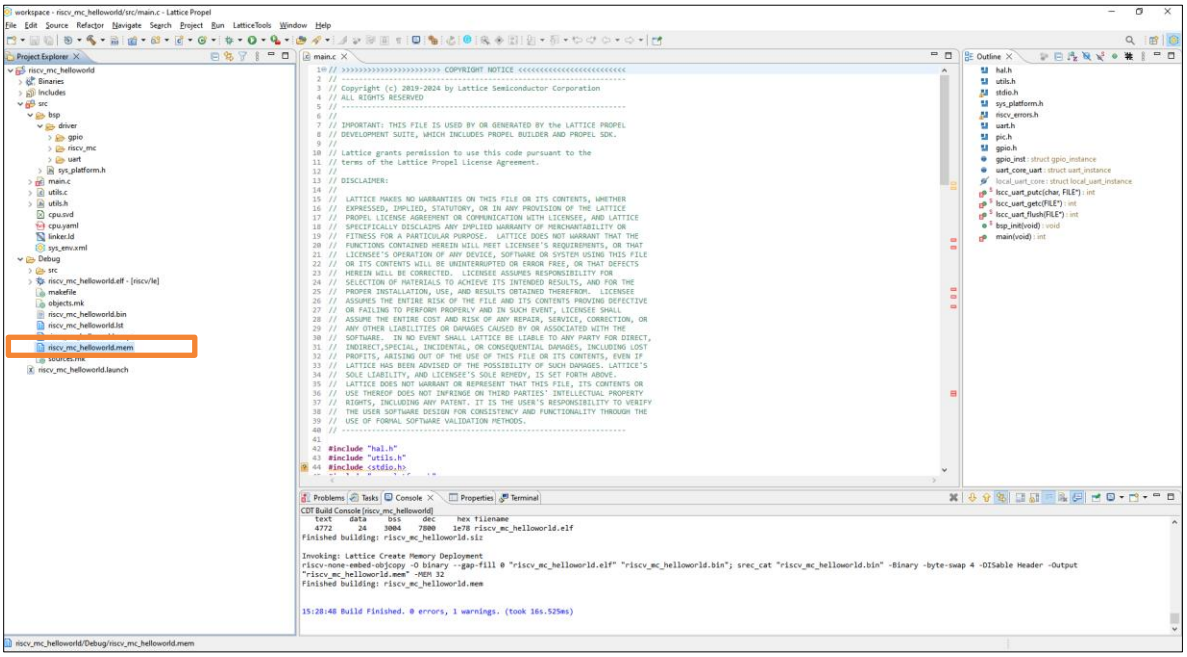


Figure 2.126. Mem File for Simulation

Right click on the mem file and choose **Show in > System Explorer** to get this file (Figure 2.127).

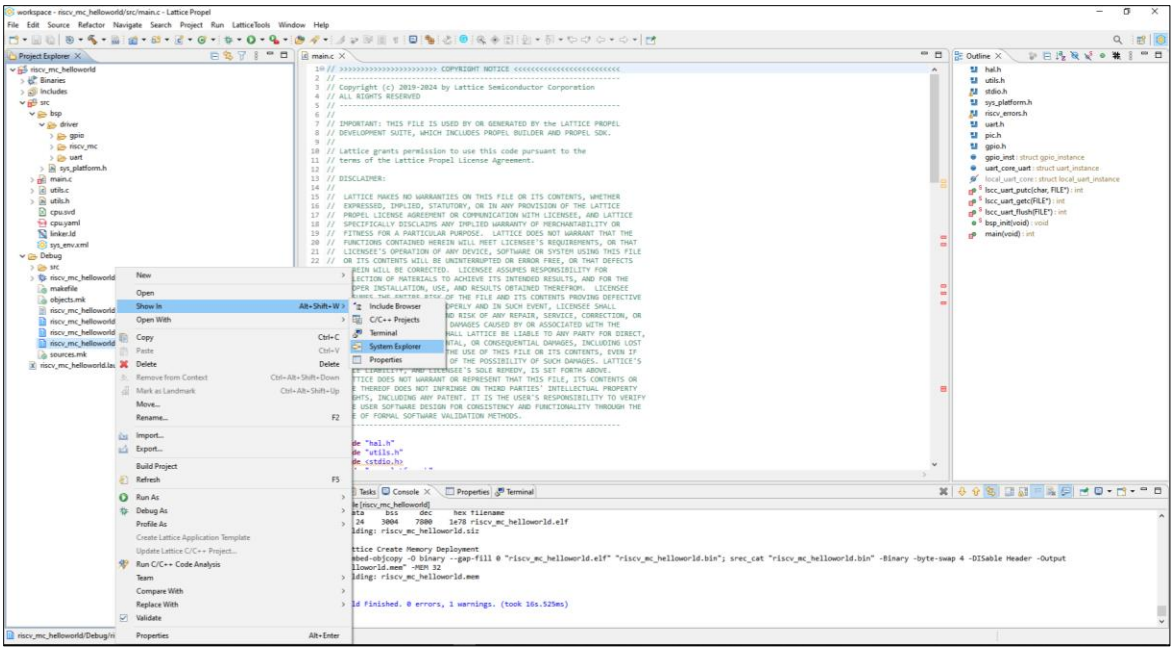


Figure 2.127. Mem File Location

7. Initialize memory for simulation:

   After generating mem file in Propel SDK, you need to initialize memory for System Memory IP in Propel Builder.

   In Propel Builder schematic view, **double-click** on system memory IP to open **Module/IP Block Wizard**. Click on **'none'** in the Initialization File area and then click on **'...'** to select mem file from project (Figure 2.128).

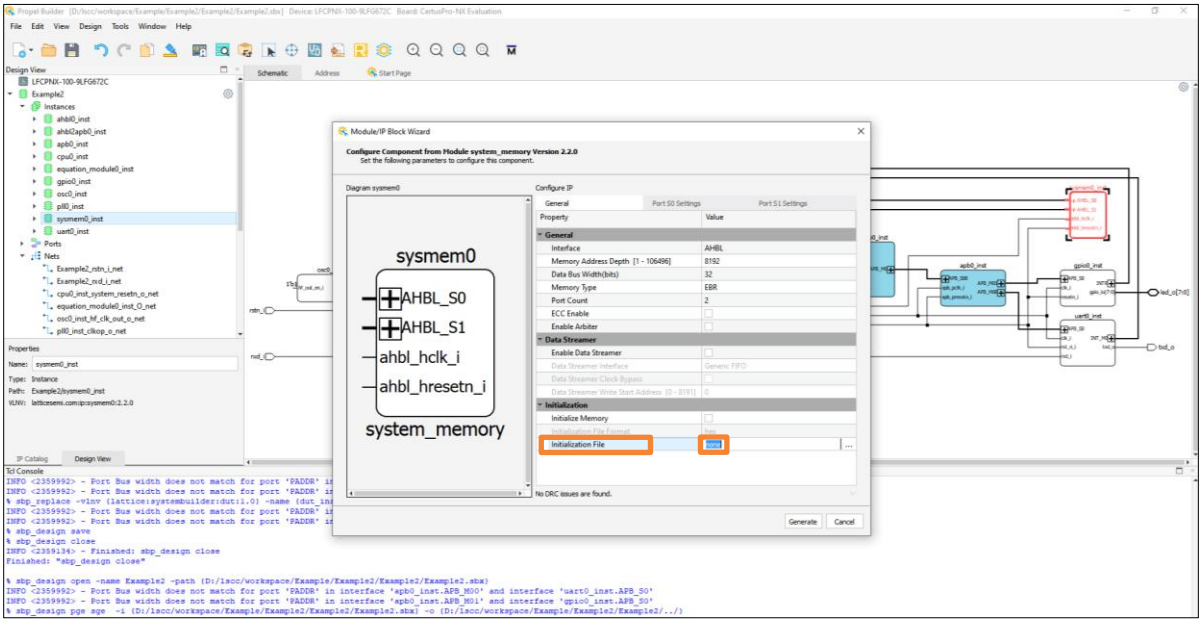


Figure 2.128. Initialize Memory for System Memory Module (1)

After the mem file is selected, check **Initialize Memory** (Figure 2.129).

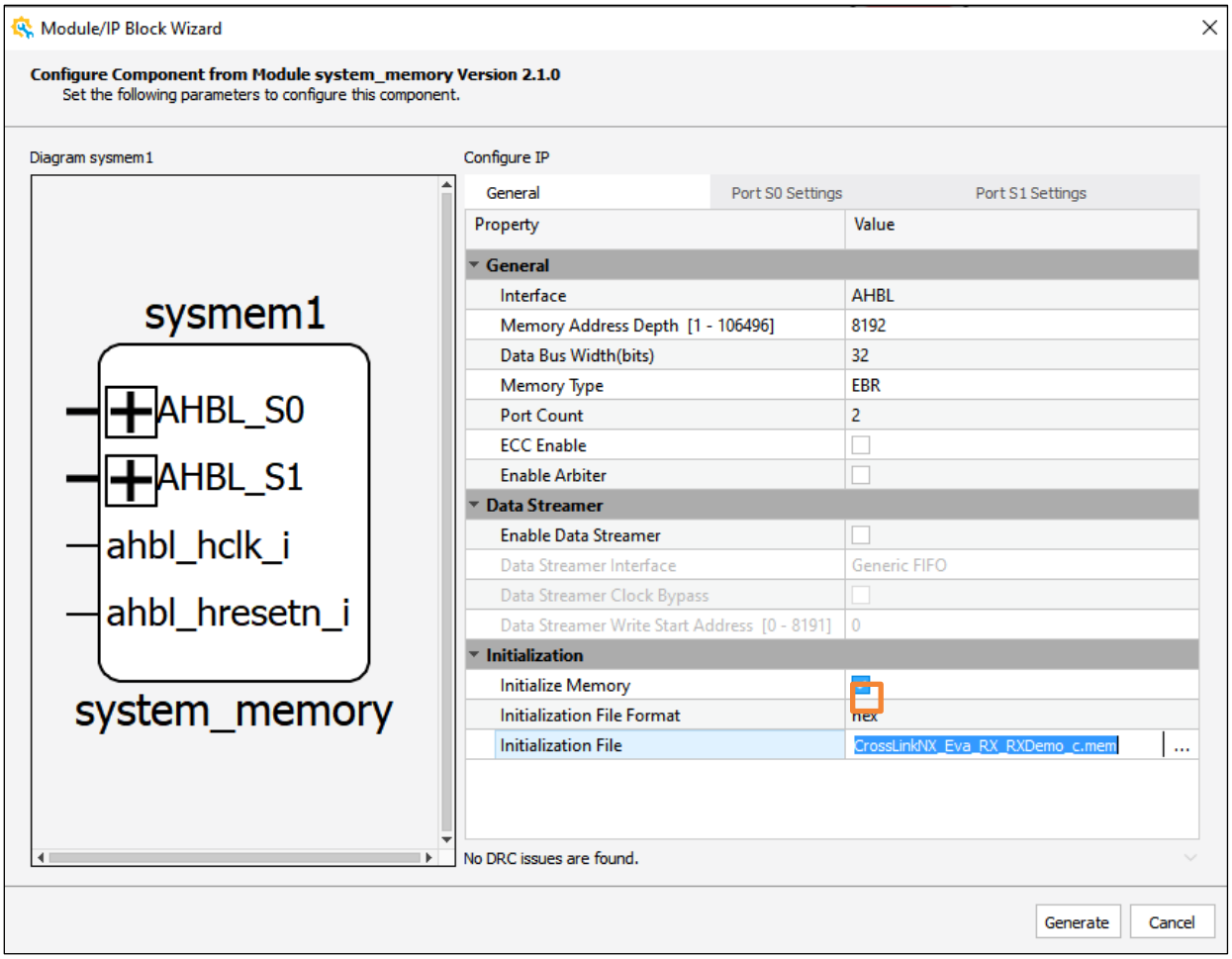


Figure 2.129. Initialize Memory for System Memory Module (2)

For a SoC design, if the initialization file of System Memory instance (mem file) is built again in C project, system memory instance should always be re-configured by double clicking on it in GUI .

Or, use the ECO flow to update the information.

ECO Editor in Radiant enables you to safely make changes to an implemented design without having to rerun the entire process flow. ECOs are requests for small changes to be made to your design after it has been placed and routed. Choose **Tools > ECO Editor** or click the **ECO Editor** button on the toolbar to open the ECO Editor. Choose the right memory component and upload the memory file (Figure 2.130).

Refer to the Lattice Diamond Help/Lattice Radiant Help for more info on how to use an ECO flow.

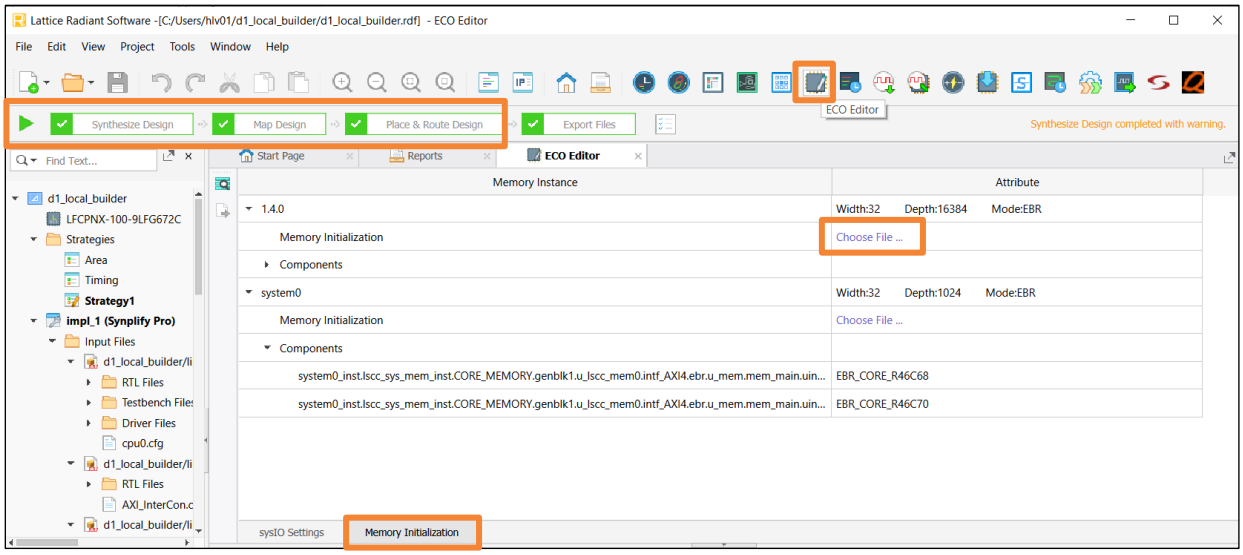


Figure 2.130. ECO flow in Radiant

2.3.14. Tools

2.3.14.1. IP Wrapper Creator

IP wrapper Creator is enabled when you open the SoC project in Propel Builder. Choose **Tools** > **IP Wrapper Creator** from Propel Builder menu bar. The Options Dialog opens (Figure 2.131).

You can set IP general information, and then click **Next**.

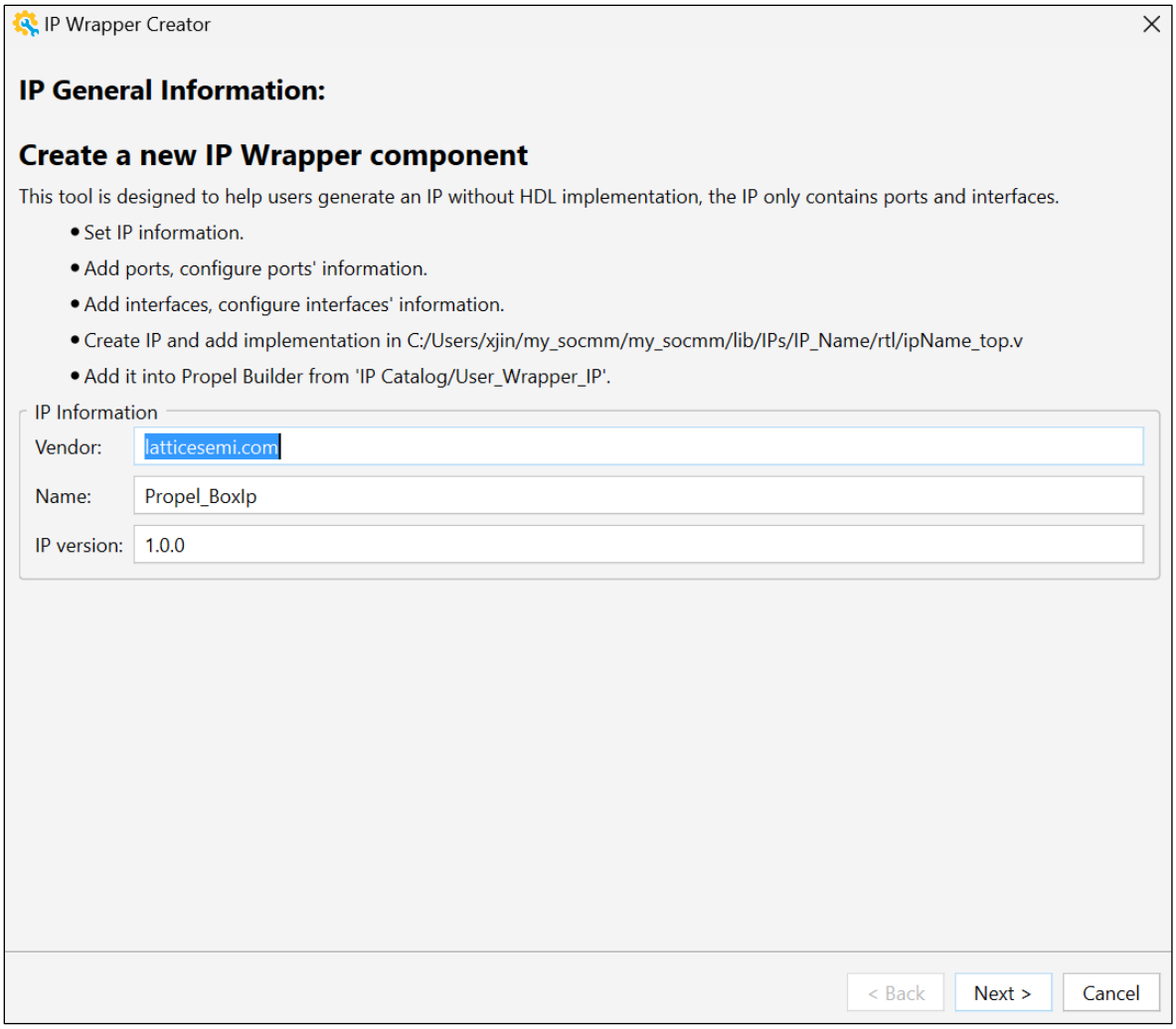


Figure 2.131. IP Wrapper Creator – General Information

You can add ports and set ports' properties (Figure 2.132), and double click on them if you want to change them, and then click **Next**.

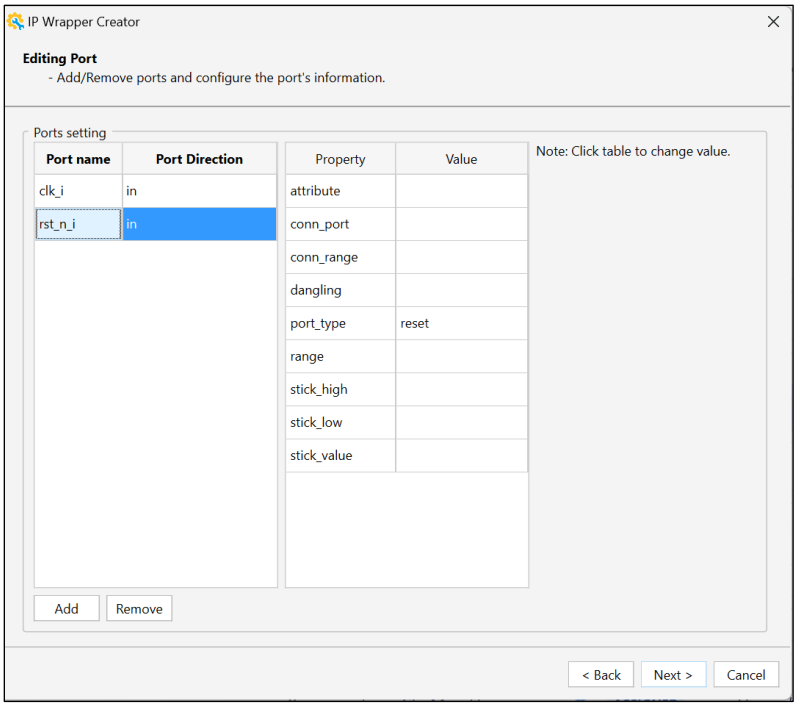


Figure 2.132. IP Wrapper Creator – Editing Port

You can add interfaces (Figure 2.133), and then click **Next**:

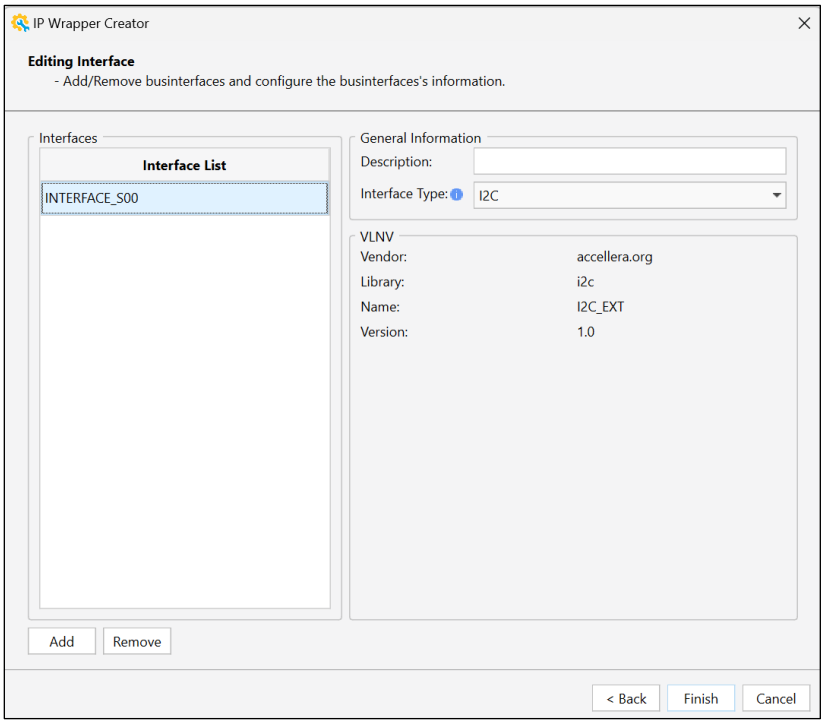


Figure 2.133. IP Wrapper Creator – Editing Interface

You can add HDL implementation in ip_top.v under project (Figure 2.134).

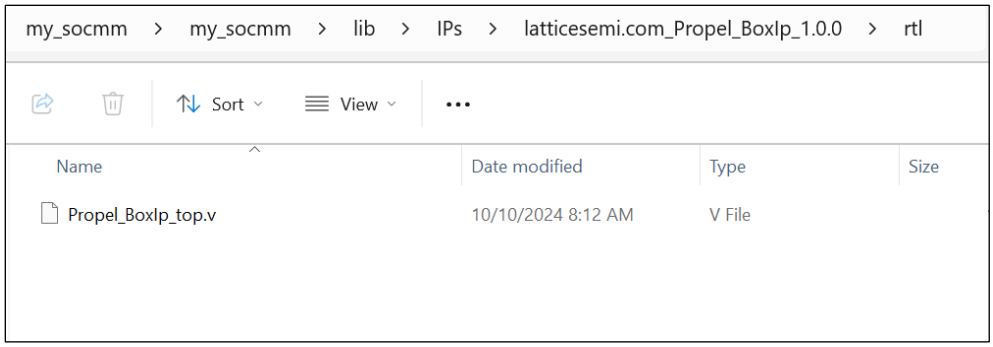


Figure 2.134. Edit in Top.v

After an IP is created, you can add it into project from IP Catalog/User_Wrapper_IP (Figure 2.135):

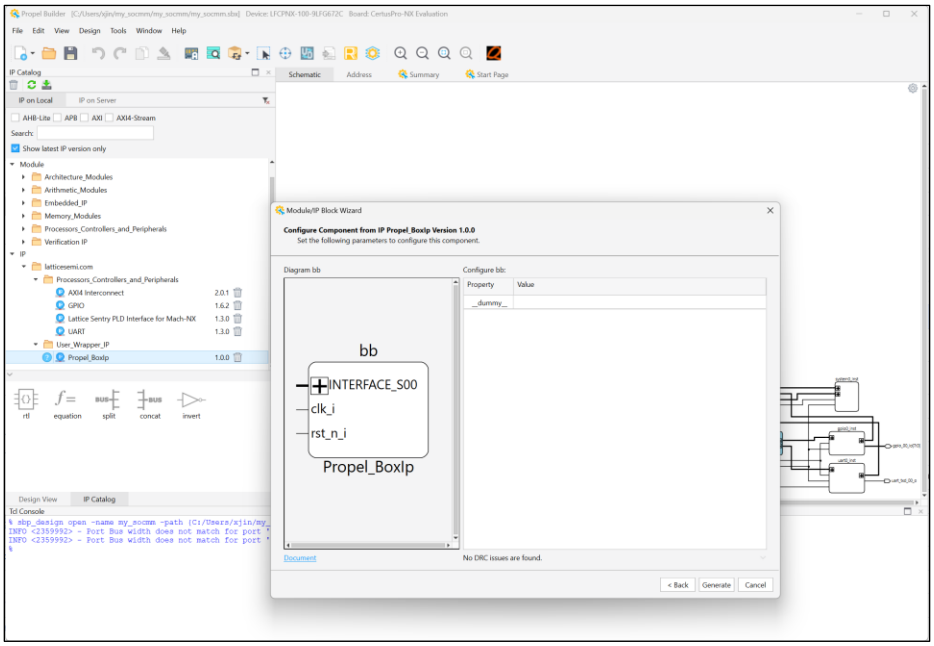


Figure 2.135. Add IP to Project

2.3.14.2. Tools Options

Choose **Tools** > **Options** from Propel Builder menu bar. The Options Dialog opens (Figure 2.136).

- Theme

You can choose Light/Dark theme from pull-down menu.

Note: A restart of Propel Builder is required to take effect of the theme change (Figure 2.136).

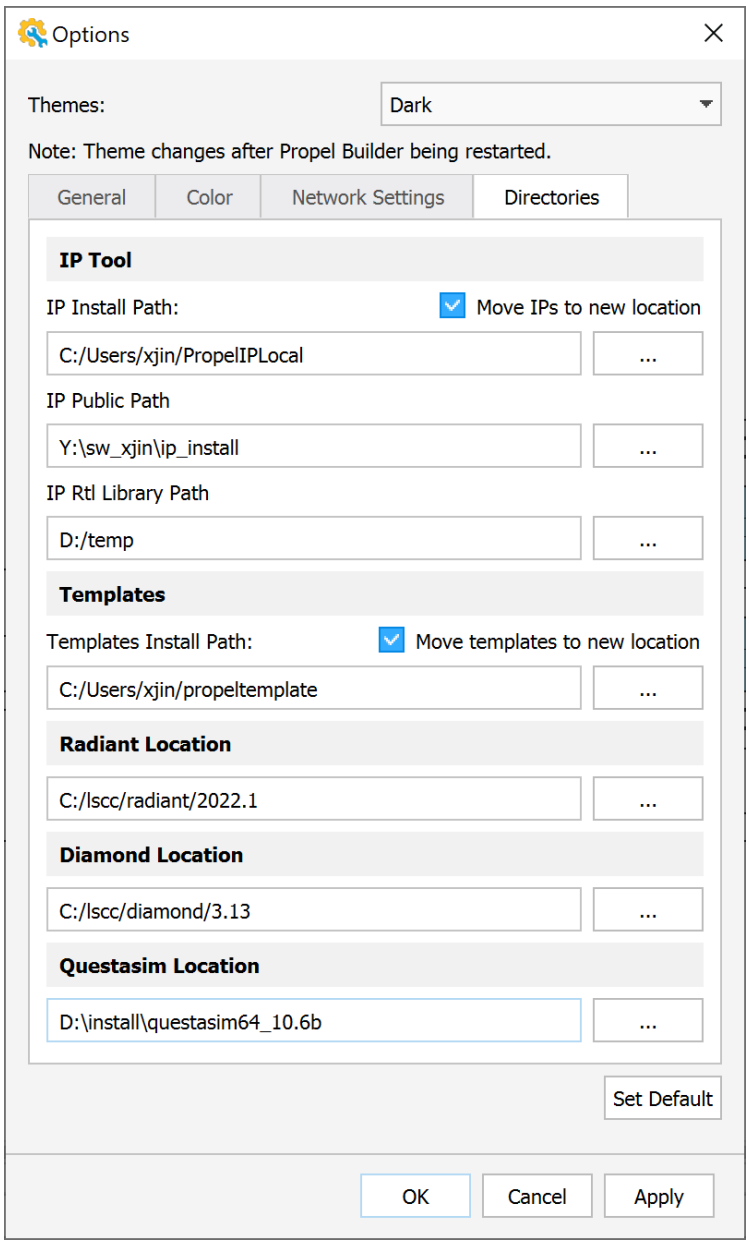


Figure 2.136. Theme Change

- General

In general page (Figure 2.137), you can use the right mouse button for zooming actions. See the Methods to Zoom section for more details.

The Automatically connect after instantiating an instance option is shown in this **Options** dialog. Click **Apply** to make this function take effect.

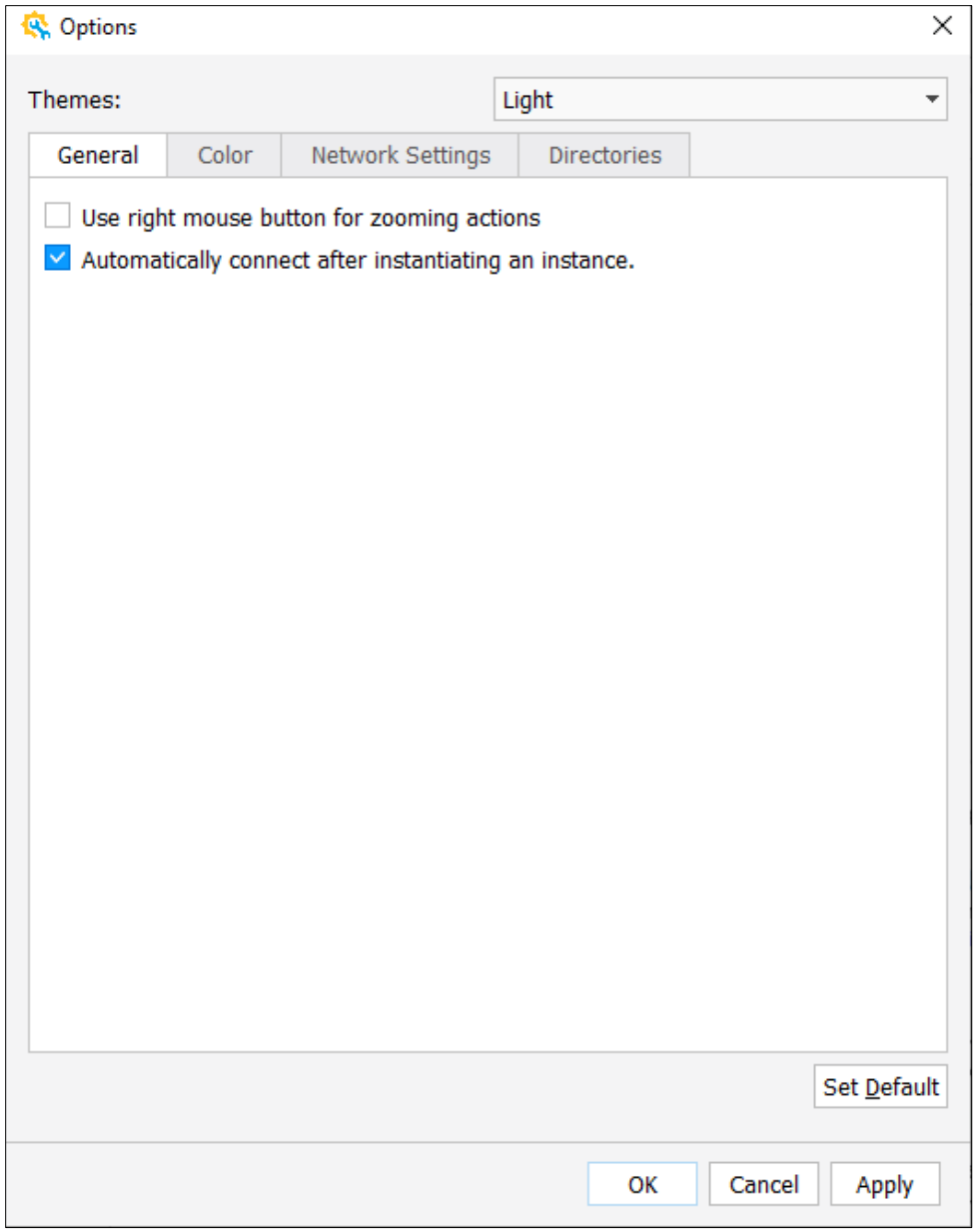


Figure 2.137. General Options

When this auto-connect function is enabled, when an instance is instantiated (see Generating and Instantiating IP/Module section for instantiate an IP), after clicking **OK** in **Define Instance** dialog (Figure 2.138), an addition dialog box pops up with some suggested Clock/Reset connection for the ports on this IP (Figure 2.139). Check/Uncheck to make the desired connections.

For functional use, refer to Connect Pins by Auto Connect for more details.

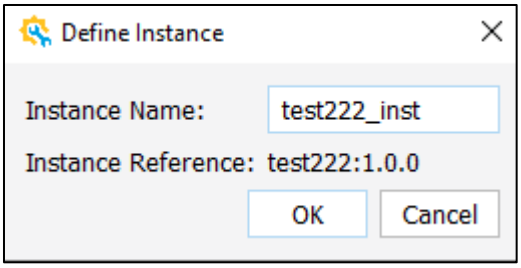


Figure 2.138. Define Instance Dialog

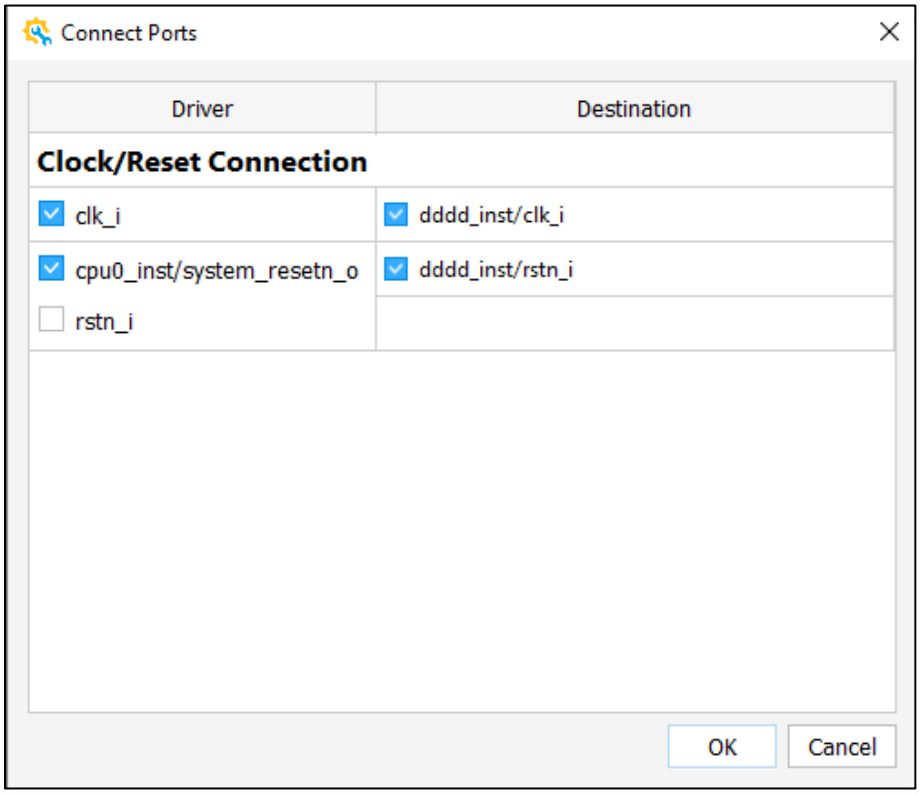


Figure 2.139. Connect Ports Dialog

- Color

You can customize color for elements in Propel Builder (Figure 2.140), such as: the color of **Error/Warning/Info Message**, schematic background, highlight.

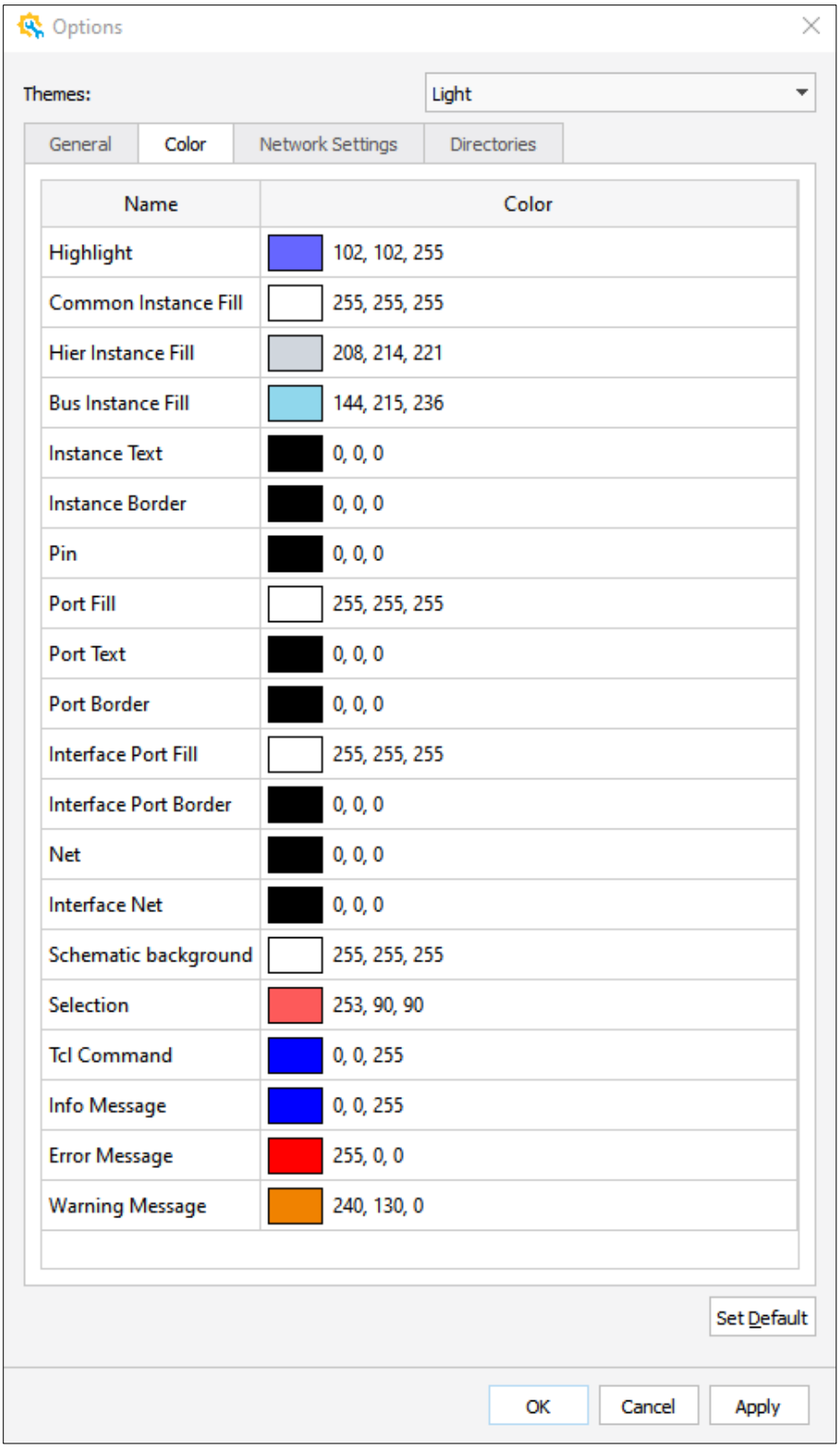


Figure 2.140. Color

- Network Settings

If you need to use a proxy server, click this **Network Settings** tab (Figure 2.141). Make the appropriate selections on this tab.

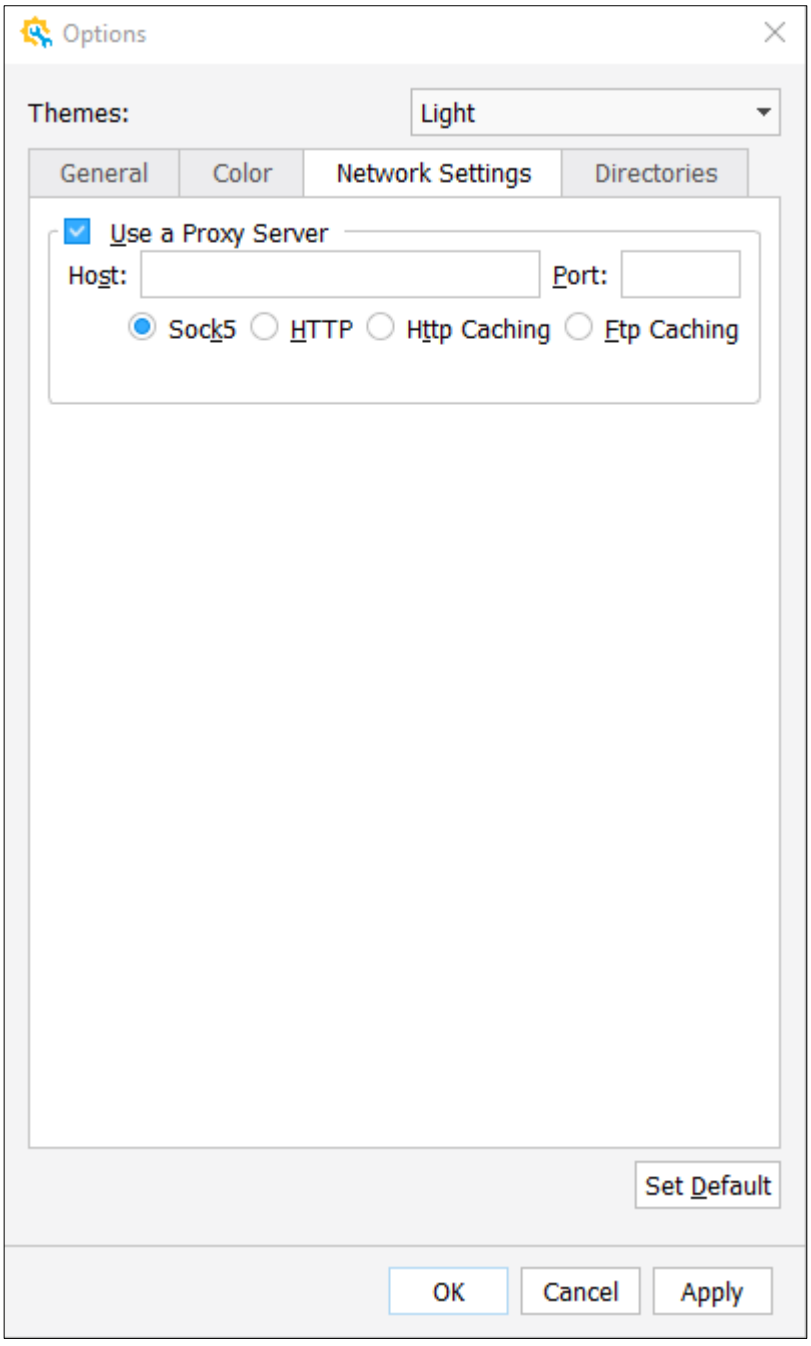


Figure 2.141. Network Settings

- Directories

On this **Directories** tab (Figure 2.142), there are path setting for related tool.

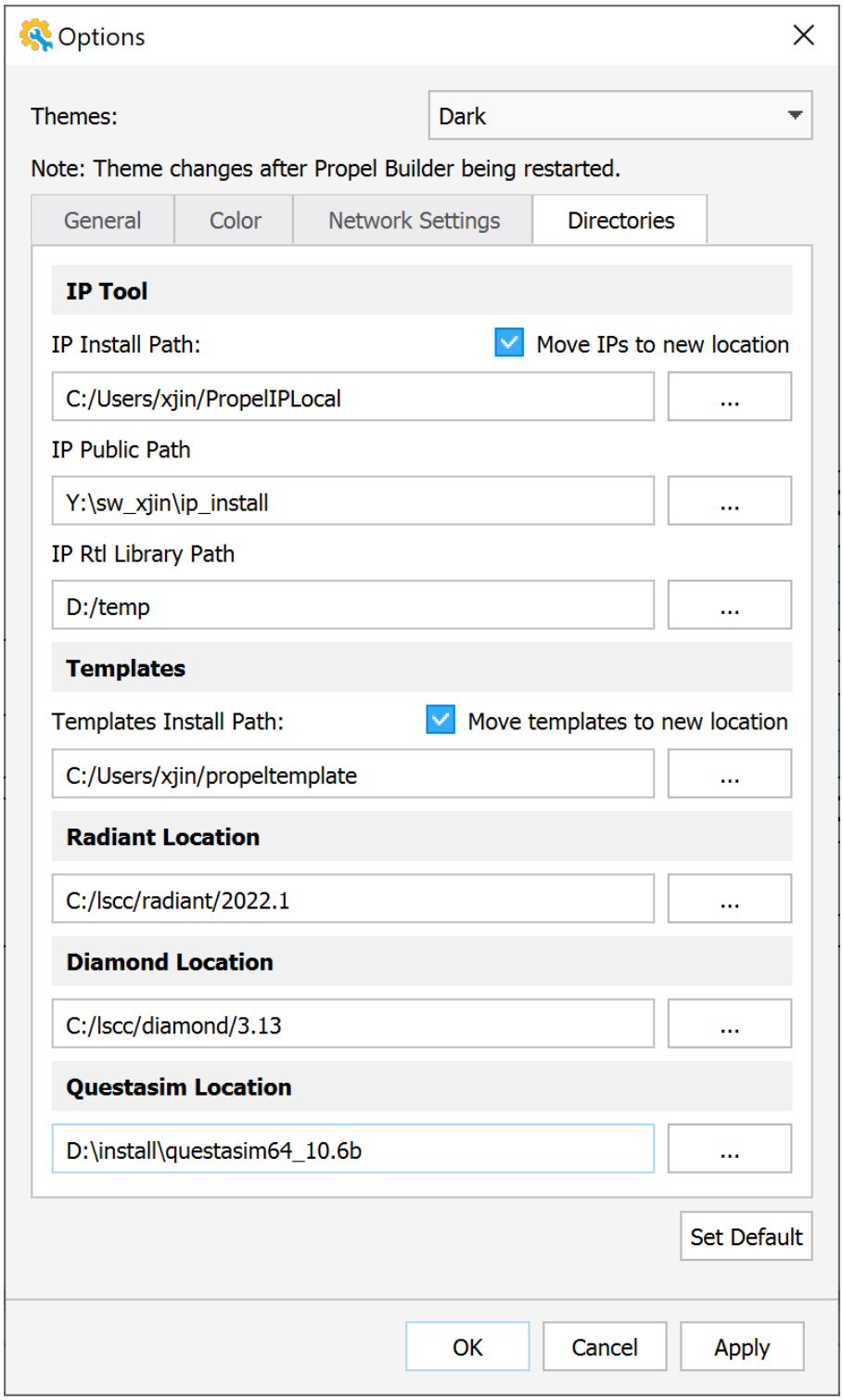


Figure 2.142. Directories

Introduction for installation location:

- Radiant Location (Figure 2.143): Folder where Radiant software installed.
- Diamond Location (Figure 2.143): Folder where Diamond software installed.
- Questasim Location (Figure 2.143): Folder where Questasim software installed (see Launching Simulation section for more information).

Note:

It is recommended to use the same version of Radiant and Propel for best compatibility. If the Radiant version is not compatible with current Propel version, there are warning message(Figure 2.143). If no Radiant is set, Propel Builder use the latest Radiant it detects.

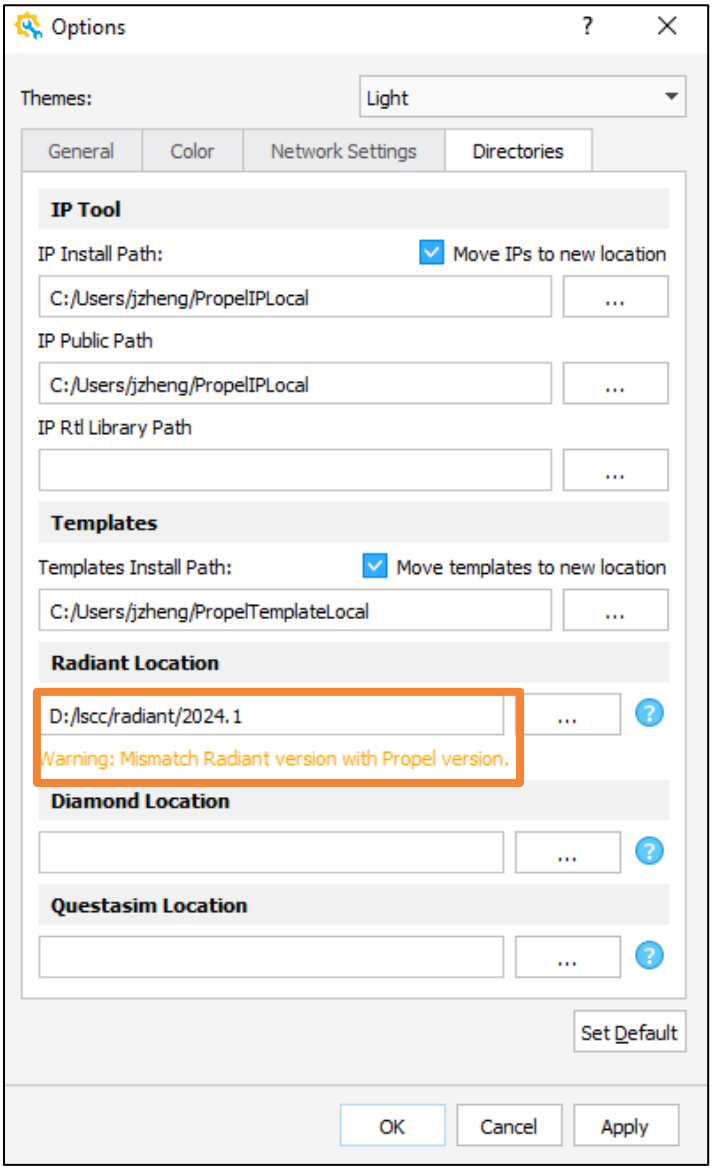


Figure 2.143. Mismatch Radiant with Propel

If the location path user input is not legitimate, a warning message pops up (Figure 2.144).

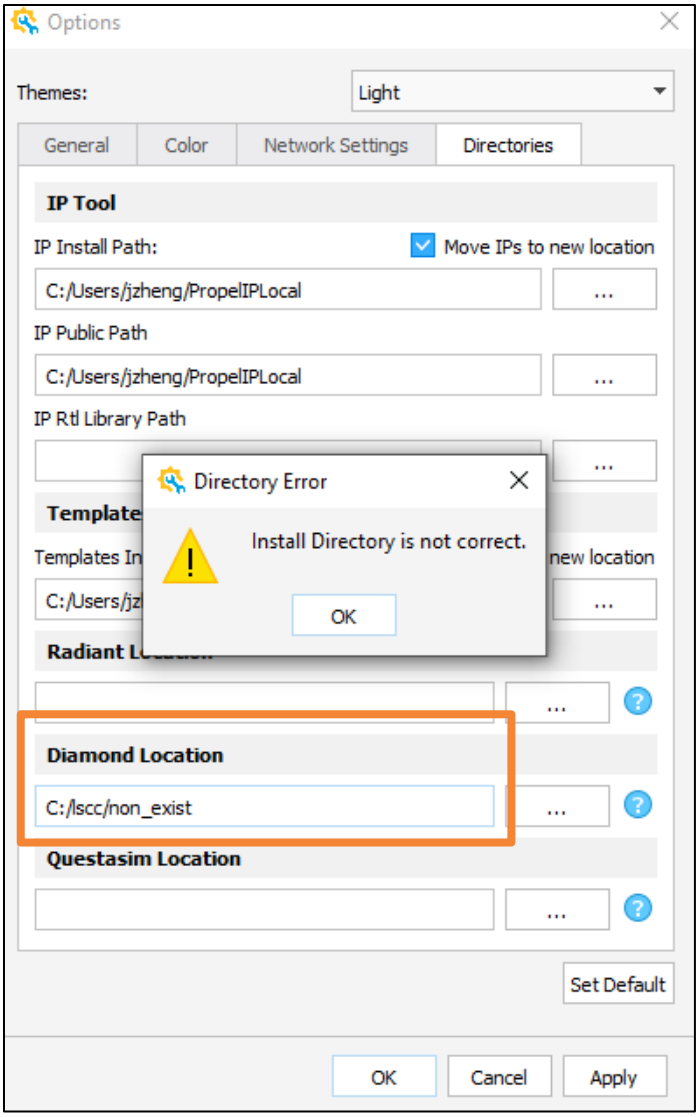


Figure 2.144. Location warning

Introduction for IP Tool (Figure 2.143):

- IP Installed Path (Figure 2.143): Folders of the IPs that are downloaded and installed. Refer to the Generating and Instantiating IP/Module section for more details.
- IP Public Path (Figure 2.145):

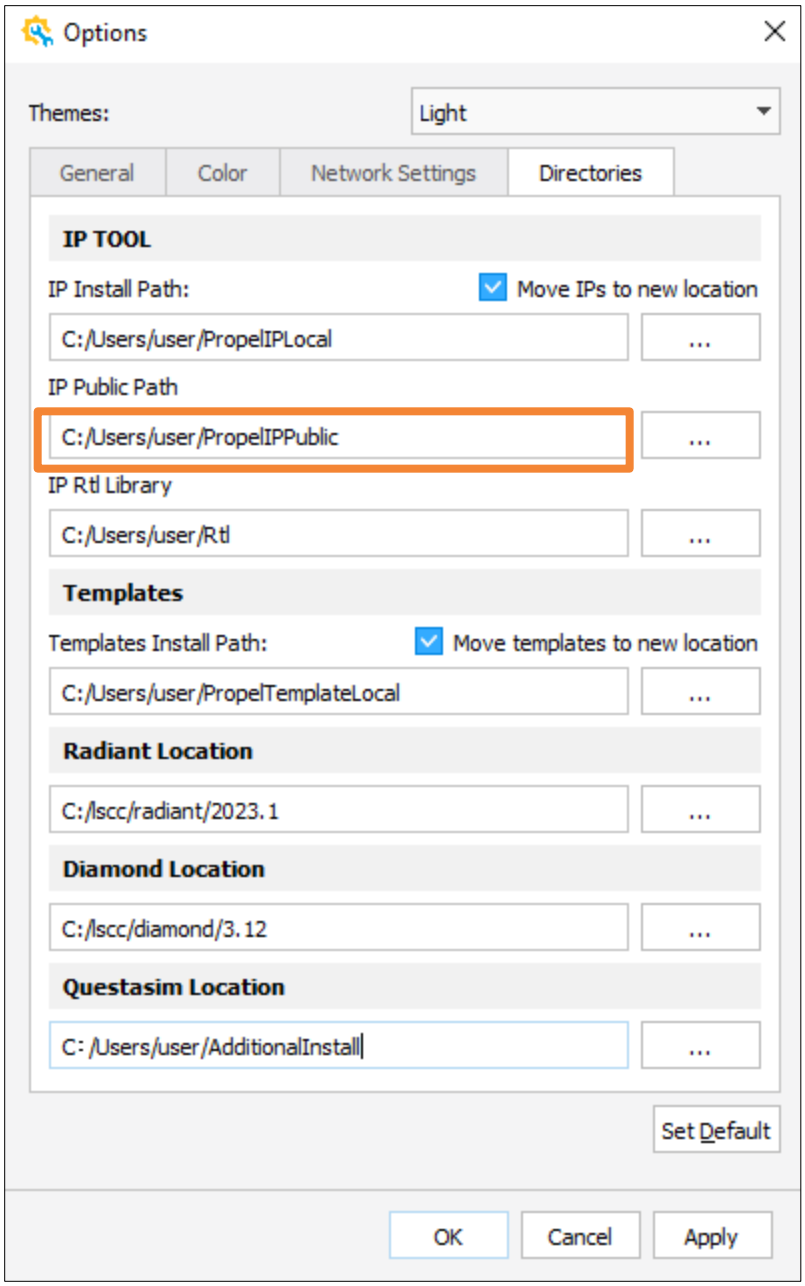


Figure 2.145. IP Public Path

IP Public Path is for administrator user to manage the public IP, and for general user to use the public IP.

Note: Make sure the path is accessible in your current system, without any additional transfer App installed.

- For administrator user to manage the public IP:
  - The administrator user must have the write permission to this path.
  - If the administrator user wants to install or remove IP from the IP Public path, just set this as the same path in the **IP Install Path** and then install/remove IP in **IP catalog**.
- For general user to use Public IP:
  - The general user must have the read permission of this path.
  - Set the IP Public Path, and then refresh **IP catalog** to get IP from this path (Figure 2.146).

Note:

IP Public Path does not support network path in Windows Operation System (OS), for example, \\192.168.11.11\shared\ip. Workaround for this is to map the Network Drive with the network path and set the path with a local disk (Figure 2.147).

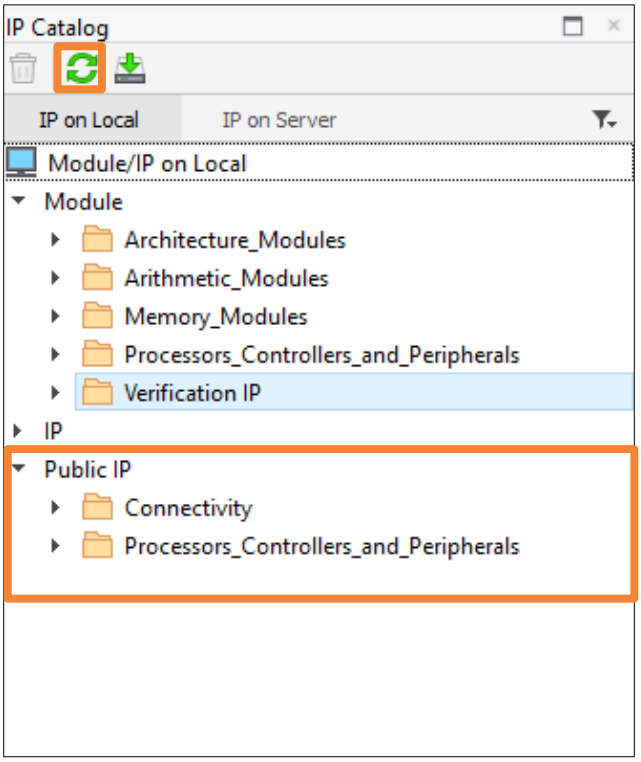


Figure 2.146. IP Catalog

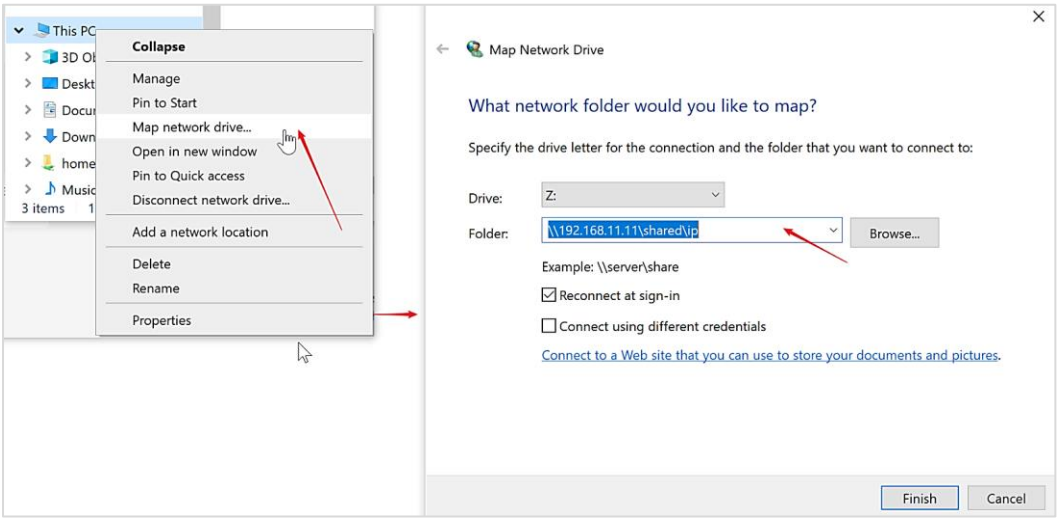


Figure 2.147. Map Network Device

- IP RTL Library (Figure 2.145): Folders of the IP RTL library. Refer to Lattice Propel 2025.2 IP Packager User Guide (FPGA-UG-02242) for more details of the IP RTL Library.

Introduction for Templates (Figure 2.145):

- Templates Install Path: Folders where the templates installed. See the Define Custom Template section for more details.

2.3.15. TCL Console Auto-suggestion/Completion

Propel Builder supports TCL Auto-suggestion/Completion function in TCL Console.

A complete widget pops up with a Tab that can be pressed. When you input half of a TCL command (Figure 2.148), pressing the Tab or pressing **Enter** can complete the TCL command that is currently selected.

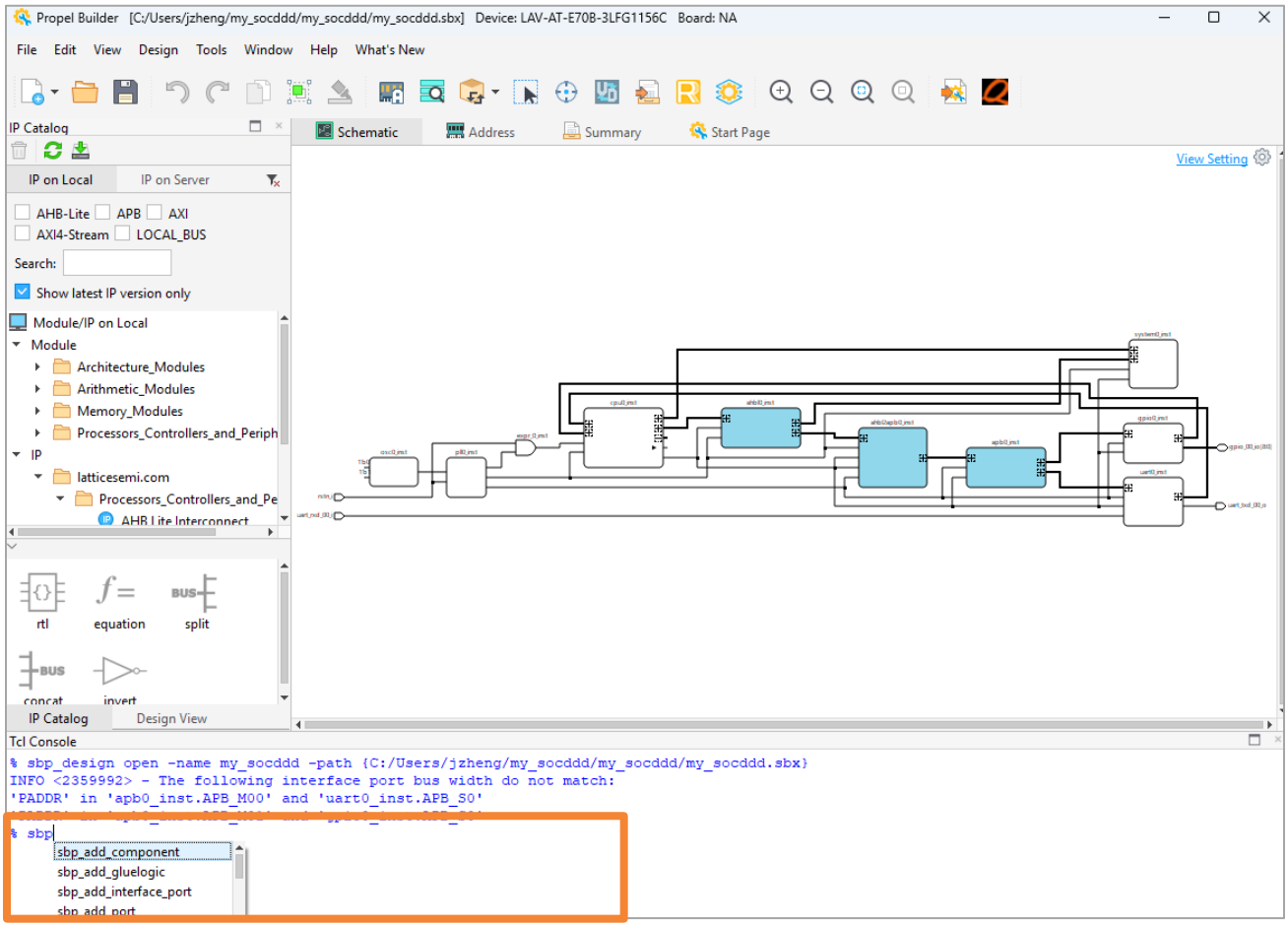


Figure 2.148. TCL Auto-suggestion/Completion

2.3.16. License Debugger Tool

The License Debug tool can help you debug license problems you may encounter when setting up a license for the Propel Builder.

If the Propel Builder closes after starting due to a license issue, the License Debug tool automatically launches. The missing license feature that caused the Propel Builder to exit is displayed in a text box to help with debugging.

You can also launch the tool manually using the **Help** > **License Debug** command.

2.3.16.1. Using the License Information Tab

1. Launch the tool by **Help** > **License Debug**. The License Information tab is displayed by default. The License File text box displays one or more license file(s) or license server(s), separated by semicolon(s).

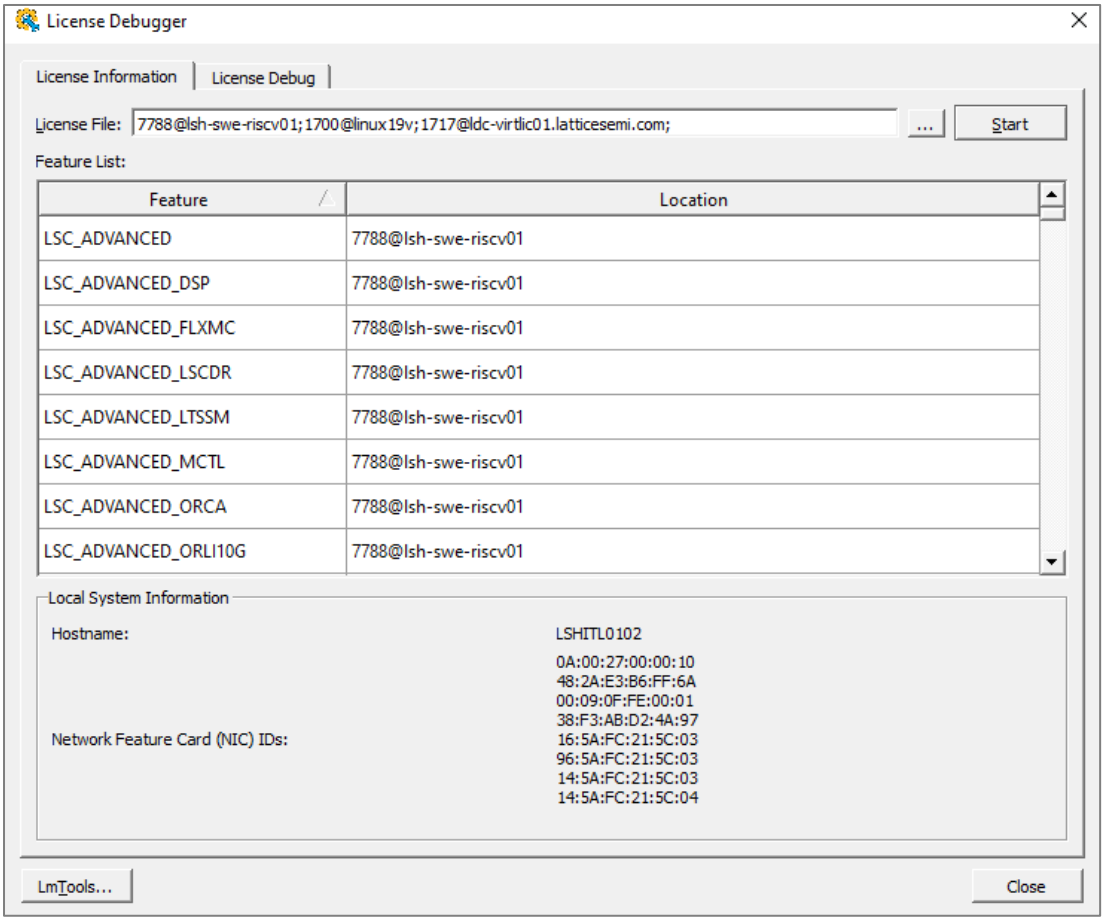


Figure 2.149. License Debugger Tool - License Information

2. Click the ... button to browse to the location of the license file (license.dat).
3. Click **Start** to display the feature list based on the specified license file(s). The **Feature List** box displays Feature(s) and file **Location**.

   The **Local System Information** box at the bottom displays the Hostname and Network Feature Card (NIC) ID. If multiple cards are available, all the NIC IDs are displayed.
4. If you need to administer the license server, click **LmTools…** to launch LMTOOLS Utility by Flexera.

The LMTOOLS Utility is a graphical user interface that enables you to administer the license server.

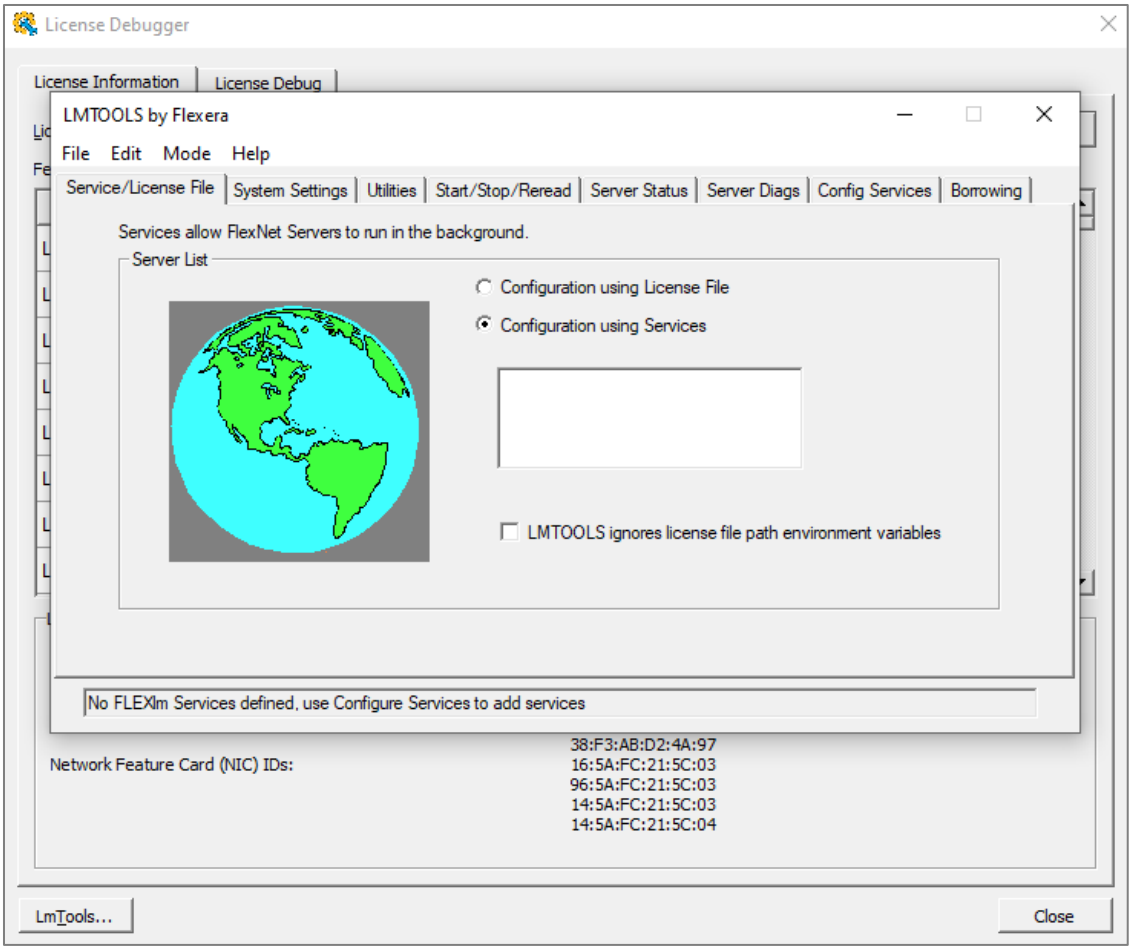


Figure 2.150. License Debugger Tool – LMTOOLS

Some of the functions LMTOOLS performs include:

- Starting, stopping, and configuring license servers.
- Getting system information, including HostID's.
- Getting server status.

LMTOOLS has two modes in which to configure a license server:

- Configuration using a license file.
- Configuration using services.

You must run LMTOOLS as an administrator. If you do not run this executable as an administrator and if the UAC prompt is not disabled on the system, the User Account Control (UAC) dialog is displayed when it is launched,.

For more information about LMTOOLS, please refer to the *FlexNet Publisher License Administration Guide* at https://www.revenera.com.

2.3.16.2. Using the License Debug Tab

1. Choose **Help > License Debug** to launch the License Debug tool.
2. Click the License Debug tab (Figure 2.151).

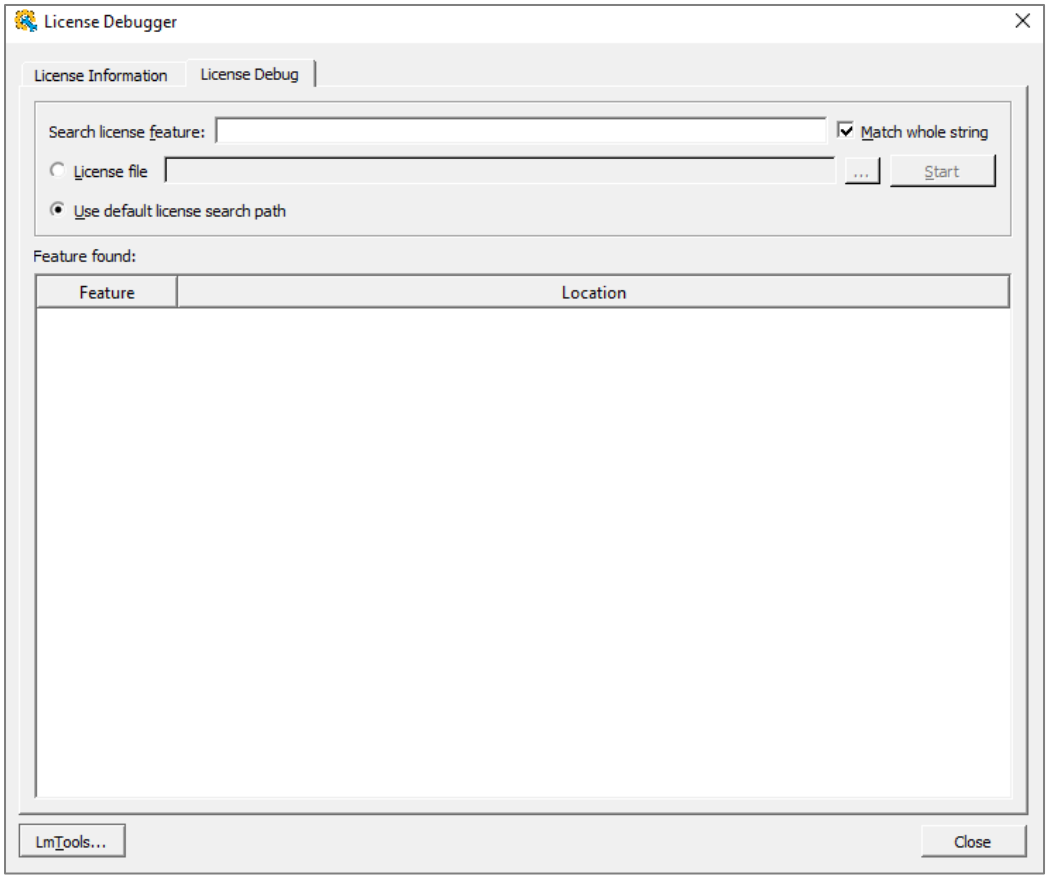


Figure 2.151. License Debugger Tool – License Debug

3. In the **Search License Feature** box, type in the license feature text string you wish to find.

   Click the **Match Whole String** box if you wish to match the entire string. If you uncheck the Match Whole String box, you can search for partial string.

4. Click the ... button to browse to the location of the license file (license.dat).

   Or click the Use Default License Search Path button.

5. Click **Start** to display the feature list based on the specified license file(s). The Feature List box displays Feature(s) and file Location.

To know more about licensing, visit the Software Licensing page.

2.3.17. Others

2.3.17.1. Modifying the Project Settings

Propel Builder supports changing the projects settings. You can modify the device, package, speed and operating conditions by double clicking the device part number from the Design View.

1. Double click the device part number from the Design View (Figure 2.152), the Modify Device Info wizard pops up (Figure 2.153).

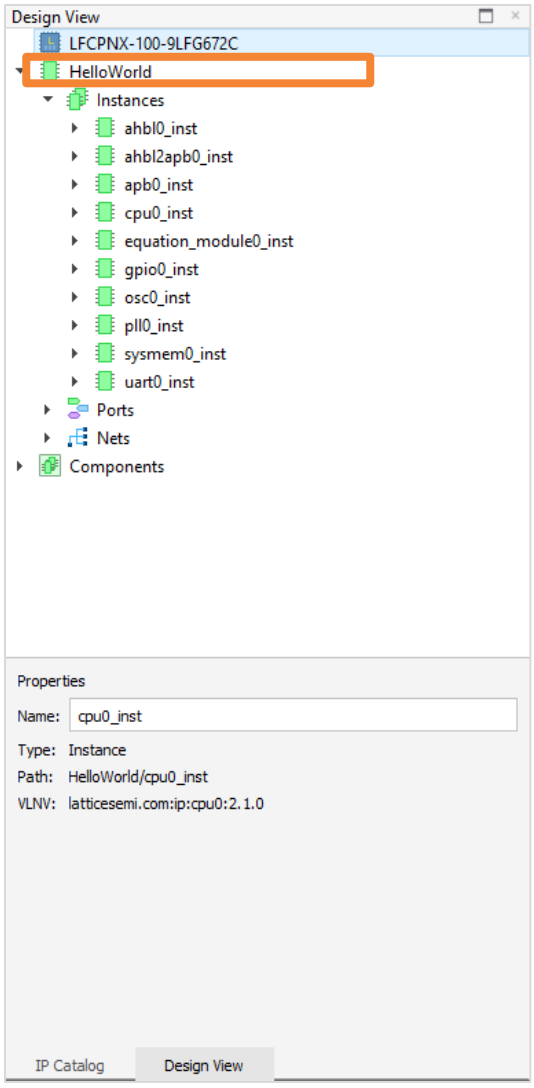


Figure 2.152. Design View of Device Part Number

2. Use the drop-down menu to choose the desired device in **Device** filed in the Modify Device Info wizard (Figure 2.153). Use the drop-down menu to change the package, speed and operating condition in **Package**, **Speed**, **Operating Condition** filed.

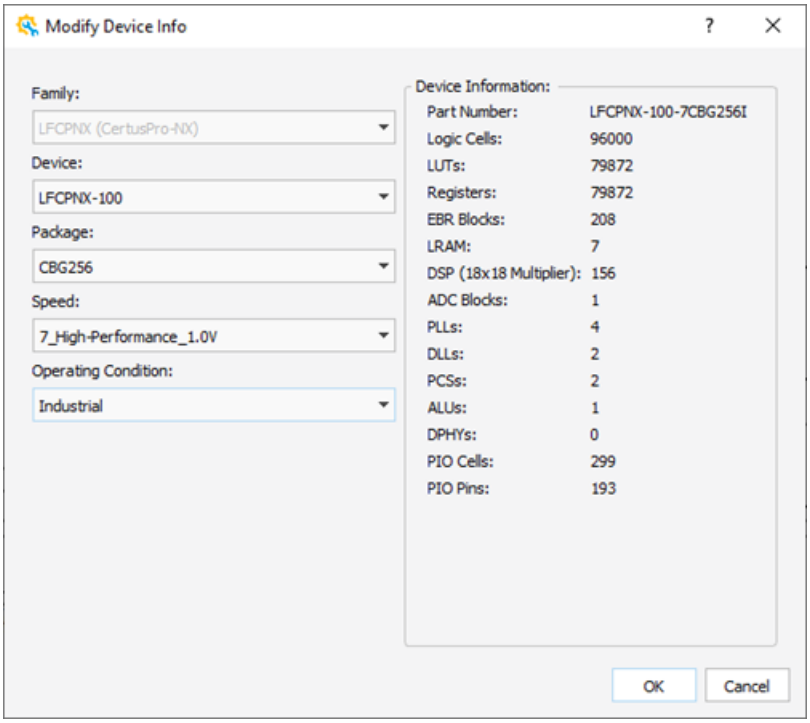


Figure 2.153. Modify Device Info

3. Click **OK**. The System Builder dialog (Figure 2.154) pops up showing a message of configuring all IPs.

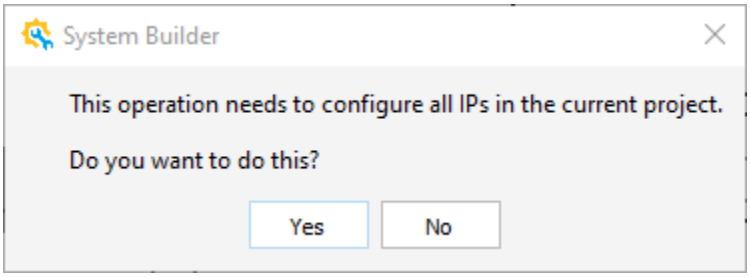


Figure 2.154. System Builder Dialog

4. Click **Yes**. By clicking **Yes**, the Builder engine regenerates each IP in the project with the updated device settings. All IPs in current project are configured. The new device part number shows in Design View (Figure 2.155).

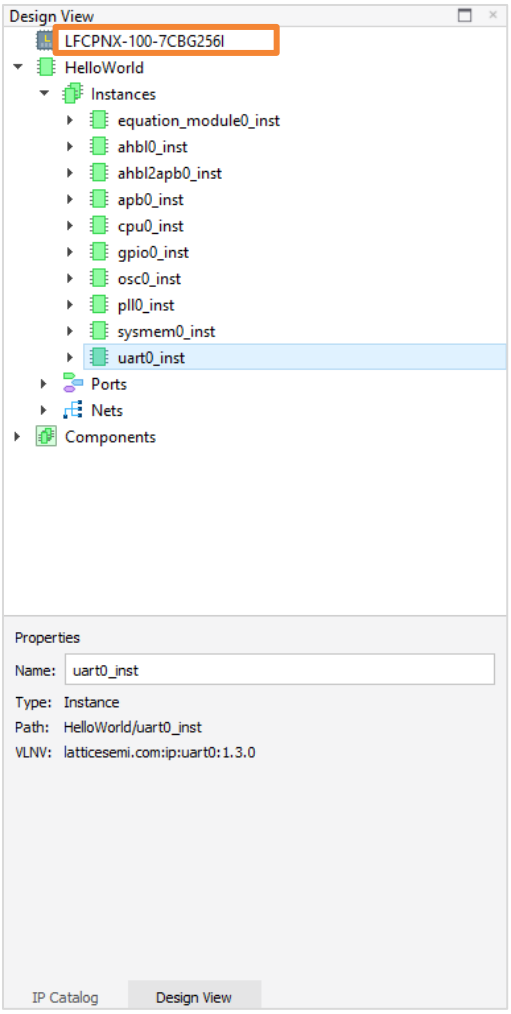


Figure 2.155. Design View of Device Part Number

2.3.17.2. Undo/Redo

Propel 2025.2 Builder supports one-level undo/redo. You can click the **Undo** icon from the Propel Builder Toolbar to go back to last action. Click the **Redo** icon from the Propel Builder Toolbar to recover last undo action.

- Undo: Choose **Edit** > **Undo** from the Lattice Propel Builder Menu bar. Or, click the **Undo** icon from Propel Builder GUI Toolbar.
- Redo: Choose **Edit** > **Redo** from the Lattice Propel Builder Menu bar. Or, click the **Redo** icon from Propel Builder Toolbar.

Note: Currently, Propel 2025.2 Builder only supports single-time undo/redo.

2.3.17.3. Modifying Color Settings for Project Level

On Schematic View, click on **View Setting** to open dialog (Figure 2.156).

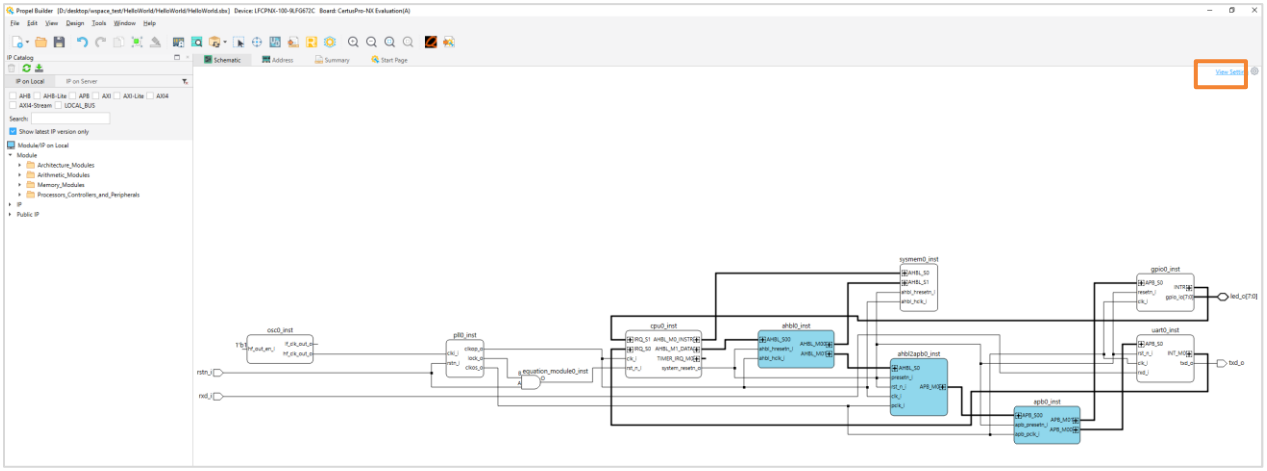


Figure 2.156. View Setting

This setting is on Project Level (Figure 2.157), which has higher priority than Software Level Setting. See Tools Option – Color section for more details.

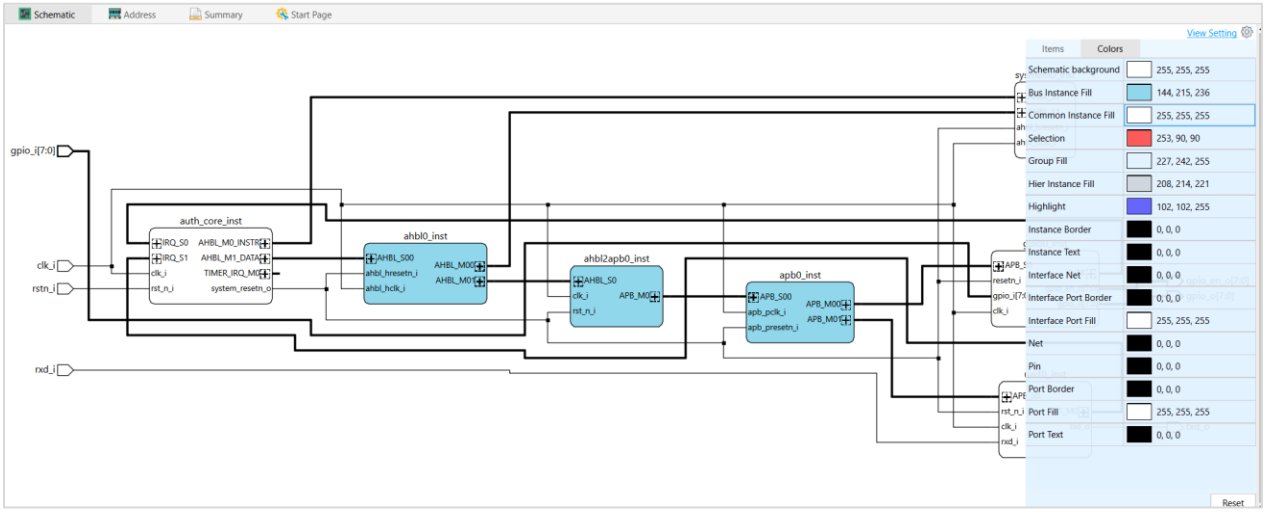


Figure 2.157. View Colors Setting

2.4. Verification Project Flow

2.4.1. Creating a Verification Project

1. Choose **File** > **New Design** from Lattice Propel Builder Menu Bar. The Create System Design wizard opens (Figure 2.158).

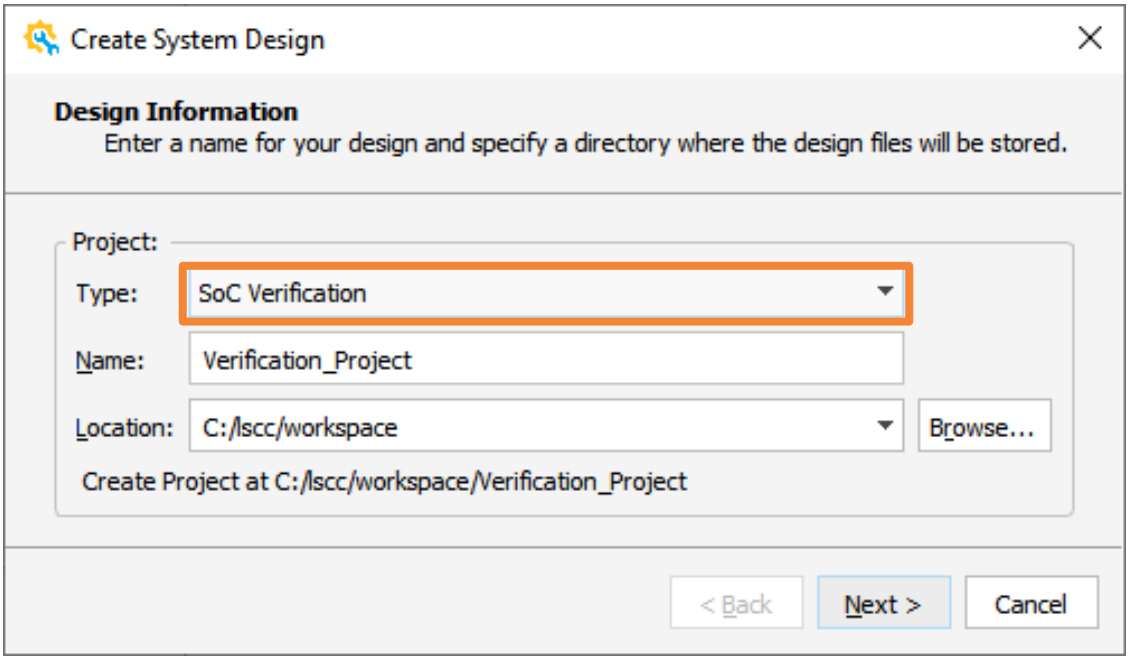


Figure 2.158. Create System Design – Design Information Wizard

2. Choose SoC Verification from the **Type** field.
3. Enter a project name in the **Name** field.
4. (Optional) Use the **Browse** option to change the project location in the **Location** field if needed.
5. Click **Next**. The Propel Project Configure wizard is shown as Figure 2.159.

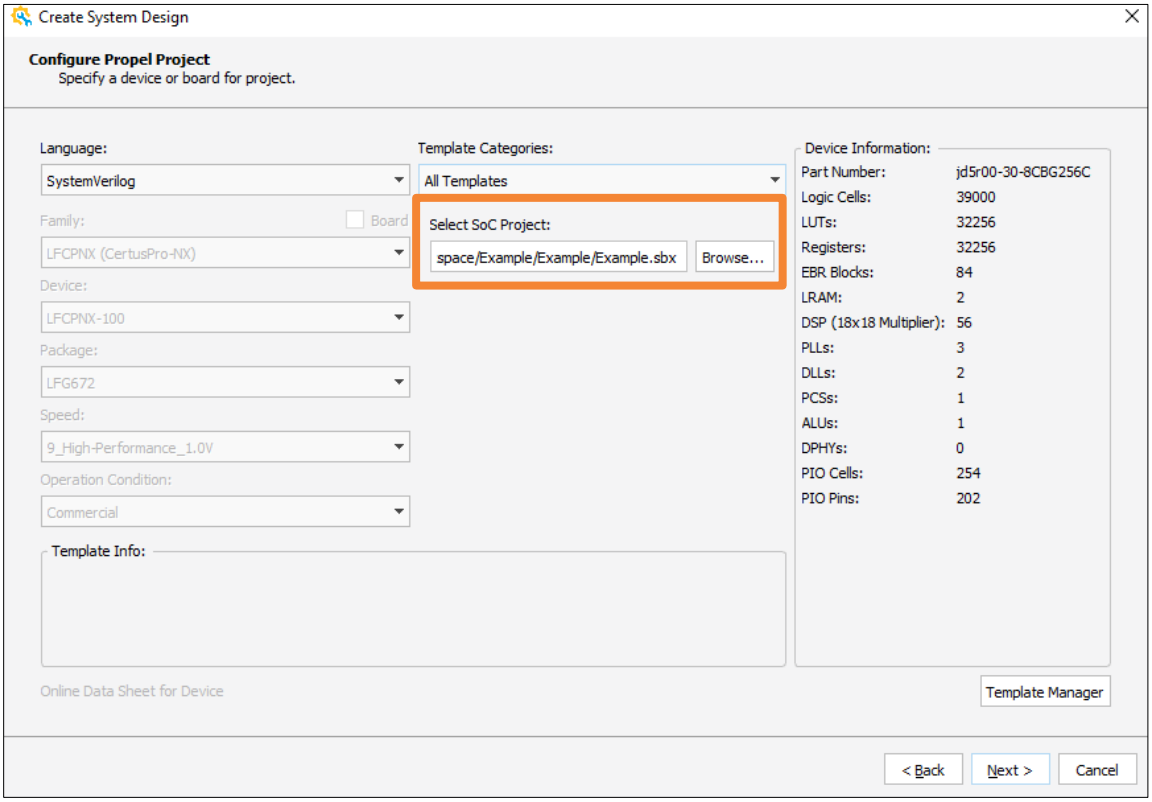


Figure 2.159. Create System Design – Propel Project Configure Wizard

6. (Optional) The default Hardware Description Language (HDL) is displayed in the Language area. Use the drop-down menu to change the default language.
7. Select an existing SBX design by using **Browse** to choose an SBX file.
8. Click **Next**. The Project Information wizard opens.
9. Click **Finish**. The dut_inst of SoC project is shown in the Schematic view (Figure 2.160).

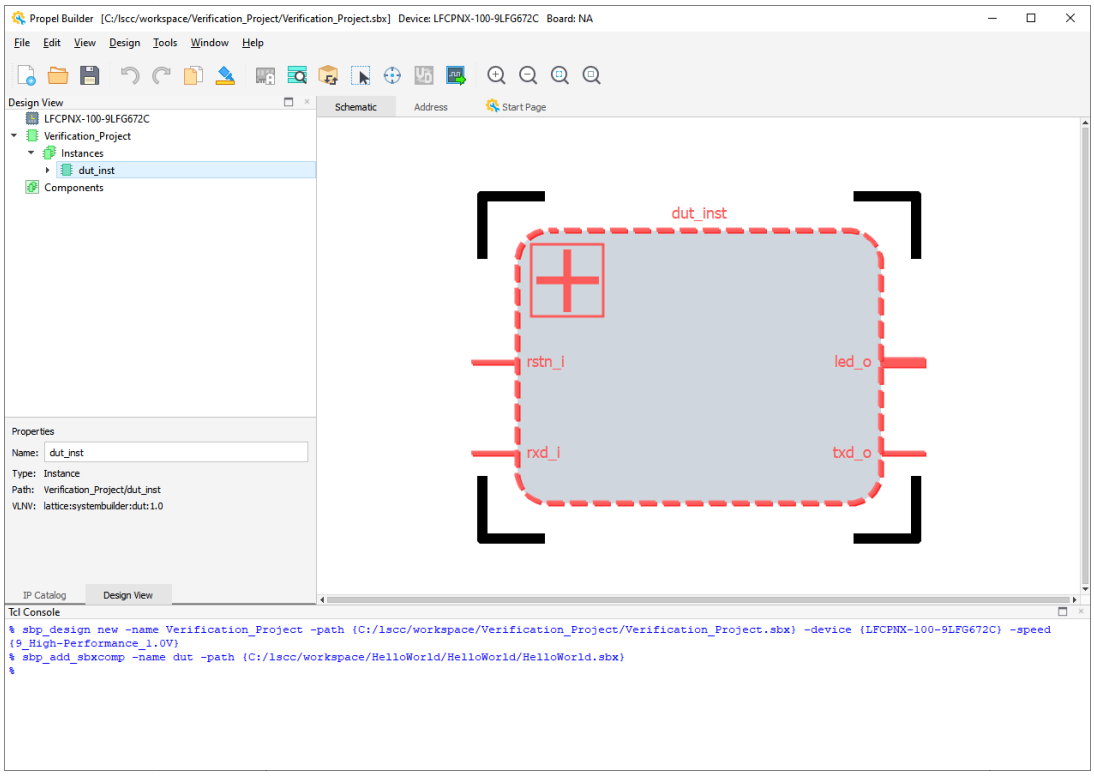


Figure 2.160. Verification Project

Note: The default instance name of an imported Design Under Test (DUT) is dut_inst. By default, its boundary is shown with dotted line, and the filled-in color is gray. If there is any change in the SoC design, the dut_inst DUT block can be updated accordingly by double-clicking this dut_inst DUT block.

10. Click the plus sign  of this dut_inst DUT block. You can see the whole SoC Design (Figure 2.161). Click the negative sign  to close the expanded bus.

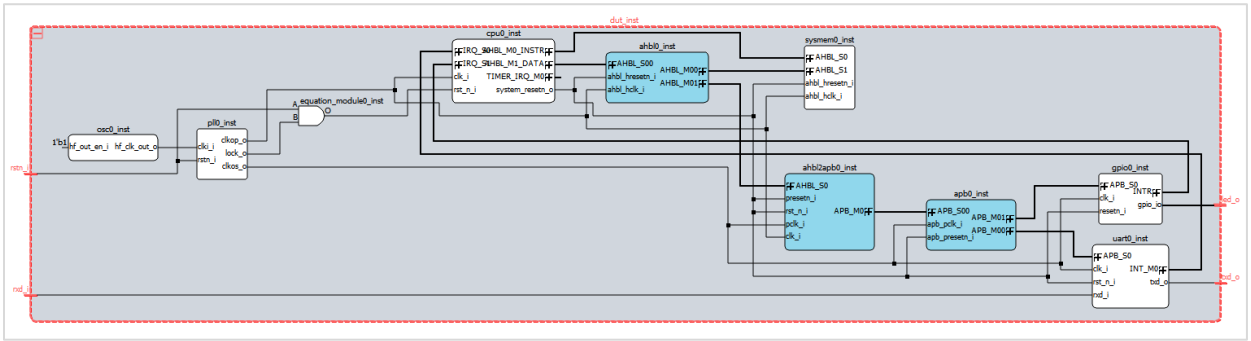


Figure 2.161. Whole SoC Design

2.4.2. Switching from SoC Design Project to Verification Project

Propel Builder also support switching from SoC project to verification project when a SoC project is already created.

1. Create a SoC design project. Refer to the previous Creating SoC Project section for more details on this.

2. From design project window, click **V/D button**  . A dialog box opens prompting you to save the changes, if the current design project is not saved yet (Figure 2.162).

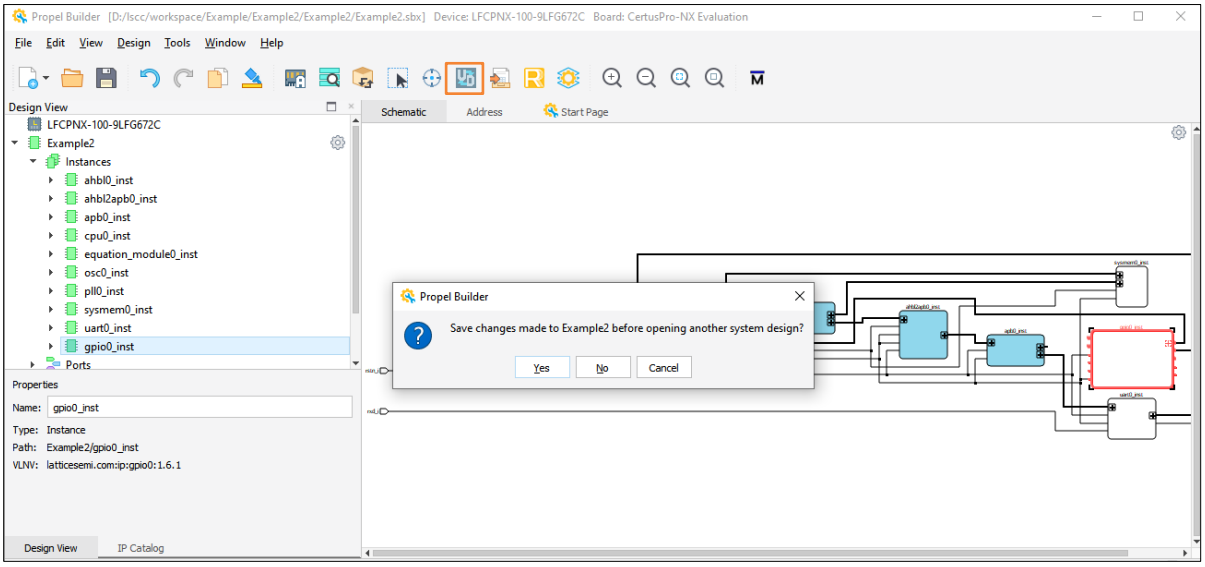


Figure 2.162. SoC Design Project

Notes:

- SoC design project is called ***.sbx. Verification project is called ***_v.sbx (Figure 2.162).
- **V/D button** is used to switch between Verification project and SoC Design project. When you create a SoC project, a related verification project is automatically created in the design project. This is how Verification/Design switch works, because they are auto-linked during project creation. Check .soc project file under the top project directory to see these details.
- For some template SoC project, they may include a pre-developed functioning verification project.

3. Click **Yes** to save the current design project. The Propel Builder GUI switches to verification project (Figure 2.163).

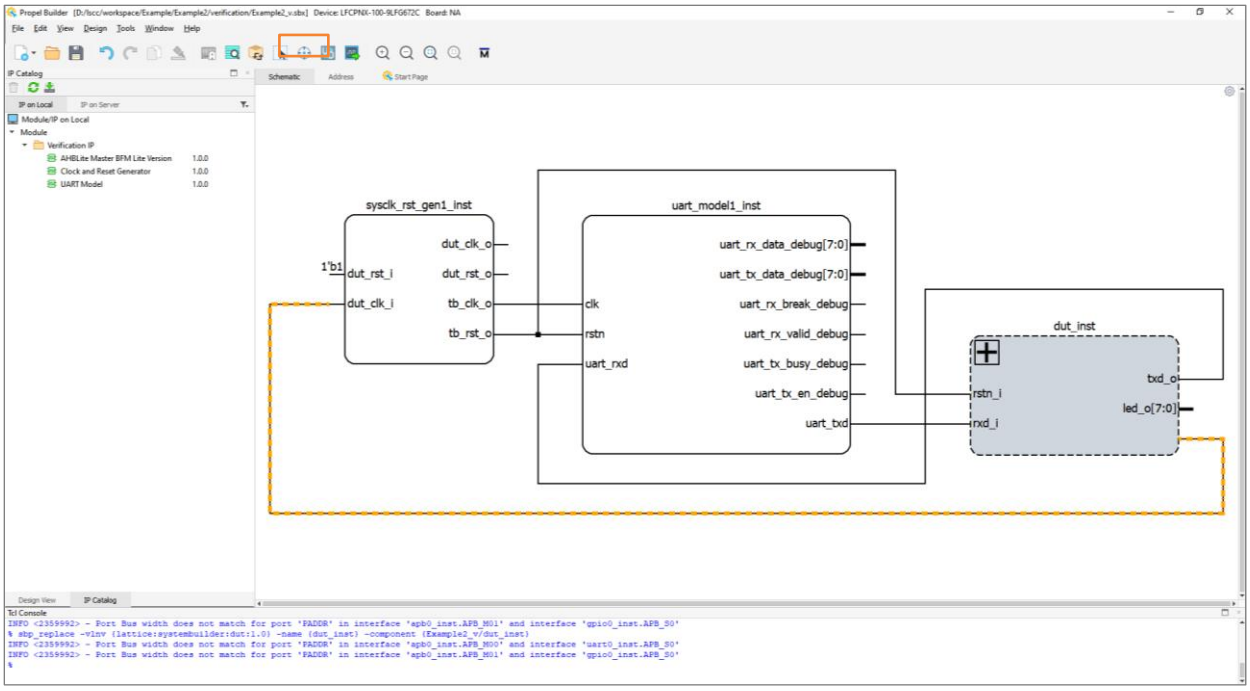


Figure 2.163. Verification Project

Notes:

- If you want to go back and design more on SoC project, click **V/D** button on the verification project window to go back to the SoC design project.(Figure 2.163)
- Each time you switch from SoC design project to Verification project, remember to:
  a. **Save** SoC Design Project first.
  b. Click on **V/D** button to switch to Verification project.
  c. **Reload** dut_inst to synchronize the SoC design change to verification project. Double click on dut_inst to do the reload (Figure 2.164).

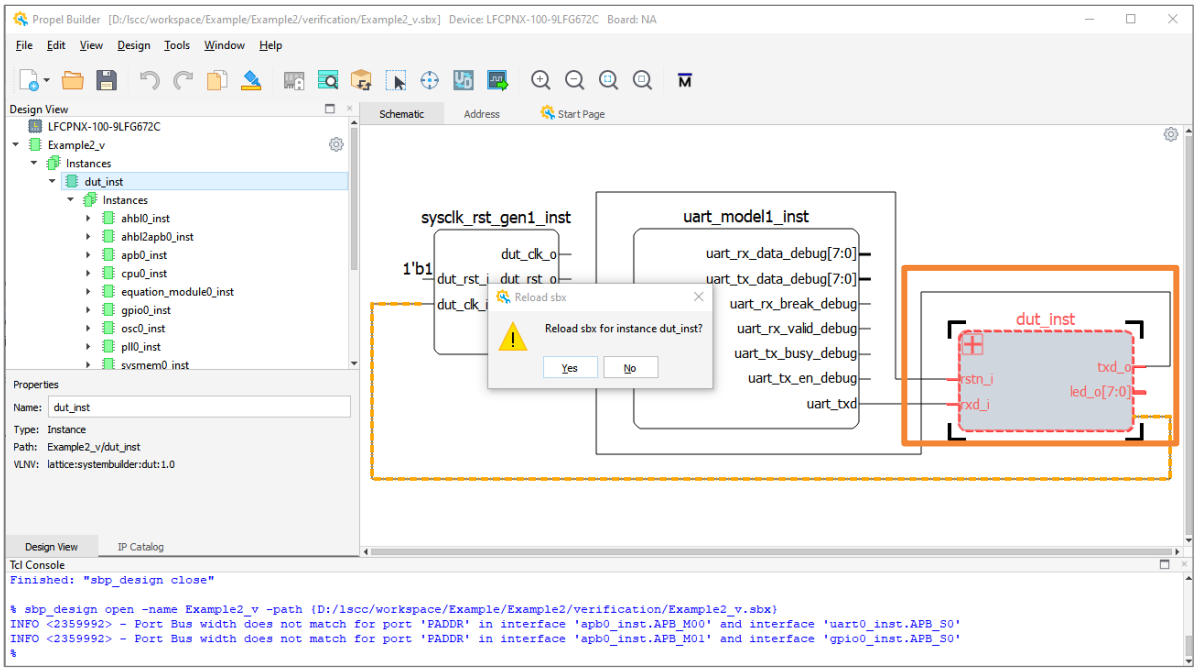


Figure 2.164. Reload dut_inst after Each SoC Project Design Change

2.4.3. Opening a Verification Project

Refer to the Opening an Existing SoC Project section for procedure in detail.

2.4.4. Adding Modules, IP and VIPs

Refer to the Generating and Instantiating IP/Module section for procedure in detail.

2.4.5. Working with the Schematic View

Refer to the previous Working with the Schematic View section for procedure in detail.

2.4.6. Connecting Modules

Refer to the previous Connecting Modules section for procedure in detail.

2.4.7. Viewing Address Maps

The Address view shows the read-only address maps of the SoC design (Figure 2.165).

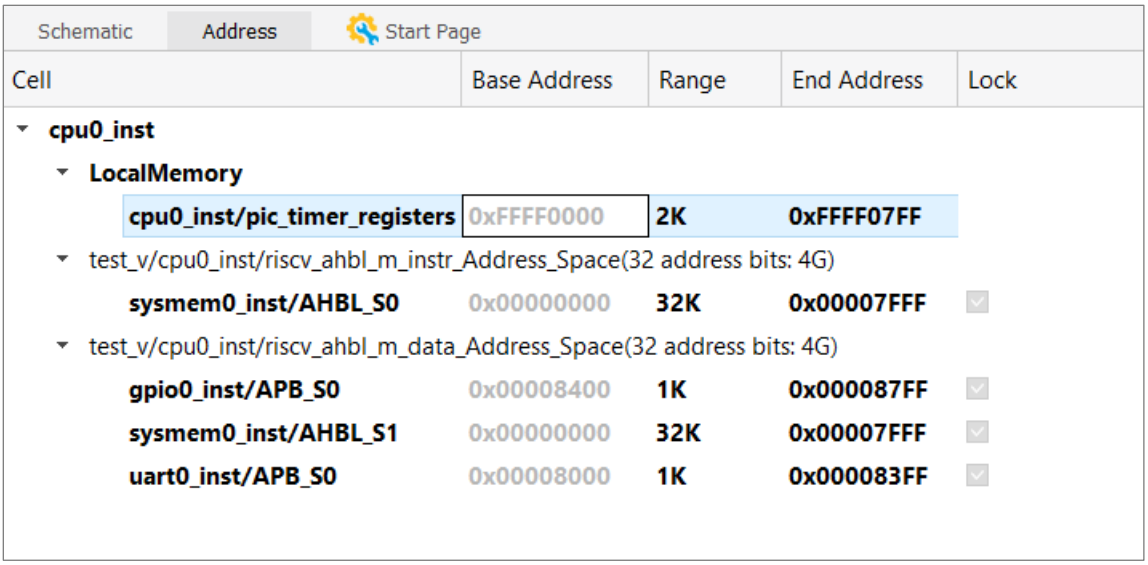


Figure 2.165. Address Maps

2.4.8. Monitoring DUT

This feature is available to Verification project only. In Propel Builder, the pin inside DUT can be connected to the input pin of a VIP. The connected pins can be found at both ends of the orange line, as shown in Figure 2.166. Only pin and pin bus are supported in the current release of Propel Builder.

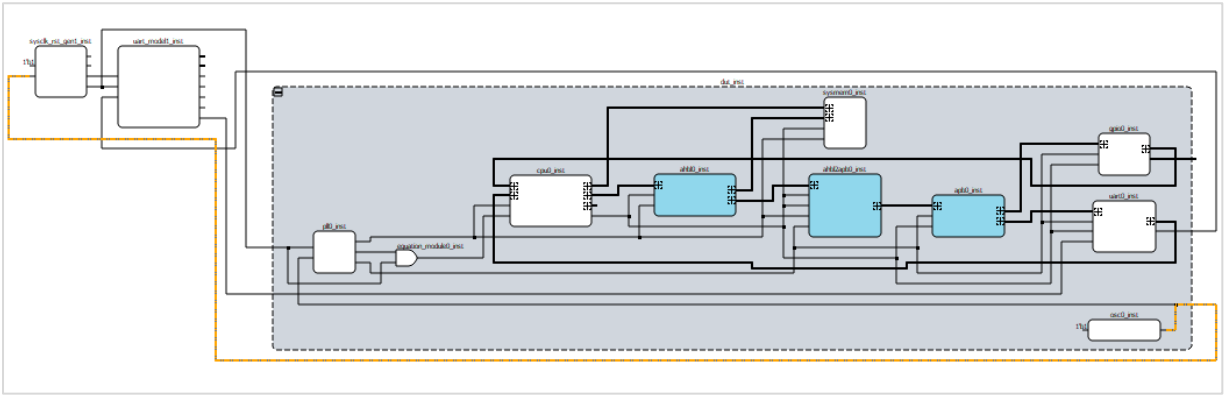


Figure 2.166. Monitoring DUT

The testbench generated for this Verification project is shown in Figure 2.167. This testbench file can be used for simulation. For testbench generation, see Generating Simulation Environment.

```
75  logic sysclk_rst_gen1_inst_dut_clk_i_net;
76
77  /*-----------------------Connection Block-----------------------*/
78  /* This section cover all the connections that related to internal*/
79  /* signals of DUT, or interface(e.g, AHBL Master BFM).           */
80  /*--------------------------------------------------------------*/
81
82  assign sysclk_rst_gen1_inst_dut_clk_i_net = dut_inst.osc0_inst.hf_clk_out_o;
83
84  /*---------------------------BFM Block--------------------------*/
85  /* This section is reserved for user to create stimulus using BFM */
86  /* APIs.                                                        */
87  /*--------------------------------------------------------------*/
88
89  ....
90
91  sysclk_rst_gen1
92  sysclk_rst_gen1_inst
93  (
94    .dut_clk_i(sysclk_rst_gen1_inst_dut_clk_i_net),
95    .dut_clk_o(sysclk_rst_gen1_inst_dut_clk_o_net),
96    .tb_rst_o(sysclk_rst_gen1_inst_tb_rst_o_net)
97  );
```

Figure 2.167. Testbench of the Verification Project

2.4.9. Generating Simulation Environment

1. (Optional) In design project view, initialize mem file in System Memory IP instance. See Launching SDK and Generate Mem File section for how to generate mem file. If you want to launch simulation without the actual program running, which is not a functioning simulation environment, you can skip this step.

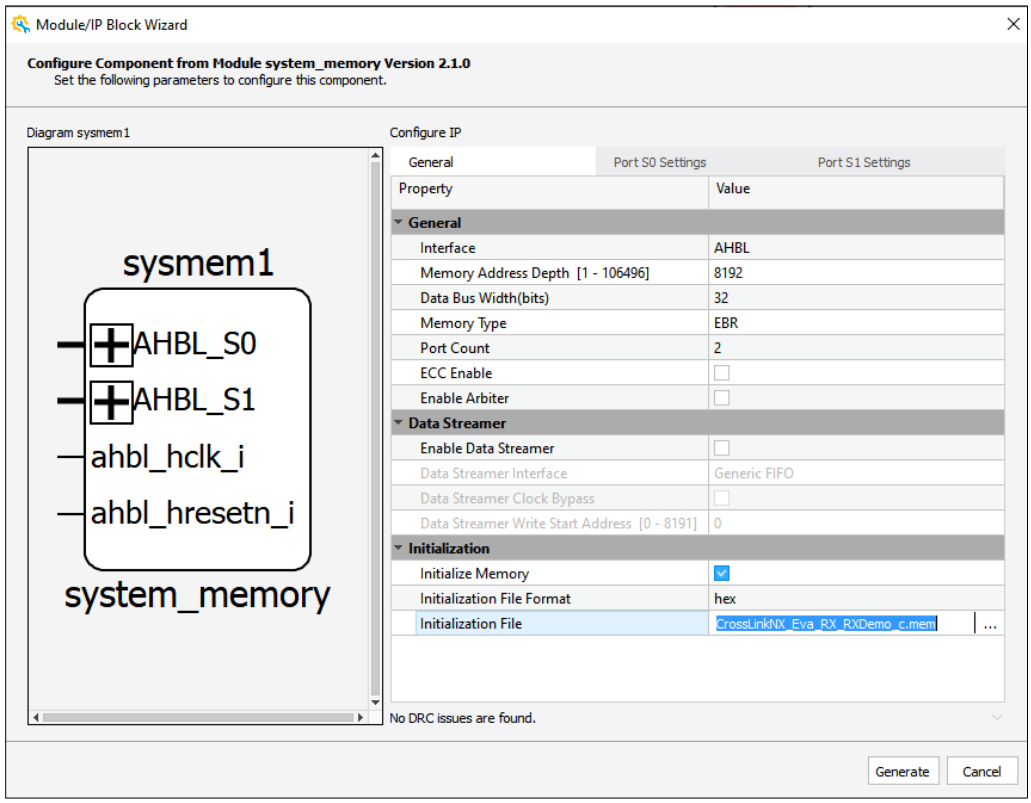


Figure 2.168. Initialization of Mem File

2. In design project view, click **V/D** button to switch to verification project. Check the Switching from SoC Design Project to Verification Project section for more notes on this operation.
   The verification project is located at ./<*project_name*>/verification.

3. In verification project view, click Generate icon  in the Propel Builder Toolbar (Figure 2.169).

   Note:

   - SoC design project is called ***.sbx. Verification project is called ***_v.sbx (Figure 2.169).

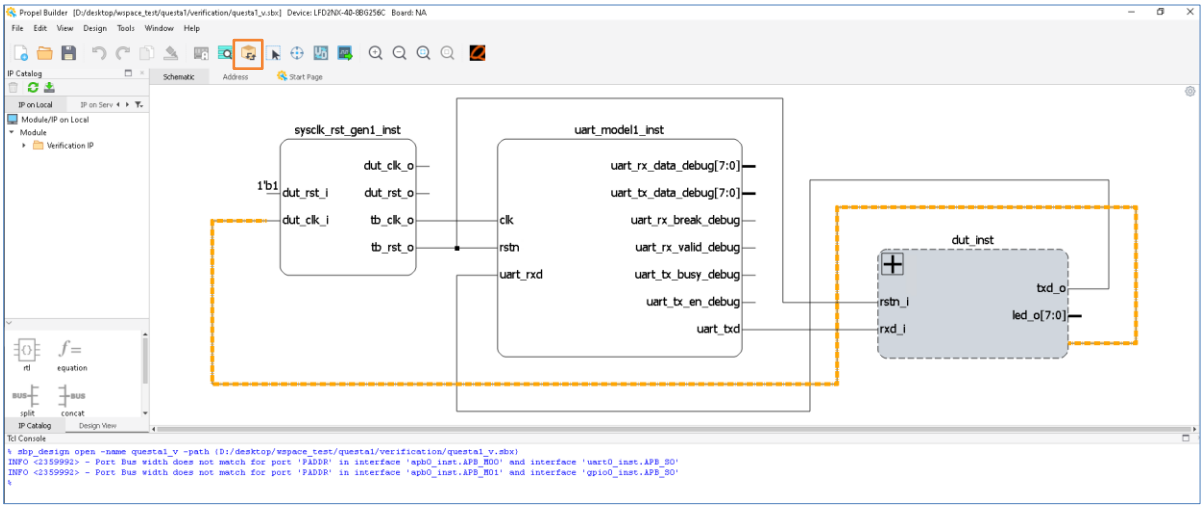


Figure 2.169. Generate Simulation Environment on Verification Project

A Simulation Wizard pops up (Figure 2.170), in which you can set run time for simulation.

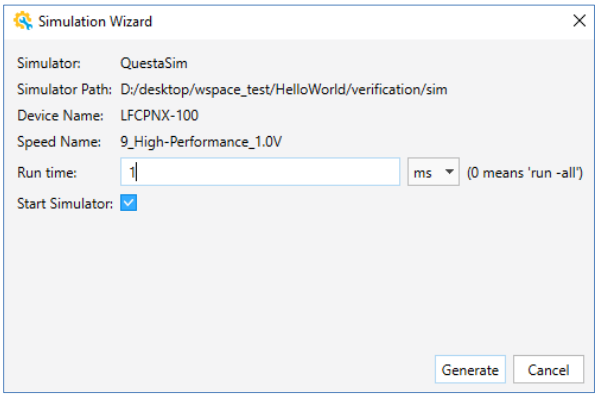


Figure 2.170. Simulation Wizard

In Figure 2.171, if TCL console prompts: INFO <2359992> – (GVE) The simulation environment has been created, it means that the testbench is generated in file system: <*project_name*>/verification/sim.

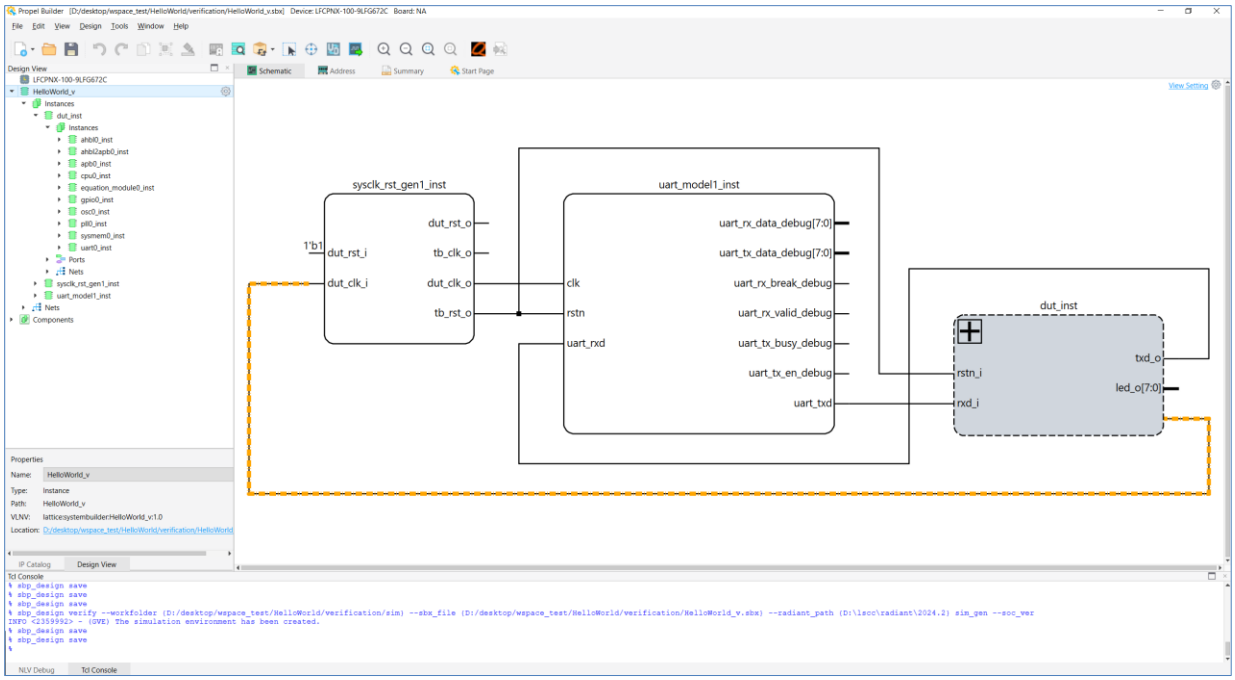


Figure 2.171. Simulation Environment Creating

The testbench file structure is shown as below (Figure 2.172):

```
+--- [sim]                    -- Generated simulation environment folder
|   +--- [hdl_header]
|   |   +--- soc_regs.v       -- Register definitions of all the components in DUT/SOC
|   |   +--- sys_platform.v   -- Base address, user settings of all the components in DUT/SOC
|   +--- [misc]
|   |   +--- *.*              -- All the mem, hex, txt files are copied here
|   +--- flist.f              -- File list for HDLs
|   +--- flist_sim.f          -- File list for all files used in simulation
|   +--- qsim.do               -- Do script for simulator,
                                 qsim.do: QuestaSim. |
                                 This file compiles project and invokes simulator with
|                                some default settings using the generated testbench.
|   +--- wave.do              -- Do script for adding signals in waveform window
|   +--- <project_name>_v.sv  -- Top testbench, it is SystemVerilog based.
```

Figure 2.172. Testbench File Structure

4. If there is any change to the design project, make sure to **save** the design in design project view, switching from design project to verification project using **V/D** button. Reload dut_inst and generate simulation in verification project again. See Switching from SoC Design Project to Verification Project section for more details.
5. Unlike those HDLs generated in the SoC design project directory, the testbench generation in the Verification project is just a start point for you to work with, not necessarily a full functioning verification project.
6. If there is a simulation tool change, make sure to generate simulation environment again. Otherwise, a dialog box pops up prompting you to make a choice of Yes or No (Figure 2.173).

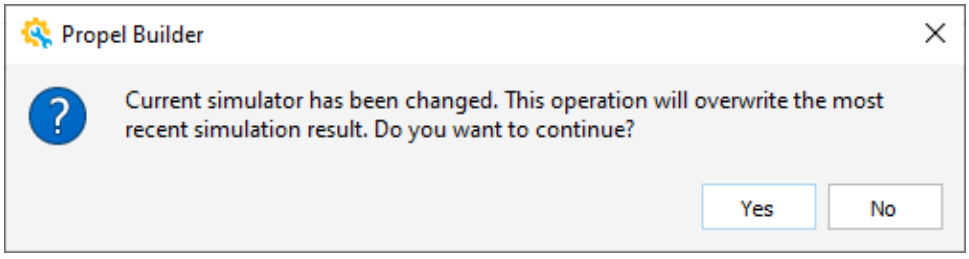


Figure 2.173. Remind for Simulation Tool Change

2.4.10. Launching Simulation

1. After Generating Simulation Environment, simulation project is generated in <*project_name*>/verification/sim.

2. Click  **Launch Simulation** icon in verification project view to launch simulation.

   Note: SoC design project is called ***.sbx. Verification project is called ***_v.sbx (Figure 2.174).

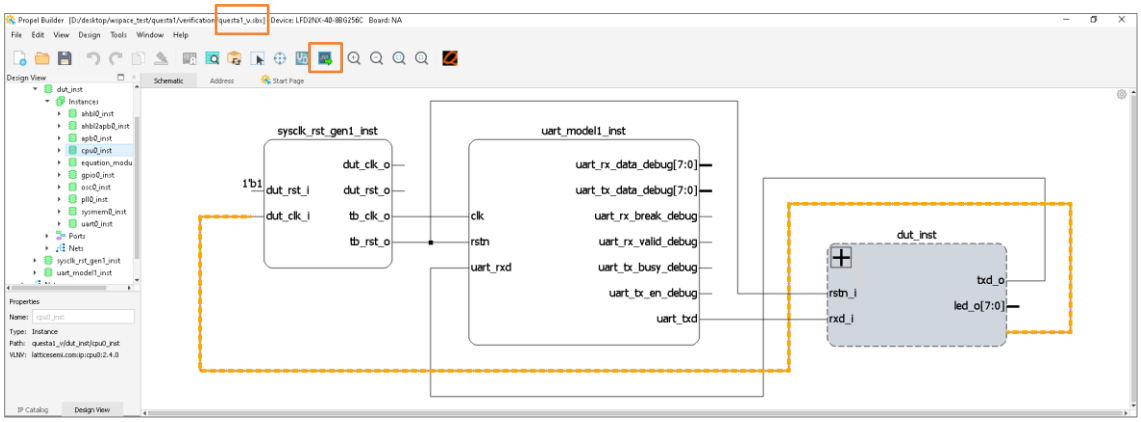


Figure 2.174. Launch Simulation in Verification Project

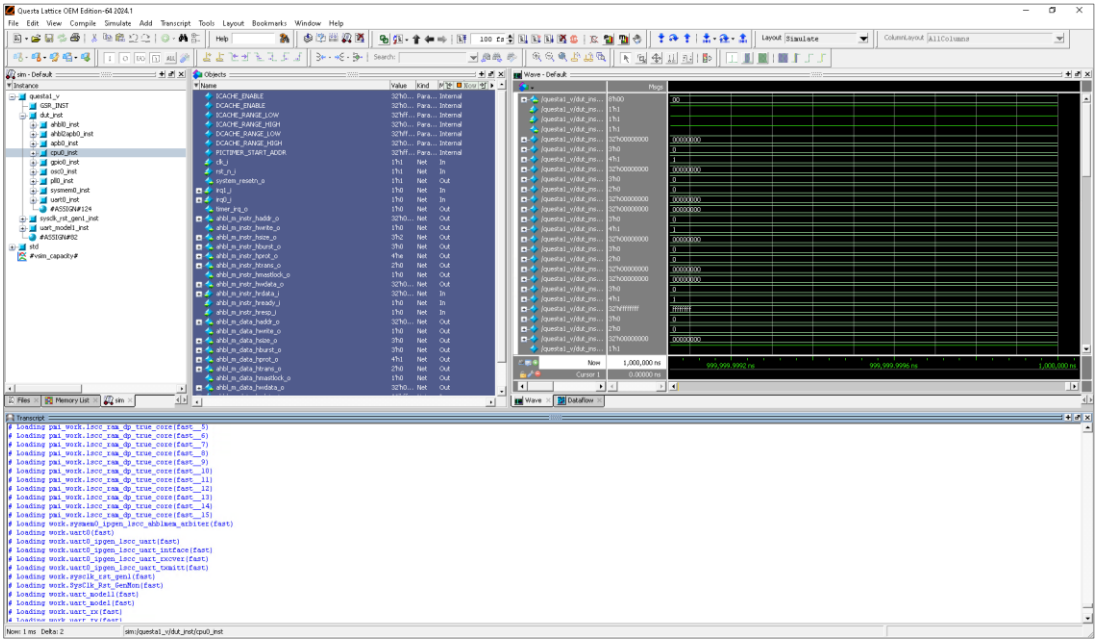


Figure 2.175. Questa Simulation GUI

3. If there is no simulation tool specified in **Tools > Options > Directories**, the default built-in simulation tool, OEM version of QuestaSim, opens (Figure 2.175). If specified, the specified simulation tool opens.
   - For OEM version QuestaSim, there are pre-compiled simulation libraries.
   - For non-OEM version simulation tool, the script under simulation project directory can detect whether or not there are existing simulation libraries under the ovi_<device_family_name> folder. If yes, simulation uses the existing library; otherwise, the device library can be created and compiled once into the ovi folder for further use, and this compiling process may take some time.
4. See Figure 2.176 for simulation file structure.

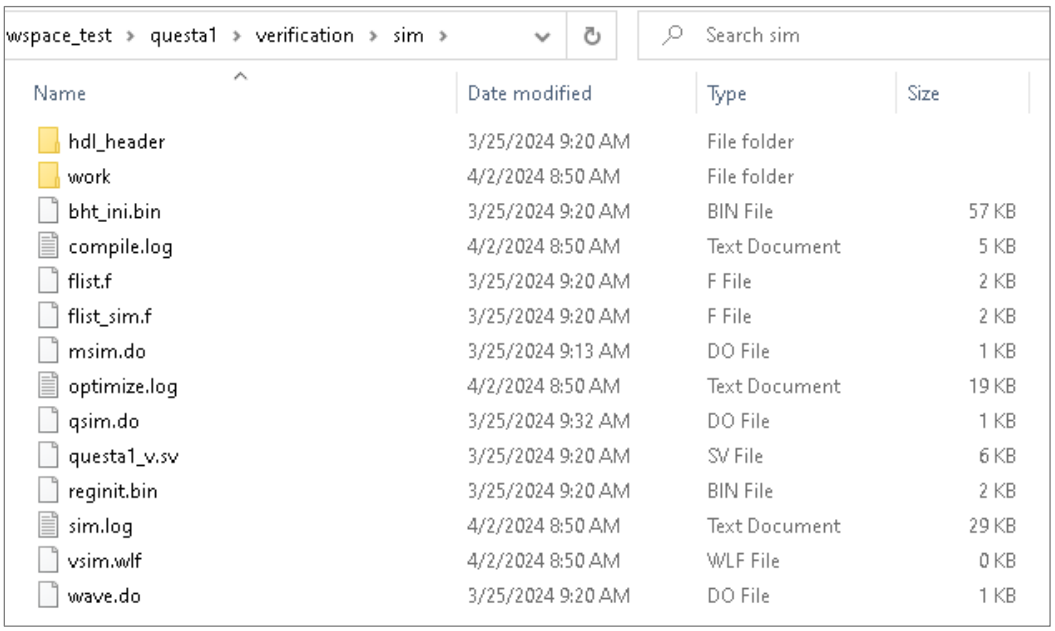


Figure 2.176. Testbench File Structure in Simulation Project

2.5. Advanced Usage

2.5.1. Supported Interface

Lattice Propel Builder and IP Packager share the same usage of interfaces. These interfaces are listed below.

- Interrupt
- AMBA3 AHB Lite
- AMBA3 APB
- AMBA4 AXI4
- AMBA4 AXI4 Lite
- AMBA4 AXI4 Stream
- Localbus

Refer to Lattice IP Packager 2025.2 User Guide (FPGA-UG-02242) for detailed usage of these interfaces in the IP Packager.

2.5.2. Supported Language

Propel 2025.2 Builder supports the following languages:

- Verilog HDL
- SystemVerilog
- VHDL
- Mixed Verilog/VHDL

Currently, verification projects and RTL module (see RTL section) only support Verilog HDL.

2.5.3. Supported Hierarchical IP

Hierarchical IP instantiates a hierarchical component that contains a reference to a design along with a description of the top-level interface of the component.

1. Click **Expand IP** sign on the left corner of the hierarchical IP (Figure 2.177) to show the detailed design scope of this IP (Figure 2.178).

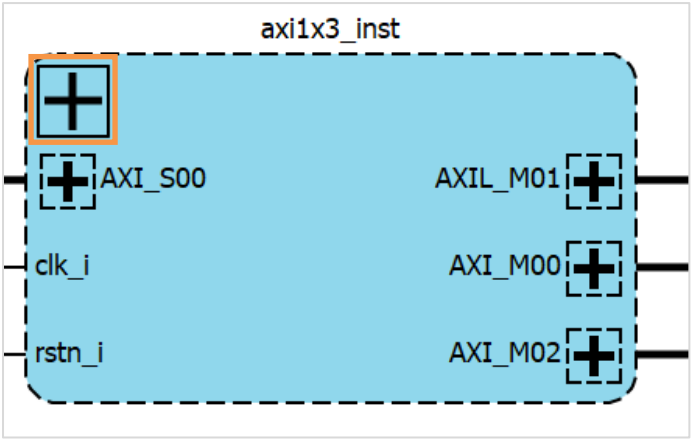


Figure 2.177. Hierarchical IP

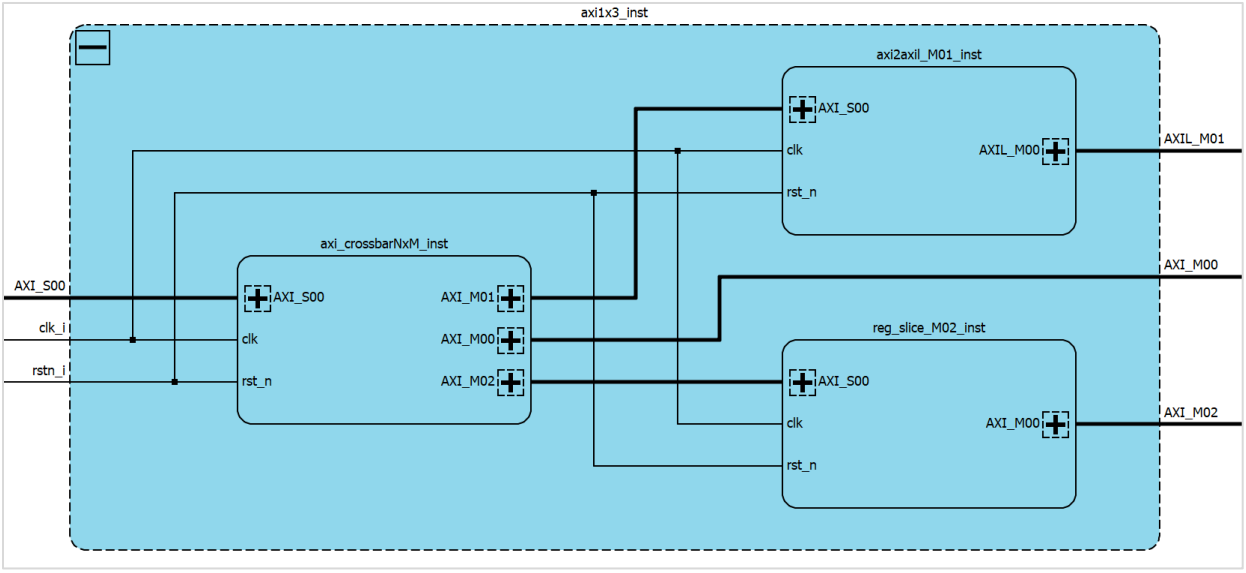


Figure 2.178. Hierarchical IP Scope in Detail

2.5.4. Address Mapping External IPs (CPU or APB, AHBL, and AXI Peripherals)

External IPs, CPU or APB, AHBL, and AXI Peripherals, outside of Propel Builder can be connected through AXI, AHB Lite or APB feedthrough modules to pass their address space or memory block information.

- External CPU or other managers:
  - For AXI interface, configure AXI feedthrough module as Manager to hold the address space information. Export AXI_S00 of the feedthrough module, and connect AXI_M00 of the feedthrough module to other AXI interface.
  - For AHB Lite interface, configure AHB-Lite feedthrough module as Manager to hold the address space information. Export AHBL_S0 of the feedthrough module, and connect AHBL_M0 to other AHB Lite interface.
  - For APB interface, configure the APB feedthrough module as Requester to hold the address space information. Export APB_S0 of the feedthrough module, and connect APB_0 of the feedthrough module to other APB interface.
- APB, AHB Lite, AXI peripherals:
  - For APB peripherals, configure the APB feedthrough module as Completer to hold memory map information, export APB_M0 of the feedthrough module, and connect APB_S0 of the feedthrough module to other APB interface.
  - For AHB Lite peripherals, configure AHB Lite feedthrough module as Subordinate to hold memory map information, export AHBL_M0 of the feedthrough module, and connect AHBL_S0 to other AHB Lite interface.
  - For AXI peripherals, configure the AXI feedthrough module as Subordinate to hold memory map information, export AXI_M00 of the feedthrough module, and connect AXI_S00 to other AXI interface.

An example is shown in Figure 2.179.

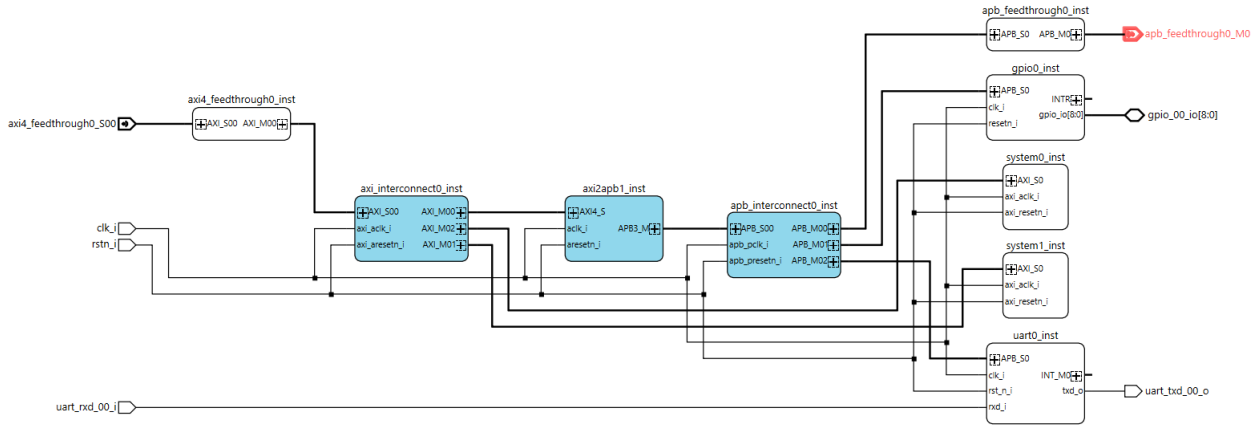


Figure 2.179. Address Mapping for External IPs

In the example above, to connect to external cpu/manager IP through AXI interface:

1. Instantiate an AXI4 feedthrough module from IP catalog, and configure it as Manager. The instance name here is axi4_feedthrough0_inst.
2. Set the address width and data width for the address space.
3. Connect axi4_feedthrough0_inst.AXI_M00 to axi_interconnect0_inst.AXI_S00.
4. Export axi4_feedthrough0_inst.AXI_S00 for external IP.

In the example above, to connect to external APB peripheral IP:

1. Instantiate an APB feedthrough module from IP catalog, and configure it as Completer. The instance name here is apb_feedthrough0_inst.
2. Set the address width and data width for the memory map.
3. Connect apb_feedthrough0_inst.APB_S0 to apb_interconnect0_inst.APB_M00.
4. Export apb_feedthrough0_inst.APB_M0 for external IP.

You can see the address space for axi4_feedthrough0_inst and memory map for apb_feedthrough0_inst are shown in the Address Editor (Figure 2.180).

Cell	Base Address	Range	End Address	Lock
axi4_feedthrough0_inst				
test_feedthrough/axi4_feedthrough0_inst/axi_feedthrough_address_space (32 address bits: 4G)				
apb_feedthrough0_inst/APB_S0	**0x40000000**	**4K**	**0x40000FFF**	☑
gpio0_inst/APB_S0	**0x40001000**	**4K**	**0x40001FFF**	☑
system0_inst/AXI_S0	**0x00200000**	**4K**	**0x00200FFF**	☑
system1_inst/AXI_S0	**0x00201000**	**4K**	**0x00201FFF**	☑
uart0_inst/APB_S0	**0x4000A000**	**4K**	**0x4000AFFF**	☑

Figure 2.180. Address Space for axi4_feedthrough0_inst in Address Editor

2.5.5. Define Custom Template

Saving a design as a template is an enhancement feature of Propel Builder, which allows you to create your own new project template based on an existing design. You can deploy this template into Propel Builder later or share it with others by saving template into a .ptmp file. See the following on how to generate a .ptmp file.

Notes:

- The GUI entry of this function takes effect from Propel Builder 2022.1, so the design created in earlier Propel Builder versions cannot define its custom template.
- Refer to Lattice Propel 2025.2 SDK User Guide (FPGA-UG-02244) for more details on how to use custom template in Propel SDK.

You can access **Template Manager** in two ways:

- Access during project creation. See the Creating SoC Project section for more information.

2.5.5.1. Export the Current Template Configuration

Choose **Tools** > **Create Template** from Propel Builder Menu Bar. Template Configuration (Figure 2.181) opens.

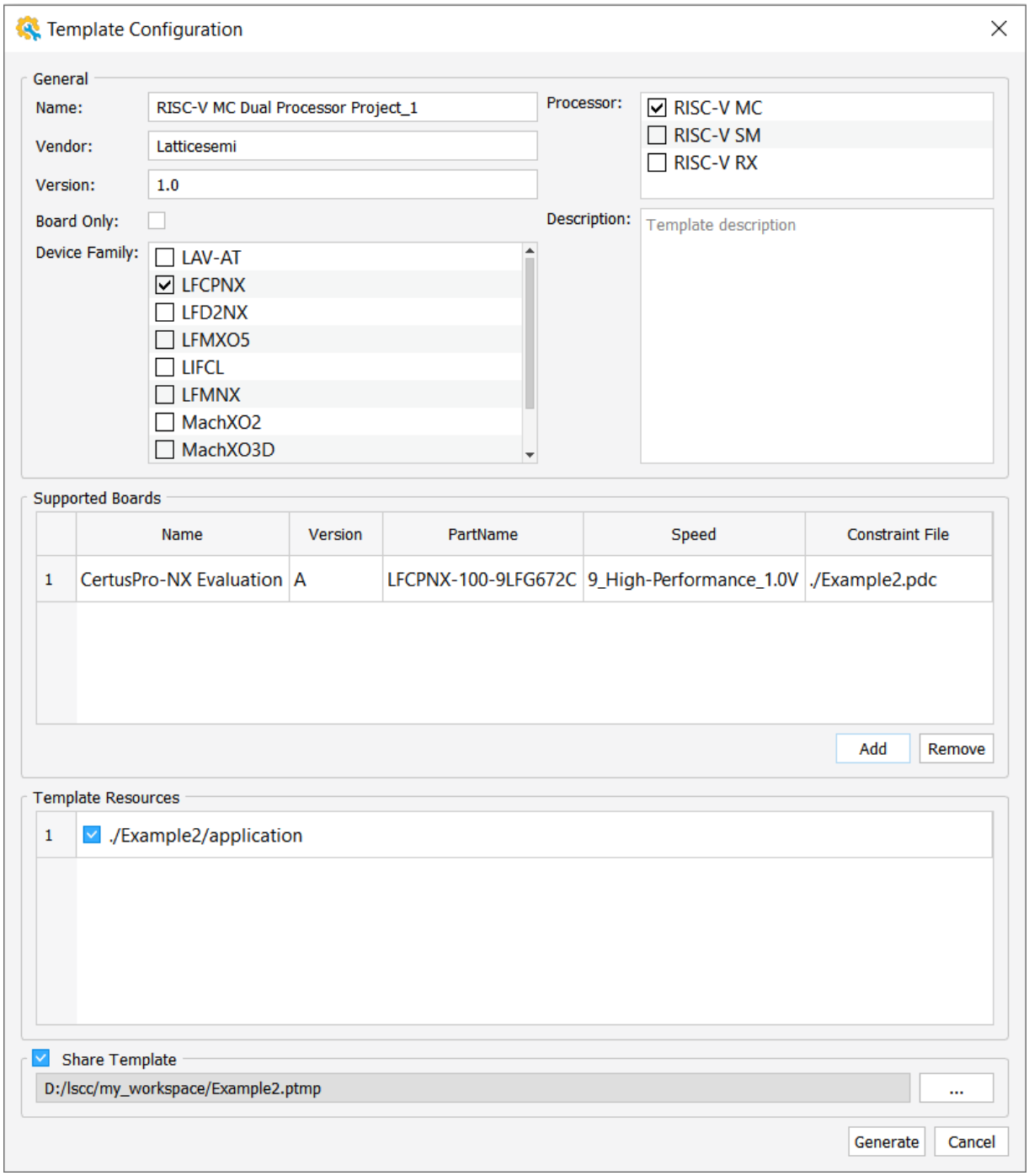


Figure 2.181. Export Template Configuration Page

1. Fill in general information such as Template name, Description, Vendor.
2. Select Processor, Device Family, and Supported Boards.
   - The device used in the current design is listed by default. You must make sure the design can work on all the devices in the list.
   - Click on an IP instance in **Schematic view**. The **Design View** shows the corresponding information of this IP. Check VLNV for this IP name (Figure 2.182). Go to **IP Catalog** and click on before this IP to show the **IP Information**. In the **Device Supported** area, all the devices this IP supports are listed (Figure 2.183). Make sure

all the IP instances in the design have the device support which are listed in the Board Family list in Template Configuration (Figure 2.181).

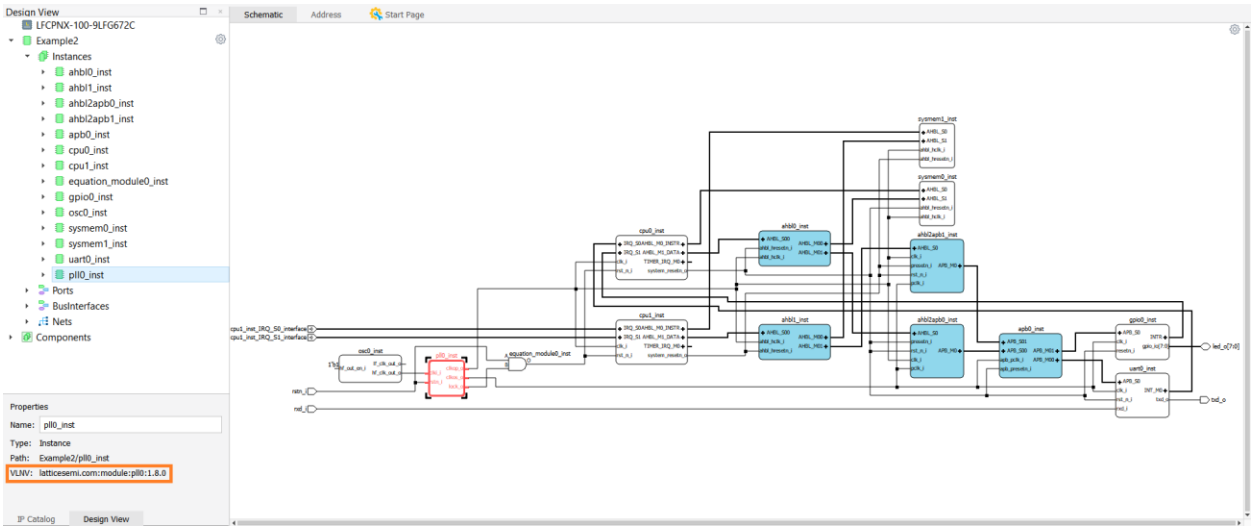


Figure 2.182. Check IP Name in Design View

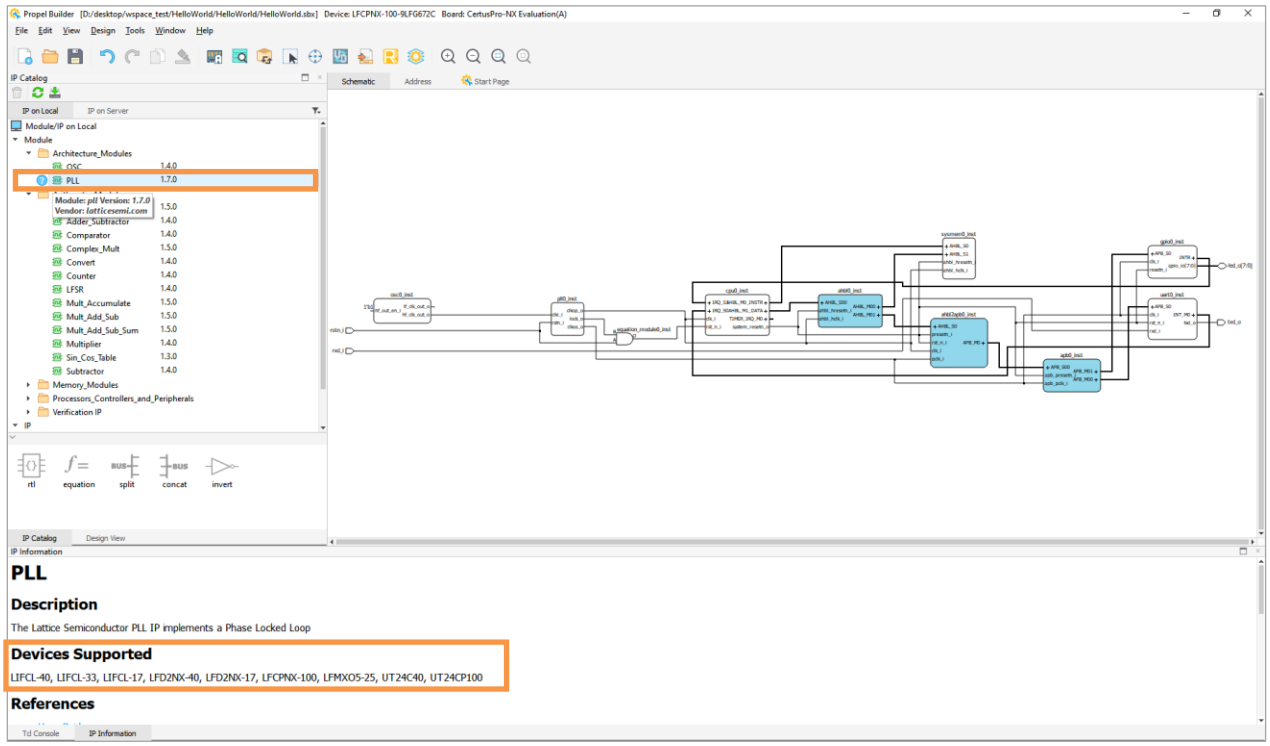


Figure 2.183. Check Device Supported in IP Information

- You can add the board information manually in **Supported Boards** (refer to Figure 2.33) for board information). You must ensure the correctness of the board information and the design can work on this board.
- Board **must** contain a Constraint File. **Double click** on the constraint file name (./Example2.pdc), and then click the … button to select the constraint file (Figure 2.184).

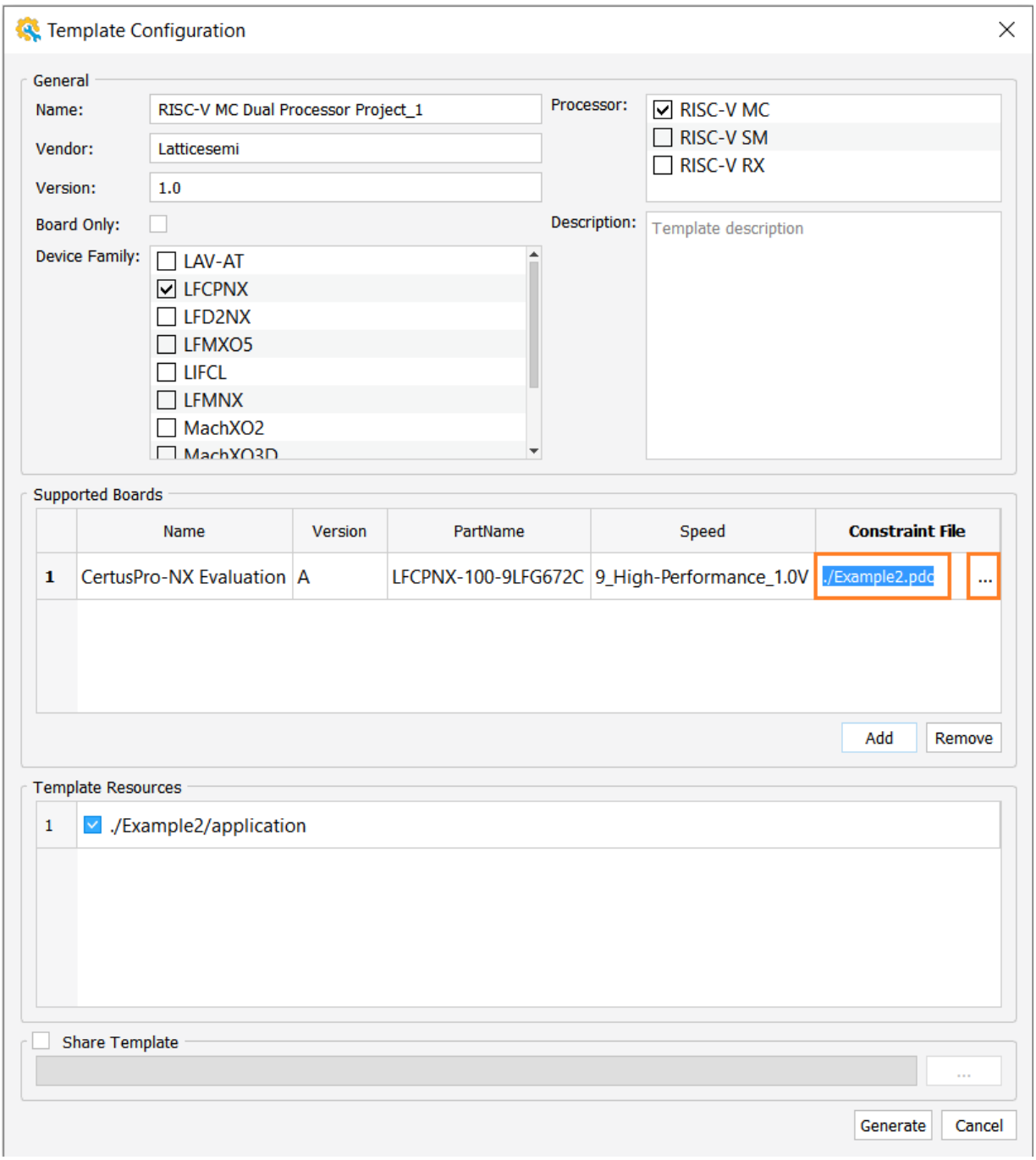


Figure 2.184. Double Click on the Constraint File Name

3. Template Resources:
   Optional resources include the newly created project such as C application project, user RTLs.

Output:

- By default, after you click the Generate button, the new template can be installed to your custom template folder, which is a folder named PropelTemplateLocal under $HOME (Figure 2.185).
- Option under Template Resources, such as the application folder, contains functional-ready embedded application source codes for C project. Check the box before it (Figure 2.184), then the application under current project is also exported to destination (Figure 2.185). Other files under this option works the same way.

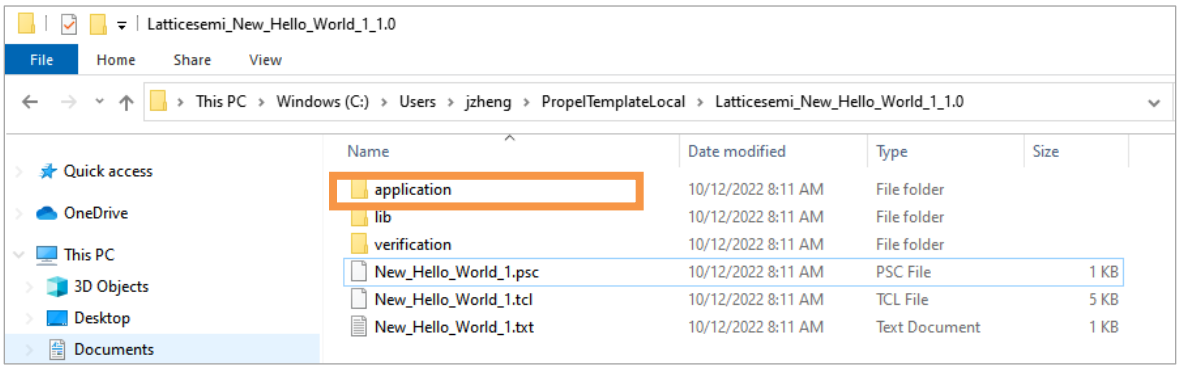


Figure 2.185. Export Template to PropelTemplateLocal Folder

- If you want to share this template, you can click **Share Template** and output this template to a .ptmp file which can be later installed to Propel Builder by other people. You can export a template to share later using template manager.
- Template manager page for custom templates.
- You can import/delete/export a selected template in **Template Manager** when creating a new system design (Figure 2.186 and Figure 2.187).

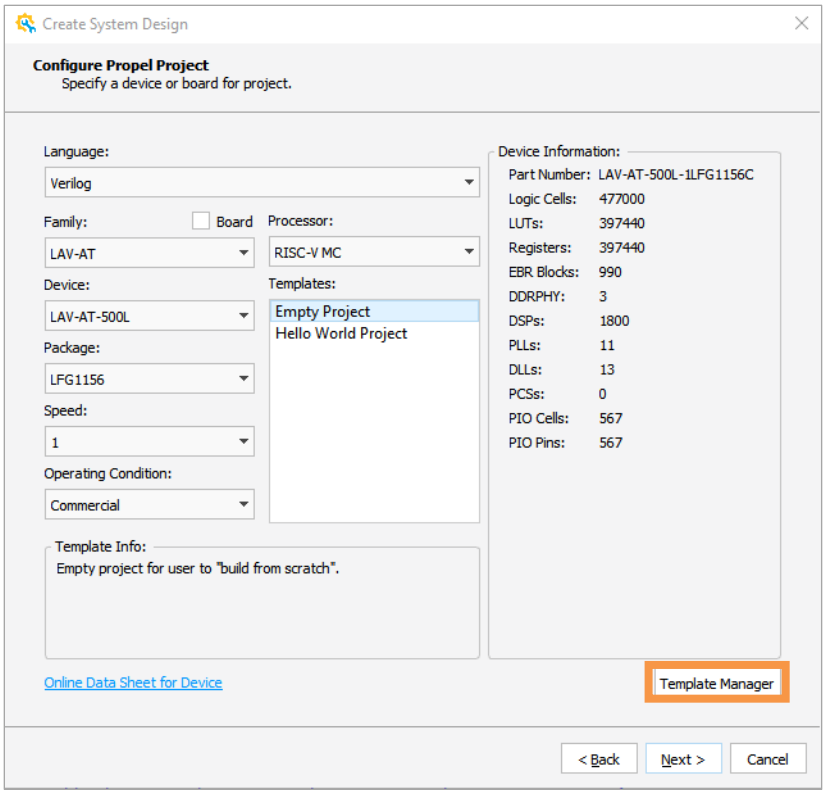


Figure 2.186. Template Manager Entry

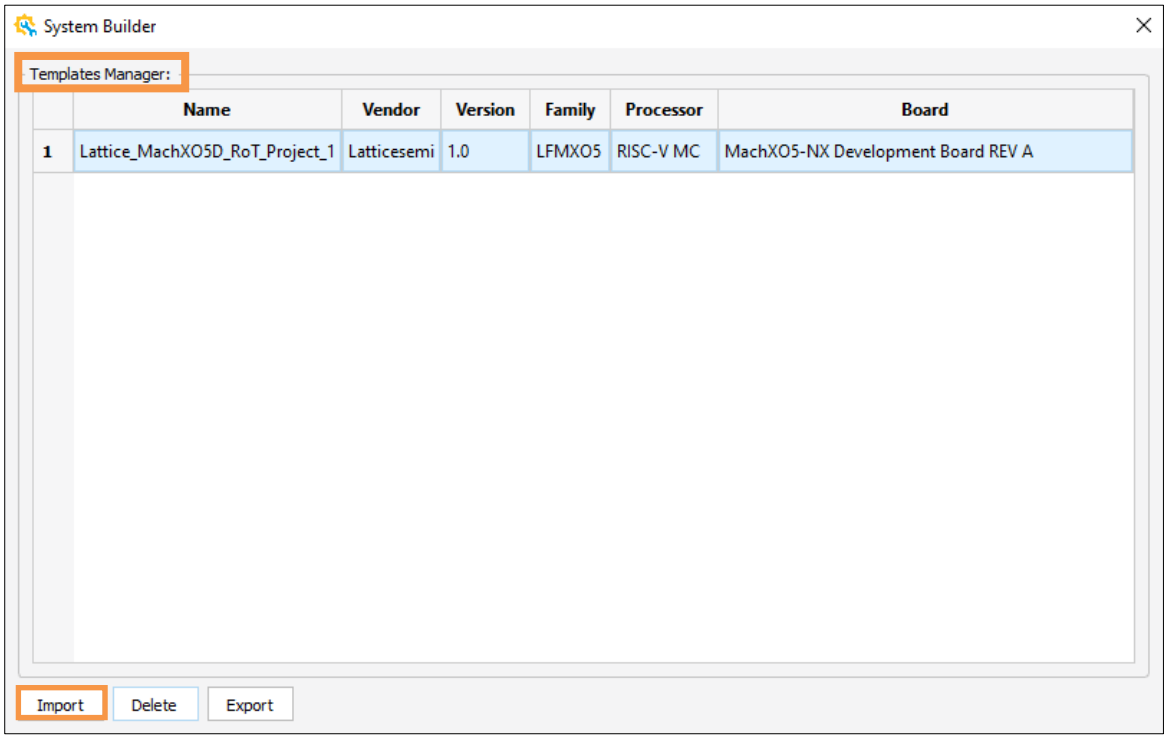


Figure 2.187. Templates Manager Page

2.5.5.2. Import a Template

1. Click **Import** (Figure 2.187), and then choose the desired .ptmp file (Figure 2.188).

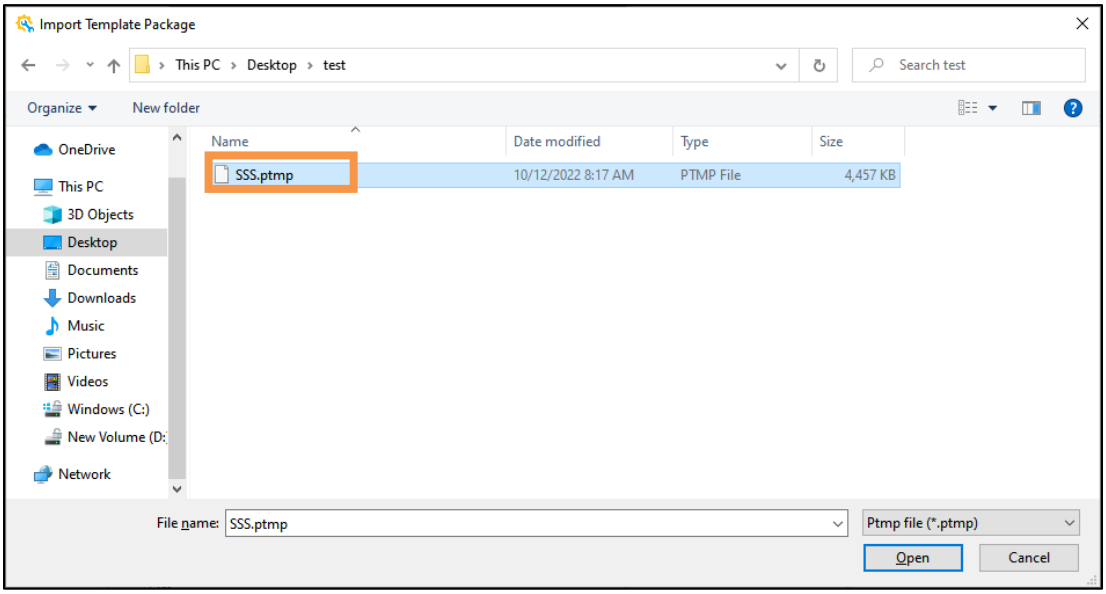


Figure 2.188. Import a .ptmp File

2. Custom template installation path.

   Custom templates are installed in $HOME/PropelTemplateLocal directory by default (Figure 2.189).

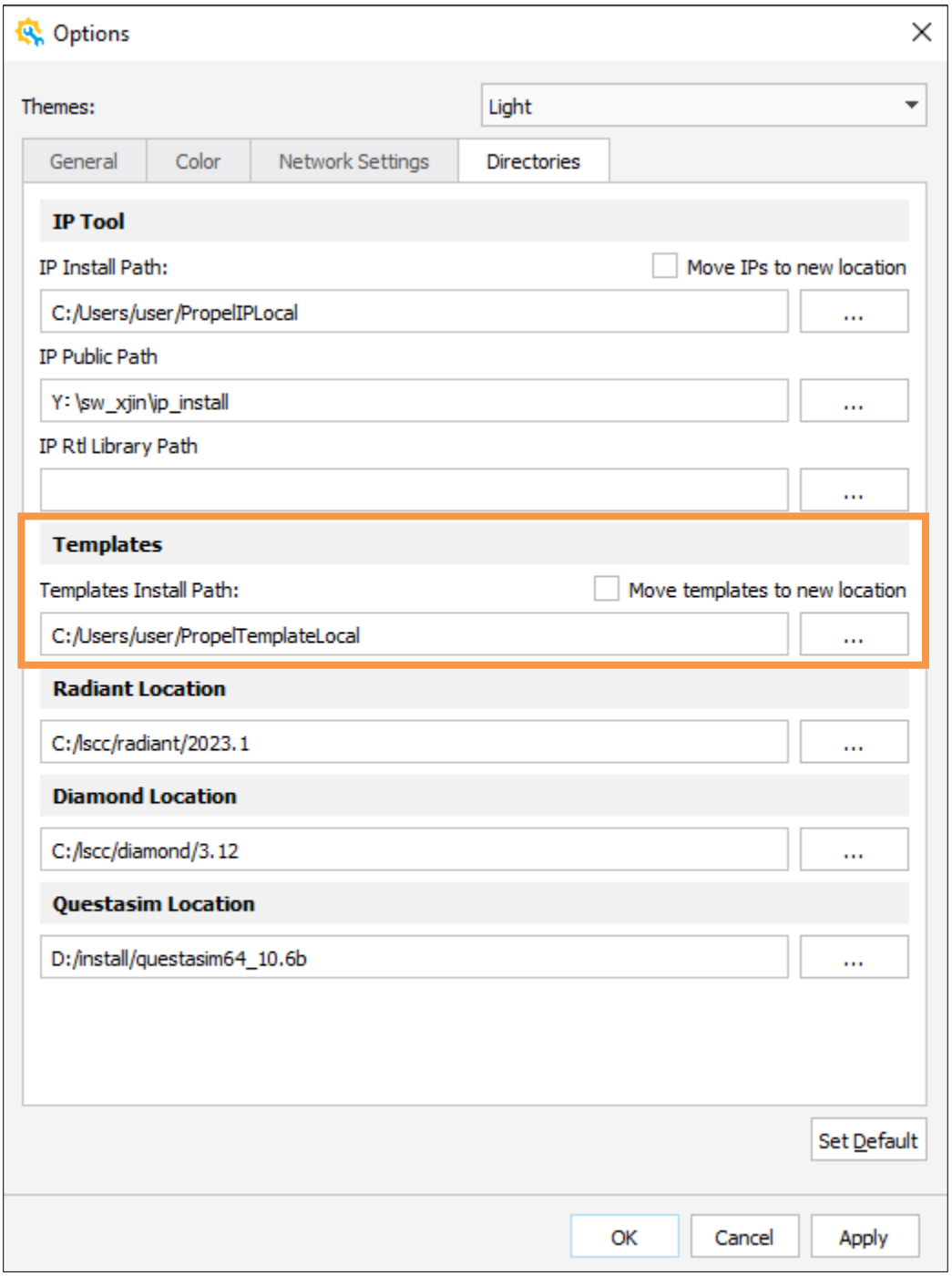


Figure 2.189. Template Manager Page

You can move it to another location by checking the *Move templates to new location* option in Directories tab of the **Options** dialog (Figure 2.190).

For custom templates usage in Propel SDK, refer to Lattice Propel 2025.2 SDK User Guide (FPGA-UG-02244).

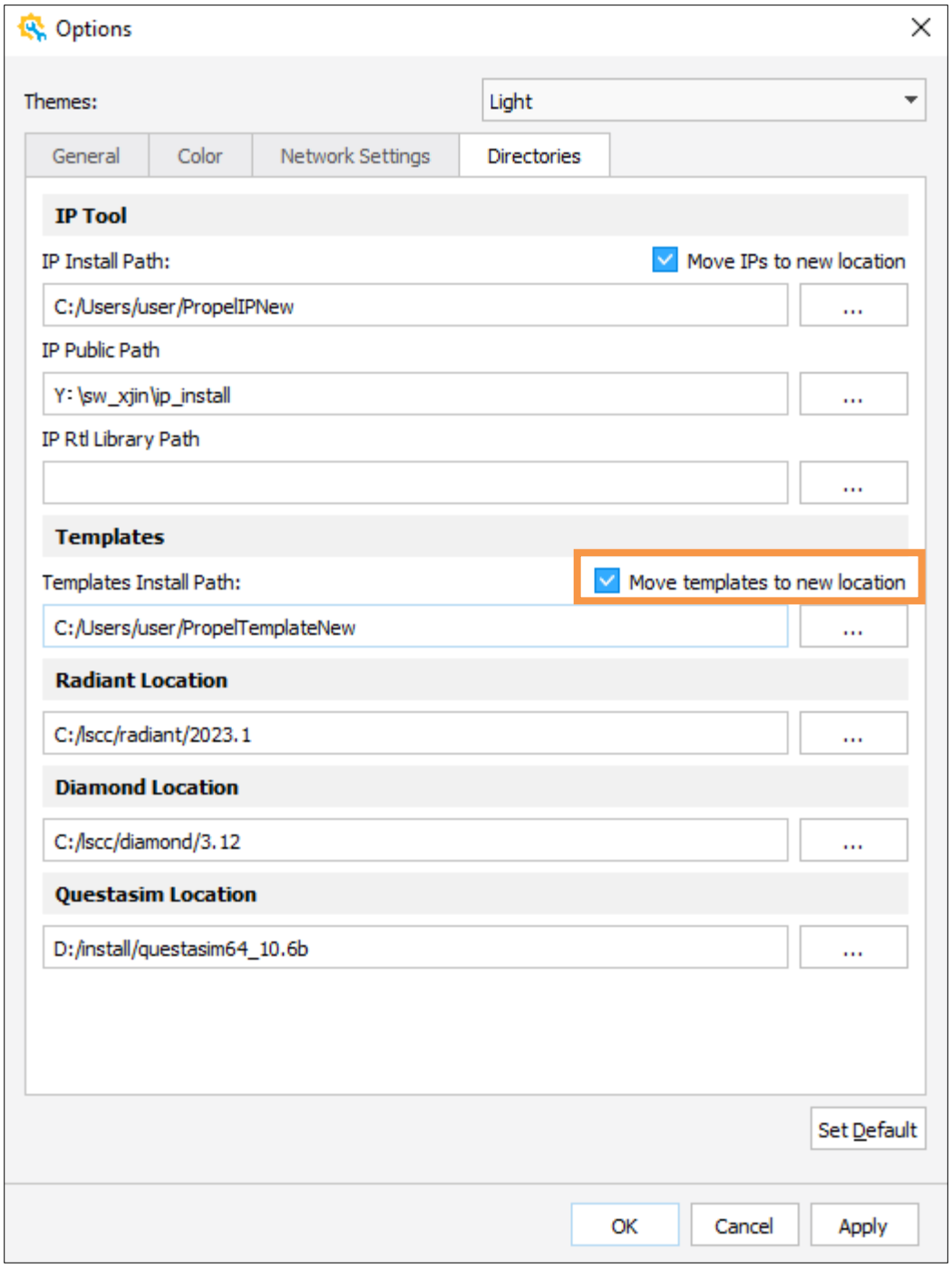


Figure 2.190. Template Manager Page – Change to New Location

2.5.5.3. Delete a Template

Click on the custom template you want to delete from the **Template Manager** Page (Figure 2.191), and then click **Delete**. The corresponding template folder under **Template Install Path** is deleted.

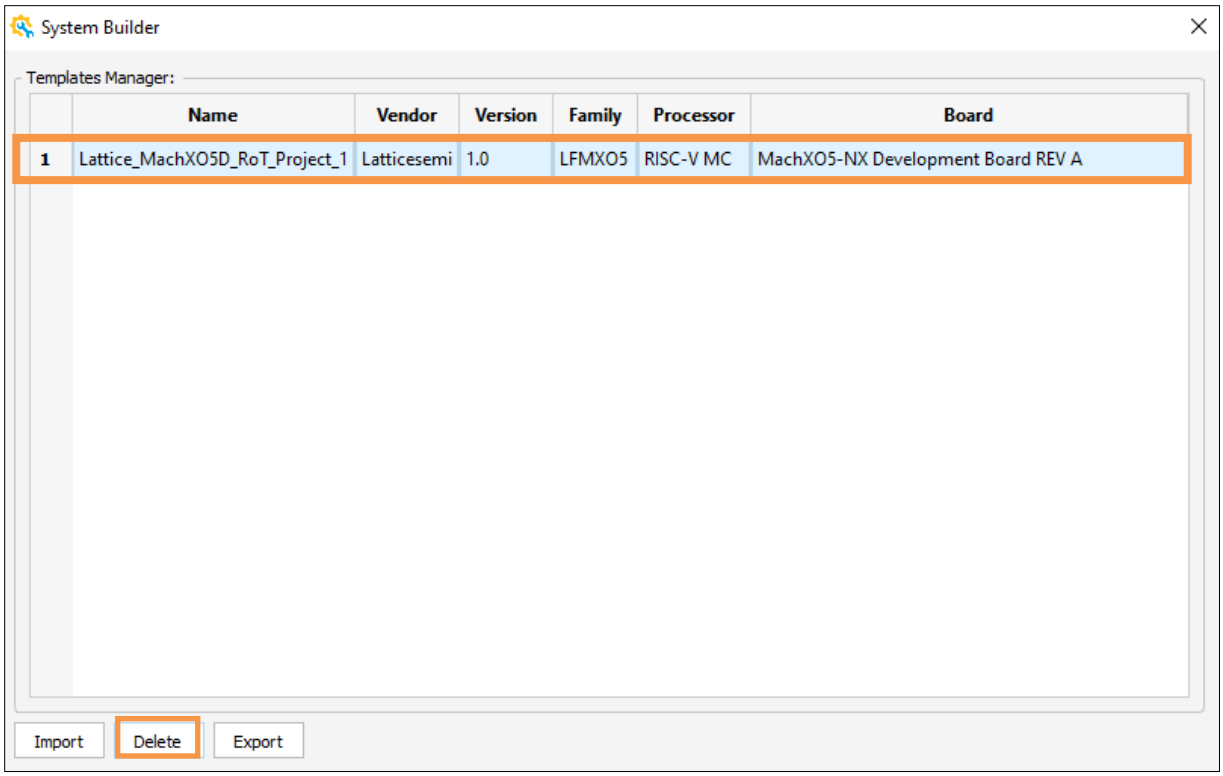


Figure 2.191. Templates Manager Page – Delete a Template

2.5.6. Include Sub Sbx File

Right-click on **Schematic View** and choose **Add Sbx Instance** (Figure 2.192), and then chose the sbx file you want to input (Figure 2.193).

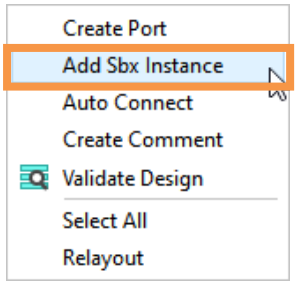


Figure 2.192. Right Click on Schematic View

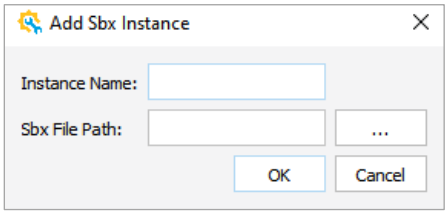


Figure 2.193. Input sbx File and Instance Name

Notes:

- The device in the sub sbx must be the same as the device in the top sbx.
- The sub sbx component name cannot be the same as that of the component in the top sbx file.

- Make sure the top-level ports of the sub sbx are the in/outs of the component in the top-level design. You need to make the ports you intend on connecting in the top sbx at the top-level in the sub sbx by exporting these ports in sub sbx.
- Only one-level of hierarchy is supported. A sub sbx file cannot have hierarchical components.
- Support verification project design flow for sub-system sbx. Only one level of sbx component instantiation is supported.

Auto memory assignment considers memory map for a subordinate or address space of a manager in the sub system sbx, if there is interconnect bus to connect them. As shown in Figure 2.194, subm_inst and subs_inst are the sub sbx instances.

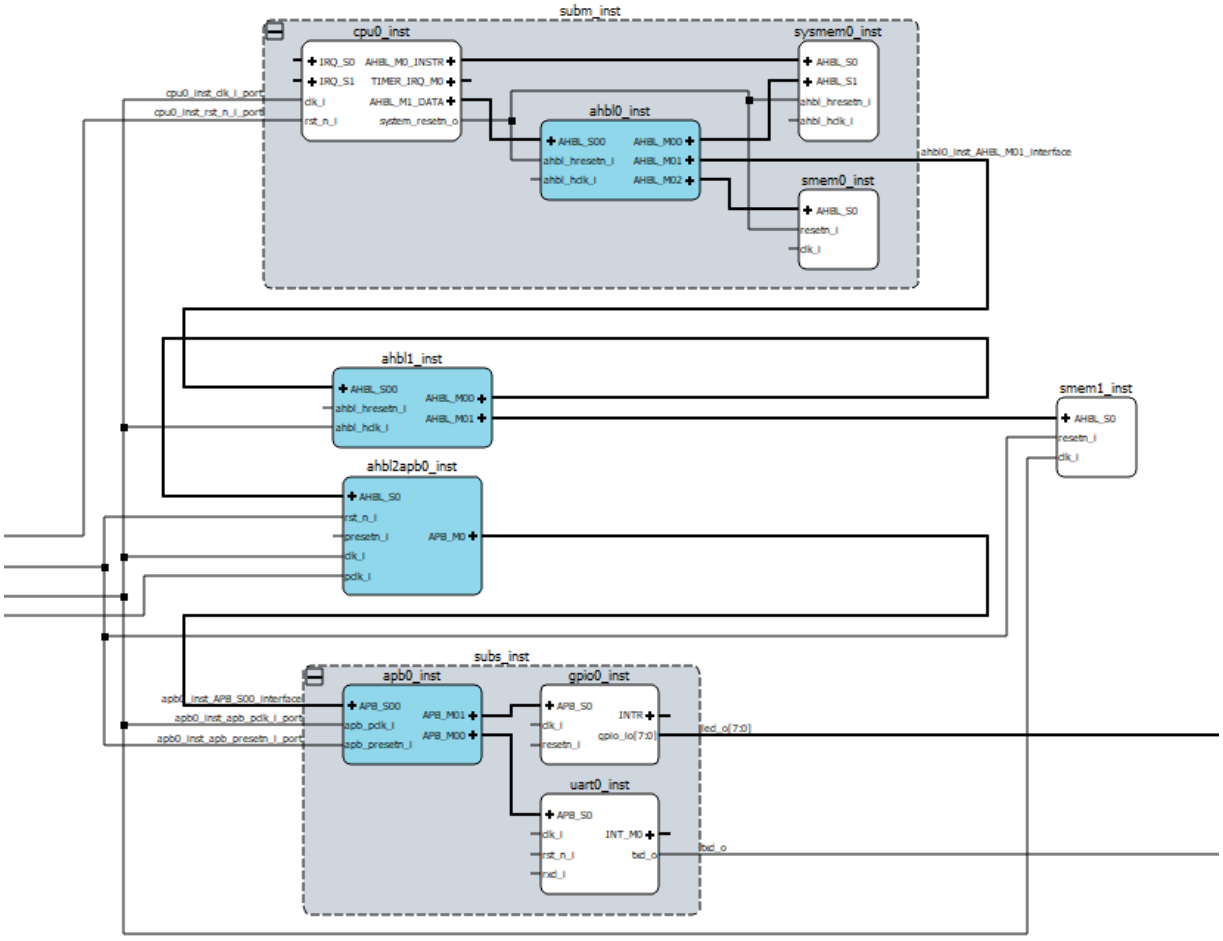


Figure 2.194. Sub Major sbx and Sub Subordinate sbx

The memory information in sub system sbx is displayed in top-level address tab (Figure 2.195).

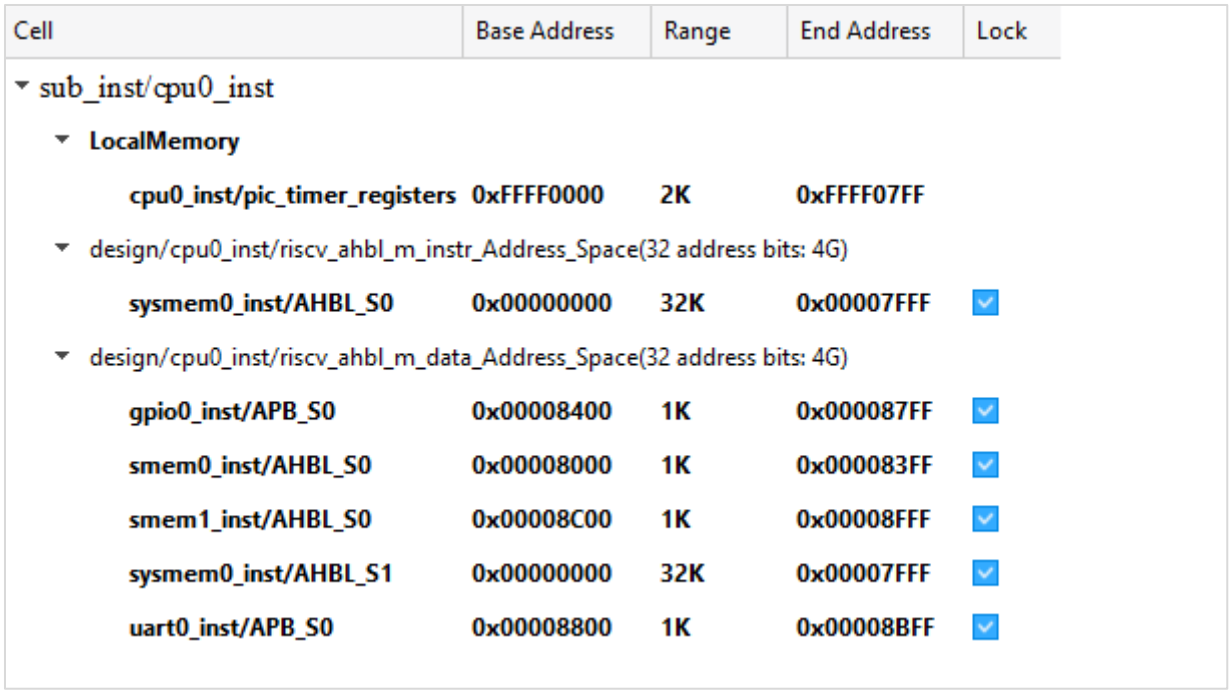


Figure 2.195. Memory Map for Sub Sbx

2.5.7. Porting Design

Apart from generating TCL for current design (see Generate Design Project TCL), Propel Builder also supports porting current project to another project with different family device.

On current project, click on **Tools > Porting Project** (Figure 2.196).

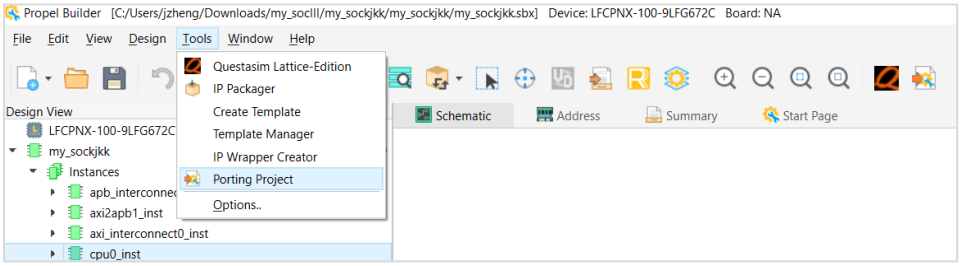


Figure 2.196. Porting Project Entry

A note pops up (Figure 2.197).

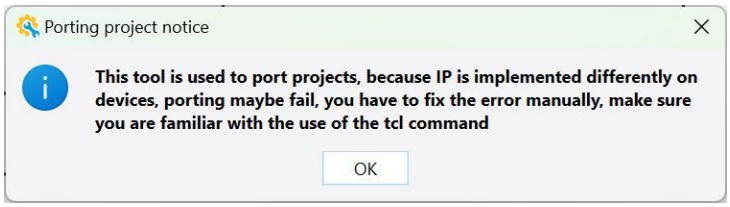


Figure 2.197. Porting Project Notice

In Porting Project Wizard, input new project information (Figure 2.198), select new device, and click **Finish** (Figure 2.199).

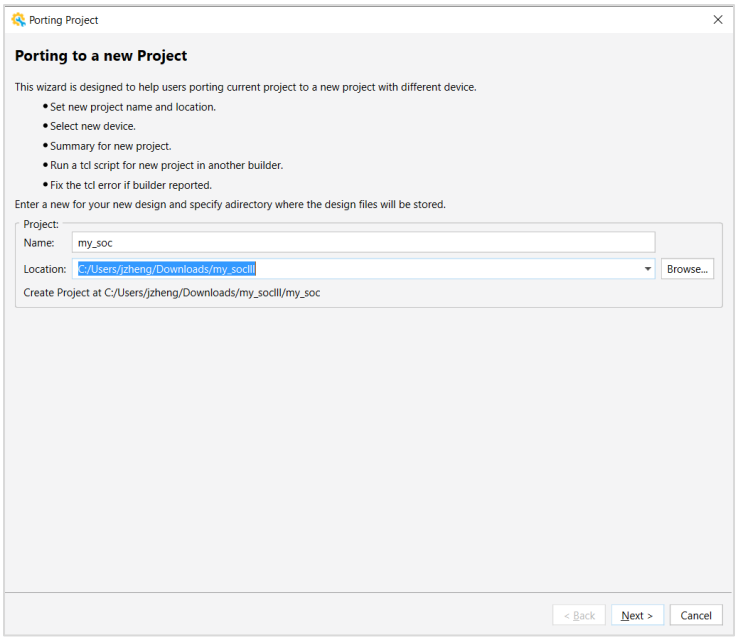


Figure 2.198. Porting Project Wizard – Input Project Name

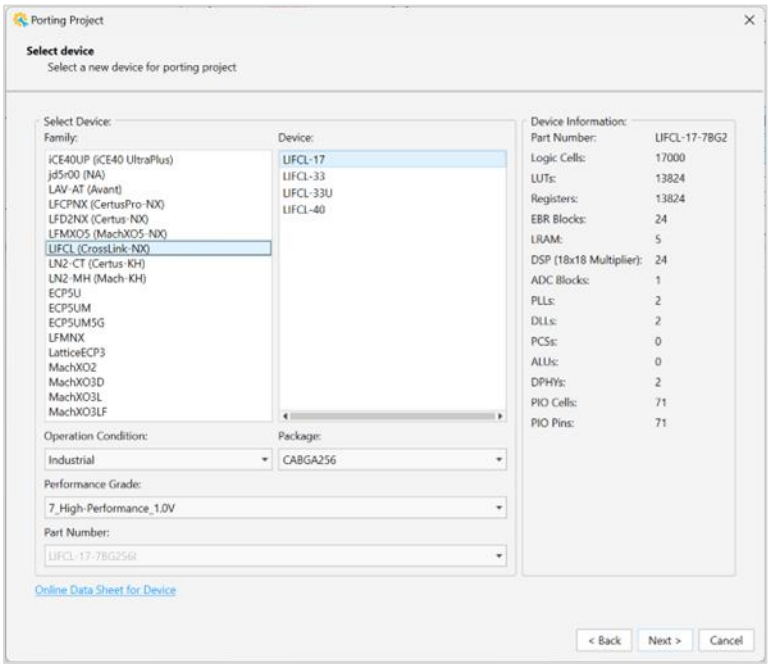


Figure 2.199. Porting Project Wizard – Choose New Family and Device

3. TCL Commands

Propel Builder provides TCL commands to execute actions. You can manually enter TCL commands in TCL Console (Figure 3.1), if you prefer using command lines rather than using the GUI.

Figure 3.1. TCL Console

3.1. sbp_design Commands

The sbp_design command is used as one of the high-level management commands such as opening, closing, of the design files created by the Propel Builder.

3.1.1. Open

Opens an existing Propel Builder design for modification.

Usage	sbp_design open -name <design name> -path <design path> [-device <device name>]
Example	sbp_design open -name project1 -path project1.sbx

3.1.2. Close

Closes a Propel Builder design currently opened.

Usage	sbp_design close

3.1.3. New

Creates a new Propel Builder design.

Usage	sbp_design new -name <new design name> -path <new design path> -device <device name> -language <language type > –board <board name>

3.1.4. Save

Saves the current Propel Builder design to file on disk or save it as a new file. You can choose to save the design to the project location (Example 1) or to a specific path (Example 2).

Usage	sbp_design save [-path <new design path>]
Example 1	sbp_design save
Example 2	sbp_design save -path new_design.sbx

3.1.5. Drc

Runs the design rule check (DRC) for the Propel Builder design file.

Usage	sbp_design drc

3.1.6. Generate

Generates RTL code to instantiate and connect the IP cores specified in the Propel Builder design file.

Usage	sbp_design generate

3.1.7. Auto Assign Addresses

Automatically assigns memory mapped addresses to all the subordinates in the system. These addresses should be chosen to avoid subordinates with multiple non-contiguous address ranges.

Usage	sbp_design auto_assign_addresses

3.1.8. Verify

Launches the SoC verification engine to verify design.

Usage	sbp_design verify [-h] [--workfolder <workfolder_path>] [--sbx_file <sbx_file_path>] {sim_gen,pfr_pack,regmap_gen,auto_run} positional arguments: {sim_gen,pfr_pack,regmap_gen,auto_run} specify the application sim_gen Simulation Generation Flow pfr_pack PFR Security Engine Packager Flow regmap_gen Memory Map Generation Flow auto_run Automation Flow optional arguments: -h, --help show this help message and exit --workfolder WORKFOLDER, -wf WORKFOLDER assign the working folder. Otherwise, the default one (current working folder) is used --sbx_file SBX_FILE, -sf SBX_FILE specify the sbx file
Example	sbp_design verify –workfolder ./mem_map –sbx_file D:/ /XO3D_Initial/XO3D_Initial.sbx regmap_gen

3.1.9. PGE

Runs command with different parameters to call SGE function, DGE function, and Signature inside of PGE (Package Generate Engine).

- Runs command to call SGE to generate files for SDK.

Usage	sbp_design *pge sge –I <input path> [-o <output path>]* -i [Required] the top-level SoC project sbx file full path. -o [Optional] output full path, if the parameter is not specified, output path is the same as SoC project path. sge folder is generated at output path, at present sge folder under the SoC project root directory.

- Runs command to call DGE to generate TCL script that can be used to generate a Diamond or Radiant project.

Usage	sbp_design *pge dge –i <input path> [-o <output path>] [-diamond|-radiant]* -i [Required] the top level SoC project sbx file full path. -o [Optional] output full path, if the parameter is not specified, output path is the same as SoC project path. For DGE, TCL script and related files are generated at output path. At present, Diamond or Radiant project share the same workspace with SoC project. -diamond [Optional] flag to execute DGE for diamond project. -radiant [Optional] flag to execute DGE for Radiant project.

- Run command to generate signature.
- PGE gets partial UFM3 contents including version packetI), Sentry PFR configure data (D), and call Flash Address Tool to sign with private key from Factory HSM.

Usage	sbp_design *pge* gen_signature -cfile <c binary file> -dfile <d binary file> -output <output binary file>

3.1.10. Undo

Undo operation. Currently, software only supports single undo.

Usage	sbp_design undo

3.1.11. Redo

Redo operation. Currently, software only supports single redo.

Usage	sbp_design redo

3.1.12. Set Device

Modify the device information including device, package, speed, operating condition.

Usage	sbp_design set_device -device <device name> -speed <speed value> -package <package value> -operating <operating condition>

3.1.13. Set Project Option

Change the output language (Verilog or VHDL) after the project was created.

Usage	sbp_design set_prj_option -language <Verilog or VHDL>
Example	sbp_design set_prj_option -language Verilog

3.1.14. Generate Design Project TCL

Generate TCL file for design project in project folder.

Usage	sbp_design gen_tcl -proj_dir <project directory> -proj_name <project name> [-propel_dir <propel directory>] [-o <output name of the generated script>]
Example	sbp_design gen_tcl -proj_dir D:/lscc/mywork -proj_name myproj -o gen_newsbx.tcl

3.2. Other TCL Commands

The following commands are used for specifying connectivity and IP instantiation to the Propel Builder backend.

3.2.1. sbp_create_project

Create a new propel builder project.

Usage	sbp_create_project -name <new_project_name> -path <project_path> -language <Verilog/Vhdl> -psc <constrain_file_name> -device <device_name> -speed <device_speed> -board <board_name(version)>

3.2.2. sbp_add_component

Instantiates an IP component into the system. Must specify the component VLNV identifier. This corresponds to a component instance in the IP-XACT design. For example, the command below can instantiate an AHB-Lite interconnect component.

Usage	sbp_add_component -vlnv <VLNV> -name <instance_name>
Example	sbp_add_component -vlnv lattice:ip:ahbl_interconnect:1.0 -name ahblite_interconnect

3.2.3. sbp_add_sbxcomp

Instantiates a hierarchical component from sbx file into the system.

Usage	sbp_add_sbxcomp -name <hname> -path <sbx_file_absolute_path_name>
Example	sbp_add_sbxcomp -name sim_comp -path “C:/test/test.sbx”

3.2.4. sbp_config_ip

args:

- -vlnv: component vlnv, consisted with vendor, library, name, version. When use this TCL command, vendor, library, version of component must be the same as meta_vlnv.
- -meta_vlnv: Location of IP configuration file by vendor library name and version, use theTCL ip_catalog_list to get it. Usage: vendor:library:name:version.
- -cfg_value: IP configuration value: {id:value, id1:value1}.
- -meta_loc: Location of IP module package.
- -cfg: Location of IP configuration file.

Note: This TCL command must contains one of -meta_vlnv and -meta_loc, also -cfg_value and -cfg.

Usage1	sbp_config_ip -vlnv <component vlnv> -meta_vlnv {IP vlnv} [-cfg_value <IP configuration value>]
Example1	sbp_config_ip -vlnv {latticesemi.com:ip:gpio0:1.6.1} -meta_vlnv {latticesemi.com:ip:gpio:1.6.1} -cfg_value {DIRECTION_DEF_VAL_INPUT:FF,IO_LINES_COUNT:8,OUT_RESET_VAL_INPUT:FF}
Usage2	sbp_config_ip -vlnv <component vlnv> -meta_loc {location} -cfg <IP configuration file>
Example2	sbp_config_ip -vlnv {latticesemi.com:module:osc1:2.0.A} -meta_loc {/home/user/work/osc} -cfg {/home/user/work/tt1/tt1/.lib/latticesemi.com/module/osc1/2.0.A/osc1.cfg}

3.2.5. ip_catalog_list

Return a list of IP, local IP contains the IP from Propel install package, IP server and customer's packaged IP, server IP contains the IP in server. Only get local IP by default.

args:

-server: Get IP list in server.

Usage	ip_catalog_list [-name <IP wild name>] [-library <IP wild library>] [-vendor <IP wild vendor>] [-version <IP wild version>] [-server]
Example	ip_catalog_list -name adder*

3.2.6. ip_catalog_install

Install one IP from local ipk file or one IP from server.
args:

- -vlnv: Location of IP configuration file by vendor library name and version, use the tcl ip_catalog_list to get it. Usage: vendor:library:name:version.
- -file: ipk file on user local path.

Usage	ip_catalog_install [-vlnv <IP vlnv>] [-file <ipk file name>]
Example	ip_catalog_install -vlnv latticesemi.com:ip:watchdog_timer:1.1.0 -file <local path>/watchdog_timer.ipk

3.2.7. ip_catalog_uninstall

Uninstall one IP from local IPs, ip_catalog_list can list all installed local IPs.
args:

-vlnv: Location of IP configuration file by vendor library name and version, use the tcl ip_catalog_list to get it. Usage: vendor:library:name:version.

Usage	ip_catalog_uninstall [-vlnv <IP vlnv>]
Example	ip_catalog_uninstall -vlnv latticesemi.com:ip:watchdog_timer:1.1.0

3.2.8. sbp_upgrade_component

Reconfig component with latest IP version.

Usage	sbp_upgrade_component -all/-component <component name> [-force_update] [-version <version number>]
Example	sbp_upgrade_component -component gpio0_inst -version 2.5.0

3.2.9. sbp_add_gluelogic

Instantiates a gluelogic component into the system.

Usage	sbp_add_gluelogic –name <instance_name> -logicinfo <logic json info from sbp_create_glue_logic>
Example	sbp_add_gluelogic -name equation_module_inst -logicinfo [sbp_create_glue_logic equation equation_module {}“{ {"”x”r":"!A ” ”B","module_”a”e":"equation_mo”ule"}}]

Note: This is an internal command. Modify existing usage is not recommended.

3.2.10. sbp_create_glue_logic

Create gluelogic information when adding gluelogic component. rtl_path must be a file path if gluelogic comes from a file. Else be empty.

Usage	sbp_create_glue_logic <type> <module_name> <rtl_path> <json cfg data>
Example	sbp_add_gluelogic -name equation_module_inst -logicinfo [sbp_create_glue_logic equation equation_module {}“{ {"”x”r":"!A ” ”B","module_”a”e":"equation_mo”ule"}}]

Note: This is an internal command. Modify existing usage is **not** recommended.

3.2.11. sbp_ reconfig _gluelogic

Allow you to reconfig gluelogic component.

Usage	sbp_ reconfig _gluelogic –name <instance_name> -logicinfo <logic json info from sbp_create_glue_logic>
Example	sbp_reconfig_gluelogic -name equation_module0_inst -logicinfo [sbp_create_glue_logic equation equation_module0 {} { {"expr":"A & B","module_name":"equation_module0"}}]

Note: This is an internal command. Modify existing usage is not recommended.

3.2.12. sbp_add_port

Creates a top-level I/O port. Must specify the direction.

Usage	sbp_add_port [-from <bit number>] [-to <bit number>] -direction <in/out/inout> <port_name>

3.2.13. sbp_modify_port

Modify existing top-level ports to change the width and the direction.

Usage	sbp_modify_port -name <port_name> [-from <bit number>] [-to <bit number>] -direction <dir.>

3.2.14. sbp_connect_net

Connects all of the specified pins and/or ports to the same net. The arguments can be pins or ports in the system design. Only one of the arguments can be the driver (output pin/port), driving all other input pin/ports. Example below connects the clk port to all components, assuming component pins are all named clk.

Usage	sbp_connect_net [-name <net name>] <pin/port> <pin/port>
Example	sbp_connect_net [sbp_get_pins clk] {CLOCK_IN}

3.2.15. sbp_connect_interface_net

Connects a bus interface pin/port to another interface pin/port. This corresponds to the interconnection element in the IP-XACT design.

Usage	sbp_connect_interface_net <pin/port> <pin/port>

3.2.16. sbp_connect_constant

Connects a constant integer to a pin/pinbus/port/portbus. To assign to a pin/pinbus, the object must be an input pin/pinbus. To assign to a port/portbus, the object must be an output port/portbus. If the integer requires multiple bits, not 0 or 1, then the object must be a bus. The TCL command can be used to assign the same constant to multiple pin/pinbus/port/portbus at the same time.

Usage	sbp_connect_constant -constant <integer> <pin/pin bus/ port/portbus> <pin/pin bus/ port/portbus>…
Example	sbp_connect_constant -constant 1 {test/i2c_mst_apb/rst_n_i} {test/riscv/clk_i}

3.2.17. sbp_connect_whitebox

You can do connection cross the hierarchy boundary for verification purpose.

Usage	sbp_connect_whitebox <design_name/vip_inst_name/pin_name> <design_name/uit_inst_name/port_name>

3.2.18. sbp_connect_ group

Allow you to connect a group of signals.

Usage	sbp_connect_group -ports {<source port1> <destination port1> <destination port2>; <source port2> <destination port3> <destination port4>} -nets {<net_name1> <destination portm1> <destination portm2>; <net_name2> <destination portm3>} -interfaces {<interface1> <interface2>; <interface3> <interface4>}

3.2.19. sbp_disconnect_whitebox

Removes the connection cross the hierarchy boundary.

Usage	sbp_disconnect_whitebox <design_name/vip_inst_name/pin_name> <design_name/uit_inst_name/port_name>

3.2.20. sbp_disconnect_interface_net

Disconnects an interface pin/port from the interface nets they attached to. Note that any interface pin or interface port can attach to one interface net at the most.

Usage	sbp_disconnect_interface_net <pin/port> <pin/port>

3.2.21. sbp_disconnect_net

Disconnects all of the specified input pins and/or ports from the nets they attached to. Note that any pin or port can attach to one net at the most. Can also be used to disconnect a constant that is connected to a pin/port with connect_constant.

Usage	sbp_disconnect_net <pin0> <pin1> <port2>

3.2.22. sbp_assign_addr_seg

Assigns a memory map between a pair of manager and subordinate interfaces. Range specifies the range of the segment, for example, 32‘h0000400, 32‘h0001000. Offset specifies the base offset of the range, for example, 32‘h0000400

Usage	sbp_assign_addr_seg -offset <offset> < subordinate connection name>
Example	sbp_assign_addr_seg -offset 32‘h00001000 simple/riscv/AHBL_S00

3.2.23. sbp_unassign_addr_seg

The TCL command unsets the fixed offset flag for a memory map allowing the auto_assign TCL command to assign the memory map offset.

Usage	sbp_unassign_addr_seg < subordinate interface name>
Example	sbp_unassign_addr_seg simple/spi/AHB_S00

3.2.24. sbp_assign_local_memory

Assigns a base address to a local memory map of a manager address space.

Usage	sbp_assign_local_memory -offset <offset> <master_addr_space>
Example	sbp_assign_local_memory -offset ‘h0050000 Foundation_SoC/riscv/ahbl_m_data_Address_Space

3.2.25. sbp_export_pins

Exports a list of pins or interface pins, or all not-yet-connected pins of the components to the top-level port list in the design. The function detects whether or not the argument is pin(s) or component(s). In the two examples below, Example 1 demonstrates a TCL command to export the pin init_done, while Example 2 demonstrates a TCL command to export all pins and interfaces of the ddr3 component.

Usage	sbp_export_pins <pin/component> <pin/component>
Example 1	sbp_export_pins {ddr3/init_done}
Example 2	sbp_export_pins {ddr3}

3.2.26. sbp_export_interface

Exports bus interfaces that are passed as arguments to the TCL command from the component to the top-level component. Example below exports the AHBL_MASTER bus interface of the RISC-V component to the top-level component.

Usage	sbp_export_interfaces <interface> <interface> <interface>
Example	sbp_export_interfaces simple/riscv/AHBL_MASTER

3.2.27. sbp_rename

The rename TCL command renames objects within the design. The new name of the object and the current hierarchical name of the given object are used as the parameter value. The object can be an interface connection, connection, port, interface, or component. The example below demonstrates the changing of the name of a port in milestone project from CLK to CLOCK.

Usage	sbp_rename -name <new name> <object name>
Example	sbp_rename -name CLOCK milestone/CLK

3.2.28. sbp_replace

The Replace (Re-Config) TCL command replaces a component with a new configuration for itself. VLNV refers to the newly-generated IP, component name refers to the existing component that is to be replaced, and instance refers to the instance name of the component with new configuration.

Usage	sbp_replace -vlnv <VLNV> -name <instance> -component <component name>
Example	sbp_replace -vlnv lattice:ip:ahblite_bus_0:1.1 -name ahbl_bus_0 -component simple/ahblite

3.2.29. sbp_copy

Copies objects, IP instances and nets, from the current or other open sbp designs to the current sbp design. All objects are post-fixed with a postfix string. For example, you can write TCL code below to duplicate the components and connections with new instance names post fixed with X, by calling copy on all the components, ports and nets. Pins are automatically duplicated while the components are duplicated.

Usage	sbp_copy -postfix <postfixString> objects
Example	sbp_copy –postfix X $selected_objs

3.2.30. sbp_delete

Deletes objects, IP instances and nets, from the current sbp design. In the examples below, Example 1 demonstrates a TCL command to delete a port, while Example 2 demonstrates a TCL command to delete ddr3 component.

Usage	Sbp_delete objects -type <type name>
Example 1	sbp_delete [sbp_get_ports <clock>] -type port
Example 2	sbp_delete {ddr3} -type component

3.2.31. sbp_get_pins

Gets a list of pin names that match a pattern string, and/or the pins that are associated with an object. The object in the [-from <objectName>] option can be a net or a component. The component name is the path name of the instance. The example below gets the clk pin from the interconnect component.

Usage	sbp_get_pins [-from <object Name>] [pattern]
Example	sbp_get_pins -from my_soc/ahblite_interconnect_inst0 clk

3.2.32. sbp_get_interface_pins

Gets a list of interface names that match a pattern string, and/or the interfaces that are associated with an object. The object in the [-from <objectName>] option can be an interface net or a component. The example below can get all AHB-Lite subordinate interface pins from the interconnect IP.

Usage:	sbp_get_interface_pins [-from <objectName>] [pattern]
Example:	sbp_get_interface_pins -from ahblite_interconnect S*_AHB

3.2.33. sbp_get_ports

Get a list of the names of ports that match a pattern string, and/or the ports that are associated with an object. The object in the [-from <objectName>] option can be a net.

Usage	sbp_get_ports [-from <objectName>] [pattern]

3.2.34. sbp_get_interface_ports

Gets a list of interface names that match a pattern string, and/or the interface ports that are associated with an object. The object in the [-from <objectName>] option can be an interface net.

Usage	sbp_get_interface_ports [-from <objectName>] [pattern]

3.2.35. sbp_get_nets

Gets a list of net names that match a pattern string, and/or the nets that are associated with an object. The object in the [-from <objectName>] option can be a pin or a port.

Usage	sbp_get_nets [-from <objectName>] [pattern]

3.2.36. sbp_get_interface_nets

Gets a list of interface net names that match a pattern string, and/or the interface nets that are associated with an object. The object in the [-from <objectName>] option can be an interface pin or an interface port.

Usage	sbp_get_interface_nets [-from <objectName>] [pattern]

3.2.37. sbp_set_property

Sets the properties of an input object. The first argument is a list of name value pairs. We have a list of parameters because the GUI IP configuration dialog submits changes to many parameters of an IP component at the same time when the dialog is closed. In the examples below, Example 1 changes the data width of the RAM block named ebr_0, while Example 2 changes the number of manager interfaces to two and number of subordinate interface to three on AHB-Lite interconnect block named ahbl_interconnect.

Usage	sbp_set_property <name0 value0 name1 value1 …> object
Example 1	sbp_set_property {datawidth 32} {test/ebr_0}
Example 2	sbp_set_property {NUM_MI 2 NUM_SI 3} test/ahbl_interconnect

3.2.38. sbp_get_property

Gets the property of the object. The example below is to get the number of subordinate interfaces of AHB-Lite interconnect block named ahbl_interconnect_0.

Usage	sbp_get_property <parameter name> <object>
Example	sbp_get_property NUM_SI ahbl_interconnect_0

3.2.39. sbp_report_properties

Prints all the properties and values associated to the type of the object.

Usage	sbp_report_properties object
Example	sbp_report_properties ahbl_interconnect
Outputs	Name: ahbl_interconnect NUM_SI: 1 NUM_MI: 2 DATA_WIDTH: 32 ADDRESS_WIDTH: 32

3.2.40. sbp_get_components

Gets a list of component names that match a pattern string, and/or the components that are associated with an object. The default pattern string is a wildcard "*" that matches all components. The pattern string may consist of string segments and wildcards. The example below returns all the component names that contain "interconnect". The command returns an empty string if no match is found.

Usage	sbp_get_components <component name>
Example	sbp_get_components {*interconnect*}

3.2.41. sbp_cable

Open/list/close FTDI USB port.

Usage1	sbp_cable open [-port <port>] [-divisor <divisor>]
Example	sbp_design open -port 0 sbp_design open -port 1 -divisor 59
Usage2	sbp_cable list
Example	% sbp_cable list ---------- Port | Name | Cable | Channel | Location ---------- 0 * | FTUSB-0 | Lattice HW-USBN-2B Ch A | A | 0 1 | FTUSB-1 | Dual RS232-HS A | A | 2 2 | FTUSB-2 | Dual RS232-HS B | B | 3 ---------- '*' indicates the port is open.
Usage3	sbp_cable close
Example	sbp_cable close

3.2.42. sbp_read_memory

Read memory value from given address. The design should include 'JTAG Bridge' IP.

-addr: 32 bits address

-data_width(optional): specify data width, valid width includes 8/16/32, and 32 is default.

Usage	sbp_read_memory -addr <address 32> [-data_width 8/16/32]
Example	sbp_read_memory -addr 0x30010000 sbp_read_memory -addr 0x30010000 -data_width 16

3.2.43. sbp_write_memory

Write memory value to the given address. The design should include ‘JTAG Bridge’ IP.

-addr: 32 bits address

-data: specify the memory value. If the width of the data is less than 32 bits, fill zero to the high bits until it reaches 32 bits. For example, 0x172A is regarded as 0x0000172A.

-data_width(optional): specify data width, valid width includes 8/16/32, and 32 is default.

Usage	sbp_write_memory -addr <address 32> -data <value> [-data_width 8/16/32]
Example	sbp_write_memory -addr 0x30010000 -data 0x172A -data_width 16

References

- Lattice Propel 2025.2 SDK User Guide (FPGA-UG-02244)
- Lattice IP Packager 2025.2 User Guide (FPGA-UG-02242)
- Revision Control – Lattice Propel Builder 2025.2 (FPGA-UG-02241)
- Lattice Propel 2025.2 Installation for Windows User Guide (FPGA-AN-02106)
- Lattice Propel 2025.2 Installation for Linux User Guide (FPGA-AN-02105)
- Lattice Propel 2025.2 Release Notes (FPGA-AN-02104)
- Lattice Diamond Help
- Lattice Radiant Help

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at https://www.latticesemi.com/Support/AnswerDatabase

Revision History

Revision 1.0, December 2025

Section	Change Summary
All	Production release.

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