LTPI Quick Start Guide

Application Note

FPGA-AN-02108-1.0

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Inclusive Language

This document was created consistent with Lattice Semiconductor’s inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice’s inclusive language FAQ 6878 for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

Contents

Figures

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Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviation	Definition
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
DC-SCM	Datacenter Secure Control Module
DDR	Dual Data Rate
EBR	Embedded Block RAM
FPGA	Field-Programmable Gate Array
GPIO	General Purpose Input/Output
HPM	Host Processor Module
I/O	Input/Output
I2C	Inter-Integrated Circuit
IP	Intellectual Property
LLGPIO	Low Latency General Purpose Input/Output
LTPI	Low-Voltage Differential Signaling Tunneling Protocol and Interface
LUT4	4-input Look-Up Table
LVDS	Low-Voltage Differential Signaling
MCTP	Management Component Transport Protocol
NLGPIO	Normal Latency General Purpose Input/Output
OCP	Open Compute Project
OEM	Original Equipment Manufacturer
PCB	Printed Circuit Board
PFU	Programmable Function Unit
SCM	Secure Control Module
SMBus	System Management Bus
UART	Universal Asynchronous Receiver/Transmitter

1. Introduction

This document serves as a quick reference for server design architects and FPGA users working with the Lattice LVDS Tunneling Protocol and Interface (LTPI), an OCP Ready™ solution. Lattice LTPI complies with the latest OCP specifications, ensuring hardware interoperability with other OCP-compliant vendors.

Defined by the OCP, LTPI is a signal aggregation protocol designed to tunnel low-speed data signals such as General Purpose I/O (GPIO), Inter-Integrated Circuit (I2C), and Universal Asynchronous Receiver/Transmitter (UART), over a Low-Voltage Differential Signaling (LVDS) channel between the DC-SCM and HPM boards.

Lattice LTPI implementation supports version 1.2 of the OCP specification. This guide provides a high-level overview of the LTPI architecture, key implementation details, and essential collateral from Lattice to help you effectively enable and integrate the protocol.

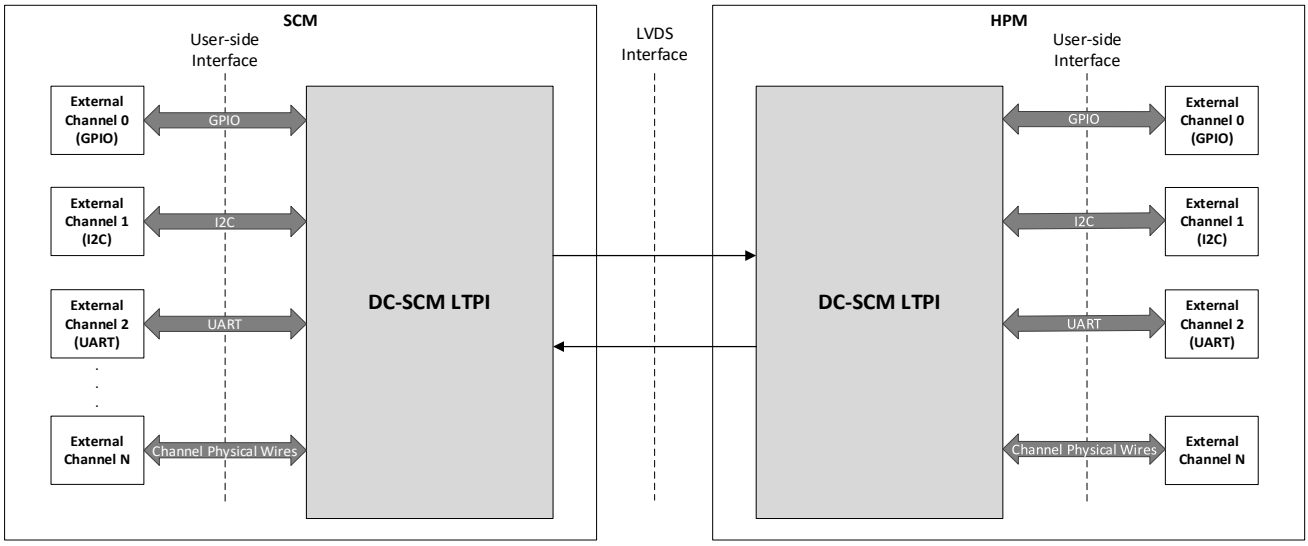

Figure 1.1. Low-Speed Data Aggregation through LTPI

2. Key Features

Key features of the Lattice LTPI solution include:

- Compliance with the DC-SCM 2.1 LTPI revision 1.1, version 1.1 specification
- Bidirectional I2C support for MCTP-type communication.
- Support for the following LTPI target speed rates:
  - Up to 600 MHz (1,200 Mbps) LTPI target speed for Lattice MachXO5™-NX devices.
  - Up to 400 MHz (800 Mbps) for Lattice MachXO3™ and MachXO3D™ devices.
- Support for AMBA 3 APB Protocol version 1.0 for register access of the soft IP and data channel.
- Interoperability with other OCP-Compliant LTPI vendors, ensuring seamless integration and compatibility across different LTPI implementations within the Open Compute Project ecosystem.
- Low power consumption:
  - 90 mW using MachXO5 devices (based on Power Calculator Tool, using LTPI Reference Design at 400 MHz target speed).
  - 360 mW using MachXO3 and MachXO3D devices (based on Power Calculator Tool, using LTPI Reference Design at 600 MHz target speed for MachXO3 devices).

For faster LTPI enablement and additional information about its features, refer to the following table.

Table 2.1. LTPI Collateral for Faster Enablement and Feature Reference

Category	Title
LTPI-specific document	DC-SCM LTPI IP User Guide (FPGA-IPUG-02200)
	DC-SCM LTPI IP Release Notes (FPGA-RN-02021)
	LVDS Tunneling Protocol and Interface (LTPI) User Guide (FPGA-RD-02247)
	LTPI Hardware Checklist (FPGA-TN-02417)
Supplemental document	MachXO5-NX Hardware Checklist (FPGA-TN-02274)
	MachXO3 Hardware Checklist (FPGA-TN-02061)
	MachXO3D Hardware Checklist (FPGA-TN-02104)
	PCB Layout Recommendations for BGA Packages (FPGA-TN-02024)
	High-Speed PCB Design Considerations (FPGA-TN-02178)
	Implementing High-Speed Interfaces with MachXO3 Devices (FPGA-TN-02057)
	Implementing High-Speed Interfaces with MachXO3D Usage Guide (FPGA-TN-02065)
	MachXO5-NX High-Speed I/O Interface (FPGA-TN-02286)
Supplemental video (available on the Lattice OCP Ready Solutions for DC-SCM and HPM CPLD Connectivity web page)	LTPI Overview
	LTPI IP Configuration Walkthrough
	LTPI Reference Design Walkthrough
	LTPI Demo

3. Resource Utilization

Table 3.1 and Table 3.3 show the resource utilization of the LTPI for SCM and HPM configurations using the following default I/O setting:

- LLGPIO: 16-bit
- NLGPIO: 16-bit
- I2C/SMBus: 6 buses
- UART: 2 channels
- OEM: 32-bit

Table 3.2 and Table 3.4 show the resource utilization for additional interfaces in the SCM and HPM configurations.

Table 3.1. SCM Default Configuration Resource Utilization

Device Family	Resource Type	LTPI Reference Design	LTPI IP (Default I/O Setting)	Miscellaneous LTPI Modules[1]
MachXO5-NX	LUT4	2702	2343	364
	PFU Register	1812	1533	276
	EBR	2	2	0
MachXO3	LUT4	2447	2087	360
	PFU Register	1708	1402	306
	EBR	2	2	0
MachXO3D	LUT4	2535	2174	361
	PFU Register	1805	1499	306
	EBR	2	2	0

Note:

1. Examples include APB Streamer, Timeout, and I2C-to-APB Bridge modules.

Table 3.2. Additional Interface Resource Utilization for SCM Configuration

Resource Utilization per Additional Data Type	LUT4	PFU Register	EBR
LLGPIO (16 bits)	0	0	0
NLGPIO (16 bits)	1	0	0
I2C/SMBus (per bus)	140	54	0
Bidirectional I2C/SMBus (per bus)	278	105	0
UART (per bus)	1	3	0
OEM (32-bit)	0	0	0

Table 3.3. HPM Default Configuration Resource Utilization

Device Family	Resource Type	LTPI Reference Design	LTPI IP (Default I/O Setting)	Miscellaneous LTPI Modules[1]
MachXO5-NX	LUT4	2936	2803	132
	PFU Register	1651	1586	65
	EBR	2	2	0
MachXO3	LUT4	2916	2822	94
	PFU Register	1671	1576	95
	EBR	2	2	0
MachXO3D	LUT4	2916	2823	93
	PFU Register	1671	1576	95
	EBR	2	2	0

Note:

1. Examples include APB Streamer, Timeout, and I2C-to-APB Bridge modules.

Table 3.4. Additional Interface Resource Utilization for SCM Configuration

Resource Utilization per Additional Data Type	LUT4	PFU Register	EBR
LLGPIO (16 bits)	0	0	0
NLGPIO (16 bits)	1	0	0
I2C/SMBus (per bus)	257	60	0
Bidirectional I2C/SMBus (per bus)	276	105	0
UART (per bus)	4	4	0
OEM (32-bit)	0	0	0

4. Power Consumption Estimate

The following table shows the power consumption of the Lattice FPGA when using LTPI, relative to the LTPI target speed.

This power data is based on the default LTPI channel configuration and was calculated using the Lattice Power Calculator Tool.

Table 4.1. Power Consumption Estimate using Lattice Power Calculator Tool

LTPI Target Speed	Power Consumption by Device Family (mW)	
	MachXO5-NX	MachXO3
600 MHz	90	—
400 MHz	78	300
200 MHz	69	253
100 MHz	65	225

5. Adaptor Board for LTPI Evaluation

Adaptor boards designed for MachXO3, MachXO3D, and MachXO5 devices are available to support rapid evaluation of the LTPI solution. These boards integrate seamlessly with either the MachXO3/XO3D Breakout Board or the MachXO5-NX Development Board.

You can purchase these adaptor boards by contacting your local Lattice Sales Office.

The following figures show the LTPI adaptor boards in various setup configurations.

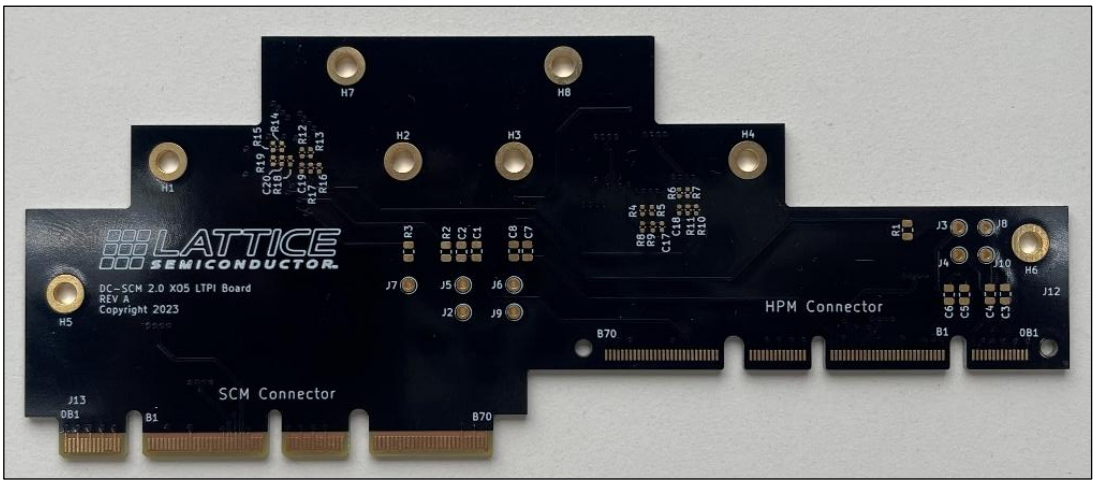

Figure 5.1. MachXO5-NX LTPI Adaptor Board

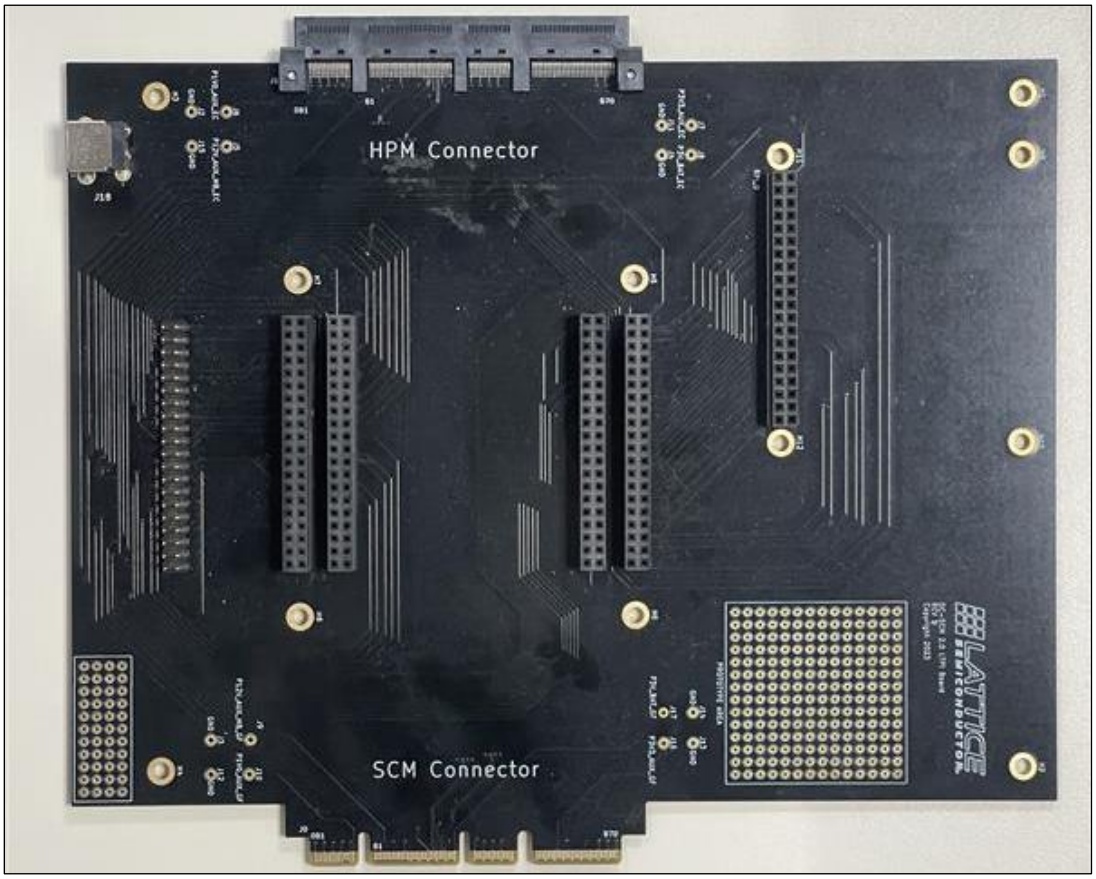

Figure 5.2. MachXO3/MachXO3D LTPI Adaptor Board

Figure 5.3. MachXO5-NX LTPI Adaptor Board with MachXO5-NX Development Board

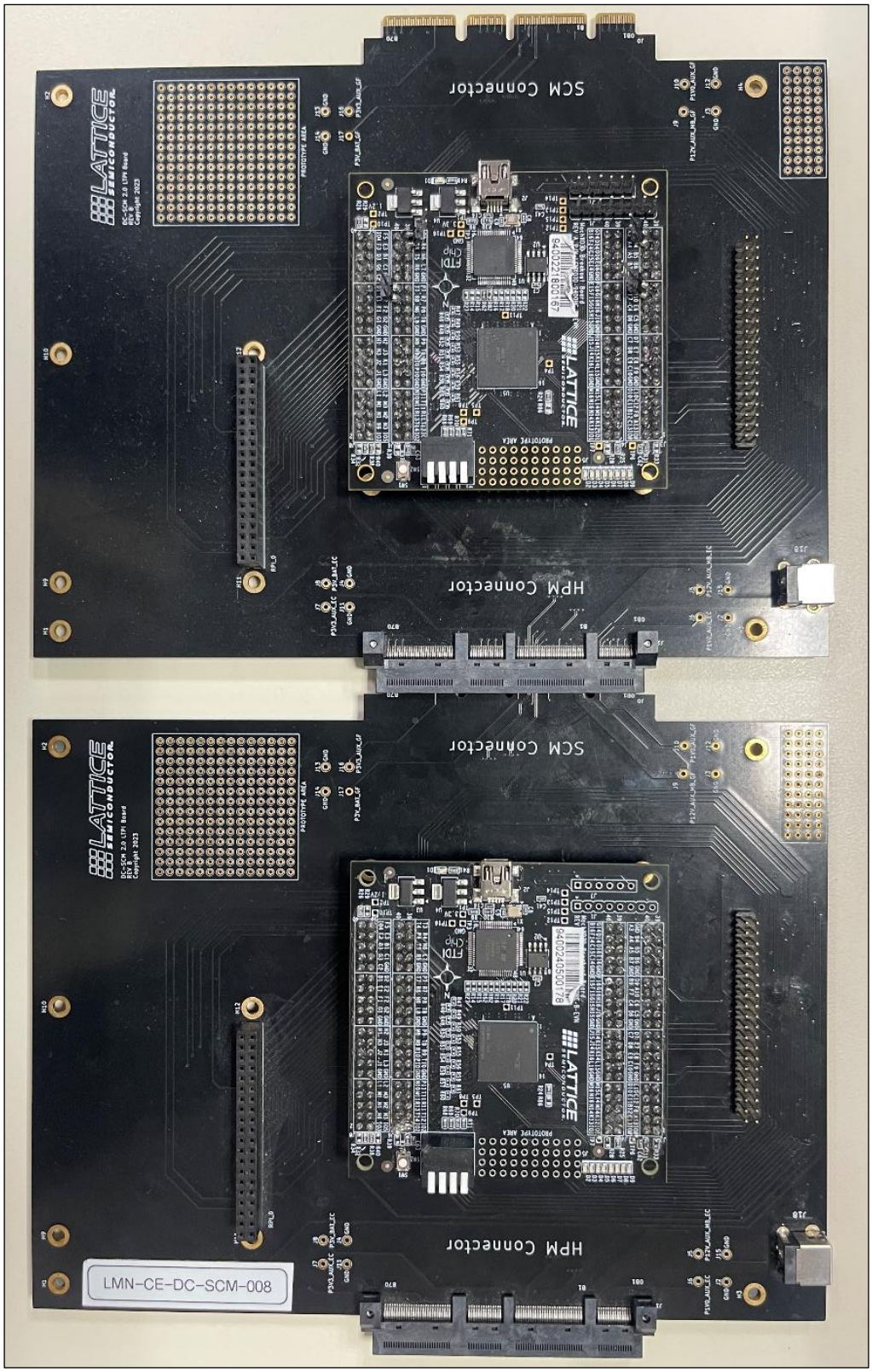

Figure 5.4. MachXO3/MachXO3D LTPI Adaptor Board with MachXO3/XO3D Breakout Board

References

- DC-SCM LTPI IP User Guide (FPGA-IPUG-02200)
- DC-SCM LTPI IP Release Notes (FPGA-RN-02021)
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- Implementing High-Speed Interfaces with MachXO3D Usage Guide (FPGA-TN-02065)
- MachXO5-NX High-Speed I/O Interface (FPGA-TN-02286)
- Open Compute Project web page
- Lattice OCP Ready Solutions for DC-SCM and HPM CPLD Connectivity web page
- MachXO3 web page
- MachXO3D web page
- MachXO5-NX web page
- Lattice Solutions IP Cores web page
- Lattice Solutions Reference Designs web page
- Lattice Insights web page for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, please refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 1.0, September 2025

Section	Change Summary
All	Initial release.

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