LTPI Hardware Checklist

Technical Note

FPGA-TN-02417-1.0

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Inclusive Language

This document was created consistent with Lattice Semiconductor’s inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice’s inclusive language FAQ 6878 for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

Contents

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Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviation	Definition
AC	Alternating Current
BGA	Ball Grid Array
CPLD	Complex Programmable Logic Device
DC	Direct Current
DC-SCM	Data Center – Secure Control Module
DDR	Dual Data Rate
FPGA	Field-Programmable Gate Array
HPM	Host Processor Module
I/O	Input/Output
LVDS	Low-Voltage Differential Signaling
LTPI	Low-Voltage Differential Signaling Tunneling Protocol and Interface
OCP	Open Compute Project
OSC	Oscillator
PCB	Printed Circuit Board
RTT	LVDS termination resistor
Rx	Receiver
SCM	Secure Control Module
Tx	Transmitter

1. Introduction

This technical note provides key hardware implementation guidelines for deploying the LVDS Tunnelling Protocol and Interface (LTPI) in an OCP Ready™ environment. This technical note includes a high-level checklist to verify that the LTPI-LVDS port supports the maximum data rate for the target device, complies with the latest OCP specifications, and ensures hardware interoperability with other OCP-compliant vendors.

Developed after evaluation boards, hardware checklists incorporate optimized designs that supersede the circuitry of the evaluation boards. If you copy circuits from evaluation boards, ensure that you optimize your design according to hardware checklists.

Refer to the following documents for detailed recommendations:

- MachXO3 Hardware Checklist (FPGA-TN-02061)
- MachXO3D Hardware Checklist (FPGA-TN-02104)
- MachXO5-NX Hardware Checklist (FPGA-TN-02274)
- PCB Layout Recommendations for BGA Packages (FPGA-TN-02024)
- High-Speed PCB Design Considerations (FPGA-TN-02178)
- Implementing High-Speed Interfaces with MachXO3 Devices (FPGA-TN-02057)
- Implementing High-Speed Interfaces with MachXO3D Usage Guide (FPGA-TN-02065)
- MachXO5-NX High-Speed I/O Interface (FPGA-TN-02286)
- LVDS Tunneling Protocol and Interface (LTPI) User Guide (FPGA-RD-02247)

2. DC-SCM 2.0 Requirements

As defined in the DC-SCM 2.0 Specification, the LVDS link is AC-coupled. As such, the following components are required on the hardware:

- DC Blocking Capacitor – placed on the SCM only.
- Voltage Bias Circuit – placed close to the LVDS Rx I/O Buffer.

To ensure these specifications are met within the board design, it is highly recommended that both the DC blocking capacitors and the voltage bias circuit be added externally on any user board design.

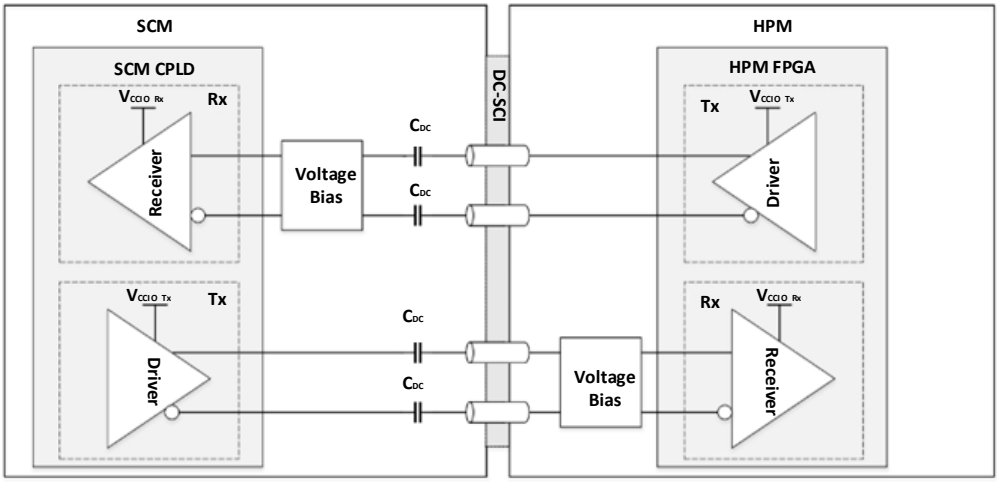

Figure 2.1. AC-Coupled LVDS Link

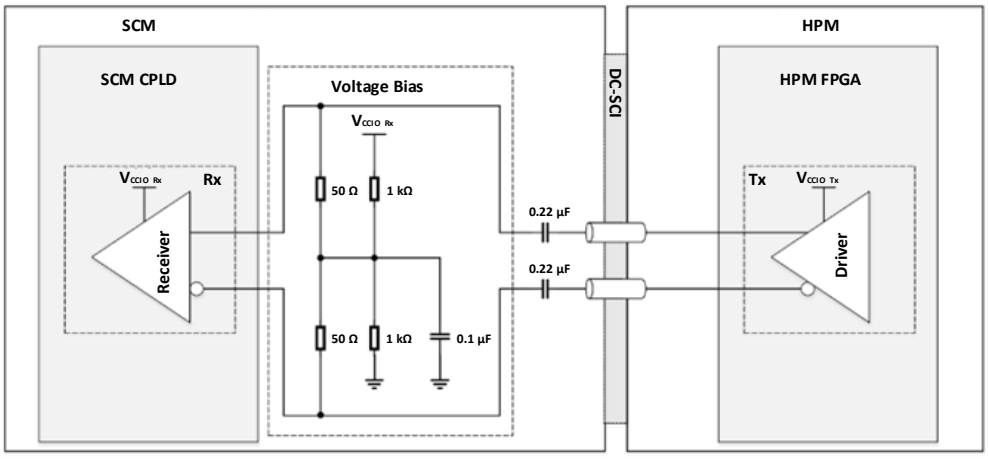

Figure 2.2. LVDS Link Resistor Value

Table 2.1. LVDS Electrical Requirements

Parameter	Minimum	Maximum	Description
VOD	100 mV	800 mV	Output differential voltage swing
VID	100 mV	800 mV	Input differential voltage swing
VCCIO Rx/Tx	2.5 V	3.3 V	LVDS VCCIO voltage. For more information, refer to the MachXO3, MachXO3D, or MachXO5-NX checklist.
VICM	—	(VCCIO RX / 2) + 20%	Input common mode voltage on LVDS I/O pins
CDC	0.22 µF	—	DC blocking capacitor
RTT	100 Ω – 5%	100 Ω + 5%	LVDS termination resistor, which can be set internally on the device.

3. FPGA Pin Assignments

This section provides guidance on the FPGA pin assignments for the input and output LVDS link.

3.1. MachXO3 and MachXO3D Devices

The FPGA pin assignments for MachXO3™ and MachXO3D™ devices are as follows:

- Input LVDS: These signals are assigned only to A/B pairs (PBxxA/PBxxB) on Bank 2. In addition, the LVDS clock is assigned to a PCLK pin (PCLKT2_x /PCLKC2_x).
- Output LVDS: These signals are assigned only to A/B pairs (PTxxA/PTxxB) on Bank 0.

3.2. MachXO5-NX Devices

For MachXO5™-NX devices, the FPGA pin assignments for the LVDS pairs (both input and output) are mapped to high-performance I/O banks, specifically the bottom banks.

4. PCB Trace Length

PCB length differences on the LTPI LVDS link must be managed to ensure DDR timing parameters are met:

- The PCB trace length difference between the LVDS pair (**_DN* and **_DP*) is less than 5 mil.
- The PCB trace length difference between CLK and Data for each lane is less than 200 mil.

5. Computing and Measuring Input Setup and Hold time.

By default, the LTPI LVDS link uses:

- GDDRX4_RX_CENTERED for MachXO3 or MachXO3D devices
- GDDR5_RX_ECLK_CENTERED for MachXO5-NX devices

To ensure the link meets the maximum LTPI speed, the measured Input Data Setup before ECLK (t_{SU}) and Input Data Hold after ECLK (t_{HO}) must exceed the minimum values specified in Table 5.1 and Table 5.2.

Timing measurements for t_{SU} and t_{HO} are defined as follows:

- t_{SU} is measured from V_{THD} (±80 mV) of the LTPI_DATA signal to V_{ICM} of LTPI_CLK.
- t_{HO} is measured from V_{ICM} of LTPI_CLK to V_{ICM} of LTPI_DATA, as shown in Figure 5.1.

Table 5.1. MachXO3 and MachXO3D DDRX4 Setup and Hold Time

Parameter	Description	Device	Speed Grade – 6	Speed Grade – 5	Units
Generic DDR4 Inputs with Clock and Data Centered – GDDR4_RX.ECLK.Centered[1]					
t_{SU}	Input Data Setup before ECLK	MachXO3 MachXO3D	0.233	0.233	ns
t_{HO}	Input Data Hold after ECLK		0.287	0.287	ns

Note:

1. The duty cycle is ±5% for system usage.

Table 5.2. MachXO5-NX DDRX5 Setup and Hold Time

Parameter	Description	Device	Speed Grade – 9	Speed Grade – 8	Speed Grade – 7	Units
Generic DDRX5 Inputs with Clock and Data Centered – GDDRX5_RX/TX.ECLK.CENTERED						
t_{SU}	Input Data Setup before ECLK	MachXO5-NX	0.231	0.231	0.224	ns
t_{HO}	Input Data Hold after ECLK		0.289	0.229	0.224	ns

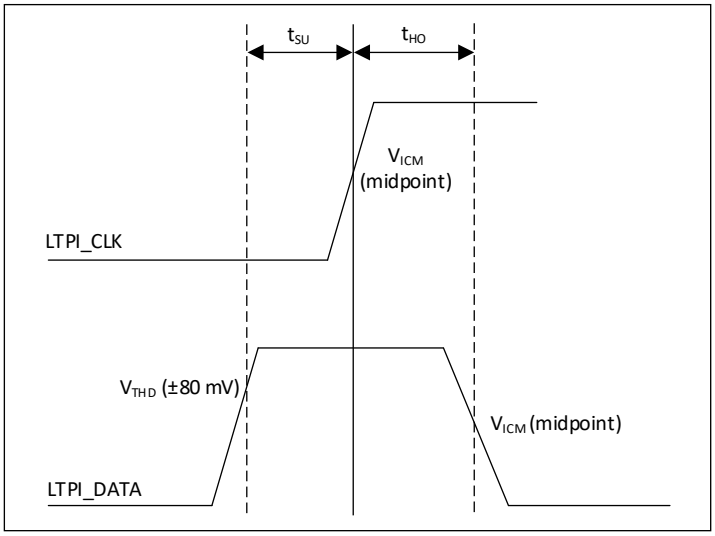

Figure 5.1. Measuring the Input Data Setup before EClk (t_{SU}) and Input Data Hold after EClk (t_{HO})

Aside from the default DDR gearing, the LVDS link can be set to GDDRX4_RX.ECLK.Aligned for MachXO3 or MachXO3D devices and GDDRX5_RX/TX.ECLK.Aligned for MachXO5-NX devices. To ensure it meets the maximum LTPI speed, the measured Input Data Valid after CLK (t_{DVA}) and Input Data Hold after CLK (t_{DVE}) must not exceed the maximum value, while the Input Data Hold after CLK (t_{DVE}) must also exceed the minimum value specified in Table 5.3 and Table 5.4.

Timing measurements for t_{SU} and t_{HO} are defined as follows:

- T_{DVA} is measured from V_{ICM} of the LTPI_CLK signal to V_{THD} of LTPI_DATA.
- T_{DVE} is measured from V_{THD} of LTPI_DATA to V_{ICM} of LTPI_DATA, as shown in Figure 5.2.

Table 5.3. MachXO3 and MachXO3D DDRX4 Data Valid and Hold Time

Parameter	Description	Device	Speed Grade – 6	Speed Grade – 5	Units
Generic DDR4 Inputs with Clock and Data Aligned – GDDR4_RX.ECLK.Aligned					
t_{DVA}	Input Data Valid after CLK	MachXO3 MachXO3D	0.384 (max)	0.4 (max)	ns
t_{DVE}	Input Data Hold after CLK		0.9775 (min)	0.874 (min)	ns

Table 5.4. MachXO5-NX DDRX5 Data Valid and Hold Time

Parameter	Description	Device	Speed Grade – 9	Speed Grade – 8	Speed Grade – 7	Units
Generic DDRX5 Inputs with Clock and Data Centered – GDDRX5_RX/TX.ECLK.Aligned						
t_{DVA}	Input Data Valid after CLK	MachXO5-NX	0.18 (max)	0.188 (max)	0.225 (max)	ns
t_{DVE}	Input Data Hold after CLK		0.62 (min)	0.646 (min)	0.775 (min)	ns

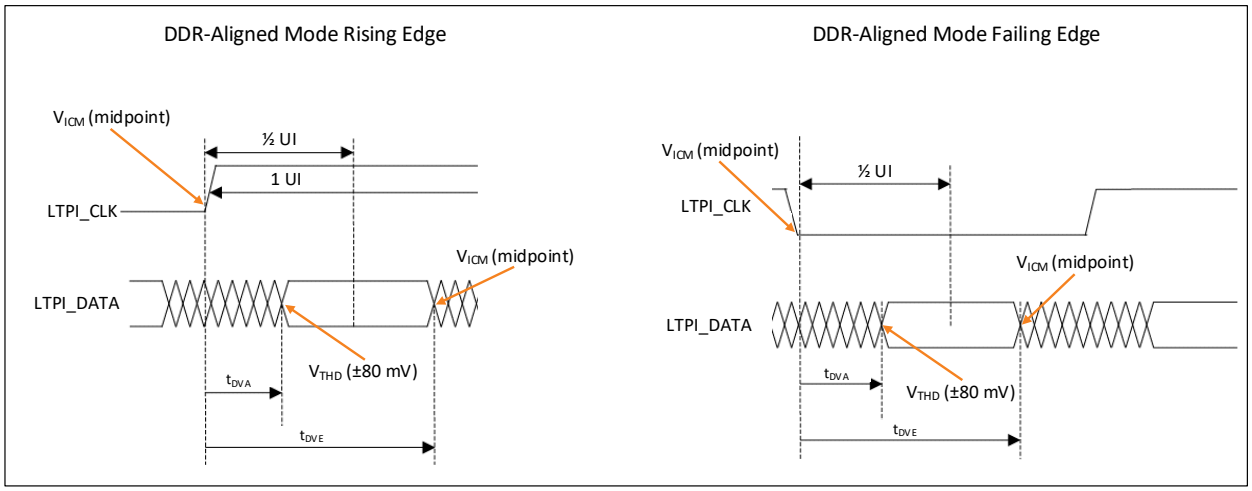

Figure 5.2. Measuring the Input Data Valid after CLK (t_{DVA}) and Input Data Hold after CLK (t_{DVE})

6. Clock Oscillator Supply Filtering

Use a low-ppm (less than 1%) reference clock for LTPI. Ensure the oscillator's power supply is properly isolated and decoupled. A typical bypassing circuit is shown in Figure 6.1.

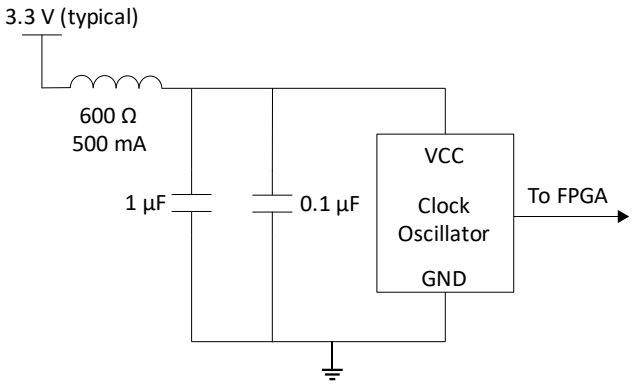

Figure 6.1. Clock Oscillator Bypassing

7. Checklist

Table 7.1. Hardware Checklist

Section	Item	OK	N/A
1	DC Blocking Capacitor		
2	Voltage Bias Circuit		
3	LTPI LVDS Pin Assignment		
2.2	PCB Trace Length difference between LTPI LVDS pair		
2.3	PCB Trace Length difference between CLK to Data for each lane		
2.3.1	Computing and Measuring Input Setup and Hold time in LTPI LVDS port		
2.4	Clock OSC low ppm		

References

- MachXO3 Hardware Checklist (FPGA-TN-02061)
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- MachXO5-NX High-Speed I/O Interface (FPGA-TN-02286)
- LVDS Tunneling Protocol and Interface (LTPI) User Guide (FPGA-RD-02247)
- Open Compute Project web page
- MachXO3 web page
- MachXO3D web page
- MachXO5-NX web page
- Lattice Solutions IP Cores web page
- Lattice Solutions Reference Designs web page
- Lattice Insights web page for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, please refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 1.0, September 2025

Section	Change Summary
All	Initial release.

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