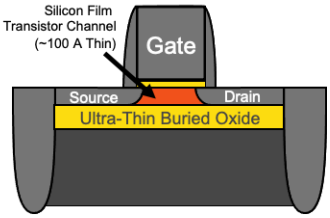
Lattice Nexus FPGA: Harnessing FD-SOI Technology for Radiation Tolerance

The Lattice Nexus FPGA platform leverages 28-nanometer fully depleted silicon-on-insulator (FD-SOI) technology, which inherently offers superior radiation tolerance compared to traditional bulk CMOS processes. This advanced technology reduces the transistor's sensitivity to radiation-induced charges, resulting in a significantly lower soft error rate (SER).

The Superiority of FD-SOI in Radiation Environments

The commercial FD-SOI technology offers a thin insulating layer that effectively isolates the transistor channel from substrate noise and radiation-induced charges. This leads to a more stable and resilient performance in radiation-prone environments, such as space, high-altitude and medical applications.



Demonstrated Radiation Performance

Publicly available data(*) from Lattice Semiconductor highlights the Nexus FPGA's low SER, which is crucial for mission-critical systems. The combination of FD-SOI and robust design methodologies ensures that the FPGA can withstand radiation exposure without compromising performance. The FD-SOI substrate slashes charge collection, giving a >100× lower soft-error rate (SER) than bulk-CMOS alternatives and preventing latch-up altogether.

Single Event Latch-up (SEL) Immunity

The FD-SOI structure of the Nexus FPGA ensures robust immunity to single event latch-up by design. This is because the insulating layer in FD-SOI effectively reduces the likelihood of latch-up events.

Parameter	Description	CertusPro (28nm)	Units
SEL	Heavy Ion Single Event Latch-up Immunity	80	MeV-cm2/mg
SEU CRAM	Single Event Upset in Configuration RAM	2.5E-8	Events/bit/day [1]
TID	Total Ionizing Dose	100	Krad (Si) [2]
Neutron SER	High Energy and Thermal Neutron	3.4	Fit / Mb

1- Worst case 2- Typical

Single Event Effects (SEE) Performance

When exposed to heavy ions, the FD-SOI technology in Nexus reduces the cross-section for single event upsets (SEUs). This means that the onset of SEEs occurs at higher radiation levels compared to bulk CMOS FPGAs with no SEFI (Single-ended Functional interrupt) observed to a LET=60 MeV-cm2/mg.

Total Ionizing Dose (TID) Performance

Backed by independent tests, Nexus FPGAs show strong total ionizing dose performance, maintaining functionality even at higher radiation doses. This is particularly valuable for long-duration space missions.

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Lattice and SpaceR3 SEE presentation to MAPLD
NASA CrossLink-NX TID Summary (page 19)

Built-in Hardened Scrubber, Error emulation and TMR Capabilities

Nexus FPGAs come equipped with a hardened memory scrubber that continuously corrects configuration memory upsets and ECC on all user memory ensuring data integrity during operation. Additionally, the platform supports the implementation of triple modular redundancy (TMR) for applications that demand the highest level of reliability and resilience. Lattice offers utilities to emulate error injection and recovery. Continuous on-chip scrubbing repairs any flipped configuration bit in ≤ 5ms, so a Nexus device statistically needs < one manual intervention per device-year in GEO. This could be through partial or full reprogramming of the configuration bits.

System-level Implications

- **Longer autonomous uptime** – Virtually eliminate in-orbit scrubbing cycles and reset events
- **Simpler designs** – No configuration supervisor or SEL clamps or power sequencing
- **Ample radiation margin** – Reduces shielding, system level redundancy and mitigation
- **SWaP-C** – <100 mW static power & small packages suit satellites, avionics and missiles

Summary

Combining 28 nm fully-depleted SOI technology, a hardened SEU Detect/Correct (SED/SEC) scrubber, a low power architecture and proven TRL9 space heritage through multiples launches in US and EU, Lattice Nexus COTS FPGAs deliver the most balanced, radiation tolerant small FPGA platform on the market.