MachXO5-NX LFMXO5-55TD Soft BSCAN Reference Design User Guide

Reference Design

FPGA-RD-02315-1.0

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Inclusive Language

This document was created consistent with Lattice Semiconductor’s inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice’s inclusive language FAQ 6878 for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

Contents

Figures

Tables

Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviation	Definition
BSCAN	Boundary Scan
ESFB	Embedded Security and Function Block
FSM	Finite State Machine
GUI	Graphical User Interface
HSM	Hardware Security Module
IP	Intellectual Property
JTAG	Joint Test Action Group
OSC	Oscillator
PCB	Printed Circuit Board
PLL	Phase-Locked Loop
RTL	Register Transfer Level
TAP	Test Access Port
TCK	Test Clock
TDI	Test Data Input
TDO	Test Data Output
TMS	Test Mode Select
TRST	Test Reset

1. Introduction

This document is the user guide for the MachXO5™-NX LFMXO5-55TD (MachXO5-NX-55TD or MachXO5-55TD) soft boundary-scan (BSCAN) reference design. To maximize device security, external access to the hardware JTAG port is disabled. The boundary scan test for board testing must be achieved through the soft JTAG boundary-scan IP. Since the automatic V_{CCIO} detection logic is not available after the device enters user functional mode, the actual V_{CCIO} voltage level for each I/O bank must be manually set up according to the customer board design.

1.1. Quick Facts

Download the reference design files from the Lattice reference design web page.

Table 1.1. Summary of the Reference Design

General	Target Devices	LFMXO5-55TD
	Source Code Format	RTL
Simulation	Functional Simulation	Not supported
	Timing Simulation	Not supported
Validation	Hardware	Fully validated
Software Requirements	Software Tool and Version	Lattice Radiant™ software 2024.1 with Synplify Pro Lattice Radiant Programmer 2024.1
	IP Version (if applicable)	Propel ESFB Soft IP version 2.0.0 Propel Soft BSCAN IP version 1.0.0
Hardware Requirements	Board	Lattice Sentry 4.0 demo board for MachXO5-NX (LFMXO5D-4P0-SENTRY-EVN)
	Cable	USB A to micro USB cable Lattice HW-USBN-2B programming cable

1.2. Features

The soft BSCAN reference design provides the test access port (TAP) and boundary-scan architecture based on IEEE 1149.1 (IEEE Standard for Test Access Port and Boundary-Scan Architecture).

1.3. Naming Conventions

1.3.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.3.2. Signal Names

Signal names that end with:

- *_n* are active low (asserted when value is logic 0)
- *_i* are input signals
- *_o* are output signals

2. Directory Structure and Files

Figure 2.1 shows the directory structure.

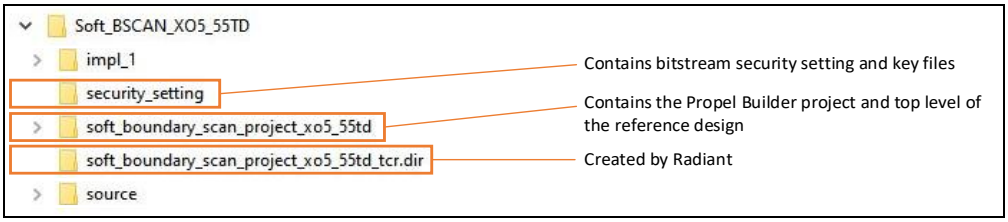

Figure 2.1. Directory Structure

Table 2.1 shows the list of files included in the reference design package.

Table 2.1. File List

Attribute	Description
<Component name>.ipx	This file contains the information on the files associated to the generated IP.
<Component name>.cfg	This file contains the parameter values used in IP configuration.
component.xml	Contains the ipxact:component information of the IP.
design.xml	Documents the configuration parameters of the IP in IP-XACT 2014 format.
rtl/<Component name>.v	This file provides an example RTL top file that instantiates the module.
rtl/<Component name>_bb.v	This file provides the synthesis closed box.
misc/<Component name>_tmpl.v misc /<Component name>_tmpl.vhd	These files provide instance templates for the module.

3. Functional Description

Figure 3.1 shows the top-level block diagram of the MachXO5-NX LFMXO5-55TD device soft BSCAN reference design.

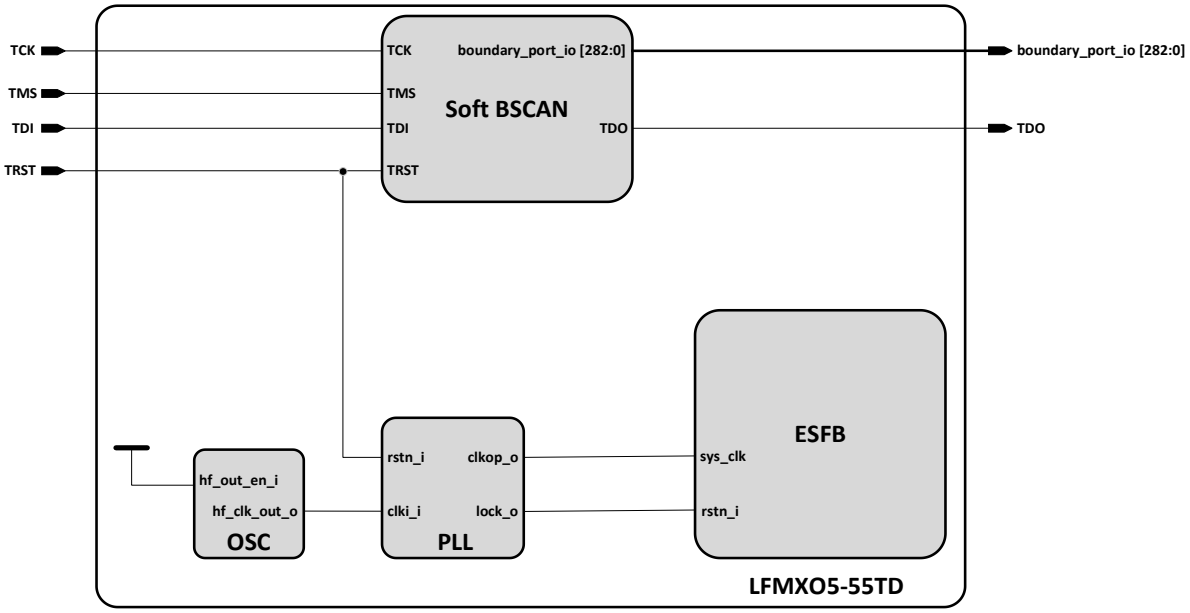

Figure 3.1. Reference Design Block Diagram

3.1. Design Components

The soft BSCAN reference design includes following blocks:

- OSC IP
- PLL IP
- ESFB module
- Soft BSCAN IP

3.1.1. OSC IP

The oscillator (OSC) module provides the clock source for the phase-locked loop (PLL), which in turn provides a stable clock with the desired frequency for the embedded security and function block (ESFB) module. Figure 3.2 shows the configuration of the OSC IP, which is exported from the Propel Builder project and cannot be altered in the Radiant project.

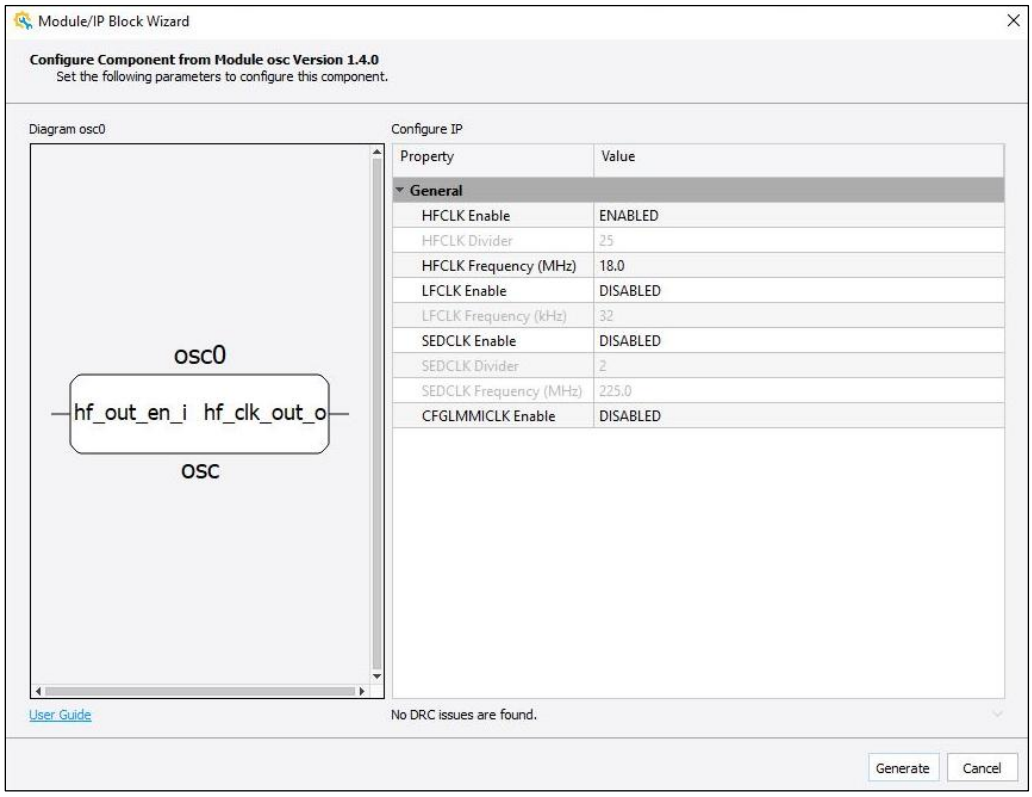

Figure 3.2. OSC IP Configuration

3.1.2. PLL IP

To operate the ESFB module, which is a closed box for this reference design and the key element for proper bitstream signing for a secured LFMXO5-55TD device, the PLL generates the 18-MHz clock for the ESFB module from an 18-MHz input clock produced by the internal oscillator. Figure 3.3 and Figure 3.4 show the general and optional ports configurations of the PLL IP, which are exported from the Propel Builder project and cannot be altered in the Radiant project.

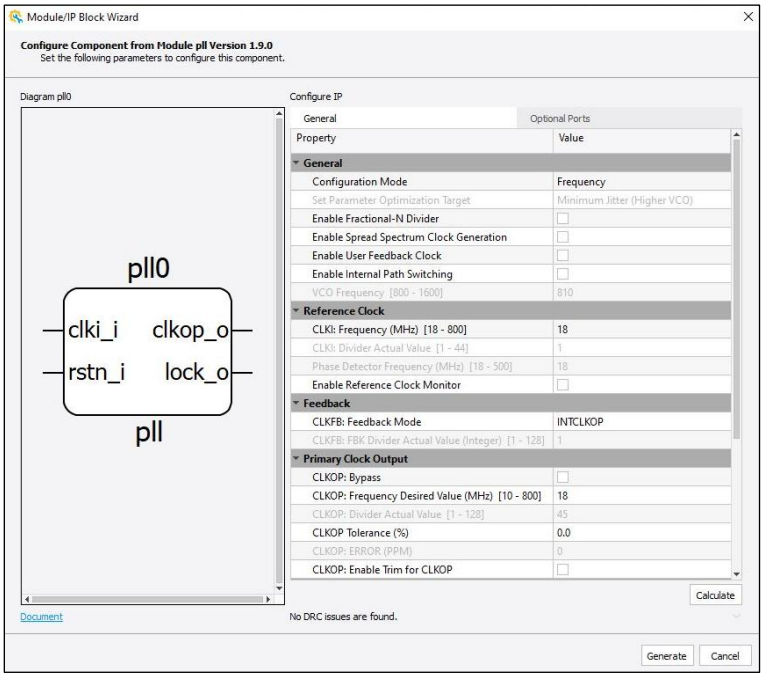

Figure 3.3. PLL General Configuration

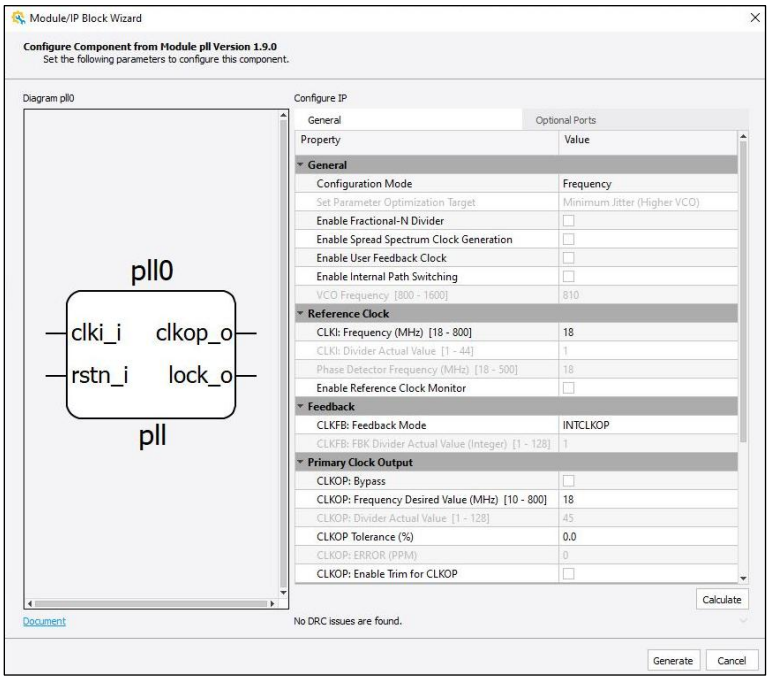

Figure 3.4. PLL Optional Ports Configuration

3.1.3. ESFB Module

The ESFB module is a closed box for this reference design and the key element for proper bitstream signing for a secured LFMXO5-55TD device. This module is exported from the Propel Builder project and cannot be altered in the Radiant project.

3.1.4. Soft BSCAN IP

The soft BSCAN IP, which is fully compliant with IEEE 1149.1, is instantiated for testing and debugging the MachXO5-NX LFMXO5-55TD device. It is used to verify designs and test printed circuit boards (PCBs). This IP is exported from the Propel Builder project and is pre-defined for this reference design targeting the LFMXO5-55TD device. Figure 3.5 shows the pre-defined configuration for this IP, which is exported from the Propel Builder project and cannot be altered in the Radiant project.

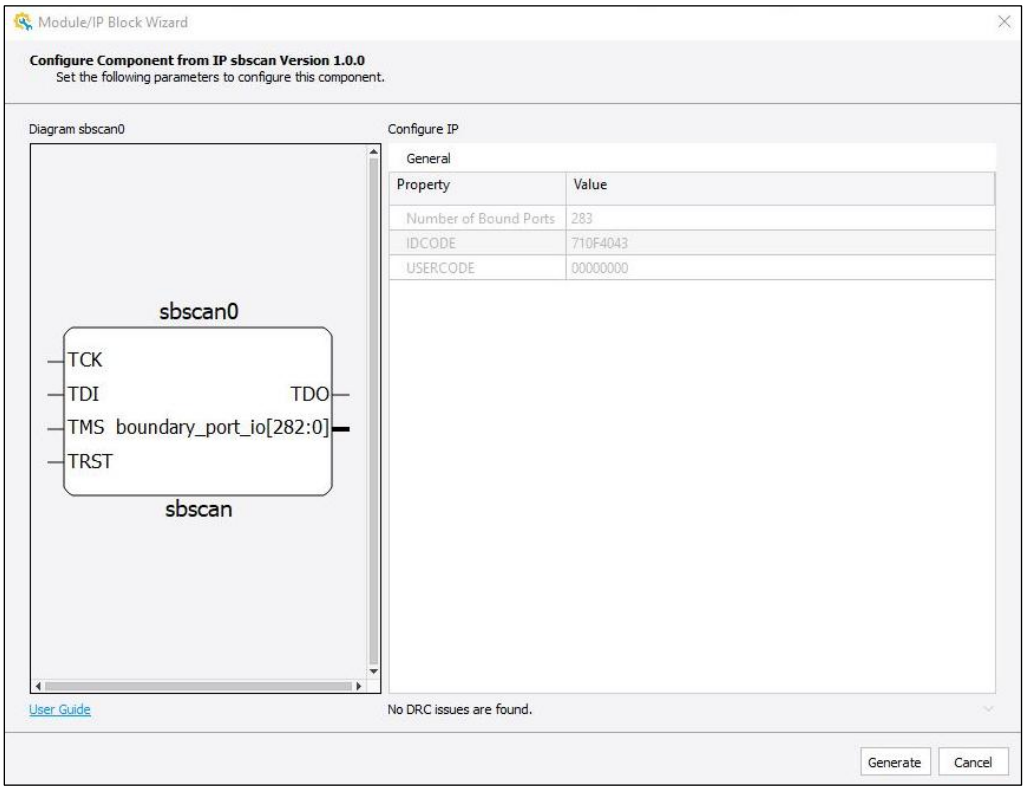

Figure 3.5. Soft BSCAN IP Configuration

For more details about the soft BSCAN IP, refer to the Soft BSCAN IP Architecture section.

3.2. Clocking Scheme

The soft BSCAN IP core runs solely on the test clock (TCK) for the JTAG operation. The ESFB module runs on the 18-MHz clock from the PLL. The PLL input clock comes from the internal oscillator.

3.2.1. Clocking Overview

Figure 3.6 shows an overview of the soft BSCAN reference design clocking scheme.

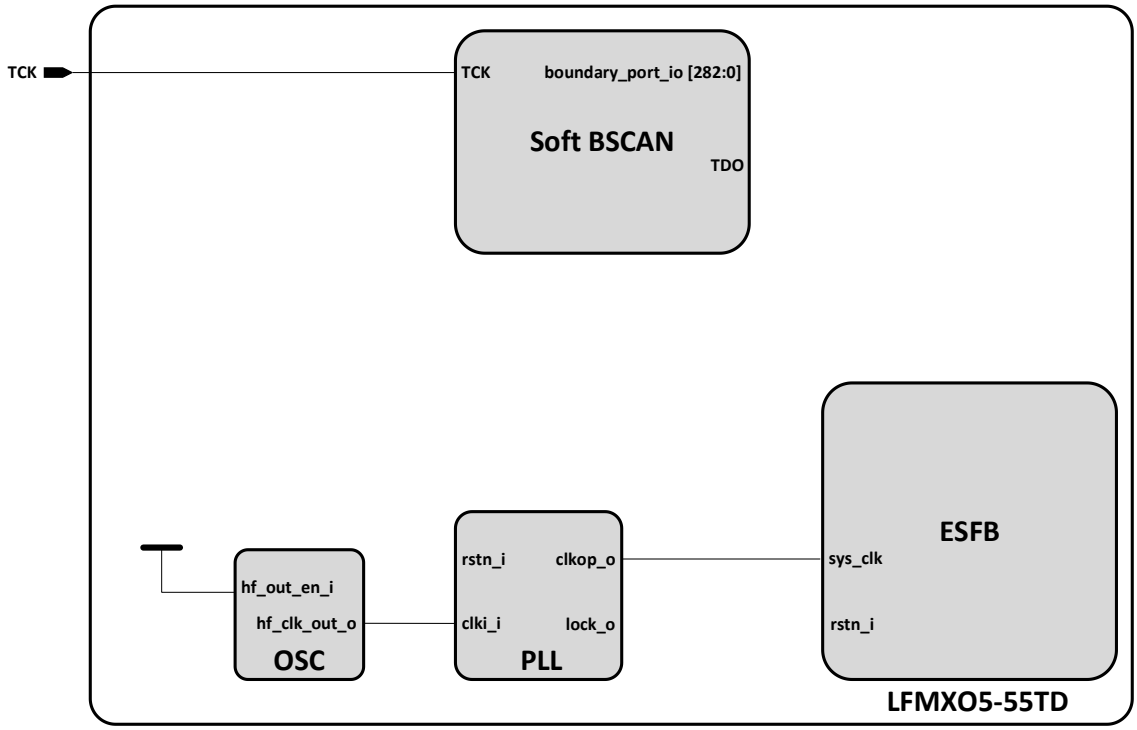

Figure 3.6. Reference Design Clock Domain Block Diagram

3.3. Reset Scheme

A dedicated test reset (TRST) pin is deployed for JTAG logic reset and PLL reset. A synchronized reset is generated for the ESFB module.

3.3.1. Reset Overview

Figure 3.7 shows an overview of the soft BSCAN reference design reset scheme.

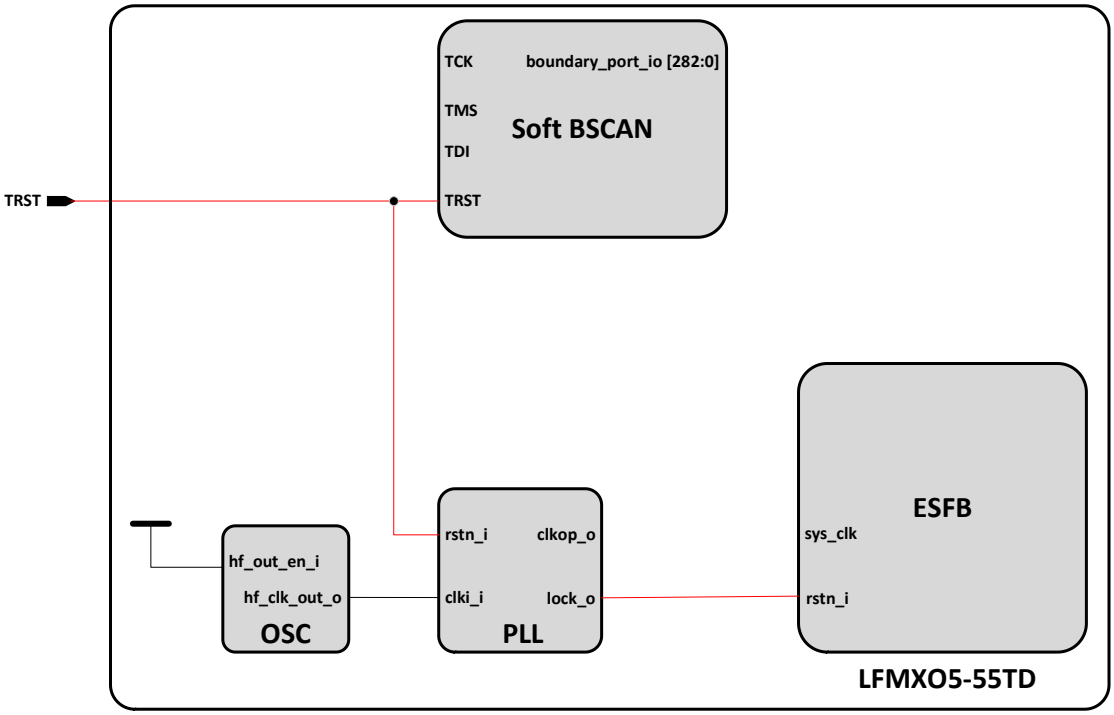

Figure 3.7. Reference Design Reset Scheme Diagram

4. Soft BSCAN IP Architecture

This section provides technical information about the soft BSCAN IP.

4.1. Functional Description

The soft BSCAN IP is fully compliant with IEEE 1149.1. The top-level block diagram of the soft BSCAN IP is shown in Figure 4.1.

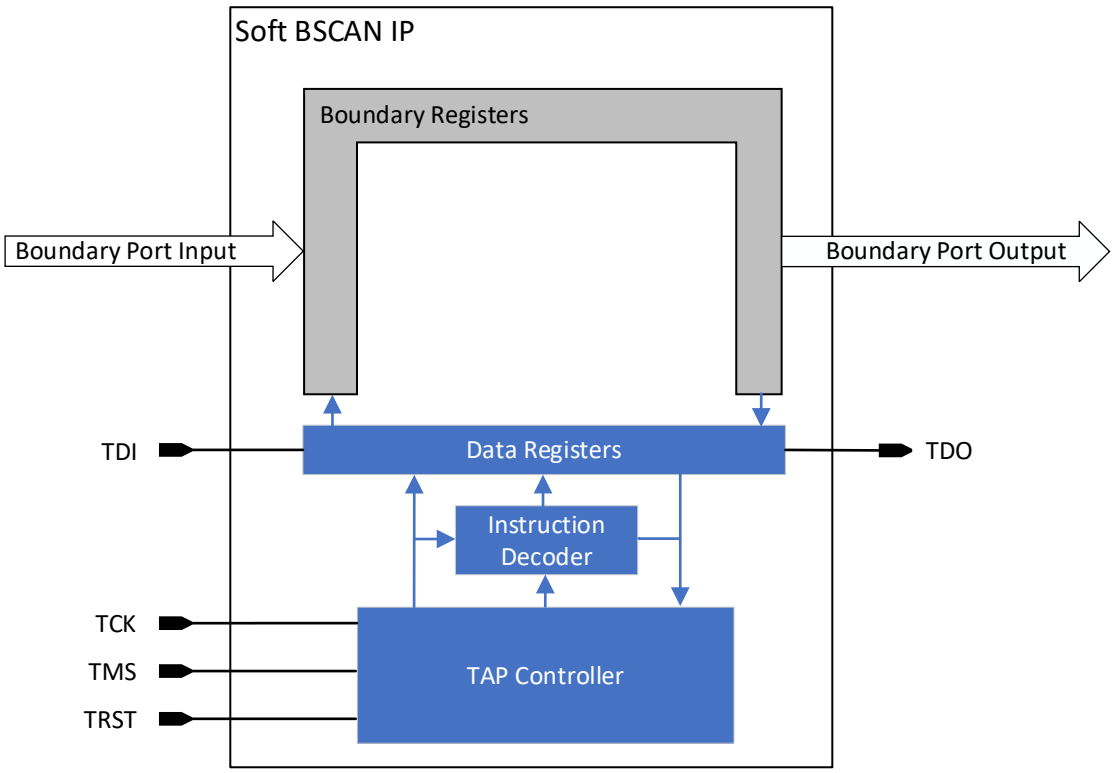

Figure 4.1. Soft BSCAN IP Block Diagram

4.2. TAP Controller

For full compliance with IEEE 1149.1, the standard TAP controller is implemented. The TAP controller contains the state machine of the whole IP. The TAP controller samples the test mode select (TMS) and updates the state machine accordingly. For more information on the TAP controller finite state machine (FSM), refer to the IEEE 1149.1 Standard for Test Access Port and Boundary-Scan Architecture.

4.3. JTAG Instruction Support

The IEEE 1149.1 mandatory and optional instructions supported by the soft BSCAN IP are listed in Table 4.1 and Table 4.2, respectively.

Table 4.1. JTAG Mandatory Instructions

Instruction	Binary Code	Shift Register	Description
BYPASS	8'b11111111	Bypass	The single BYPASS shift-register is used to provide a minimum-length serial path between the TDI and the TDO pins of a component when no operation is required.
SAMPLE	8'b00011100	Boundary-Scan Register	Allows a snapshot of the normal operation of the component to be taken and examined.
PRELOAD	8'b00011100	Boundary-Scan Register	Allows data values to be loaded onto the latched parallel outputs of the boundary-scan shift register before selecting other boundary-scan test instructions.
EXTEST	8'b00010101	Boundary-Scan Register	Allows testing of off-chip circuitry and board-level interconnections. Typically, data is loaded onto the latched parallel outputs of boundary-scan shift-register stages using the *PRELOAD* instruction before selection of the *EXTEST* instruction.

Table 4.2. JTAG Optional Instructions

Instruction	Binary Code	Shift Register	Description
IDCODE	8'b11100000	32-bit ID Code Register	Provides information on the base component, which is the pre-defined 32-bit device identification code.
USERCODE	8'b11000000	32-bit Usercode Register	Provides information on the programming of a programmable component, which is the user-defined 32-bit electronic signature code.
CLAMP	8'b01111000	Bypass	Allows the state of the signals driven from component pins to be determined from the boundary-scan register. The signals driven from the component pins will not change while the *CLAMP* instruction is selected.
HIGHZ	8'b00011000	Bypass	Places the component in a state in which all its system logic outputs are placed in an inactive drive state (high impedance). In this state, an in-circuit test system may drive signals onto the connections normally driven by a component output without incurring the risk of damage to the component.

4.4. Boundary-Scan Register

For every bidirectional pin on the LFMXO5-55TD device, the boundary-scan register cell is deployed to achieve the boundary test functionalities. For more information on the structure of the boundary-scan register for a bidirectional pin, refer to the IEEE 1149.1 Standard for Test Access Port and Boundary-Scan Architecture.

4.5. Soft BSCAN IP Parameters

The soft BSCAN IP has parameters to allow you to specify the number of I/O pins, device ID code (32 bits), and usercode (32 bits). Currently, these parameters are fixed for the LFMXO5-55TD device. Refer the Reference Design Parameter Description section for details.

5. Reference Design Parameter Description

The MachXO5-NX LFMXO5-55TD soft BSCAN reference design includes the parameters shown in Table 5.1, preset for the LFMXO5-55TD device.

Table 5.1. Parameters for the Reference Design

Parameter	Value	Description
Number of Bound Ports	283	Number of boundary scan I/O pins
IDCODE	32'h710F4043	Device ID code
USERCODE	32'h00000000	Usercode

6. Signal Description

The input/output interface signals for the MachXO5-NX LFMXO5-55TD soft BSCAN reference design are shown in Table 6.1.

Table 6.1. Primary I/O

Pin Name	I/O	Width	Description
TCK	Input	1	Test clock input
TMS	Input	1	Test mode select
TDI	Input	1	Test data input
TDO	Output	1	Test data output
TRST	Input	1	Test reset
boundary_port_io	Input/Output	283	Bi-directional I/O pins of the LFMXO5-55TD device

7. Customizing the Reference Design

This section describes how to customize the MachXO5-NX LFMXO5-55TD soft BSCAN reference design using the Lattice Radiant software. For more details on this software tool, refer to the Lattice Radiant Software User Guide.

7.1. Opening a Radiant Project

To create the FPGA bitstream file, open the Lattice Radiant software. Then, click on the **Open Project** icon as shown in Figure 7.1.

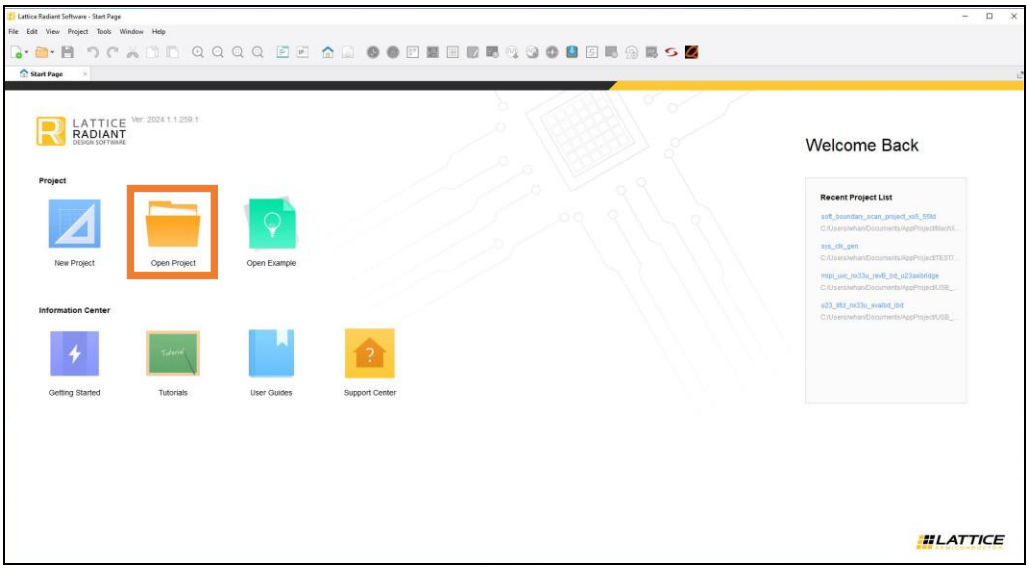

Figure 7.1. Lattice Radiant Software

Open the Radiant project file *soft_boundary_scan_project_xo5_55td.rdf* from the *\MachXO5-55TD_BSCAN\Soft_BSCAN_XO5_55TD* folder as shown in Figure 7.2. The design should have no errors but might have four warnings due to unused signals from an instance. These warnings do not affect the design compilation and bitstream generation.

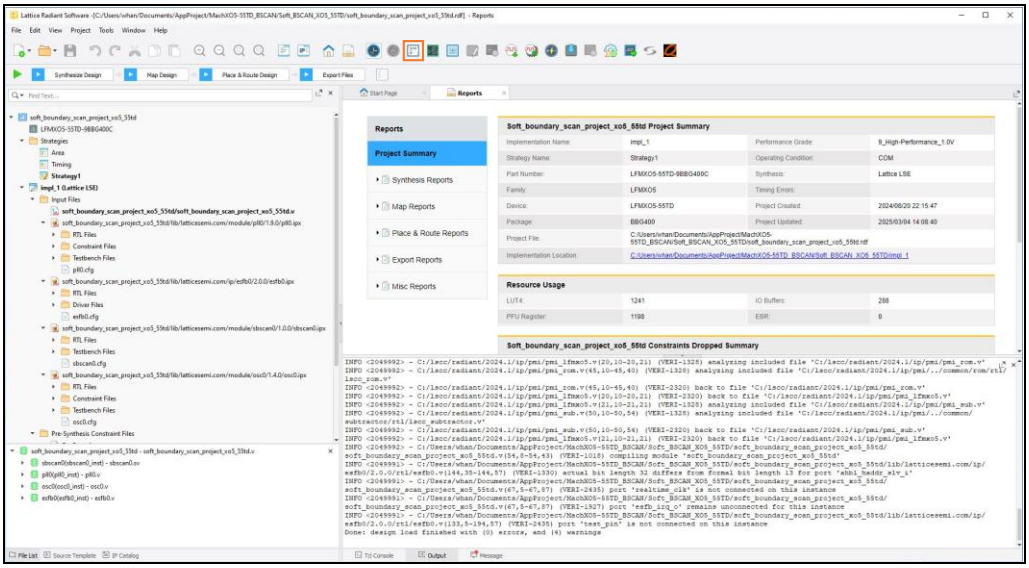

Figure 7.2. Opening a Radiant Project

7.2. Customizing V_{CCIO} Setting

To set up the actual V_{CCIO} voltage level for each I/O bank to match your board design, open the Device Constraint Editor. Then, modify the voltage level for each I/O bank as shown in Figure 7.3.

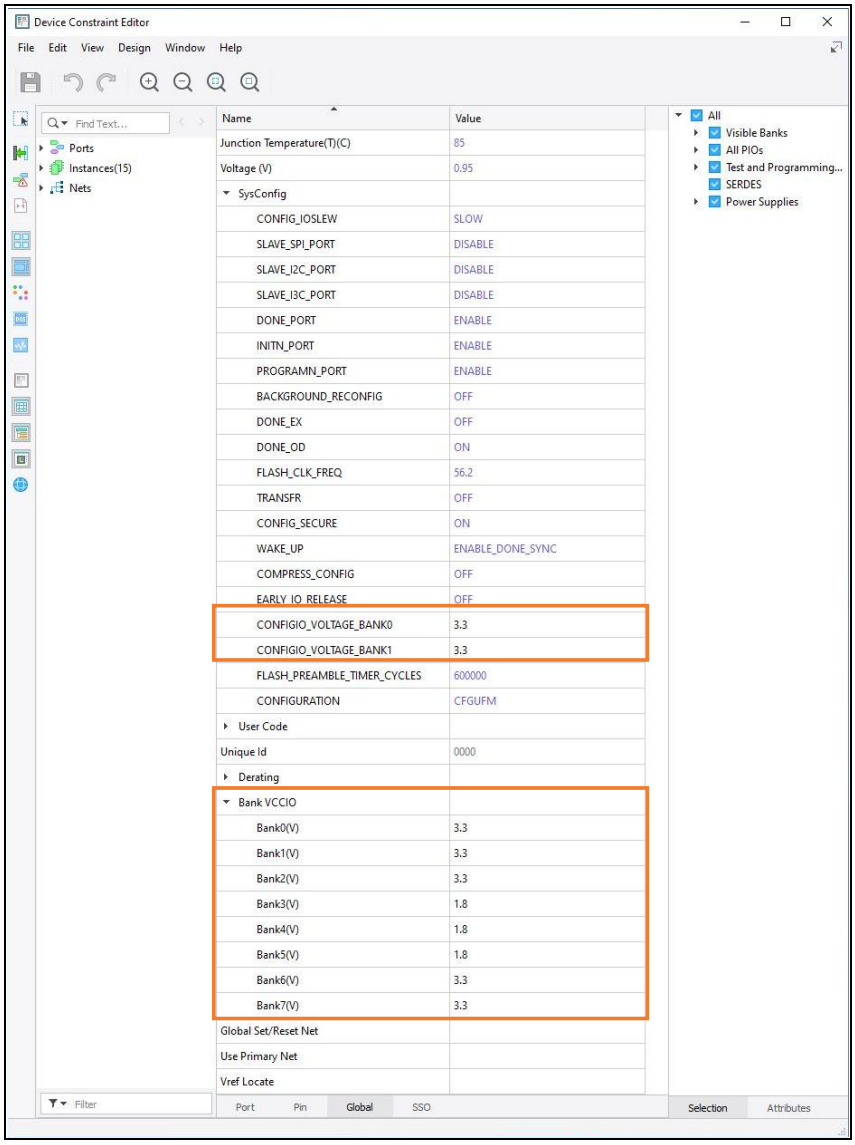

Figure 7.3. Customizing V_{CCIO} Voltage Setting

7.3. Security Setting

For a fully secured device, the LFMXO5-55TD bitstream security setting must be enabled.

7.3.1. Bitstream Security Setting

Open the bitstream security setting GUI from **Tools > Bitstream Security Settings** as shown in Figure 7.4.

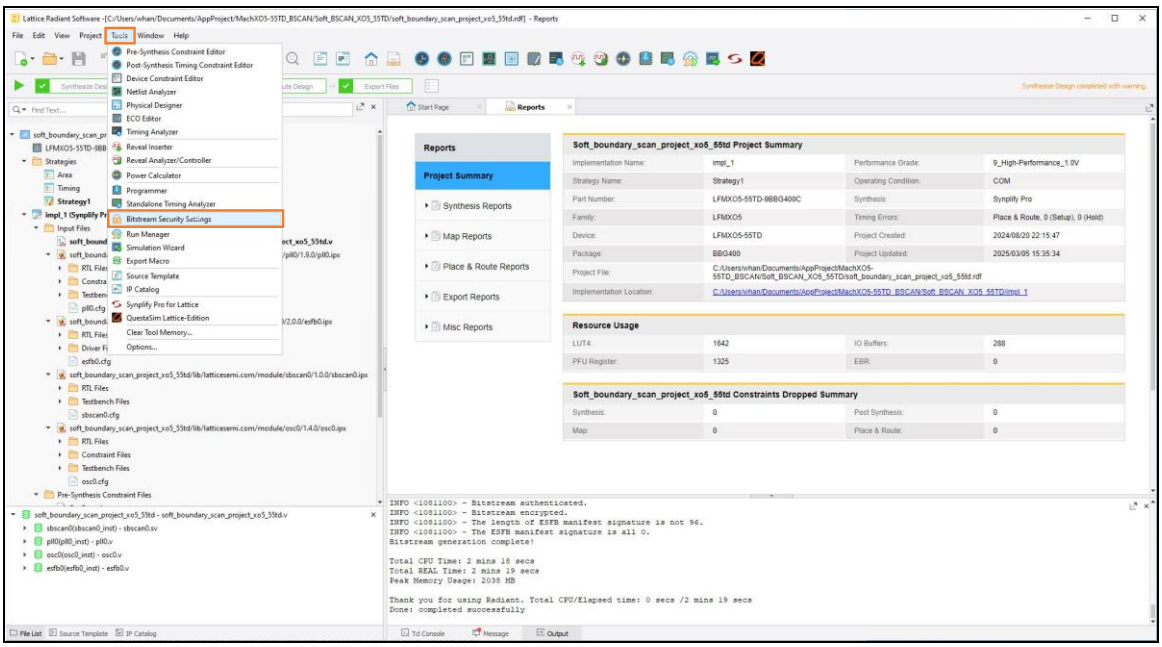

Figure 7.4. Opening Bitstream Security Setting GUI

Provide the password for security setup files, then click **OK** as shown in Figure 7.5.

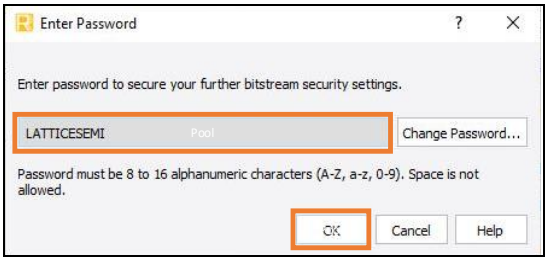

Figure 7.5. Entering Password for Security Setting

In the security setting Dialog window, generate the following key and key pairs (or load the pre-generated key) as shown in Figure 7.6.

- AES2 encryption key
- KAK key pair
- ISK key pair

Then, click **OK** to complete the bitstream security setting.

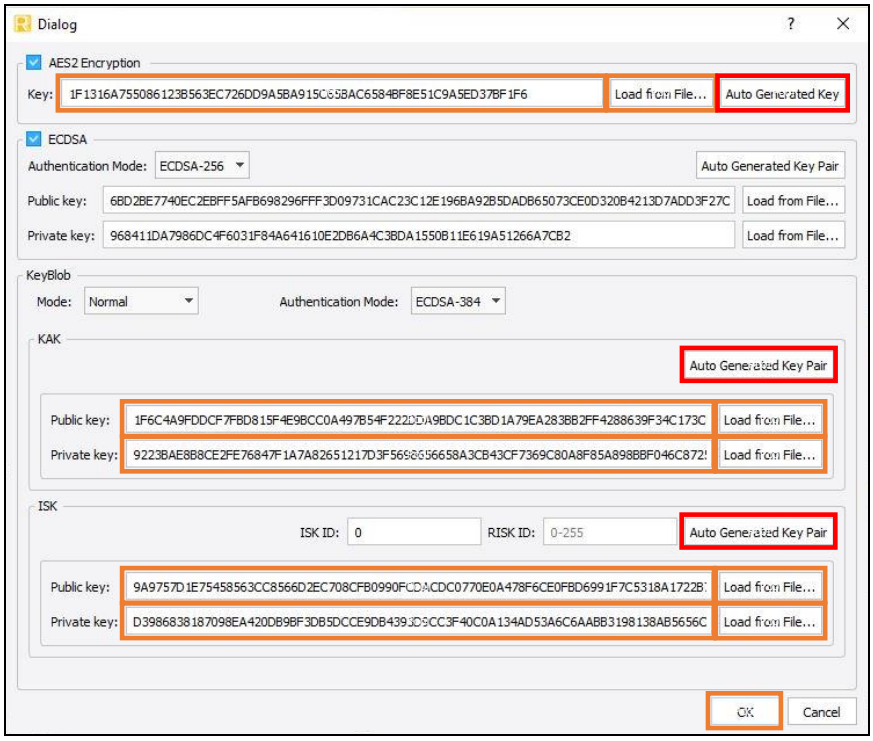

Figure 7.6. Setting Up Keyblob and AES Encryption Key

Besides the bitstream security setting GUI, Lattice provides the HSM script to handle keyblob generation and revocation for advance security. For more information regarding HSM script support, contact Lattice Technical Support.

7.4. Generating the Bitstream File

To generate the FPGA bitstream file, click **Export Files** as shown in Figure 7.7.

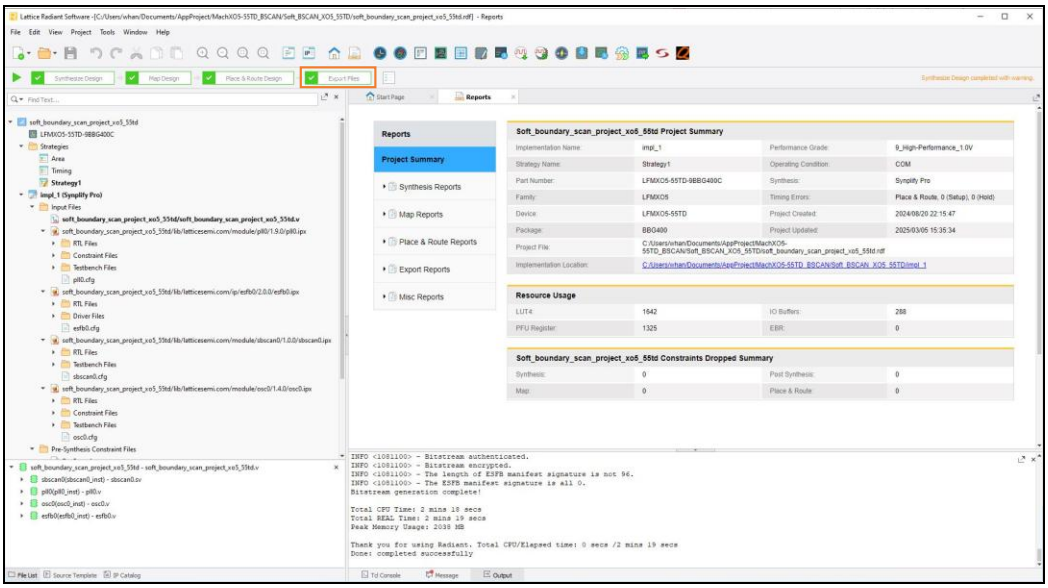

Figure 7.7. Generating Bitstream File

You can view the log message and find the generated bitstream file *soft_boundary_scan_project_xo5_55td_impl_1.bit* in the *\MachXO5-55TD_BSCAN\Soft_BSCAN_XO5_55TD\impl_1* folder.

8. Implementing the Reference Design on Board

Before the JTAG boundary-scan test can be performed on the customer board, the LFMXO5-55TD device must be provisioned with the correct keyblob and programmed with an updated (with correct V_{CCIO} levels) MachXO5-NX LFMXO5-55TD soft BSCAN reference design bitstream.

8.1. Programming Cable Connections

For the LFMXO5-55TD device provisioning and reference design bitstream programming, connect the Lattice HW-USBN-2B programming cable to the JTAG configuration port of the LFMXO5-55TD device. Table 8.1 shows the cable connections.

Table 8.1. HW-USBN-2B Programming Cable Connections

HW-USBN-2B Pin Name	Name	LFMXO5-55TD Pin Name	LFMXO5-55TD Ball	Description
VCC	Programming Voltage	VCCIO1	C18, D17	V_{CCIO} for I/O bank 1
TCK	Test Clock	PL13A	B19	Test clock input to LFMXO5-55TD device
TMS	Test Mode Select	PR6B	B16	Test mode select input
TDI	Test Data Input	PR8B	C16	Test data input
TDO	Test Data Output	PR10B	E16	Test data output
GND	Ground	VSS	—	Ground of customer board

Note: For JTAG programming, connect the JTAG_EN pin of the LFMXO5-55TD device to V_{CCIO1}.

8.2. LFMXO5-55TD Device Provisioning

To successfully load the MachXO5-NX LFMXO5-55TD soft BSCAN reference design to the target device, this reference design must be provisioned as the customer test image with the correct keyblob. Refer to the MachXO5-NX Root-of-Trust Device Provisioning User Guide (FPGA-TN-02333) for information on performing the LFMXO5-55TD device provisioning.

9. Performing the Boundary Scan Test

Before performing the boundary-scan test, connect the JTAG host to the JTAG port of the MachXO5-NX LFMX05-55TD soft BSCAN reference design.

9.1. JTAG Port Connections for Boundary-Scan Test

The JTAG port connections for the soft BSCAN reference design are shown in Table 9.1.

Table 9.1. Reference Design JTAG Port Connections

HW-USBN-2B Pin Name	Name	LFMXO5-55TD Pin Name	LFMXO5-55TD Ball	Description
VCC	Programming Voltage	—	—	V_{CCIO} for I/O bank 7
TCK	Test Clock	PL31A	H3	Test clock input to the soft BSCAN reference design
TMS	Test Mode Select	PL33A	H1	Test mode select input to the soft BSCAN reference design
TDI	Test Data Input	PL29B	H4	Test data input to the soft BSCAN reference design
TDO	Test Data Output	PL31B	H2	Test data output from the soft BSCAN reference design
TRST	Test Reset	PL29A	H5	Test logic reset to the soft BSCAN reference design
GND	Ground	—	—	Ground of customer board

9.2. Running the Boundary-Scan Test

To make the device stay with the customer test image after reboot, set the MODE[2:0] pins (J3, J2, J1) of the LFMXO5-55TD device to 3'b110. To perform the JTAG boundary-scan test, refer to the supported instructions for the soft BSCAN reference design in the JTAG Instruction Support section.

References

- MachXO5-NX Root-of-Trust Device Provisioning User Guide (FPGA-TN-02333)
- MachXO5-NX web page
- IEEE 1149.1 Standard for Test Access Port and Boundary-Scan Architecture
- Lattice Radiant FPGA design software
- Lattice Propel Design Environment web page
- Lattice Solutions IP Cores web page
- Lattice Solutions Reference Designs web page
- Lattice Insights for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, please refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 1.0, April 2025

Section	Change Summary
All	Initial release.

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