MachXO4 sysI/O User Guide

Technical Note

FPGA-TN-02398-1.0

December 2025

Disclaimers

Lattice makes no warranty, representation, or guarantee regarding the accuracy of information contained in this document or the suitability of its products for any particular purpose. All information herein is provided AS IS, with all faults, and all associated risk is the responsibility entirely of the Buyer. The information provided herein is for informational purposes only and may contain technical inaccuracies or omissions, and may be otherwise rendered inaccurate for many reasons, and Lattice assumes no obligation to update or otherwise correct or revise this information. Products sold by Lattice have been subject to limited testing and it is the Buyer's responsibility to independently determine the suitability of any products and to test and verify the same. LATTICE PRODUCTS AND SERVICES ARE NOT DESIGNED, MANUFACTURED, OR TESTED FOR USE IN LIFE OR SAFETY CRITICAL SYSTEMS, HAZARDOUS ENVIRONMENTS, OR ANY OTHER ENVIRONMENTS REQUIRING FAIL-SAFE PERFORMANCE, INCLUDING ANY APPLICATION IN WHICH THE FAILURE OF THE PRODUCT OR SERVICE COULD LEAD TO DEATH, PERSONAL INJURY, SEVERE PROPERTY DAMAGE OR ENVIRONMENTAL HARM (COLLECTIVELY, "HIGH-RISK USES"). FURTHER, BUYER MUST TAKE PRUDENT STEPS TO PROTECT AGAINST PRODUCT AND SERVICE FAILURES, INCLUDING PROVIDING APPROPRIATE REDUNDANCIES, FAIL-SAFE FEATURES, AND/OR SHUT-DOWN MECHANISMS. LATTICE EXPRESSLY DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY OF FITNESS OF THE PRODUCTS OR SERVICES FOR HIGH-RISK USES. The information provided in this document is proprietary to Lattice Semiconductor, and Lattice reserves the right to make any changes to the information in this document or to any products at any time without notice.

Inclusive Language

This document was created consistent with Lattice Semiconductor’s inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice’s inclusive language FAQ 6878 for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

Contents

Figures

Tables

Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviation	Definition
ASCII	American Standard Code for Information Interchange
BLVDS	Bidirectional Low Voltage Differential Signaling
DDR	Double Data Rate
DRC	Design Rule Check
FPGA	Field-Programmable Gate Array
HDL	Hardware Description Language
IBIS	Input/Output Buffer Information Specification
LVCMOS	Low-Voltage Complementary Metal Oxide Semiconductor
LVDS	Low-Voltage Differential Signaling
LVPECL	Low Voltage Positive Emitter Coupled Logic
LVTTL	Low Voltage Transistor-Transistor Logic
MIPI	Mobile Industry Processor Interface
MLVDS	Multipoint Low-Voltage Differential Signaling
PCI	Peripheral Component Interconnect
PIO	Parallel Input/Output
PIC	Programmable Input/Output Cell
VHDL	VHSIC Hardware Description Language
VIH	Voltage Input High
VIL	Voltage Input Low

1. Introduction

The Lattice MachXO4™ family devices feature sysI/O™ buffers tailored to accommodate the diverse range of I/O standards required in modern design environments. These buffers support both single-ended and differential I/O standards, facilitating seamless integration with standard buses, memory devices, video applications, and emerging standards. This technical note outlines the various supported I/O standards and the banking scheme associated with the MachXO4 FPGA family devices. Additionally, it delves into the sysI/O architecture and software usage to enhance comprehension of the I/O functionality and placement guidelines.

2. sysI/O Buffer Overview

The basic building block of the MachXO4 sysI/O is the Programmable I/O Cell (PIC) block. There are three types of PIC blocks in the MachXO4 device architecture. These include the basic PIC block, the receiving PIC block with gearing, and the transmitting PIC block with gearing. The PIC blocks with gearing are used for video and high-speed applications and have a built-in control module for word alignment. The details of the gearing PIC block can be found in Implementing High-Speed Interfaces with MachXO4 Devices (FPGA-TN-02410).

A common feature of all three types of PIC blocks is that each PIC block consists of four programmable I/O (PIOs). Each PIO includes a sysI/O buffer and an I/O logic block. A simplified sysI/O block diagram is shown in Figure 2.1. The I/O logic block consists of an input block, an output block, and a tri-state block. These blocks have registers, input delay cells, and the necessary control logic to support various operational modes. The sysI/O buffer determines the compliance to the supported I/O standards. It also supports features such as hysteresis to meet common design needs. The I/O logic block and the sysI/O buffer are designed with a minimal use of die area, providing easy bus interfacing and pin out efficiency.

Two adjacent PIOs can form a pair of complementary output drivers. In addition, PIOA and PIOB of the PIC block form the primary pair of the buffer, while PIOC and PIOD form the alternate pair of the buffer. The primary pairs have additional capability that is not available on the alternate pair. The sysI/O buffers of the PIC block are equivalent when implemented as the single-ended I/O standards.

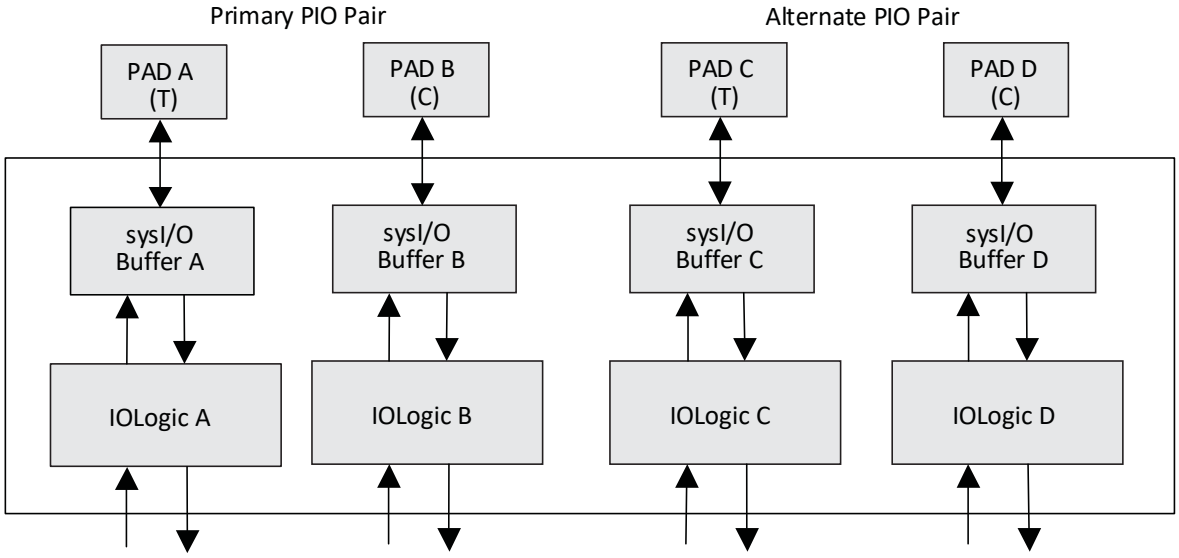


Figure 2.1. PIC Block Diagram

3. Supported sysI/O Standards

The MachXO4 sysI/O buffer supports both single-ended and differential standards. The internally ratioed standards support individually configurable drive strength and bus maintenance circuits, weak pull-up, weak pull-down, or bus keeper.

All banks of the MachXO4 devices support true differential inputs, and emulated differential outputs using external resistors and the complementary LVCMOS outputs. The true-LVDS differential outputs and LVDS input termination are supported in specific banks, as described in the sysI/O Banking Scheme section of this document.

Table 3.1. Supported Input Standards

Input Standard	V_{REF} (Nominal)	V_{CCIO}[1] (Nominal)
Single-Ended Interfaces		
LVTTL33	—	—
LVCMOS33	—	—
LVCMOS25	—	—
LVCMOS18	—	—
LVCMOS15	—	—
LVCMOS12	—	—
Differential Interfaces		
LVDS25	—	—
LVPECL33	—	—
MLVDS25	—	—
BLVDS25	—	—
LVTTL33D	—	—
MIPI[2]	—	—

Notes:
1. If not specified, refer to mixed voltage support in Table 7.1.
2. This interface can be emulated with external resistors.

Table 3.2. Supported Output Standards

Output Standard	Drive (mA)	V_{CCIO} (Nominal)
Single-Ended Interfaces		
LVTTL33	4, 8, 12, 16	3.3
LVCMOS33	4, 8, 12, 16	3.3
LVCMOS25	4, 8, 12	2.5
LVCMOS18	4, 8, 12	1.8
LVCMOS15	4, 8	1.5
LVCMOS12	2, 6	1.2
Differential Interfaces		
LVDS25	3.5	2.5, 3.3
LVDS25E	8	2.5
LVPECL33E	16	3.3
MLVDS25E	16	2.5
BLVDS25E	16	2.5
LVTTL33 Differential	4, 8, 12, 16	3.3
LVCMOS33 Differential	4, 8, 12, 16	3.3
LVCMOS25 Differential	4, 8, 12	2.5
MIPI[1]	2	2.5

Note:
1. This interface can be emulated with external resistors. Refer to MIPI D-PHY Interface IP (FPGA-RD-02040) for information on support for MIPI input and output.

4. sysI/O Banking Scheme

The MachXO4 family has a non-homogeneous I/O banking structure. LFMXO4-010 and LFMXO4-015 devices in non-256 Ball packages have four I/O banks each, with one I/O bank per side. LFMXO4-015 devices in 256 Ball packages, LFMXO4-025, LFMXO4-050, LFMXO4-080, and LFMXO4-110 devices have six I/O banks each, with one I/O bank on each of the top, bottom and right sides, and three banks on the left side.

The MachXO4 devices support true LVDS differential outputs through the primary pairs on the top bank, Bank 0. These devices also support 100 Ω differential input termination on every I/O pair on the bottom I/O bank. Each of the I/O pins on all MachXO4 FPGAs has a clamp feature which can be disabled or enabled. This clamp is similar to the PCI clamp but it is not PCI compliant. The arrangements of the I/O banks are shown in Figure 4.1 and Figure 4.2. When the CLAMP DIODE is ON, careful design considerations must be followed. See Appendix D for more information.

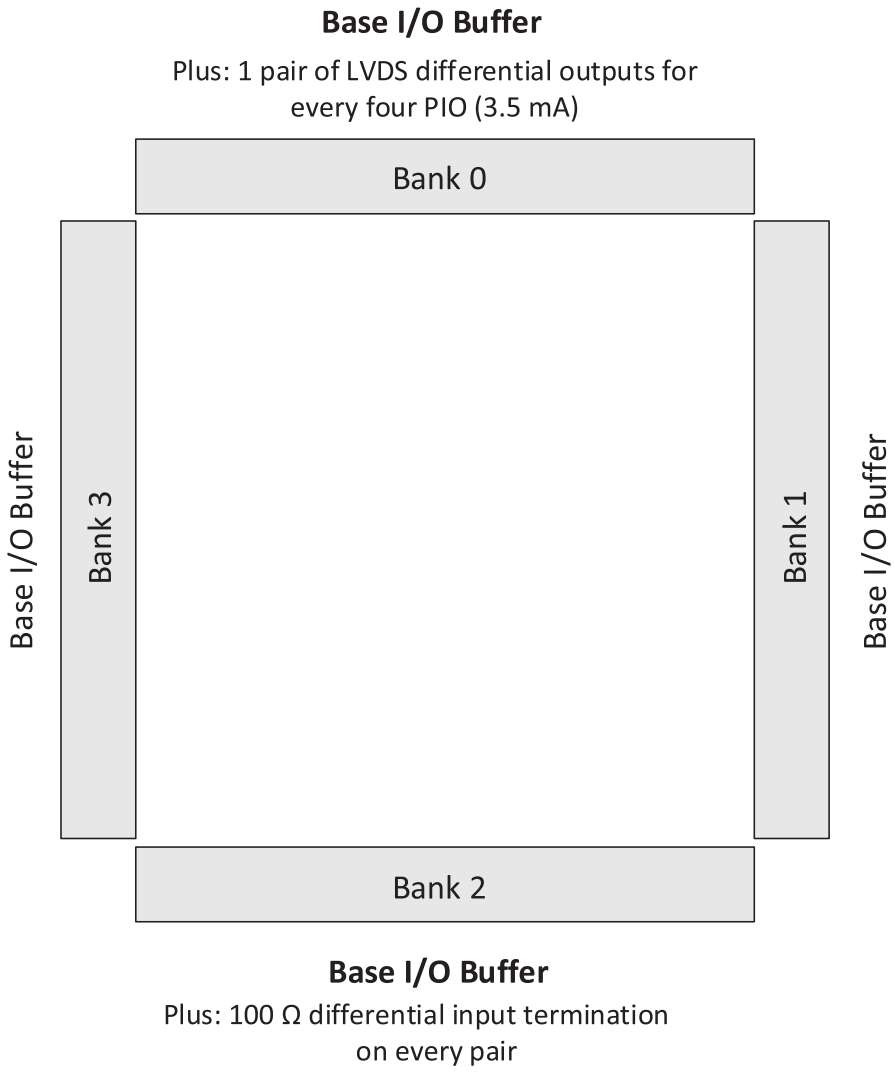


Figure 4.1. LFMXO4-010 and LFMXO4-015 in Non-256 Ball Packages Devices Banking Arrangement

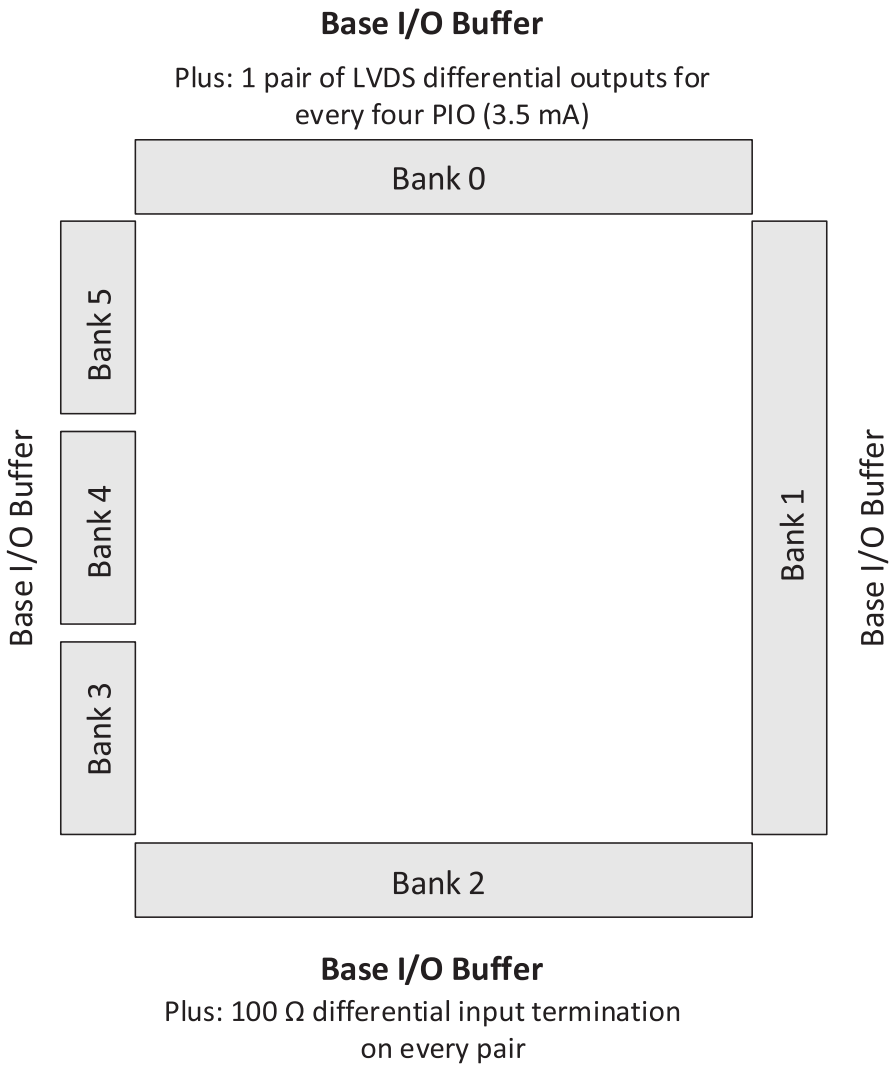


Figure 4.2. LFMXO4-015 in 256 Ball Packages, LFMXO4-025, LFMXO4-050, LFMXO4-080, and LFMXO4-110 I/O Banking Arrangement

5. sysI/O Standards Supported by I/O Banks

All banks can support multiple I/O standards under the VCCIO rules discussed above. Table 5.1 and Table 5.2 summarize the I/O standards supported on various sides of a MachXO4 device.

Table 5.1. Single-Ended I/O Standards Supported on Various Sides

Standard	Top	Bottom	Left	Right
LVTTL33	Yes	Yes	Yes	Yes
LVCMOS33	Yes	Yes	Yes	Yes
LVCMOS25	Yes	Yes	Yes	Yes
LVCMOS18	Yes	Yes	Yes	Yes
LVCMOS15	Yes	Yes	Yes	Yes
LVCMOS12	Yes	Yes	Yes	Yes

Table 5.2. Differential I/O Standards Supported on Various Sides

Standard	Top	Bottom	Left	Right
LVDS output	Yes[1]	—	—	—
LVPECL33E[2]	Yes	Yes	Yes	Yes
MLVDS25E[2]	Yes	Yes	Yes	Yes
BLVDS25E[2]	Yes	Yes	Yes	Yes
LVDS25E[2]	Yes	Yes	Yes	Yes
LVTTL33D output	Yes	Yes	Yes	Yes
LVCMOS33D output	Yes	Yes	Yes	Yes
LVCMOS25D output	Yes	Yes	Yes	Yes
LVDS input	Yes	Yes	Yes	Yes
LVPECL33 input	Yes	Yes	Yes	Yes
MLVDS25 input	Yes	Yes	Yes	Yes
BLVDS25 input	Yes	Yes	Yes	Yes
LVTTL33D input	Yes	Yes	Yes	Yes
LVCMOS33D input	Yes	Yes	Yes	Yes
LVCMOS25D input	Yes	Yes	Yes	Yes
MIPI	Yes	Yes	Yes	Yes

Notes:

1. True LVDS output is supported at the top bank.
2. Emulated output standards are denoted with a trailing *E* in the name of the standard.

6. Power Supply Requirements

The MachXO4 device family has a simplified power supply scheme for sysI/O buffers. The core power V_{CC} and the bank power V_{CCIO} are the two main power supplies. A MachXO4 device can be powered and operated with a single power supply by connecting V_{CC} and V_{CCIO} to nominal voltages of 1.2 V. The JTAG programming pins are powered by V_{CCIO} in Bank 0 where the JTAG pins reside. All the user sysI/O have a weak pull-down after power-up is complete and before the device configuration is done.

7. V_{CCIO} Requirement for I/O Standards

Each I/O bank of a MachXO4 device has a separate V_{CCIO} supply pin that can be connected to 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V. This voltage is used to power the output I/O standard and source the drive strength for the output. In addition to this, V_{CCIO} also powers the ratioed input buffers such as LVTTL and LVCMOS. This ensures that the threshold of the input buffers is tracking the V_{CCIO} voltage level.

Input buffer set up to be a 1.2 V ratioed input can be used on a bank set to any V_{CCIO}. This is possible because the MachXO4 sysI/O buffer has two ratioed input buffers connected to V_{CCIO} and V_{CC} in parallel.

Table 7.1. Mixed Voltage Support for LVCMOS and LVTTL I/O Types[8]

V_{CCIO}	Inputs						Outputs					
	1.0 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	1.0 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V
1.2 V	—	Yes	Yes[6]	—	—	—	—	Yes	—	—	—	—
1.5 V	—	Yes[1]	Yes	Yes[6]	Yes[6]	Yes[6]	—	—	Yes	—	—	—
1.8 V	—	Yes[1]	Yes[5]	Yes	Yes[6]	Yes[6]	—	—	—	Yes	—	—
2.5 V	Yes[1, 9]	Yes[1, 10]	Yes[2, 5, 7]	Yes[3, 5, 7]	Yes	Yes[6]	Yes[11]	Yes[11]	—	—	Yes	—
3.3 V	Yes[1, 9]	Yes[1, 10]	Yes[2, 5, 7]	Yes[3, 5, 7]	Yes[4, 5, 7]	Yes	Yes[11]	Yes[11]	—	—	—	Yes

Notes:

1. Leakage occurs if bus hold or weak pull-up is turned on.
2. This input standard can be supported using the ratioed input buffer in under-drive conditions or using the I/O types LVCMOS15R25 or LVCMOS15R33 with the referenced input buffer.
3. This input standard can be supported using the ratioed input buffer in under-drive conditions or using the I/O type LVCMOS18R25 or LVCMOS18R33 with the referenced input buffer.
4. This input standard can be supported using the ratioed input buffer in under-drive conditions or using the I/O type LVCMOS25R33 with the referenced input buffer.
5. Under-drive condition when using the ratioed input buffer and the input standard voltage is below V_{CCIO}.
   a. Under-drive causes higher DC current when the I/O is at logic high. It is recommended to use Power Calculator to estimate the power consumption under such condition.
   b. Hysteresis is not supported. In the Lattice Radiant™ software, HYSTERESIS must be set to N/A.
   c. CLAMP is not supported. In the Lattice Radiant software, CLAMP must be set to OFF.
   d. I/O termination is not supported. In the Lattice Radiant software, PULLMODE must be set to NONE.
6. Over-drive condition when using the ratioed input buffer and the input standard voltage is above V_{CCIO}.
   a. Hysteresis is not supported. In the Lattice Radiant software, HYSTERESIS must be set to N/A.
   b. CLAMP is not supported. In the Lattice Radiant software, CLAMP must be set to OFF.
   c. I/O termination is not supported. In the Lattice Radiant software, PULLMODE must be set to NONE.
7. Ratioed input buffer in under-drive conditions is preferred over referenced input buffer due to lower power requirement for the ratioed input buffer.
8. When using the ratioed input buffers in under-drive or over-drive conditions, the HYSTERESIS setting is N/A, the CLAMP setting is OFF, and the UP and KEEPER PULLMODE settings are not supported.
9. This input standard can be supported using the I/O types LVCMOS10R25 or LVCMOS10R33 with the referenced input buffer. However, LVCMOS10R25 and LVCMOS10R33 I/O types are available only for –6 speed grade.
10. This input standard can be supported using the ratioed input buffer in under-drive conditions or using the I/O types LVCMOS12R25 or LVCMOS12R33 with the referenced input buffer.
11. This output standard is supported as a Bidirectional open-drain buffer only. I/O termination is not supported. In the Lattice Radiant software, OPENDRAIN must be set to ON, PULLMODE must be set to NONE, and CLAMP must be set to OFF.

For differential input standards, certain mixed voltage support is allowed in the architecture, as shown in Table 7.2.

Table 7.2. Mixed Voltage Support for Differential Input Standards

V_{CCIO}	Differential Inputs		
	LVDS LVPECL33 MLVDS25 BLVDS25	**LVTTL33D LVCMOS33D**	**LVCMOS25D**
1.2 V	—	—	—
1.5 V	—	—	—
1.8 V	—	—	—
2.5 V	Yes	—	Yes
3.3 V	Yes	Yes	Yes

8. Input Reference Voltage

To support mixed voltage I/O using the referenced input buffer, each I/O bank supports one reference voltage, VREF. Any I/O in the bank can be configured as the input reference voltage pin. This pin is a regular I/O if it is not used as reference voltage input.

9. sysI/O Buffer Configuration

Each sysI/O buffer pair is made of two PIO buffers. PIO A and B pads form the primary pair, and PIO C and D pads form the alternate pair. Pads A and C of the pair are considered the true pad, while pads B and D are considered the comp pad. The true pad is associated with the positive side of the differential signal, while the comp pad is associated with the negative side of the differential signal.

All the PIOs support bus maintenance circuitry to allow a weak pull-up, or a weak pull-down, or a weak bus keeper. The LVDS sysI/O buffer pairs have additional LVDS output drivers in the primary PIO and are available on the top side of the device. The bottom sysI/O buffer pairs have additional 100 Ω termination resistors between the true and comp pads.

9.1. LVCMOS Buffer Configurations

The LVCMOS buffers can be configured in a variety of modes to support common circuit design needs.

9.1.1. Bus Maintenance Circuit

Each pad has a weak pull-up, weak pull-down, and weak bus keeper capability. These are selected with ON and OFF programmability. The pull-up and pull-down settings offer a fixed characteristic, which is useful in creating wired logic such as wired ORs. The bus keeper option latches the signal in the last driven state, holding it at a valid level with minimal power dissipation. Input leakage can be minimized by turning off the bus maintenance circuitry. However, it is important to ensure that inputs are driven to a known state to avoid unnecessary power dissipation in the input buffer. The bus maintenance circuit is available for single-ended ratioed I/O standards.

9.1.2. Programmable Drive Strength

All single-ended drivers have programmable drive strength. This option can be set for each I/O independently. The drive strengths available for each I/O standard can be found in Table 10.2. The MachXO4 programmable drive architecture is guaranteed with minimum drive strength for each drive setting. The V/I curves in the data sheet provide details of output driving capability versus the output load. This information, together with the current per bank and the package thermal limit current, should be taken into consideration when selecting the drive strength.

9.1.3. Input Hysteresis

Voltage Input High (VIH) is the trip point for a low-to-high transition and Voltage Input Low (VIL) is the trip point for a high-to-low transition, hysteresis voltage is the difference between VIH and VIL. Hysteresis is used to prevent several quick successive changes, for example, when the input signal contains some noise. The noise could mean that you cross the trip point more than just once, which causes a glitch in the system.

All ratioed input receivers, except LVCMOS12, support input hysteresis. The input hysteresis for the LVCMOS33, LVCMOS25, LVCMOS18 and LVCMOS15 have two settings for flexibility. The ratioed input receivers have no input hysteresis when they are operated in under-drive or over-drive input conditions, as shown in Table 10.1.

9.1.4. Programmable Slew Rate

The single-ended output buffer for each device I/O pin has programmable output slew rate control that can be configured for either low noise performance, SLEWRATE=SLOW, or high speed performance, SLEWRATE=FAST. Each I/O pin has an individual slew rate control. This slew rate control affects both the rising and the falling edges. The rise and fall ramp rates for each I/O standard can be found in the in the device Input/Output Buffer Information Specification (IBIS) file for a given I/O configuration.

9.1.5. Tri-state and Open Drain Control

Each single-ended output driver has a separate tri-state control in addition to the global tri-state control for the device. The single-ended output drivers also support open drain operation on each I/O independently. The open drain output is typically pulled up externally and only the sink current specification is maintained.

9.2. Differential Buffer Configurations

The sysI/O buffer pair supports differential input standards. The top and bottom edges support some additional functions over those supported by the base sysI/O buffer pairs.

9.2.1. Differential Receivers

All the sysI/O buffer pairs support differential input on all edges of the device. When a sysI/O buffer pair is configured as differential receiver, the input hysteresis and the bus maintenance capabilities are disabled for the buffer.

9.2.2. On-Chip Input Termination

The MachXO4 device supports on-chip 100 Ω nominal input differential termination on the bottom edge. The termination is available on all input PIO pairs of the bottom edge and is programmable.

9.2.3. Emulated Differential Outputs

All sysI/O buffer pairs support complementary outputs as described above. This feature can be used to drive complementary LVCMOS signals. It can also be used together with off-chip resistor networks for emulating the differential output standards such as LVPECL, MLVDS, MIPI, and BLVDS differential standards. When a sysI/O buffer pair is configured as differential transmitter, the bus maintenance and open drain capabilities are disabled. All single-ended sysI/O buffers pairs in the MachXO4 family can support emulated differential output standards.

9.3. True Differential Output and Output Drive

MachXO4 devices support true differential output drivers on the top edge of these devices. These true differential outputs are only available on the primary PIO pairs. The output driver has a fixed common mode of 1.2 V and a programmable drive current of 3.5 mA. The bank VCCIO for true differential output can be 2.5 V or 3.3 V.

10. Software sysI/O Attributes

The sysI/O attributes or primitives must be used in the Lattice development software to control the functions and capabilities of the sysI/O buffers. sysI/O attributes or primitives can be specified in the HDL source code, in the Lattice Radiant Device Constraint Editor interface, or in the ASCII preference .pdc file directly. Appendix A and Appendix B list examples of using such attributes in different environments. This section describes each of these attributes in detail.

10.1.HDL Attributes

All the attributes discussed in this section, except two, can be used in the HDL source code to direct the sysI/O buffer functionality.

10.1.1. IO_TYPE

This attribute is used to set the sysI/O standard for an I/O. The VCCIO required to set these I/O standards are embedded in the attribute names. The BANK VCCIO attribute is used to specify the allowed VCCIO combinations for each I/O type. Table 10.1 shows the valid I/O types for the MachXO4 family devices.

Table 10.1. Supported I/O Types

sysI/O Signaling Standard	IO_TYPE
LVDS 2.5 V	LVDS25
Emulated LVDS 2.5 V[1]	LVDS25E
Bus LVDS 2.5 V	BLVDS25
Emulated Bus LVDS 2.5 V[1]	BLVDS25E
MLVDS 2.5 V	MLVDS25
Emulated MLVDS 2.5 V[1]	MLVDS25E
LVPECL 3.3 V	LVPECL33
Emulated LVPECL 3.3 V[1]	LVPECL33E
LVTTL 3.3 V	LVTTL33
LVTTL 3.3 V differential[2]	LVTTL33D
LVCMOS 3.3 V	LVCMOS33
LVCMOS 3.3 V differential[2]	LVCMOS33D
LVCMOS 2.5 V (default)	LVCMOS25
LVCMOS 2.5 V differential[2]	LVCMOS25D
LVCMOS 2.5 V in 3.3 V VCCIO bank[3]	LVCMOS25R33
LVCMOS 1.8 V	LVCMOS18
LVCMOS 1.8 V in 3.3 V VCCIO bank[3]	LVCMOS18R33
LVCMOS 1.8 V in 2.5 V VCCIO bank[3]	LVCMOS18R25
LVCMOS 1.5 V	LVCMOS15
LVCMOS 1.5 V in 3.3 V VCCIO bank[3]	LVCMOS15R33
LVTTL 3.3 V	LVTTL33
LVCMOS 1.5 V in 2.5 V VCCIO bank[3]	LVCMOS15R25
LVCMOS 1.2 V	LVCMOS12
LVCMOS 1.2 V in 3.3 V VCCIO bank[4]	LVCMOS12R33
LVCMOS 1.2 V in 2.5 V VCCIO bank[4]	LVCMOS12R25
LVCMOS 1.0 V in 3.3 V VCCIO bank[4]	LVCMOS10R33
LVCMOS 1.0 V in 2.5 V VCCIO bank[4]	LVCMOS10R25
MIPI	MIPI

Notes:

1. These differential output standards are emulated by using a complementary LVCMOS driver pair together with an external resistor pack.
2. These differential standards are implemented by using a complementary LVCMOS driver pair.
3. These are input only and require VREF to be set to certain value to allow the specified I/O types to be used.
4. These are input or bidirectional only and require VREF to be set to certain value to allow the specified I/O types to be used.

10.1.2. DRIVE

The DRIVE strength attribute is available for the output and bidirectional I/O standards. The default drive value depends on the I/O standard used. Table 10.2 shows the supported drive strength for the single-ended I/O types under designated I/O standards.

Table 10.2. Output Drive Capability for Ratioed sysI/O Standards

Drive Strength (mA)	I/O Type					
	LVCMOS12	LVCMOS15	LVCMOS18	LVCMOS25	LVCMOS33	LVTTL33
2	Yes	—	—	—	—	—
4	—	Yes	Yes	Yes	Yes	Yes
6	Yes	—	—	—	—	—
8	—	Yes	Yes	Yes	Yes	Yes
12	—	—	Yes	Yes	Yes	Yes
16	—	—	—	—	Yes	Yes

10.1.3. DIFFDRIVE

The DIFFDRIVE strength attribute is available for the true LVDS output standard. All true LVDS differential drivers on the top edge is set to 3.5 mA setting. This is not programmable on the MachXO4 devices.

Values: 3.5

Default: 3.5

10.1.4. PULLMODE

The PULLMODE option can be enabled or disabled independently for each I/O. When you select OPENDRAIN=ON, the PULLMODE for the output standard is default to NONE.

Values: UP, DOWN, NONE, KEEPER

Default: DOWN for LVTTL and LVCMOS, all others are NONE.

10.1.5. CLAMP

The CLAMP option can be enabled or disabled independently for each I/O. The settings are available on the bottom edge. All other I/O have ON or OFF settings for this attribute.

Values: OFF, ON

Default value of the CLAMP for output: OFF

Default value of the CLAMP for input: ON if V_{CCIO} is the same or higher than the I/O standard.

Default value of the CLAMP for input: OFF if V_{CCIO} is lower than the I/O standard.

When the CLAMP diode is ON, careful design considerations must be followed. See Appendix D for more information.

10.1.6. HYSTERESIS

The ratioed input buffers have two input hysteresis settings. The HYSTERESIS option can be used to change the amount of hysteresis for the LVTTL and LVCMOS input and bidirectional I/O standards, except for the LVCMOS12 inputs. The LVCMOS12 inputs do not support HYSTERESIS.

The LVCMOS25R33, LVCMOS18R25, LVCMOS18R33, LVCMOS15R25, LVCMOS15R33, LVCMOS12R33, LVCMOS12R25, LVCMOS10R33, and LVCMOS10R25 input types do not support HYSTERESIS. The HYSTERESIS option for each of the input pins can be set independently when it is supported for the I/O type.

Values: SMALL, LARGE, N/A

Default: SMALL

10.1.7. VREF

The VREF option is enabled for referenced LVCMOS input buffers. The referenced LVCMOS input buffers are specified by choosing the I/O type as LVCMOS25R33, LVCMOS18R25, LVCMOS18R33, LVCMOS15R25, LVCMOS15R33, LVCMOS12R33, LVCMOS12R25, LVCMOS10R33, or LVCMOS10R25. The default value of N/A applies for all I/O types that do not use a VREF signal.

The VREF defaults to external VREF pin for the single-ended LVCMOS25R33, LVCMOS18R25, LVCMOS18R33, LVCMOS15R25, LVCMOS15R33, LVCMOS12R33, LVCMOS12R25, LVCMOS10R33, or LVCMOS10R25 inputs. You may enter a VREF_NAME value in the VREF Location(s) pop-up window of the Device Constraint Editor of the Lattice Radiant software. In doing so, the software presents the VREF_NAME as an available value in the VREF column of the Port tab of the Lattice Radiant Device Constraint Editor. A pin location specified by the VREF_NAME value is used as the VREF driver for that I/O bank. VREF_NAME is only necessary if you want to specify a pin to be used as an external VREF pin. Otherwise, the software automatically assigns a pin for the VREF signal.

There is only one VREF pin needed per I/O bank and only one VREF driver can be used in each I/O bank. This attribute can be set in the software interface or in the ASCII preference file.

Values: OFF, VREF_NAME, N/A

Software Default: N/A

Hardware Default (Erased): OFF

10.1.8. OPENDRAIN

The OPENDRAIN option is available for all LVTTL and LVCMOS output and bidirectional I/O standards. Each sysI/O can be assigned independently to be open drain. When the OPENDRAIN attribute is used, the PULLMODE must be NONE and the CLAMP must be OFF.

Values: OFF, ON

Default: OFF

10.1.9. SLEWRATE

Each I/O pin has an individual slew rate control. This allows you to specify slew rate control on a pin-by-pin basis for outputs and bidirectional I/O pins. This is not a valid attribute for inputs or true differential outputs.

Values: FAST, SLOW, N/A

Default: FAST

10.1.10. DIFFRESISTOR

The bottom side I/O pins support on-chip differential input termination resistors. The termination resistor is available for both the primary pair and the alternate pair of a sysI/O. The values supported are OFF or 100 Ω.

Values: OFF, 100

Default: OFF

10.1.11. DIN/DOUT

The DIN/DOUT option is available for each I/O and can be configured independently. An input register is used for the input if the DIN attribute is assigned. Similarly, the software assigns an output register when the DOUT attribute is specified. By default, the software automatically assigns DIN or DOUT to input or output registers if possible.

10.1.12. LOC

This attribute specifies the site location for the component after the mapping process. When attached to multiple components, it indicates that these blocks are to be mapped together in the specified site. It specifies the PIC site for the pad when it is assigned to a pad. The LOC attribute can be attached to components that ends up on an I/O cell, clocks, and internal flip-flops. However, it should not be attached to combinational logic that ends up on a logic cell, as doing so can cause failure in generating a locate preference. The LOC attribute overrides register ordering.

10.1.13. Bank VCCIO

This attribute is necessary to verify the valid I/O types for a bank, to determine which input buffer to use, and to set the correct drive strength for the applicable I/O types. Since the I/O bank information is not required at the HDL level, this attribute is available through either the Lattice Radiant software's Device Constraint Editor or in the ASCII preference file.

Values: AUTO, 3.3, 2.5, 1.8, 1.5, 1.2

Default: AUTO

10.2.sysI/O Primitives

There are many sysI/O primitives in the software library. A few are selected to be discussed in this section because some sysI/O capabilities can only be utilized through instantiating the primitives in the HDL source code.

10.2.1. Tri-State All (TSALL)

The MachXO4 device supports the TSALL function that is used to enable or disable the tri-state control to all the output buffers. You can choose to assign any general purpose I/O pin to control the TSALL function since there is no dedicated TSALL pin. The TSALL primitive must be instantiated in the source code in order to enable the TSALL function. The input of the primitive can be assigned to an input pin or to an internal signal.

A value of TSALL=1 tri-states all outputs but the outputs are under individual OE control when TSALL=0.

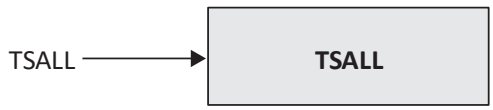


Figure 10.1. TSALL Primitive

10.2.2. Fixed Data Delay (DELAYE)

This primitive supports up to 32 steps of static delay for all sysI/O buffers in all banks of a MachXO4 device. Although you can choose the USER_DEFINED mode to set input delay, this primitive is primarily used by pre-defined source synchronous interfaces as described in Implementing High-Speed Interfaces with MachXO4 Devices (FPGA-TN-02410).

Figure 10.2. DELAYE Primitive and Associated Attributes

Table 10.3. Output Drive Capability for Ratioed sysI/O Standards

Attribute	Description	Value	Software Default
DEL_MODE	Fixed delay value depending on interface or user-defined delay values	SCLK_ZEROHOLD ECLK_ALIGNED ECLK_CENTERED SCLK_ALIGNED SCLK_CENTERED USER_DEFINED	USER_DEFINED
DEL_VALUE	User-defined value	DELAY0…DELAY31	DELAY0

10.2.3. Dynamic Data Delay (DELAYD)

This primitive supports dynamic delay for the sysI/O buffers in the bottom bank, that is, Bank 2 of the MachXO4 device only. The 5-bit inputs can be controlled by the user logic to modify the delay during the device operation.

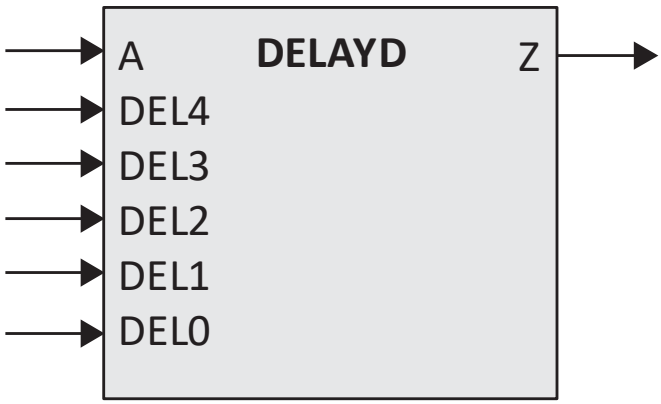


Figure 10.3. DELAYD Primitive

11. Design Consideration and Usage

This section summarizes the MachXO4 designs rules and considerations that have been discussed in detail in previous sections. Table 11.1 lists the miscellaneous I/O features on each side of a MachXO4 device.

11.1.sysI/O Buffer Features Common to All MachXO4 Devices

- All banks support true differential inputs.
- All banks support emulated differential outputs using external resistors and complementary LVCMOS outputs. Emulated differential output buffers are supported on both primary and alternate pairs.
- All banks have programmable I/O clamps.
- All banks support weak pull-up, pull-down, and bus keeper settings on each I/O independently.
- V_{CCIO} voltage levels, together with the selected I/O types, determine the characteristics of an I/O, such as the pull mode, hysteresis, clamp behavior, and drive strength, supported in a bank. Each bank can support 1.2 V inputs regardless of the V_{CCIO} setting of the bank.
- Each bank supports one V_{CCIO} signal.

11.2.sysI/O Buffer Rules

- Only the top side Bank 0 supports true differential output buffers with programmable drive strengths. Only the primary pair supports true differential output buffers.
- Only the bottom side Bank 2 supports internal 100 Ω differential input terminations.

Table 11.1. Miscellaneous I/O Features on Each Device Edge

Feature	Top	Bottom	Left	Right
100 Ω Differential Resister	—	Yes	—	—
Hot Socket	Yes	Yes	Yes	Yes
Clamp[2]	Yes	Yes	Yes	Yes
Weak Pull-Up[2]	Yes	Yes	Yes	Yes
Weak Pull-Down[1]	Yes	Yes	Yes	Yes
Bus Keeper[2]	Yes	Yes	Yes	Yes
Input Hysteresis[2]	Yes	Yes	Yes	Yes
Slew Rate Control	Yes	Yes	Yes	Yes
Open Drain	Yes	Yes	Yes	Yes
Dynamic Pull-Up Control	—	—	Yes, Bank 3 only	—

Notes:

1. Software default setting.
2. I/O characteristic under special conditions:
   a. The HYSTERESIS option is not available for LVCMOS12.
   b. The HYSTERESIS option and BUS KEEPER option are not available for referenced input standards.
   c. When using the ratioed input buffers in under-drive or over-drive conditions, the HYSTERESIS setting is N/A, the CLAMP setting is OFF, and the UP and KEEPER PULLMODE settings are not supported.
   d. HYSTERESIS and the bus maintenance capabilities are disabled for differential receivers.

Appendix A. sysI/O HDL Attributes

The sysI/O attributes can be used directly in the HDL source codes. This section provides a list of sysI/O attributes supported by the MachXO4 family devices. The correct syntax and examples for the Synplify® synthesis tool are provided here for reference.

A.1. Attributes in VHDL Language

This section lists syntax and examples for the sysI/O attributes in VHDL.

Syntax

Table A.1. VHDL Attribute Syntax

Attribute	Syntax
IO_TYPE	attribute IO_TYPE: string; attribute IO_TYPE of *Pinname*: signal is *"IO_TYPE Value";*
DRIVE	attribute DRIVE: string; attribute DRIVE of *Pinname:* signal is *"Drive Value";*
DIFFDRIVE	attribute DIFFDRIVE: string; attribute DIFFDRIVE of *Pinname:* signal is *"Diffdrive Value";*
DIFFRESISTOR	attribute DIFFRESISTOR: string; attribute DIFFRESISTOR of *Pinname:* signal is *"Diffresistor Value";*
CLAMP	attribute CLAMP: string; attribute CLAMP of *Pinname:* signal is *"Clamp Value";*
HYSTERESIS	attribute HYSTERESIS: string; attribute HYSTERESIS of *Pinname:* signal is *"Hysteresis Value";*
VREF	N/A
PULLMODE	attribute PULLMODE: string; attribute PULLMODE of *Pinname:* signal is *"Pullmode Value";*
OPENDRAIN	attribute OPENDRAIN: string; attribute OPENDRAIN of *Pinname:* signal is *"OpenDrain Value";*
SLOWSLEW	attribute SLOWSLEW: string; attribute SLOWSLEW of *Pinname:* signal is *"Slewrate Value";*
DIN	attribute DIN: string; attribute DIN of *Pinname*: signal is " ";*
DOUT	attribute DOUT: string; attribute DOUT of *Pinname:* signal is " ";*
LOC	attribute LOC: string; attribute LOC of *Pinname:* signal is "pin_locations";
BANK VCCIO	N/A

Examples:

IO_TYPE

```
--***Attribute Declaration*** ATTRIBUTE IO_TYPE: string;
--***IO_TYPE assignment for I/O Pin***
ATTRIBUTE IO_TYPE OF portB: SIGNAL IS "LVCMOS33";
ATTRIBUTE IO_TYPE OF portD: SIGNAL IS "LVDS25";
```

DRIVE

```
--***Attribute Declaration***
ATTRIBUTE DRIVE: string;
--***DRIVE assignment for I/O Pin***
ATTRIBUTE DRIVE OF portB: SIGNAL IS “8”;
```

DIFFDRIVE

```
--***Attribute Declaration***
ATTRIBUTE DIFFDRIVE: string;
--*** DIFFDRIVE assignment for I/O Pin***
ATTRIBUTE DIFFDRIVE OF portD: SIGNAL IS “2.0”;
```

DIFFRESISTOR

```
--***Attribute Declaration***
ATTRIBUTE DIFFRESISTOR: string;
--*** DIFFRESISTOR assignment for I/O Pin***
ATTRIBUTE DIFFRESISTOR OF portD: SIGNAL IS "100";
```

CLAMP

```
--***Attribute Declaration***
ATTRIBUTE CLAMP: string;
--*** CLAMP assignment for I/O Pin***
ATTRIBUTE CLAMP OF portA: SIGNAL IS “PCI33”;
```

HYSTERESIS

```
--***Attribute Declaration***
ATTRIBUTE HYSTERESIS: string;
--*** HYSTERESIS assignment for Input Pin***
ATTRIBUTE HYSTERESIS OF portA: SIGNAL IS " LARGE ";
```

PULLMODE

```
--***Attribute Declaration***
ATTRIBUTE PULLMODE : string;
--***PULLMODE assignment for I/O Pin***
ATTRIBUTE PULLMODE OF portA: SIGNAL IS “DOWN”;
ATTRIBUTE PULLMODE OF portB: SIGNAL IS “UP”;
```

OPENDRAIN

```
--***Attribute Declaration***
ATTRIBUTE OPENDRAIN: string;
--***Open Drain assignment for I/O Pin***
ATTRIBUTE OPENDRAIN OF portB: SIGNAL IS “ON”;
```

SLEWRATE

```
--***Attribute Declaration***
ATTRIBUTE SLEWRATE : string;
--*** SLEWRATE assignment for I/O Pin***
ATTRIBUTE SLEWRATE OF portB: SIGNAL IS “FAST”;
```

DIN/DOUT

```
--***Attribute Declaration***
ATTRIBUTE din : string; ATTRIBUTE dout : string;
--*** din/dout assignment for I/O Pin***
ATTRIBUTE din OF input_vector: SIGNAL IS “TRUE “;
ATTRIBUTE dout OF output_vector: SIGNAL IS “TRUE “;
```

LOC

```
--***Attribute Declaration***
ATTRIBUTE LOC : string;
--*** LOC assignment for I/O Pin***
ATTRIBUTE LOC OF input_vector: SIGNAL IS “E3,B3,C3 “;
```

A.2. Attributes in Verilog Language

This section lists syntax and examples for the sysI/O Attributes in Verilog.

Syntax

Table A.2. Verilog Attribute Syntax

Attribute	Syntax
IO_TYPE	PinType PinName /* synthesis IO_Type=”IO_Type Value”*/;
DRIVE	PinType PinName /* synthesis DRIVE=”Drive Value”*/;
DIFFDRIVE	PinType PinName /* synthesis DIFFDRIVE =” DIFFDRIVE Value”*/;
DIFFRESISTOR	PinType PinName /* synthesis DIFFRESISTOR =” DIFFRESISTOR Value”*/;
CLAMP	PinType PinName /* synthesis CLAMP =” Clamp Value”*/;
HYSTERESIS	PinType PinName /*synthesis HYSTERESIS = “Hysteresis Value” */;
VREF	N/A
PULLMODE	PinType PinName /* synthesis PULLMODE=”Pullmode Value”*/;
OPENDRAIN	PinType PinName /* synthesis OPENDRAIN =”OpenDrain Value”*/;
SLOWSLEW	PinType PinName /* synthesis SLEWRATE=”Slewrate Value”*/;
DIN	PinType PinName /* synthesis DIN= “value” */;
DOUT	PinType PinName /* synthesis DOUT= “value” */;
LOC	PinType PinName /* synthesis LOC=”pin_locations “*/;
Bank VCCIO	N/A

Examples:

//IO_TYPE, PULLMODE, SLEWRATE and DRIVE assignment

```
output portB /*synthesis IO_TYPE=”LVCMOS33”
PULLMODE =”UP” SLEWRATE =”FAST” DRIVE =”20”*/;
output portC /*synthesis IO_TYPE=”LVDS25” */;
```

//DIFFDRIVE

```
output portD /* synthesis IO_TYPE="LVDS25" DIFFDRIVE="2.0"*/;
```

//DIFFRESISTOR

```
output [4:0] portA /* synthesis IO_TYPE="LVDS25" DIFFRESISTOR ="100"*/;
```

//CLAMP

```
output portA /*synthesis IO_TYPE=”LVCMOS33” CLAMP =”ON” */;
```

//HYSTERESIS

```
input mypin /* synthesis HYSTERESIS = “LARGE” */;
```

//OPENDRAIN

```
output portA /*synthesis OPENDRAIN =”ON”*/;
```

// DIN Place the flip-flops near the load input

```
input load /* synthesis din=”” TRUE */;
```

// DOUT Place the flip-flops near the outload output

```
output outload /* synthesis dout=”TRUE” */;
```

//LOC pin location

```
input [2:0] DATA0 /* synthesis loc=”E3,B1,F3”*/;
```

//LOC Register pin location

```
reg data_in_ch1_buf_reg3 /* synthesis loc=”R10C16” */;
```

//LOC Vectored internal bus

```
reg [3:0] data_in_ch1_reg /*synthesis loc =”R10C16,R10C15,R10C14,R10C9” */;
```

Appendix B. sysI/O Attributes Using the Lattice Radiant Device Constraint Editor

The sysI/O buffer attributes can be assigned using the Device Constraint Editor available in the Lattice Radiant software. The attributes that are not available as HDL attributes, such as Bank VCCIO, are available in the Device Constraint Editor.

The Port tab lists all the ports in a design and all the available sysI/O attributes in multiple columns. Click on each of these cells for a list of all the valid I/O preferences for that port. Each column takes precedence over the next. Therefore, when you choose a particular IO_TYPE, the columns for the DRIVE, PULLMODE, SLEWRATE, and other attributes list the valid combinations for that IO_TYPE.

Pin locations can be locked using the Pin column of the Port tab or by using the Pin tab. You can right-click on a cell and go to **Assign Pins** to see a list of all the available pin locations.

In Device Constraint Editor, go to **Design** > **Constraint DRC** to run a design rule check (DRC) to check for incorrect sysI/O attribute assignments.

All the preferences assigned using the Device Constraint Editor are written into the .pdc post synthesis constraint file.

Figure B.1 shows the Port tab of the Device Constraint Editor.

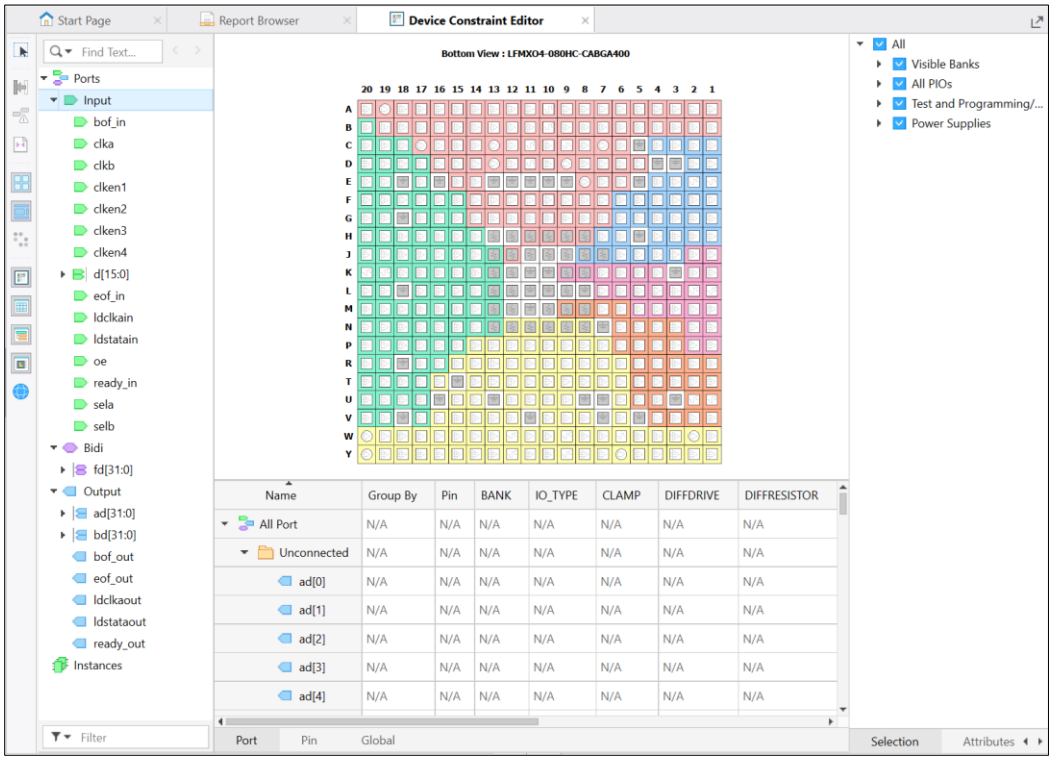


Figure B.1. Port Tab of Device Constraint Editor

B.1. Bank VCCIO Setting in Lattice Radiant Device Constraint Editor

Bank VCCIO is editable in the Global tab of the Device Constraint Editor. You can choose the value of the Bank V_{CCIO} to determine the value of the VCCIO of a specific bank (Figure B.2).

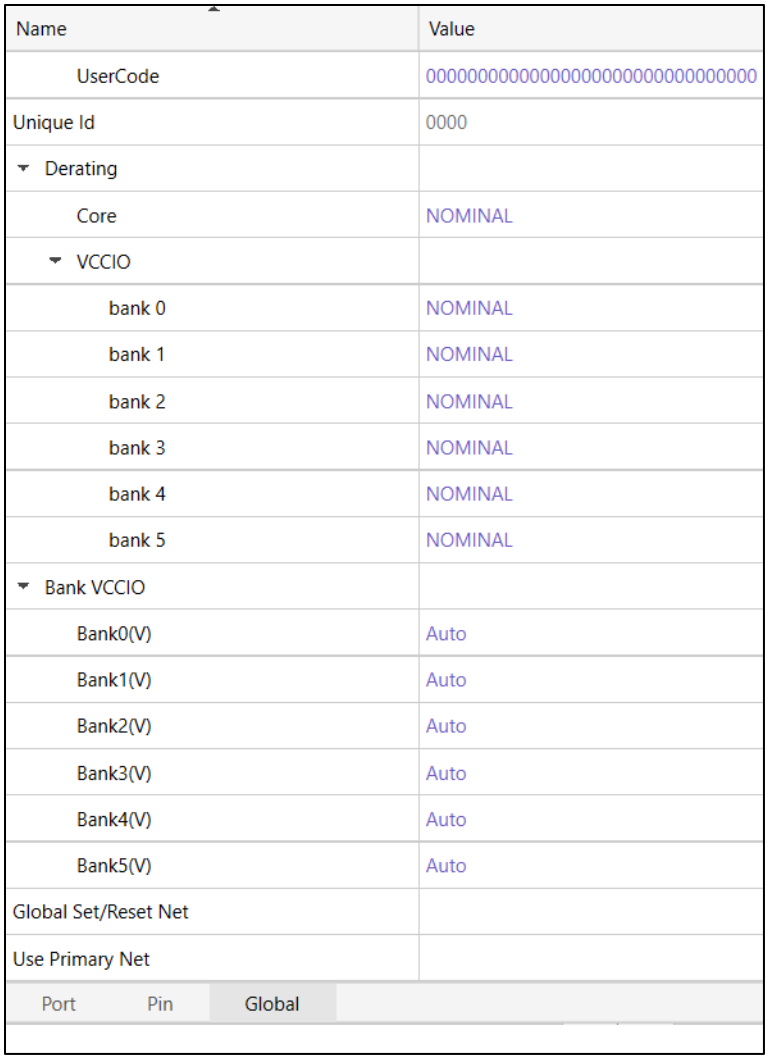


Figure B.2. Bank VCCIO in Global Tab

Appendix C. Issue: GPIO Input Prevents Powering Down the FPGA

For MachXO4 devices that involve the same voltages for V_{CC} and bank V_{CCIOx} , either 3.3 V or 2.5 V, and they are connected together, careful design consideration must be followed. This is to avoid the FPGA not fully powering down and operating in an undefined state.

Note: Chip failures can occur when the input current limits of the datasheet are exceeded.

C.1. GPIO Input Current Leakage Pathway

The FPGA is powered on, with the bitstream program input CLAMPs ON.
While the FPGA powers down, the external circuit continues to drive input pins.
As the FPGA V_{CC} and V_{CCIOx} voltage drop, the GPIO input pins allow external devices to drive reverse current into the FPGA through the on CLAMPs. This current appears at the V_{CCIOx} pins that are connected to V_{CC} and keeps the V_{CC} voltage high enough for the input CLAMPs to remain active.

Other devices besides the FPGA, can be connected to the V_{CC} rail, with each device drawing current from the FPGA. As a result, the FPGA can pass enough reverse current to cause internal burnouts or failures to occur quickly or gradually, depending on the overcurrent of each pin and the number of pins involved.

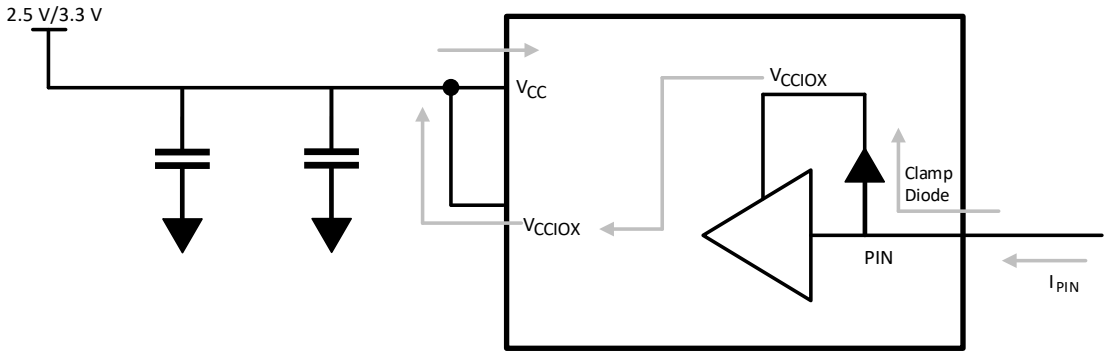


Figure C.1. Potential Current Path for Powered Down FPGA with Driven Input

C.2. Workarounds

Workaround 1

Turn off any external devices connected to the FPGA that are operating at 2.5 V or higher while the FPGA is running.

Workaround 2

Configure the Lattice Radiant software to keep GPIO CLAMPs off in the bitstream when CLAMPs are not required.

Workaround 3

- Ensure that external circuits do not exceed the datasheet I/O pad current limits for banks operating at 2.5 V or higher.
- In each bank, the current should not exceed n × 8 mA. Where n represents the number of I/O pads in between two consecutive power pins. See below scenarios.
  - V_{CCIO} – I/O_1 – I/O_2 – I/O_x – V_{CCIO}
  - GND – I/O_1 – I/O_2 – I/O_x – GND
  - V_{CCIO} – I/O_1 – I/O_2 – I/O_x – GND
- The I/O groupings can be found in the pin tables generated by the Lattice Radiant software.

Example: Limit the pin current by connecting a series resistor to an FPGA GPIO input.

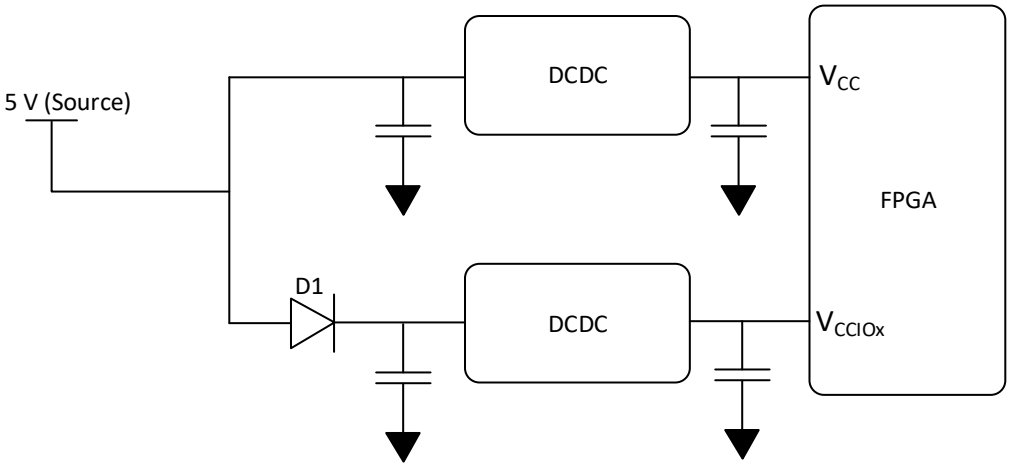
Most non-high-speed designs work well with a 200 Ω to 1 kΩ series resistor.

$$Formula: R \times C \times 2\,Tau = Trise / Tfall$$

$$200\ \Omega\ series\ resistor\ at\ GPIO\ input \times 10\ pF\ etch\ and\ pin\ capacitance \times 2\,Tau = 4ns\ Trise / Tfall$$

Workaround 4

For V_{CCIO}, use a separate voltage regulator with a diode D1 connecting the voltage source to the input.



References

For more information refer to:

- MachXO4 Devices web page
- Implementing High-Speed Interfaces with MachXO4 Devices (FPGA-TN-02410)
- MIPI D-PHY Interface IP (FPGA-RD-02040)
- MachXO4 Family Devices Data Sheet (FPGA-DS-02125)
- Lattice Radiant FPGA design software
- Lattice Insights for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 1.0, December 2025

Section	Change Summary
All	Updated the document to include LFMXO4 devices information only.
Software sysI/O Attributes	• In the DRIVE section, changed *Table 10.3 shows the supported drive strength for the single-ended I/O types under designated V_{CCIO} conditions* to *Table 10.3 shows the supported drive strength for the single-ended I/O types under designated I/O standards*. • In Table 10.2. Output Drive Capability for Ratioed sysI/O Standards, changed 16 mA drive strength support for LVCMOS25 from *YES* to —.
References	Added a reference to *Implementing High-Speed Interfaces with MachXO4 Devices (FPGA-TN-02410)*.

Revision 0.80, March 2025

Section	Change Summary
All	Preliminary release.

www.latticesemi.com