MachXO4 Single Event Upset (SEU) Report

Technical Note

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Inclusive Language

This document was created consistent with Lattice Semiconductor’s inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice’s inclusive language FAQ 6878 for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

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Tables

Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviation	Definition
CRAM	Configuration RAM
CRC	Cyclic Redundancy Check
EBR	Embedded Block RAM
ECC	Error Correction Codes
FIT	Failures-in-Time
FPGA	Field-Programmable Gate Array
IP	Intellectual Property
JEDEC	Joint Electron Device Engineering Council
LUT	Look-Up Table
RAM	Random Access Memory
NYC	New York City
SEC	Soft Error Correction
SED	Soft Error Detect
SEFI	Single Event Functional Interrupt
SEI	Soft Error Injection
SER	Soft Error Rate
SEU	Single Event Upset
SRAM	Static Random Access Memory

1. Introduction

This document discusses single event upsets (SEUs), a radiation effect that may be observed during normal operation of MachXO4™ FPGAs. SEUs, often referred to as soft errors, occur when energetic particles interact with memory components, causing what is observed as a random bit flip.

SRAM is susceptible to SEU and requires characterization according to the JEDEC JESD89 set of standards. Lattice FPGAs typically use SRAM memory in two applications: logic configuration RAM (CRAM) and user memory embedded block RAM (EBR).

This document provides Lattice's SEU characterization data for the above-mentioned FPGA family and types of memories, which can be used for estimating failure rates due to radiation effects.

Additionally, Lattice's FPGA architecture allows for significant failure derating, primarily due to unused routing resources within designs. Because of these redundant circuits, not all memory bits directly influence design functionality; those that do are known as *critical bits*. Derating guidelines based on critical bit analysis are provided for assessing the single event functional interrupt (SEFI) rate that is observed during field usage.

Finally, mitigation strategies offered by Lattice for handling SEUs are discussed.

2. Soft Error Rate Data for MachXO4 FPGA Family

Table 2.1 summarizes the SEU data collected for Lattice's 65-nm flash process used for the MachXO4 FPGA family. The soft error rate (SER) is represented in FIT, that is the number of upset bits (failures) per billion device-hours. This rate is further normalized to FIT/Mbit of memory to allow for scaling across different devices with varying amounts of memory.

The data is divided by radiation and memory type to allow for use-case customization:

- Radiation type
  - Neutron – Naturally occurring atmospheric neutrons can cause SEU. Results are scaled to the industry standard flux of NYC sea-level (14 n/cm2/hr), and can be further scaled based on latitude, longitude, and altitude.
  - Alpha – Device packaging impurities may produce alpha particles as a decay product, which are able to cause SEU. Results are scaled for ultra-low alpha mold compound flux (0.001 a/cm2/hr) and are considered use-case independent.
- SRAM type
  - Configuration – Logic configuration memory for controlling FPGA function.
  - EBR – Embedded user memory.

Table 2.1. SEU Data for MachXO4 FPGA Devices

Device Type	Radiation Type	SRAM Type	SER (FIT/Mbit)
MachXO4 (LFMXO4)	Neutron	Configuration	363.0
		EBR	611.0
	Alpha	Configuration	128.0
		EBR	363.0

3. Functional Interrupt Rate

Understanding the field impact of SEU is critical for assessing risk and implementing mitigation strategies. The architecture of Lattice FPGAs allows for derating of the above upset rates:

- Configuration
  - User logic designs implemented on Lattice FPGAs rely on a small fraction of *critical bits* in the configuration memory to continue operating properly. A customer design sample is used to derive typical and worst-case critical bit ratios for assessing the risk of functional failure.
- EBR
  - Lattice FPGAs allow for the implementation of error correction codes (ECC) into the user memory, which can detect and correct flipped bits, eliminating the functional impact of EBR SEU.

Combining these principles allows for the calculation of the expected field failure rate due to SEU, namely the SEFI rate. Table 3.1 shows an example for the MachXO4 family.

Table 3.1. SEFI Rate by Device Density

Device	Configuration Memory Size (Mbit)	Typical[1] SEFI Rate (FIT)	Worst-Case[2] SEFI Rate (FIT)
LFMXO4-010 LFMXO4-015	0.360	22.6	37.6
LFMXO4-015 (256 Ball Package) LFMXO4-025	0.534	33.4	55.7
LFMXO4-050	0.972	60.9	101.5
LFMXO4-050 (400 Ball Package) LFMXO4-080	1.534	96.1	160.1
LFMXO4-110	2.11	132.1704	220.284

Notes:

1. Typical designs range from 50% to 70% LUT utilization based on sample benchmark designs.
2. Worst-case designs range from 70% to 90% LUT utilization based on sample benchmark designs.

4. Customer Down-Time Calculation

You can enable the soft error detection (SED) function to detect soft error events. The SED scan happens in the background mode and the duration is variable but does not impact normal device functionality until an SED error is detected.

Once an SED error is detected, developers can arrange to flag the error to the system level or to reconfigure the FPGA. The MachXO4 family takes from 0.6 ms to 5.2 ms to reconfigure the device depending on the density.

5. Soft Error Event and Repair Sequences

The SED feature detects errors that are inserted by soft error injection (SEI) or actual soft bit errors. Depending on the available features of the FPGA family and the customer pattern architecture, soft error correction (SEC) can be done offline, or while the device is still running the customer pattern.

MachXO4 devices have a hardware implemented SED circuit, which is used to detect configuration SRAM errors and allow them to be corrected. The on-chip error detection cyclic redundancy check (CRC) circuitry allows you to perform these operations without any impact on design fitting or performance of the device.

The MachXO4 device supports both SED and SEC. The SED feature can be user controlled by the pattern implementation, or it can be one-shot that executes upon first configuration. When a soft error is detected, the device can be reconfigured if desired by pulsing the PROGRAMN pin or issuing a REFRESH command. The SED run time is under 100 ms but will not add to the amount of time the device is offline. Reconfiguration takes 5.2 ms or less. Thus, the total offline time is less than a few milliseconds. For further details on the hardware-based SRAM CRC error detect approach, refer to the document in the References section.

References

- MachXO4 Soft Error Detection (SED) and Correction (SEC) User Guide (FPGA-TN-02406)
- MachXO4 web page
- Lattice Insights web page for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 1.0, December 2025

Section	Change Summary
All	Initial release.

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