



Power and Thermal Estimation and Management for MachXO4 Devices

Technical Note

FPGA-TN-02409-1.0

September 2026

Disclaimers

Lattice makes no warranty, representation, or guarantee regarding the accuracy of information contained in this document or the suitability of its products for any particular purpose. All information herein is provided AS IS, with all faults, and all associated risk is the responsibility entirely of the Buyer. The information provided herein is for informational purposes only and may contain technical inaccuracies or omissions, and may be otherwise rendered inaccurate for many reasons, and Lattice assumes no obligation to update or otherwise correct or revise this information. Products sold by Lattice have been subject to limited testing and it is the Buyer's responsibility to independently determine the suitability of any products and to test and verify the same. LATTICE PRODUCTS AND SERVICES ARE NOT DESIGNED, MANUFACTURED, OR TESTED FOR USE IN LIFE OR SAFETY CRITICAL SYSTEMS, HAZARDOUS ENVIRONMENTS, OR ANY OTHER ENVIRONMENTS REQUIRING FAIL-SAFE PERFORMANCE, INCLUDING ANY APPLICATION IN WHICH THE FAILURE OF THE PRODUCT OR SERVICE COULD LEAD TO DEATH, PERSONAL INJURY, SEVERE PROPERTY DAMAGE OR ENVIRONMENTAL HARM (COLLECTIVELY, "HIGH-RISK USES"). FURTHER, BUYER MUST TAKE PRUDENT STEPS TO PROTECT AGAINST PRODUCT AND SERVICE FAILURES, INCLUDING PROVIDING APPROPRIATE REDUNDANCIES, FAIL-SAFE FEATURES, AND/OR SHUT-DOWN MECHANISMS. LATTICE EXPRESSLY DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY OF FITNESS OF THE PRODUCTS OR SERVICES FOR HIGH-RISK USES. The information provided in this document is proprietary to Lattice Semiconductor, and Lattice reserves the right to make any changes to the information in this document or to any products at any time without notice.

Inclusive Language

This document was created consistent with Lattice Semiconductor's inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice's inclusive language [FAQ 6878](#) for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

Contents

Contents	3
Abbreviations in This Document.....	5
1. Introduction	6
2. FPGA Power Consumption.....	6
3. Power and Thermal Considerations in Device Selection.....	6
3.1. Thermal Mitigation Techniques	6
4. Power Modes	8
5. Power Controller	9
6. Bank Controller	13
7. Power Guard	14
8. Low Power Design Implementation	15
9. Power Supply Sequencing and Hot Socketing.....	17
9.1. Power Calculator	17
9.2. Power Calculator and Power Equations	17
9.3. Typical and Worst-Case Process Power/ I_{CC}	18
9.4. Junction Temperature	18
9.5. Maximum Safe Ambient Temperature.....	18
9.6. Operating Temperature Range	18
9.7. Dynamic Power Multiplier (DPM)	19
9.8. Power Budgeting	19
9.9. Activity Factor Calculation.....	19
9.10. Thermal Impedance and Airflow	19
9.11. Reducing Power Consumption	20
9.12. Power Calculator Assumptions.....	21
References	22
Technical Support Assistance	23
Revision History.....	24

Figures

Figure 5.1. Power Controller State Diagram (STDBY, STOP)	9
Figure 5.2. Power Controller Block Diagram	9
Figure 5.3. IP Catalog Power Controller	11
Figure 5.4. Power Controller Waveform	12
Figure 6.1. INRDB, LVDSOB Primitive	13
Figure 6.2. IP Catalog Dynamic Bank Controller	13
Figure 7.1. Power Guard Primitive	14
Figure 7.2. IP Catalog Power Guard	14
Figure 8.1. Low Power Design Implementation	16
Figure 9.1. Power Calculator Main Window	17

Tables

Table 4.1. Power Supply Description and Voltage Levels	8
Table 5.1. Power Supply Description and Voltage Levels	10
Table 5.2. IP Catalog Power Controller Descriptions	11

Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviation	Definition
AC	Alternating Current
AF	Activity Factor
DC	Direct Current
FPGA	Field-Programmable Gate Array
I2C	Inter-Integrated Circuit
I/O	Input/Output
JTAG	Joint Test Action Group
LUT	Look Up Table
LVDS	Low-Voltage Differential Signaling
NCD	Native Circuit Description
PCB	Printed Circuit Board
POR	Power-On-Reset

1. Introduction

The key requirements for many of today's high-volume FPGA applications are low power consumption and operation within challenging thermal environments. The MachXO4™ family is available in two V_{CC} variants ($E=1.2$ V, $C=2.5$ V/3.3 V) and in a variety of packages with varying thermal characteristics. In addition, design characteristics and ambient temperature affect the overall power consumption and thermal performance. This technical note describes how to estimate and analyze power and thermal characteristics, and how to use the Lattice Power Calculator Tool to achieve system design goals.

Note: In this document, *MachXO4* refers to both LFMXO4 and LFMXO4D unless explicitly identified as *MachXO4 (LFMXO4)*. *MachXO4 RoT* refers only to LFMXO4D.

2. FPGA Power Consumption

The power consumption of a device can be broken down coarsely into the static (or DC) element and the dynamic (or AC) element. These elements have the following dependencies with respect to the junction temperature (T_J) of the die.

- Static power is a result of the leakage associated with the transistors. There are two types of static leakage.
 - Static leakage which has a strong temperature dependency
 - DC bias which is constant across temperature
- Dynamic power is caused by the toggling of signals in the transistor.
 - Dynamic power is constant across temperature

3. Power and Thermal Considerations in Device Selection

To ensure a package stays within a safe operating environment envelope system, select the appropriate MachXO4 device variant (see the [Maximum Safe Ambient Temperature](#) section). As the design progresses, you must follow the power calculation process described in this technical note to determine final power and thermal performance of their selected density, package, and V_{CC} . To assist with the initial decision, below are some general guidelines.

System designs with thermally controlled environments (less than 60 °C ambient) can typically choose a $V_{CC}=3.3$ V MachXO4 'C' device. If significant logic resources are used (high LUT utilization in 4K densities and up) and the FPGA design operates with a moderate to high activity factor (see the [Activity Factor Calculation](#) section), you are strongly encouraged to use the Lattice Power Estimator tool before finalizing a $V_{CC}=3.3$ V MachXO4 'C' device selection. MachXO4 designs with a high dynamic power component may require using one of the mitigation techniques described below.

3.1. Thermal Mitigation Techniques

For MachXO4 designs that operate in higher ambient temperature environments or include a significant number of resources with a high activity factor, you must consider one of the following mitigation techniques:

Use a lower core V_{CC} : The MachXO4 'C' devices support a V_{CC} of either 3.3 V or 2.5 V. Power dissipation inside the FPGA can typically be reduced by 25% using a $V_{CC}=2.5$ V (over $V_{CC}=3.3$ V). This improves the thermal performance of the FPGA.

Use the lowest core V_{CC} : The MachXO4 'E' devices support a V_{CC} of 1.2 V and provide more thermal headroom for a typical MachXO4 design. Power dissipation inside the FPGA can typically be reduced by 60% using a $V_{CC}=1.2$ V (over $V_{CC}=3.3$ V), significantly improving the thermal performance of the FPGA.

Add a Heatsink: Thermal performance of an FPGA design, including the maximum safe ambient temperature, is highly dependent on the thermal impedance of the MachXO4 density and package. Adding a heat sink or other thermal management strategy may be required, depending on the design. See the Thermal Impedance and Airflow section for more details.

When designing complex hardware using the MachXO4 PLD, specifically the L version, you must pay special attention to critical hardware configuration requirements. This technical note steps through these critical hardware requirements related to the MachXO4 devices. This document does not provide detailed step-by-step instructions but gives a high-level summary checklist to assist in the design process.

4. Power Modes

FPGA users often minimize power consumption by turning off subsystems while configured and operational. Design modes of operation are typically categorized into the following:

Normal Operation:

- Device is fully operational and all circuits are active
- Highest power consumption

Low Power Operation:

- Subsystems are dynamically shut down when not required
- Average to low power consumption

Ultra Low Power Standby:

- All subsystems are shut down
- Lowest power consumption provides the best option for prolonged battery life

The MachXO4 device offers flexible architecture that allows many on-chip components to be dynamically turned off during the low power operation modes. These features are listed in [Table 4.1](#).

Table 4.1. Power Supply Description and Voltage Levels

Device Component	Description
Bandgap	The Bandgap can be turned off in standby mode. When the Bandgap is turned off, analog circuitry such as the PLLs, on-chip oscillator, and referenced and differential I/O buffers are also turned off.
Power-On-Reset (POR)	The POR can be turned off in standby mode. This circuit monitors V_{CC} levels. In the event of unsafe V_{CC} drops, this circuit reconfigures the MachXO4 device. When the POR circuitry is turned off, limited power detection circuitry is still active. This option is only recommended for applications in which the power supply rails are reliable.
On-Chip Oscillator	The on-chip oscillator has two power-saving features. It may be statically switched off when not used in a design. It can also be turned off in standby mode.
PLL	Similar to the on-chip oscillator, the PLL also has two power-saving features. It can be statically switched off if it is not needed in a design. It can also be turned off in standby mode.
I/O Bank Controller	Referenced and differential I/O buffers (used to implement standards such as LVDS) consume more than ratioed single-ended I/O such as LVCMOS. The I/O bank controller allows the you to turn these I/O off dynamically on a per-bank basis.
Dynamic Clock Enable for Primary Clock Nets	Each primary clock net can be dynamically disabled to save power.
Power Guard	Power Guard is a feature implemented in input buffers. This feature allows you to switch off the input buffer when it is not needed. This feature can be used in both clock and data paths. Its biggest impact is in the standby mode, when it can be used to switch off clock inputs that are distributed using general routing resources.

5. Power Controller

The MachXO4 PLD includes a Power Controller to ensure smooth transitions into and out of standby mode. The Power Controller's two primary signals, STOP and STDBY, transitions are shown in Figure 5.1.

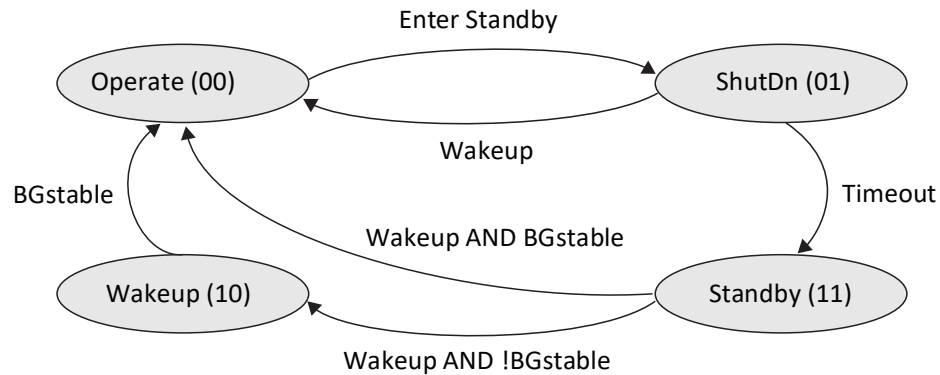


Figure 5.1. Power Controller State Diagram (STDBY, STOP)

The detailed Power Controller block diagram is shown in Figure 5.2 and its ports are defined in Table 5.1. The timeout signal is generated from an optional 8-bit Timer Counter that divides the input clock source by 28 (or 256). This injects a delay between the STOP and STDBY signals.

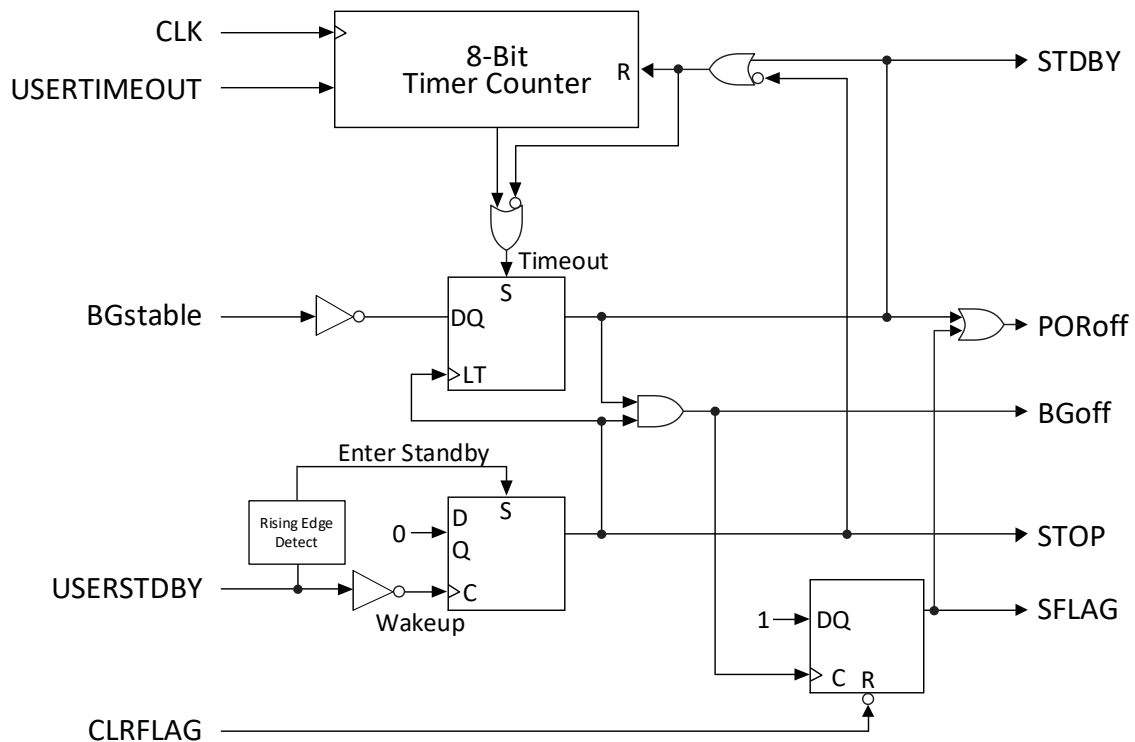


Figure 5.2. Power Controller Block Diagram

Table 5.1. Power Supply Description and Voltage Levels

Port	I/O	Optional	Description
CLK	Input	Yes	Clock source to the Timer Delay block.
USERTIMEOUT	Input	Yes	An active high enable signal for the Timer Counter block.
USERSTDBY	Input or Hardwired	Yes	A rising edge of this signal begins the shut-down sequence to enter standby. A falling edge of this signal begins the wake-up sequence from standby. The USERSTDBY signal is from user logic or hardwire from the Configuration logic. The signals CFGSTDBY and CFGWAKE are used to provide simulation support for the Configuration I2C and SPI standby and wake commands. These ports must be connected to the matching ports on the EFB.
CLRFLAG	Input	Yes	Asynchronous active high reset for the standby flag. User logic must assert a high pulse on this signal once device has woken up to clear the SFLAG.
STOP	Output	Yes	Active high signal that is a precursor to the STDBY signal. The delay from STOP to STDBY is determined by the 8-bit Timer Counter block. The STOP signal is used to prepare logic for standby by switching off clocks, signals, and others.
STDBY	Output	No	Active high signal through general routing to user logic, I/O pads, oscillator, and PLLs. Used to place logic in standby.
SFLAG	Output	Yes	This flag signal goes high to alert user logic that the device is on standby.
PORoff	Hardwired	Yes	Shut-off signal to the Power Detector circuitry (POR). Power Detector circuitry is used to determine if there has been a drop in V_{CC} . If so, the device is reconfigured.
BGoff	Hardwired	Yes	Shut-off signal to bandgap circuitry found in the MachXO4 E versions for additional power savings. When the bandgap circuitry is turned off, POR circuitry, analog circuits (PLL, oscillator, and differential I/O) are turned off.
BGstable	Hardwired	No	The BGstable signal is a signal from the bandgap circuit. This signal is released only after the bandgap circuitry is stable.

Note: When POR is shut off, limited Power Detector circuitry is still active. This option is only recommended for applications where the power supply rails are reliable. V_{CC} must remain within the data sheet recommended range; otherwise, device functionality cannot be guaranteed.

The Power Controller can be configured using the IP Catalog, as shown in [Figure 5.3](#).

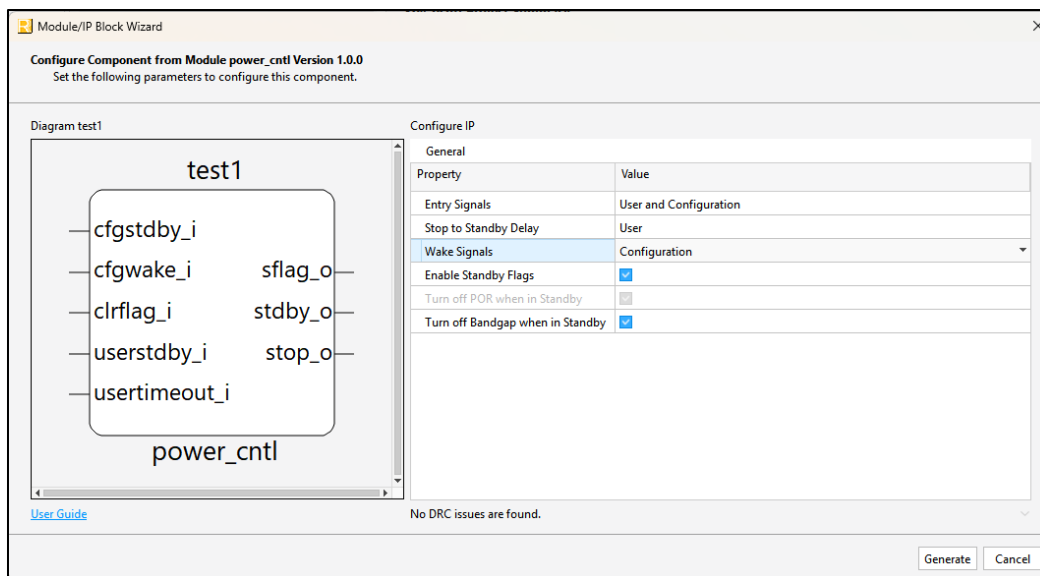


Figure 5.3. IP Catalog Power Controller

Table 5.2. IP Catalog Power Controller Descriptions

Entry	Type	Values	Default Value	Comment
Entry Signals	Combo Box	User, Configuration, User and Configuration	User	Configuration includes JTAG and I2C.
Stop to Standby Delay	Combo Box	User, Counter, Bypass	Bypass	User enables the USERTIMEOUT signal for the Timer Counter. When Bypass is selected, there is no delay between the STOP and STDBY signals.
Wake				
Wake Signals	Combo Box	User, Configuration	User	—
Standby				
Enable Standby Flags	Check Box	TRUE, FALSE	TRUE	—
Turn off Bandgap when in Standby ¹	Check Box	TRUE, FALSE	FALSE	When the bandgap circuitry is turned off, POR circuitry, analog circuits (PLL, oscillator, and differential I/O) are turned off.
Turn off POR when in Standby ¹	Check Box	TRUE, FALSE	FALSE	Power Detector circuitry is used to determine if there has been a drop on V _{CC} . If there has been one, then the device is reconfigured.

Note:

- When POR is shut off, limited Power Detector circuitry is still active. This option is only recommended for applications where the power supply rails are reliable. V_{CC} must remain within the data sheet recommended range; otherwise, device functionality cannot be guaranteed.

The Power Controller sequence for entering and exiting standby is shown in Figure 5.4.

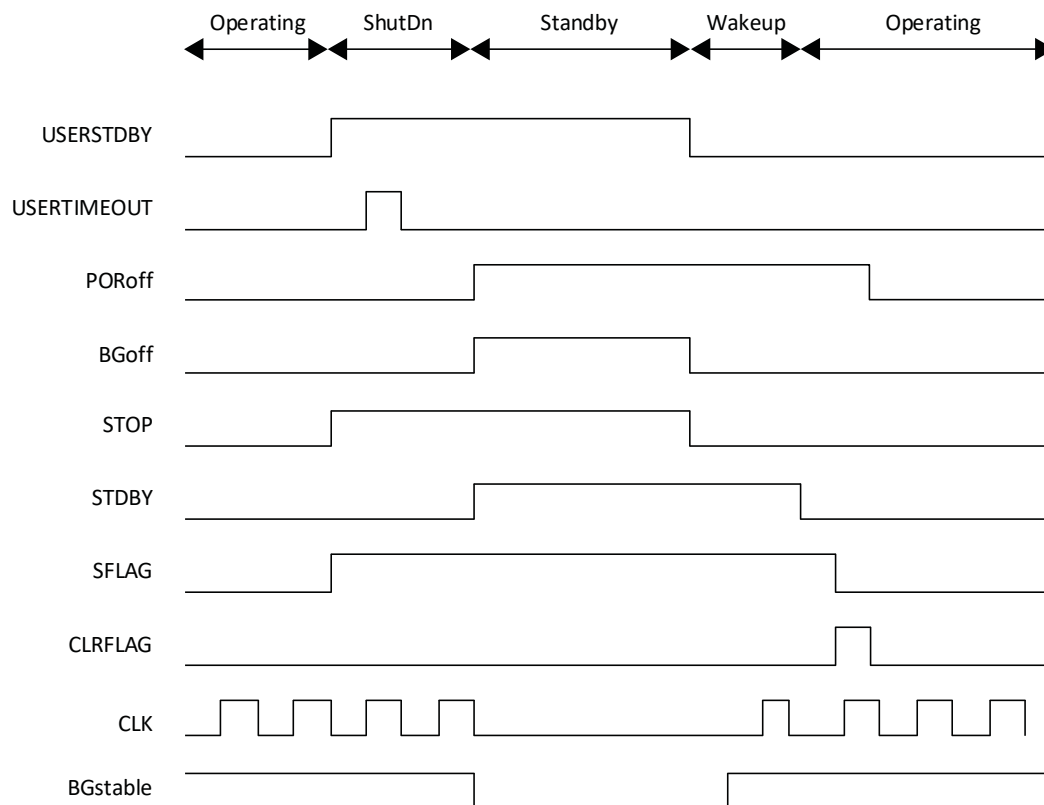


Figure 5.4. Power Controller Waveform

When designing with the Power Controller, you must be aware of the following:

- The software produces an error if the Power Controller USERSTDBY signal is turned off during standby. This is to prevent a lock-up situation.
- When the Power Detector circuitry is turned off, there is still some limited circuitry within the Power Detector that is active. It is recommended to turn off the Power Detector circuitry only if the power supply rails are reliable. V_{CC} must remain within the data sheet, recommended range or functionality cannot be guaranteed.
- When the Bandgap circuitry is turned off, Power Detector circuitry, analog circuits (PLL, oscillator, and differential I/O) are turned off.

6. Bank Controller

Referenced, differential and LVDS I/O standards consume more power than other I/O standards and are not always required to be active. The active high Bank Controller allows you to turn these I/O off dynamically on a per bank selection. The Dynamic InRD (input referenced and differential I/O) is used to turn off referenced and differential inputs. Dynamic LVDS control is used to turn off the LVDS output driver. The Bank Controller can be instantiated using the primitives shown (BCINRD for dynamic InRD, BCLVDSO for dynamic LVDS) in Figure 6.1 or using IP Catalog, as shown in Figure 6.2.

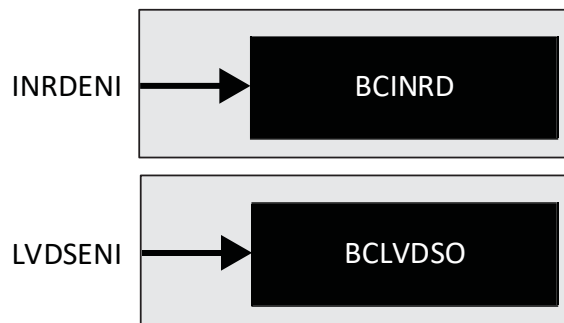


Figure 6.1. INRDB, LVDSOB Primitive

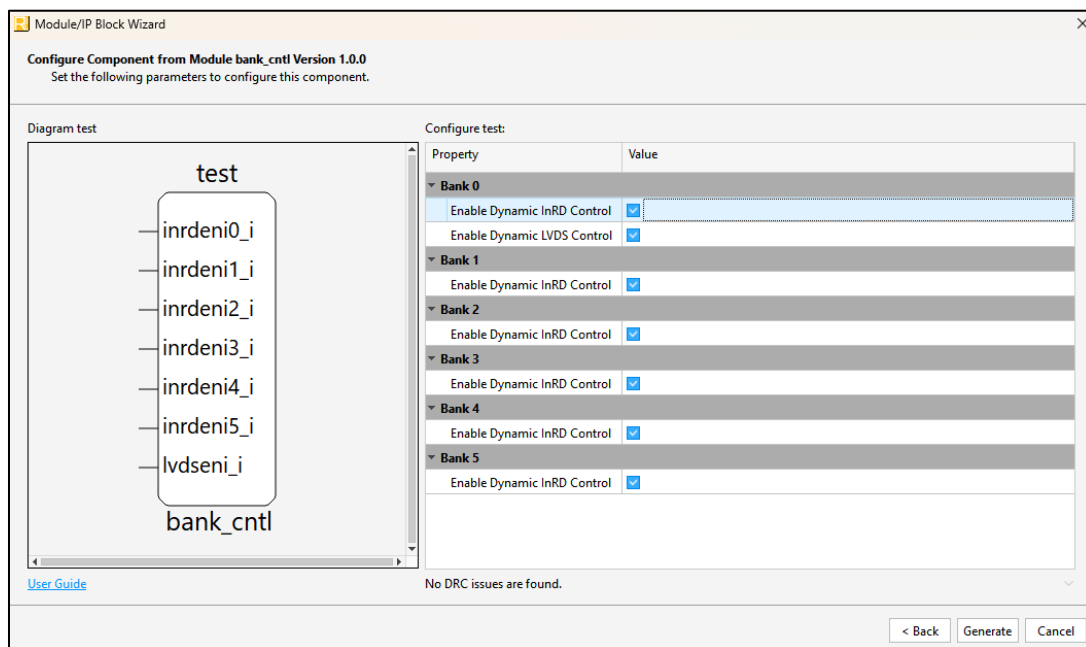


Figure 6.2. IP Catalog Dynamic Bank Controller

When designing with the Bank Controller, you must be aware of the following:

- The software produces an error if the Bank Controller control signal is from a referenced or differential I/O in the bank that is enabled by the Bank Controller. This is to prevent a lock-up situation.
- Powering off the bandgap overrides the Bank Controller.

7. Power Guard

The Power Guard (PG) feature minimizes dynamic power consumption on routing by gating signals at the input pin. To prevent this loss, especially on large fan-out or heavily loaded nets like clocks, inputs can be *Power Guarded*. Power Guard prevents logic from getting on nets using an active high control signal. The Power Guard primitive component, as shown in Figure 7.1, can be included in your clock or data paths. For large buses, IP Catalog can be used as shown in Figure 7.2.

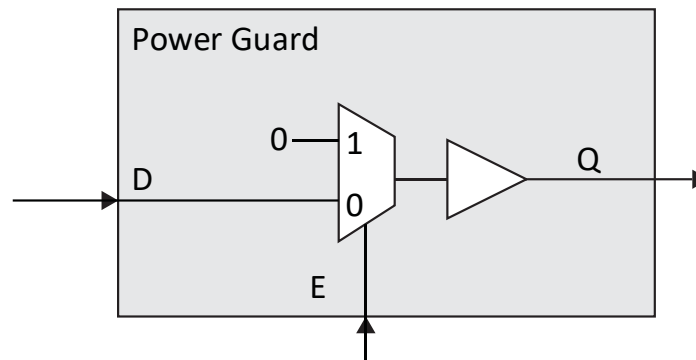


Figure 7.1. Power Guard Primitive

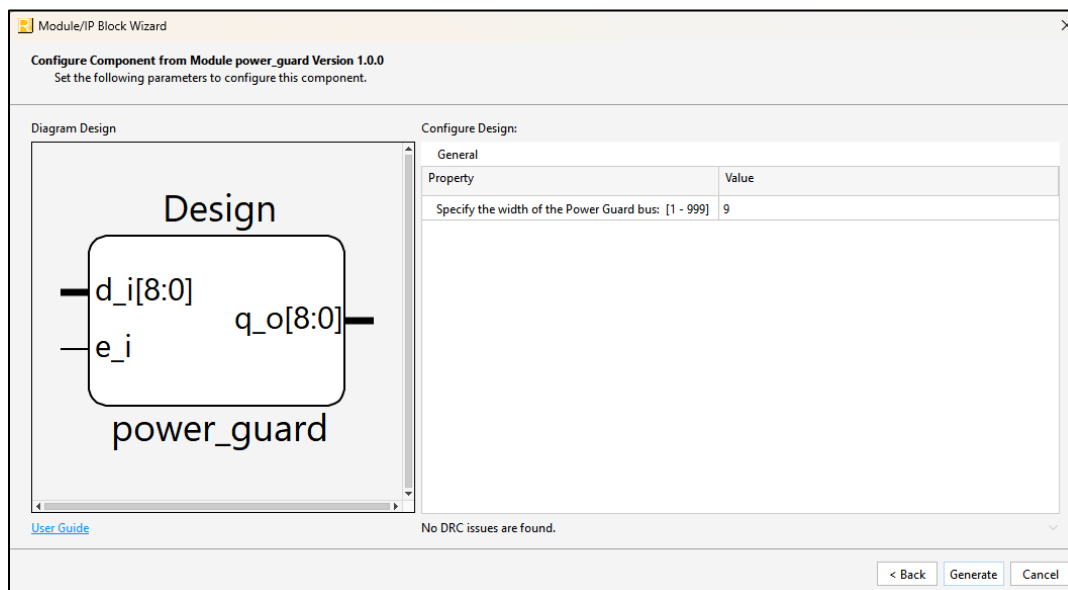


Figure 7.2. IP Catalog Power Guard

When designing with Power Guard, be aware of the following:

- The software produces an error if the Power Guard control signal is from the output of the Power Guard component. This is to prevent a lock-up situation.

8. Low Power Design Implementation

Figure 8.1 shows an example design implementation using the MachXO4 low-power architectural components.

In this design, there are four power level states:

1. Normal operation
2. Normal operation except video display is turned off
3. Preparing for standby
4. Standby

In this example design:

- White blocks are normal FPGA logic.
- Gray blocks are MachXO4 components associated with low power consumption.
- The clock CLK goes through the Power Guard component because it is a high fan-net in the design. The STDBY signal is used to block the clock signal from getting onto the routing, thus reducing dynamic power.
- The signal LVDSENI is used to turn off the LVDS I/O of the video display using the Bank Controller BCLVDSO, reducing static and dynamic power.
- A Power State Machine is used to step through the various states of the design. The bullets below describe what happens in each state:
 - Normal operation video display and I/O Expander are communicating with external memory and peripherals.
 - The video display is not being used, and the LVDSENI signal is asserted high. The LVDS I/O are disabled, thereby reducing static and dynamic power.
 - The device begins the low power standby sequence:
 - USERSTDBY is asserted high and is used by the Power Controller to assert high STOP.
 - The video display and I/O Expander logic prepare for standby.
 - After the delay CLKX/256 from the Power Controller Timer Counter, the STDBY signal is asserted high.
 - SFLAG is asserted high. Power Guard blocks the CLK signal from getting on high fan-out routing. The Bank Controller turns off the LVDS I/O. Video Display and I/O Expander logic are on standby, reaching the lowest power state.
 - When in the low power standby state, the device waits for the signal Wakeup before resuming normal operation.

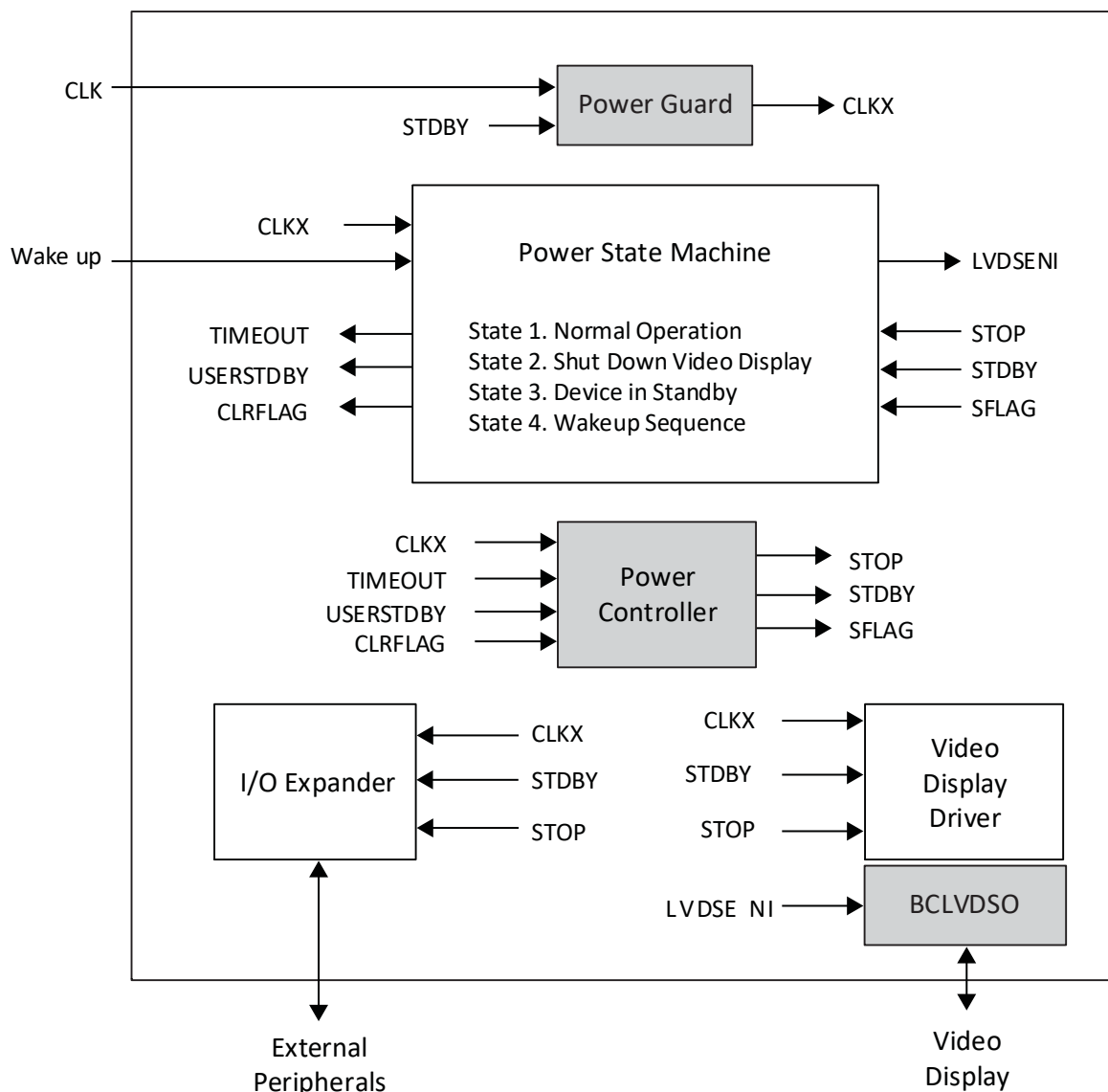


Figure 8.1. Low Power Design Implementation

9. Power Supply Sequencing and Hot Socketing

The MachXO4 devices are designed to ensure predictable behavior during power-up and power-down. During power-up and power-down sequences, the I/O remain in tri-state until the power supply voltage is high enough (VCCMIN) to ensure reliable operation. In addition, leakage into I/O pins is controlled to within the limits specified in [MachXO4 Family Data Sheet \(FPGA-DS-02125\)](#), allowing for integration with the rest of the system.

9.1. Power Calculator

The Power Calculator is a powerful tool that allows you to estimate the power consumption of a device. This tool offers an Estimation mode for “what-if” analysis and enables you to import NCD design files to accurately estimate power for their designs. The background engine performs each calculation quickly and accurately.

When running the Power Calculator tool in Estimation mode, you can provide estimates of the utilization of various components, and the tool provides an estimate of the power consumption. This is a good start, especially for “what-if” analysis and device selection.

Calculation mode is a more accurate approach, where you import the actual device utilization by importing the post Place and Route netlist design file (or NCD file). Each component of the device (for example, LUT, register, EBR, and I/O) has its own coefficients for static and dynamic power. Certain selections in the Power Calculator tool affect some of these coefficients, as discussed in the next section.

You can also import a Trace Report (or TWR) file where the frequencies for various clocks are imported. Note that the Trace Report only includes frequencies of the clock nets that are constrained in the Preference file.

The default Activity Factor (AF%) for dynamic power calculation is set to 10% in the Power Calculator. You can change the default AF for the entire project or for each clock net individually. Activity Factor is discussed in more detail later in this document.

9.2. Power Calculator and Power Equations

Refer to the Lattice Radiant™ Tutorial for launching and using the Power Calculator tool under **Help > Radiant Help**. Once you step through the procedure, you can see the window illustrated in [Figure 9.1](#).

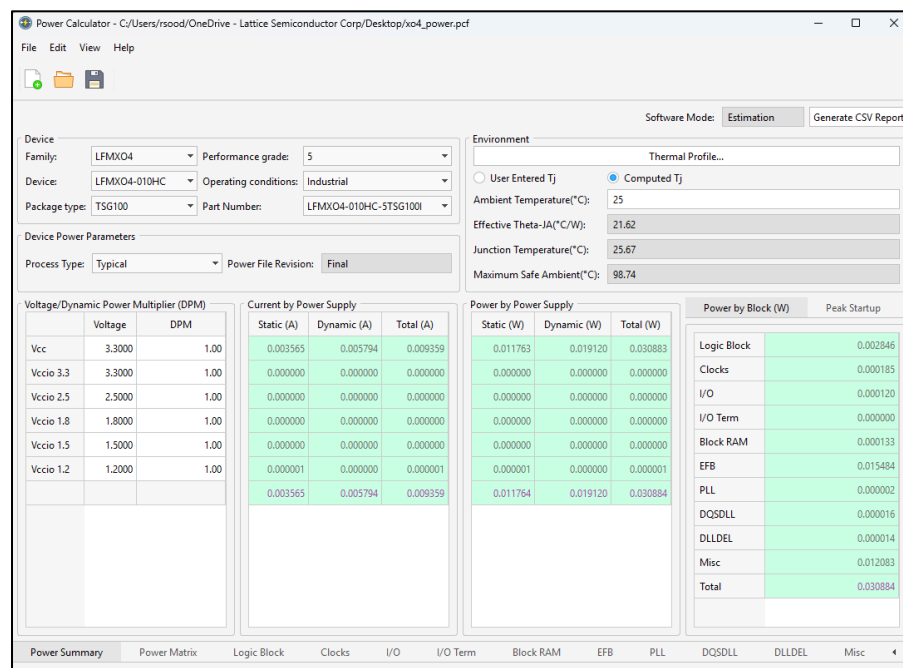


Figure 9.1. Power Calculator Main Window

It is important to understand how the options available with the Power Calculator affect the power consumption of a device. For example, if the ambient temperature changes, it affects the junction temperature, according to the following equation:

$$T_J = T_A + \theta_{JA_EFFECTIVE} * P \quad (1)$$

Where T_J and T_A are the junction and ambient temperatures, respectively, and P is the power.

$\theta_{JA_EFFECTIVE}$ is the effective thermal impedance between the die and its environment.

The junction temperature is directly proportional to the ambient temperature. An increase in T_A increases T_J and results in an increase in the static leakage component.

Selecting the Process Type again affects static leakage; in particular, the static leakage coefficient changes. The DC Bias component is constant across the range.

For dynamic power, increasing the frequency of toggling increases the dynamic component of power.

9.3. Typical and Worst-Case Process Power/ I_{CC}

Another factor that affects DC power is process variation. This variation, in turn, causes variation in quiescent power.

Power Calculator takes these factors into account and allows you to specify either a typical process or a worst-case process.

9.4. Junction Temperature

Junction temperature is the temperature of the die during operation. It is one of the most important factors that affect the device power. For a fixed junction temperature, voltage, and device package combination, quiescent power is fixed.

Ambient temperature affects the junction temperature as shown in Equation 1. Devices operating in a high-temperature environment have higher leakage since their junction temperatures are higher. Power Calculator models this ambient-to-junction temperature dependency. When you provide an ambient temperature, it is rolled into an algorithm that calculates the junction temperature and power through an iterative process to find the thermal equilibrium of the system (device running with the design) with respect to its environment (T_A , airflow, and others).

9.5. Maximum Safe Ambient Temperature

Maximum Safe Ambient Temperature is one of the most important numbers displayed in the Summary tab of the Power Calculator. This is the maximum ambient temperature at which the design can run without violating the junction temperature limits for commercial or industrial devices.

Power Calculator uses an algorithm to accurately predict this temperature. The algorithm adjusts itself as you change the options such as voltage, process, frequency, AF% (or any factor that may affect the power dissipation of the device).

9.6. Operating Temperature Range

When designing a system, you must make sure that a device operates at specified temperatures within the system environment. This is particularly important to consider before a system is designed. With Power Calculator, you can predict device thermodynamics and estimate the dynamic power budget. The ability to estimate the device operating temperature prior to board design also allows you to better plan for power budgeting and airflow.

Although total power, ambient temperature, thermal resistance and airflow all contribute to device thermodynamics, the junction temperature (as specified in [MachXO4 Family Data Sheet \(FPGA-DS-02125\)](#)) is the key to device operation. The allowed junction temperature range is 0 °C to 85 °C for commercial-grade devices and –40 °C to 100 °C for industrial grade devices. If the junction temperature of the die is not within these temperature ranges, the performance and reliability of the device's functionality cannot be guaranteed.

9.7. Dynamic Power Multiplier (DPM)

The user-defined frequency of operation makes this problem even more complex. To help resolve this issue, the Dynamic Power Multiplier provides some guard bands for system and board users.

The Dynamic Power Multiplier is defaulted to “1” that means the dynamic power is what it is. If you wish to add 20% additional dynamic power, the DPM can be set to 1.2 (1 + 20%) and it can be placed against the appropriate power supply. This increases the dynamic power for that supply by 20% and provides you with some guard band (if needed).

9.8. Power Budgeting

The Power Calculator provides the power dissipation of a design under a given set of conditions. It also predicts the junction temperature (T_j) for the design. If the junction temperature is outside the limits specified in [MachXO4 Family Data Sheet \(FPGA-DS-02125\)](#), the viability of operating the device at this junction temperature must be re-evaluated.

A commercial-grade device is likely to show speed degradation with a junction temperature above 85 °C and an industrial grade device at a junction temperature degrades above 100 °C. It is required that the die temperature be kept below these limits to achieve the guaranteed speed operation.

Operating a device at a higher temperature also means a higher Static ICC. The difference between the Total ICC and the Static ICC (both Static ICC and Dynamic ICC) at a given temperature provides the Dynamic ICC budget available. If the device runs at a Dynamic ICC higher than this budget, the total ICC is also higher. This causes the die temperature to rise above the specified operating conditions.

The four factors of power, ambient temperature, thermal resistance and airflow, can also be varied and controlled to reduce the junction temperature of the device. The Power Calculator is a powerful tool to help system users to properly budget the FPGA power that, in turn, helps improve the overall system reliability.

9.9. Activity Factor Calculation

The Activity Factor% (or AF%) is defined as the percentage of frequency (or time) that a signal is active or toggling the output. Most resources associated with the clock domain are running or toggling at some percentage of the frequency at which the clock is running. You must provide this value as a percentage under the AF% column in the Power Calculator tool.

Another term for I/O is the I/O Toggle Rate. The AF% is applicable to the PFU, Routing, and Memory Read Write Ports, etc. The activity of I/O is determined by the signals you provide (in the case of inputs) or as an output of the design (in the case of outputs). The rates at that the I/O toggle define their activity. The I/O Toggle Rate or the I/O Toggle Frequency is a better measure of their activity.

The Toggle Rate (or TR) in MHz of the output is defined in the following equation:

$$\text{Toggle Rate (MHz)} = 1/2 * f * \text{AF\%} \quad (2)$$

You are required to provide the TR (MHz) value for the I/O instead of providing the frequency and AF% for other resources. AF can be calculated for each routing resource, output or PFU. However, this involves long calculations. The general recommendation for a design occupying roughly 30% to 70% of the device is an AF% between 15% and 25%. This is an average value. The accurate value of an AF depends upon clock frequency, stimulus to the design and the final output.

9.10. Thermal Impedance and Airflow

A common method for characterizing thermal performance of a packaged device is with Thermal Resistance, T . For a semiconductor device, thermal resistance indicates the steady-state temperature rise of the die junction above a given reference for each watt of power (heat) dissipated at the die surface. Its units are °C/W.

The most common examples are θ_{JA} , Thermal Resistance Junction-to-Ambient (in °C/W) and θ_{JC} , Thermal Resistance Junction-to-Case (also in °C/W). Another factor is θ_{JB} , Thermal Resistance Junction-to-Board (in °C/W).

Knowing the reference (that is ambient, case, or board) temperature, the power, and the relevant T value, the junction temperature can be calculated per the following equations.

$$T_J = T_A + \theta_{JA} * P \quad (3)$$

$$T_J = T_C + \theta_{JC} * P \quad (4)$$

$$T_J = T_B + \theta_{JB} * P \quad (5)$$

Where T_J , T_A , T_C and T_B are the junction, ambient, case (or package) and board temperatures (in °C), respectively. P is the total power dissipation of the device.

θ_{JA} is commonly used with natural and forced convection air-cooled systems. θ_{JC} is useful when the package has a high-conductivity case mounted directly to a PCB or heatsink. And θ_{JB} applies when the board temperature adjacent to the package is known.

Power Calculator utilizes the ambient temperature (°C) to calculate the junction temperature (°C) based on the θ_{JA} for the targeted device. You can also provide the airflow values (in LFM) to obtain a more accurate junction temperature value.

To improve airflow effectiveness, it is important to maximize the amount of air that flows over the device or the surface area of the heat sink. The airflow around the device can be increased by providing an additional fan or increasing the output of the existing fan. If this is not possible, baffling the airflow to direct it across the device may help. This means the addition of sheet metal or objects to provide the mechanical airflow guides to guide air to the target device. Often the addition of simple baffles can eliminate the need for an extra fan. In addition, the order in which air passes over devices can impact the amount of heat dissipated.

9.11. Reducing Power Consumption

One of the most critical challenges for users today is reducing system power consumption. A low-order reduction in power consumption has significant impact, especially in modern hand-held devices and electronics. There are several design techniques that can be used to significantly reduce overall system power consumption. Some of these include:

- Using the MachXO4 power-saving architecture features like Power Controller, Bank Controller and Power Guard.
- Reducing operating voltage while staying within data sheet limits.
- Operating within the specified package temperature limitations.
- PLL jitter/power option within IP Catalog
- Confirm if input-only bank saves power
- Using optimum clock frequency reduces power consumption, as the dynamic power is directly proportional to the frequency of operation. You must determine if some portions of the design can be clocked at a lower rate that reduces power.
- Reducing the span of the design across the device. A more closely-placed design uses fewer routing resources and therefore less power.
- Reducing the voltage swing of the I/O where possible.
- Ensuring input logic levels are not left floating but pulled either up or down.
- Ensuring no I/O pull-up/down conflicts with other components on the board.
- Using optimum encoding where possible. For example, a 16-bit binary counter has, on average, only 12% activity factor and a 7-bit binary counter has an average of 28% activity factor. On the other hand, a 7-bit LFSR counter toggles at an activity factor of 50%, that causes higher power consumption. A gray code counter, where only one bit changes at each clock edge, uses the least amount of power, as the activity factor is less than 10%.
- Minimizing the operating temperature by the following methods:
 - Use packages that can better dissipate heat, such as ceramic packages.
 - Place heat sinks and thermal planes around the device on the PCB.
 - Use better airflow techniques, such as mechanical airflow guides and fans (both system fans and device mounted fans).
- To achieve the lowest standby power:
 - All clocks and combinatorial logic must be held at a steady-state
 - All inputs must be held at a rail; if not possible, toggling inputs must be gated using Power Guard

- All outputs must be tri-stated and the Bank Controller must turn off referenced and LVDS outputs
- Internal oscillator must be turned off using the STDBY port
- PLLs must be turned off using the STDBY port
- Bandgap and POR must be turned off using the Power Controller

9.12. Power Calculator Assumptions

The following are the assumptions made by the Power Calculator.

- The Power Calculator tool uses equations with constants based on a room temperature of 25 °C. The default temperature of 25 °C can be changed.
- You can define the ambient temperature (T_A) for device junction temperature (T_J) calculation based on the power estimation. T_J is calculated from the user-entered T_A and the power calculation of typical room temperature.
- I/O power consumption is based on an output loading of 5 pF. You can change this capacitive loading.
- You can estimate power dissipation and current for each type of power supply (V_{CC} , V_{CCIO}).
- The nominal V_{CC} is used by default to calculate power consumption. A lower or higher V_{CC} can be chosen from a list of available values.
- θ_{JA} can be changed to better estimate the operating system manually or by entering Airflow in Linear Feet per Minute (LFM) along with a Heat Sink options.
- The default value of the I/O types for MachXO4 devices is LVCMOS25, 8 mA.
- The activity factor (AF) is defined as the toggle rate of the registered output. For example, assuming that the input of a flip-flop is changing at every clock cycle, 100% AF of a flip-flop running at 100 MHz is 50 MHz. The default activity factor for logic is 10%.

References

For more information related to power and thermal estimation and management for MachXO4 Devices, refer to the web pages below.

- [MachXO4 Family Devices](#) web page
- [MachXO4 Family Data Sheet \(FPGA-DS-02125\)](#)
- [MachXO4 Family Root-of-Trust Devices Data Sheet \(FPGA-DS-02126\)](#)
- IP Cores and Reference Designs for MachXO4 Devices
- Kits, Boards, and Demonstration for MachXO4 Devices
- [Lattice Insights](#) for Lattice Semiconductor training courses and learning plans
- [Lattice Radiant](#) FPGA design software

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 1.0, September 2026

Section	Change Summary
All	Initial release



www.latticesemi.com