MachXO4 Family Hardware Checklist

Technical Note

FPGA-TN-02411-1.1

September 2026

Disclaimers

Lattice makes no warranty, representation, or guarantee regarding the accuracy of information contained in this document or the suitability of its products for any particular purpose. All information herein is provided AS IS, with all faults, and all associated risk is the responsibility entirely of the Buyer. The information provided herein is for informational purposes only and may contain technical inaccuracies or omissions, and may be otherwise rendered inaccurate for many reasons, and Lattice assumes no obligation to update or otherwise correct or revise this information. Products sold by Lattice have been subject to limited testing and it is the Buyer's responsibility to independently determine the suitability of any products and to test and verify the same. LATTICE PRODUCTS AND SERVICES ARE NOT DESIGNED, MANUFACTURED, OR TESTED FOR USE IN LIFE OR SAFETY CRITICAL SYSTEMS, HAZARDOUS ENVIRONMENTS, OR ANY OTHER ENVIRONMENTS REQUIRING FAIL-SAFE PERFORMANCE, INCLUDING ANY APPLICATION IN WHICH THE FAILURE OF THE PRODUCT OR SERVICE COULD LEAD TO DEATH, PERSONAL INJURY, SEVERE PROPERTY DAMAGE OR ENVIRONMENTAL HARM (COLLECTIVELY, "HIGH-RISK USES"). FURTHER, BUYER MUST TAKE PRUDENT STEPS TO PROTECT AGAINST PRODUCT AND SERVICE FAILURES, INCLUDING PROVIDING APPROPRIATE REDUNDANCIES, FAIL-SAFE FEATURES, AND/OR SHUT-DOWN MECHANISMS. LATTICE EXPRESSLY DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY OF FITNESS OF THE PRODUCTS OR SERVICES FOR HIGH-RISK USES. The information provided in this document is proprietary to Lattice Semiconductor, and Lattice reserves the right to make any changes to the information in this document or to any products at any time without notice.

Inclusive Language

This document was created consistent with Lattice Semiconductor’s inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice’s inclusive language FAQ 6878 for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

Contents

Figures

Tables

Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviation	Definition
DDR	Double Data Rate
FB	Ferrite Bead
FPGA	Field-Programmable Gate Array
GPIO	General Purpose Input/Output
GPLL	General Purpose PLL
HCSL	High-Speed Current Steering Logic
I2C	Inter-Integrated Circuit
I3C	Improved Inter-Integrated Circuit
IBIS	I/O Buffer Information Specification
JTAG	Joint Test Action Group
LVCMOS	Low Voltage Complementary Metal Oxide Semiconductor
LVDS	Low Voltage Differential Signaling
LVTTL	Low Voltage Transistor-Transistor Logic
MIPI	Mobile Industry Processor Interface
MSPI	Master Serial Peripheral Interface
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
PLL	Phase-Locked Loop
POR	Power-On-Reset
SI	Signal Integrity
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SSO	Simultaneous Switching Output
SSPI	Secondary Serial Peripheral Interface
USB	Universal Serial Bus
WISHBONE	Open Source Bus Interface

1. Introduction

When designing complex hardware using the MachXO4™ device, you must pay special attention to critical hardware configuration requirements. In this document, MachXO4 refers to both LFMXO4 and LFMXO4D devices unless explicitly identified as MachXO4 (LFMXO4). MachXO4 RoT refers only to LFMXO4D devices. This technical note outlines the critical hardware requirements related to the MachXO4 device. This document does not provide detailed step-by-step instructions but offers a high-level summary checklist to assist in the design process.

Hardware checklists are developed after evaluation boards and incorporate optimized designs that improve upon the circuitry of the evaluation boards. If you copy circuits from evaluation boards, ensure that you optimize your designs according to the hardware checklists.

The MachXO4 devices come in high-performance versions, HC and HE, and a ZC device that has ultra-low static and dynamic power consumption. The HC devices are designed to provide high performance. The HC and ZC devices have a built-in voltage regulator to allow for 2.5 V V_{CC} and 3.3 V V_{CC}.

The high-performance devices are available in two speed grades, –5 and –6, with –6 being faster. HC and ZC devices have an internal linear voltage regulator supporting external VCC supply voltages of 3.3 V or 2.5 V, while HE devices accept only 1.2 V as the external VCC supply voltage. All HC and HE parts are functionally and pin-compatible.

The ZC devices are available in two speed grades at industrial temperatures, –2 and –3, with –3 being faster.

This technical note assumes familiarity with the MachXO4 device features as described in the MachXO4 Family Data Sheet (FPGA-DS-02125).

The critical hardware areas covered in this technical note are:

- Power supplies, including MachXO4 supply rails and their connections to the PCB and associated system.
- Configuration, including mode selection connection for proper power-up.
- Device I/O interfaces and critical signals.

Important: Refer to the following documents for detailed recommendations:

- Power and Thermal Estimation and Management for MachXO4 Devices (FPGA-TN-02409)
- MachXO4 sysIO User Guide (FPGA-TN-02398)
- Implementing High-Speed Interfaces with MachXO4 Devices (FPGA-TN-02410)
- MachXO4 Programming and Configuration User Guide (FPGA-TN-02393)
- Using Hardened Control Functions in MachXO4 Devices (FPGA-TN-02403)

2. Power Supply

The V_{CC} and V_{CCIO0} power supplies determine the MachXO4 internal power-good condition. These supplies must be at a valid and stable level before the device can become operational. In addition, five supplies (V_{CCIO1} to V_{CCIO5}) power the remaining I/O banks. Table 2.1 shows the power supplies and their corresponding voltage levels. Refer to the MachXO4 Family Data Sheet (FPGA-DS-02125) for more information on the Power-On-Reset (POR), V_{CC}, and V_{CCIOx} voltage levels.

Table 2.1. Power Supply Description and Voltage Levels

Supply	Voltage (Nominal Value)	Description
V_{CC}	1.2 V	Core power supply for 1.2 V devices (HE)
	2.5 V/3.3 V	Core power supply for 2.5 V/3.3 V devices (HC and ZC)
V_{CCIOx}	1.2 V to 3.3 V	Power supply pins for I/O Bank x. There are up to five I/O banks.

2.1. Power Noise

The power rail voltages of the FPGA allow for a worst-case normal operating tolerance of ±5% of these voltages. The 5% tolerance includes any noise.

Power Source

V_{CC} and V_{CCIOx} power rails of the same voltage should originate from the same voltage regulator to ensure proper power sequencing.

It is recommended that the designed voltage regulators are accurate to within 3% of the optimum voltage to allow power noise design margin.

When calculating the total voltage regulator tolerance, include:

- Regulator voltage reference tolerance.
- Regulator line tolerance.
- Regulator load tolerance.
- Tolerances of any resistors connected to the regulator feedback pin, which sets the regulator output voltage.
- Expected voltage drops due to the power filtering ferrite bead ESR × expected current draw.
- Expected voltage drops due to the current measuring resistor resistance × expected current draw.

With a 3% tolerance allocated to the voltage source, the design has a remaining 2% tolerance for noise and layout related issues. The 1.2 V rail is particularly sensitive to noise, as every 12 mV represents 1% of the rail voltage. For banks supporting sensitive differential signals (LVDS, MIPI, and the like) target for the bank's V_{CCIOx} less than 1.0% peak noise to minimize jitter.

2.2. Power Regulator Derating

A standard best practice among power supply designers is to derate a regulator's output current to 85% of its maximum rated limit, ensuring that even transient peak current demands remain below this threshold.

As a design approaches full capacity, performance significantly degrades. Datasheet oscilloscope screenshots often illustrate these penalties; a close examination reveals that operating near maximum current leads to poor load regulation, typically causing an additional 1% to 2% drop in output voltage. It also results in a significant increase in output noise, increased internal voltage drops across the power path, reduced efficiency, and excessive waste heat. In linear regulators, this waste heat increases linearly as the input-to-output voltage differential (Vin – Vout) increases. In switching DC-DC regulators, high current operation introduces specific risks to peripheral passives, including magnetic core saturation in the inductor and ripple-current stress on input/output capacitors.

Maintaining a design margin is critical because maximum datasheet ratings assume an ideal PCB layout with extensive copper thermal pads and thermal via arrays, conditions rarely met in real-world designs. Furthermore, these maximum current specifications assume relatively low ambient temperatures. When operating in confined or hot environments, engineers must consult the datasheet's ambient temperature derating curves, as allowable current capacity drops linearly once a critical thermal threshold is exceeded.

Finally, leaving zero headroom provides no margin for applications that may occasionally demand more current than expected. For example, variations in a customer's supply chain may eventually introduce "Fast-Fast" process corners that exhibit higher peak current draws.

Summary

Select regulators so that the nominal design uses no more than 85% of the device maximum rated current during peak transients. For high-reliability applications demanding an extended operational life, high manufacturing yields, and margin for non-ideal PCB designs/layouts, target a stricter 75% utilization limit.

3. Power

Providing a quiet, filtered supply is important for all rails, and critical for the analog rails. Supplies should be decoupled using adequate power filters. Bypass capacitors must be located close to the device package pins, with very short traces to minimize inductance.

For optimal performance, assign pins carefully to keep noisy I/O pins away from sensitive functional pins. PCB-related crosstalk with sensitive blocks is often caused by FPGA outputs located near sensitive power supplies. These supplies require careful board layout to ensure immunity to switching noise generated by FPGA outputs. Guidelines are provided for building quiet-filtered analog supplies; however, robust PCB layout is required to prevent noise infiltration.

3.1. Recommended Power Filtering Groups and Components

Table 3.1. Recommended Power Filtering Groups and Components

Power Input	Recommended Filter	Notes
V_{CC}	10 µF x 2 + 1.0 µF + 100 nF x (# rail power pins – 1)	Core and clock logic. For 1.2 V devices (HE) For 2.5 V/3.3 V devices (HC and ZC)
VCCIO[6:0]	Each V_{CCIOx}: 10 µF + 1.0 µF + 100 nF x (# rail power pins – 1) For banks supporting sensitive differential signals (LVDS, MIPI, and the like) add a series ferrite bead: FB 120 Ω + 10 µF + 1.0 µF + 100 nF x (# rail power pins – 1)	Bank I/O. For unused banks, a single 1.0 µF is sufficient. For banks with many outputs or large capacitive loading, replace the 10 µF with a 22 µF (or use two 10 µF). 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V

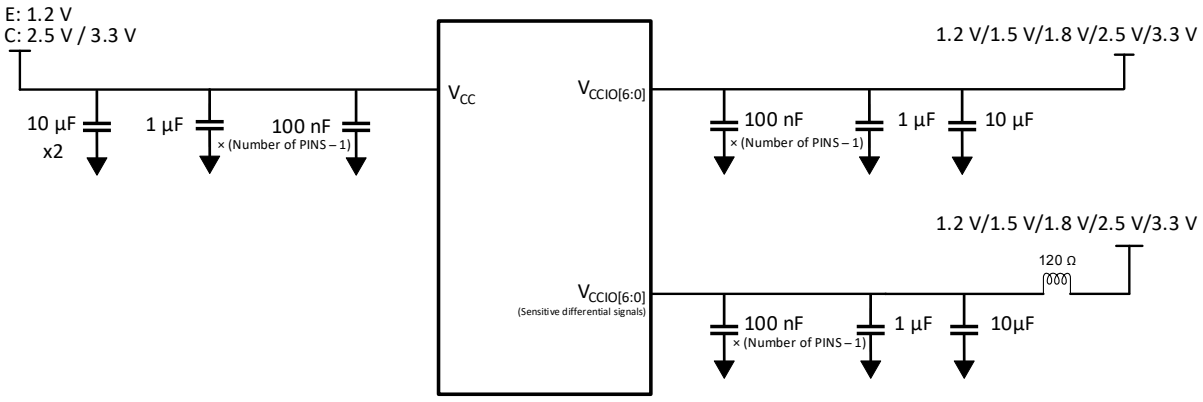


Figure 3.1. Recommended Power Filter Group

3.2. Ground Pins

All ground pins must be connected to the board ground plane.

For the TQFP-144 package, the EPAD (Exposed PAD) must be connected with low inductance to the ground plane using ground vias in a grid pattern. The recommended grid spacing is 1.5 mm between vias.

3.3. Unused GPIO Pins Summary

Leave all unused GPIO pins open.
(It is recommended to connect a few unused GPIOs to test points to facilitate debugging and bring-up rework.)

3.4. Unused Banks (V_{CCIOx})

Connect unused V_{CCIOx} pins to a power rail; do not leave them unconnected.
It is recommended to bypass unused bank rail pins with a single 1.0 µF or 100 nF capacitor.

3.5. Clock Oscillator Supply Filtering

When providing an external reference clock to the FPGA — such as from a single-ended or differential clock oscillator, ensure proper power supply isolation and decoupling of the oscillator.

When specifying components, choose good-quality ceramic capacitors in small packages, and place them as close as possible to the clock oscillator supply pins.

3.6. Power Sequencing

On HC and ZC devices, like power supplies must be tied together. For example, if V_{CCIO} and V_{CC} are both the same voltage, they must also be the same supply.

On HE devices, VCC needs to be powered up prior to VCCIO with fast ramp rate applied on V_{CC} and at least 20 ms delay before V_{CCIO} is powered up.

Table 3.2. Power Supply Ramp Rates

Symbol	Parameter	Min	Type	Max	Unit
t_{RAMP}	Power supply ramp rates for all power supplies.	0.01	—	40	V/ms

3.7. Power Estimation

Once the MachXO4 device density, package, and logic implementation are determined, power estimation can be performed using the Power Calculator tool, provided as part of the Lattice Radiant™ design software. During power estimation, keep the following two goals in mind:

- Power supply budgeting must be based on the maximum power-up in-rush current, configuration current, and maximum DC and AC current under the system's environmental conditions.
- The ability of the system environment and MachXO4 device packaging to maintain the specified maximum operating junction temperature must be considered.

By evaluating these two criteria, system design planning can incorporate the MachXO4 device power requirements early in the design phase.

These considerations are detailed in Power and Thermal Estimation and Management for MachXO4 Devices (FPGA-TN-02409).

4. Component Selection

4.1. Ferrite Bead Selection

- Most designs work well with ferrite beads rated between 120 Ω at 100 MHz and 240 Ω at 100 MHz.
- Ferrite bead-induced noise voltage from ESR × CURRENT should be less than 1% of the rail voltage.
- Use ferrite beads with ESR between 0.01 Ω and 0.10 Ω, depending on current load.
- Small-package ferrite beads have higher ESR than large-package beads of the same impedance.
- High-impedance ferrite beads have higher ESR than low-impedance beads of the same package size.

4.2. Capacitor Selection

When specifying components, choose good-quality ceramic capacitors in small packages, and place them as close to the supply pins as possible. *Good quality* capacitors for bypassing generally meet the following requirements:

4.2.1. Capacitor Dielectric

Use dielectrics such as X5R, X7R, which have good capacitance tolerance (≤ ±20%) over temperature range. Avoid Y5V, Z5U, and other dielectrics with poor capacitance control.

4.2.2. Voltage Rating

A capacitor's working capacitance decreases nonlinearly with increasing voltage bias. To maintain capacitance, the capacitor voltage rating should be at least 80% higher than the maximum rail voltage. For example, bypass capacitors on a 3.3 V rail should have a minimum rating of 6.3 V.

4.2.3. Size

Smaller-body capacitors have lower inductance, operate at higher frequencies, and improve board layout. For a given voltage rating, smaller-body capacitors tend to cost more than larger ones. Balancing market pricing and size-related inductance, the following capacitor sizes are recommended:

Table 4.1. Recommended Capacitor Sizes

Capacitance	Size Preferred	Size Next Best
0.1 µF, 1.0 µF	0201	0402
2.2 µF	0402	0201
4.7 µF	0402	0603
10 µF	0402	0603
22 µF	0805	0603

4.2.4. Mounting Location

Place the 0.1 µF and 1.0 µF capacitors close to the MachXO4 associated power rail pins. Selecting 0201 package size allows these capacitors to fit on the opposite side of the PCB from the MachXO4 device, between ball pad via holes.

5. Configuration Considerations

The MachXO4 devices contain two types of memory: SRAM and Flash. SRAM is a volatile memory and contains the active configuration. Flash is nonvolatile memory that provides on-chip storage for the SRAM configuration data and user data.

The MachXO4 device includes multiple programming and configuration interfaces:

- IEEE 1149.1 JTAG
- Self-download
- Target SPI (SSPI)
- Controller SPI (MSPI)
- Dual Boot
- I2C
- WISHBONE bus

For ease of prototype debugging, it is recommended that every PCB provide easy access to the programming and configuration pins.

The configuration logic arbitrates access among the interfaces in the following priority. When higher-priority ports are enabled, Flash access by lower-priority ports is blocked.

- JTAG Port
- Target SPI (SSPI) Port (SN low activates the SPI port)
- I2C Controller Port

Note: Erased devices have all programming and configuration ports enabled by default. When the device is erased, ensure that SN and PROGRAMN are not driven low.

For a detailed description of the programming and configuration interfaces, refer to the MachXO4 Programming and Configuration User Guide (FPGA-TN-02393).

External resistors are required when configuration signals are used to handshake with other devices. Pull-up and pull-down resistor (4.7 kΩ) recommendations for various configuration pins are listed below.

Table 5.1. Default States of the sysCONFIG Pins[1]

Pin Name	Pin Function (Configuration Mode)	Pin Direction (8-Bit Size)	Data In Bits that Get Masked (9-Bit Size)
PROGRAMN	PROGRAMN	Input with weak pull-up; external pull-up to V_{CCIO0}.	PROGRAMN
INITN	I/O	I/O with weak pull-up; external pull-up to V_{CCIO0}.	User-defined I/O
DONE	I/O	I/O with weak pull-up, external pull-up to V_{CCIO0}.	User-defined I/O
MCLK/CCLK[2]	SSPI	Input with weak pull-up. MCLK function requires a 510 Ω to 1 kΩ pull-up to V_{CCIO2}; place the series resistor near the Tx side.	User-defined I/O
SN	SSPI	Input with weak pull-up; external pull-up to V_{CCIO2}.	User-defined I/O
SI/SPISI	SSPI	Input	User-defined I/O
SO/SOSPI	SSPI	Output	User-defined I/O
CSSPIN	I/O	I/O with weak pull-up; external pull-up to V_{CCIO2}.	User-defined I/O
SCL	I2C	Bidirectional open-drain; external pull-up; noise filter (200 Ω series/100 pF to GND).	User-defined I/O
SDA	I2C	Bidirectional open-drain; external pull-up; noise filter (100 Ω series/100 pF to GND).	User-defined I/O
TDI	TDI	Input with weak pull-up.	TDI
TDO	TDO	Output with weak pull-up.	TDO
TCK	TCK	Input. Recommended 4.7 kΩ pull-down resistor.	TCK

Pin Name	Pin Function (Configuration Mode)	Pin Direction (8-Bit Size)	Data In Bits that Get Masked (9-Bit Size)
TMS	TMS	Input with weak pull-up.	TMS
JTAGENB	I/O	Input with weak pull-down.	I/O

Notes:

1. Leave the unused configuration ports open.
2. The series resistor value depends on the PCB design. The range is from 22 Ω to 39 Ω.

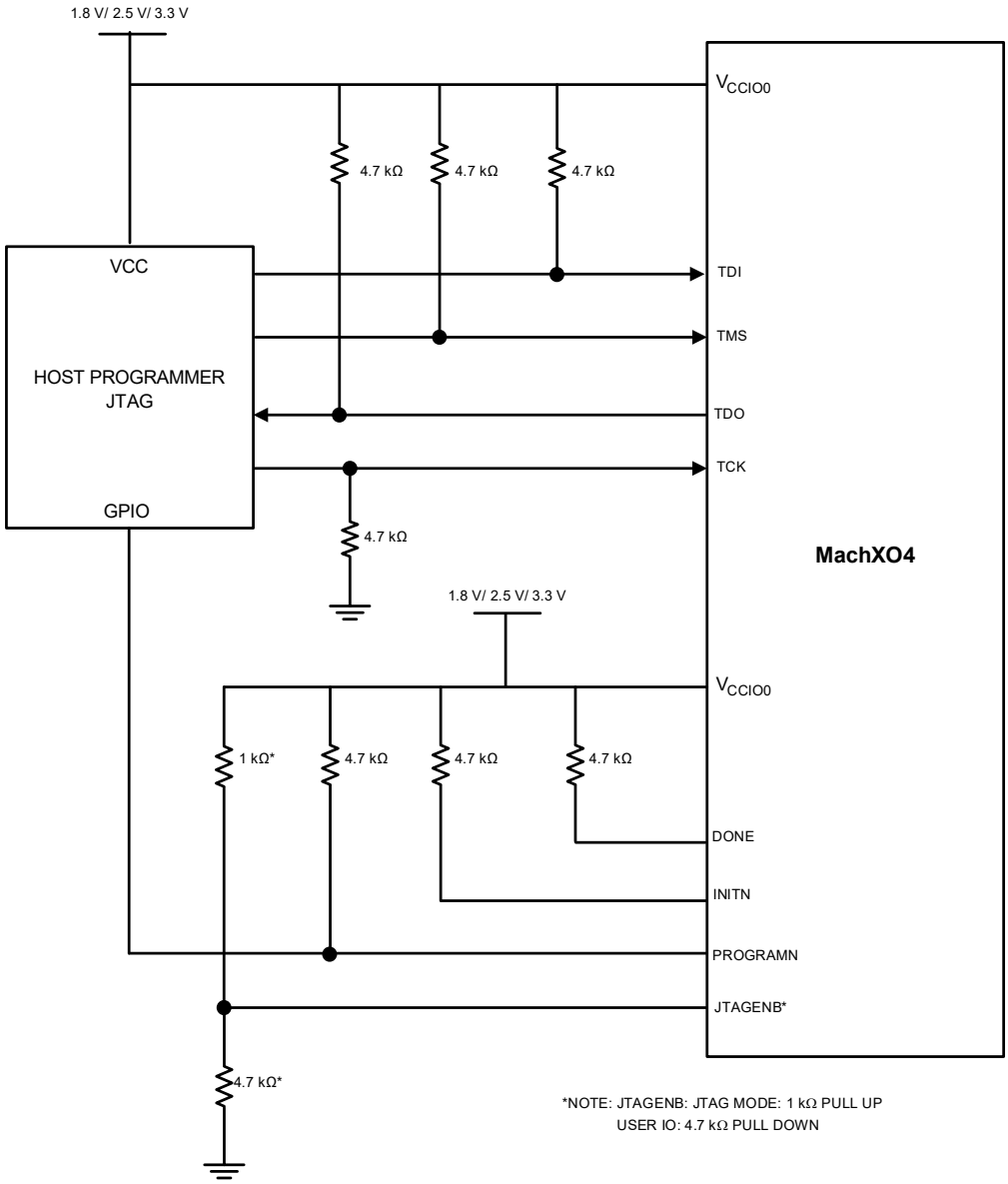


Figure 5.1. Typical Connections for Programming SRAM or Internal Flash via JTAG

JTAG Pull Resistors

Active JTAG lines use push-pull drivers and do not rely on pull-ups to set a high logic level. Pull resistors are only necessary when the JTAG interface is disconnected or tri-stated. They prevent inputs from floating and oscillating, which avoids excessive power draw and accidental TAP controller activation.

Either standard 4.7kΩ or 10kΩ resistors are ideal for TMS and TDI. For tight layouts with high crosstalk, 4.7kΩ is preferred over 10kΩ due to better noise immunity.

A lower-value 2.2kΩ pull-down resistor on TCK is recommended to increase crosstalk immunity to the sensitive clock line.

A pull-up resistor on TDO is optional due to TDO typically connecting to another TDI in a chain or to the TDI of the JTAG controller, each of which should include a pull-up resistor on its input.

JTAG Signal Integrity

For best signal integrity, it is recommended to add a source series termination resistor close to the driver of TDO (and TCK if buffered on the PCB). Tune the combined output impedance of the driver plus resistor to equal the characteristic impedance of the transmission line (PCB or wires). Often a value from 22Ω to 33Ω works well.

The layout should feature extra spacing on each side of the TCK signal to reduce crosstalk into this sensitive net; the distance from the edge of the TCK trace to any adjacent trace should be at least three times the width of the TCK trace.

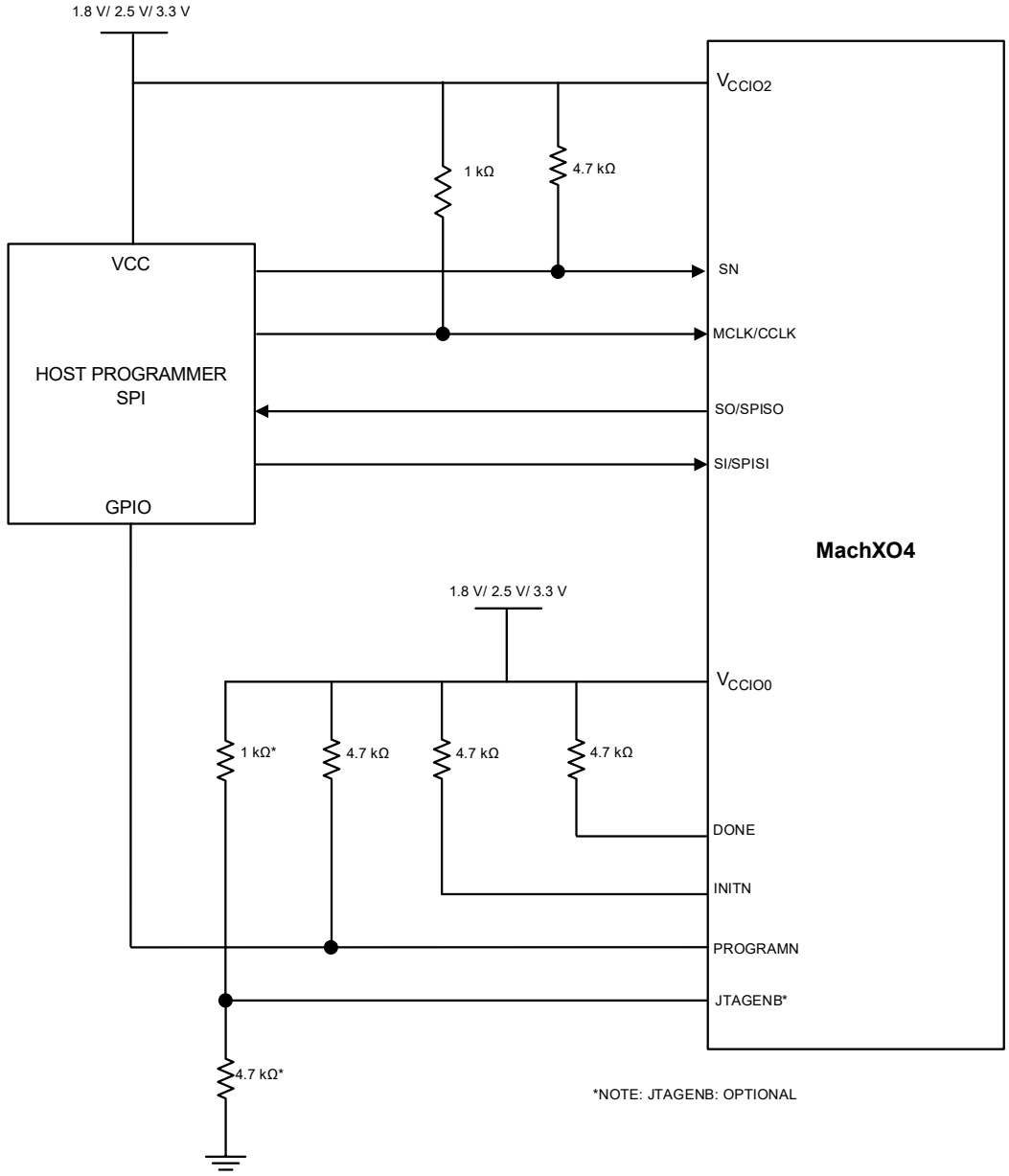


Figure 5.2. Typical Connections for Programming SRAM or Internal Flash via SSPI

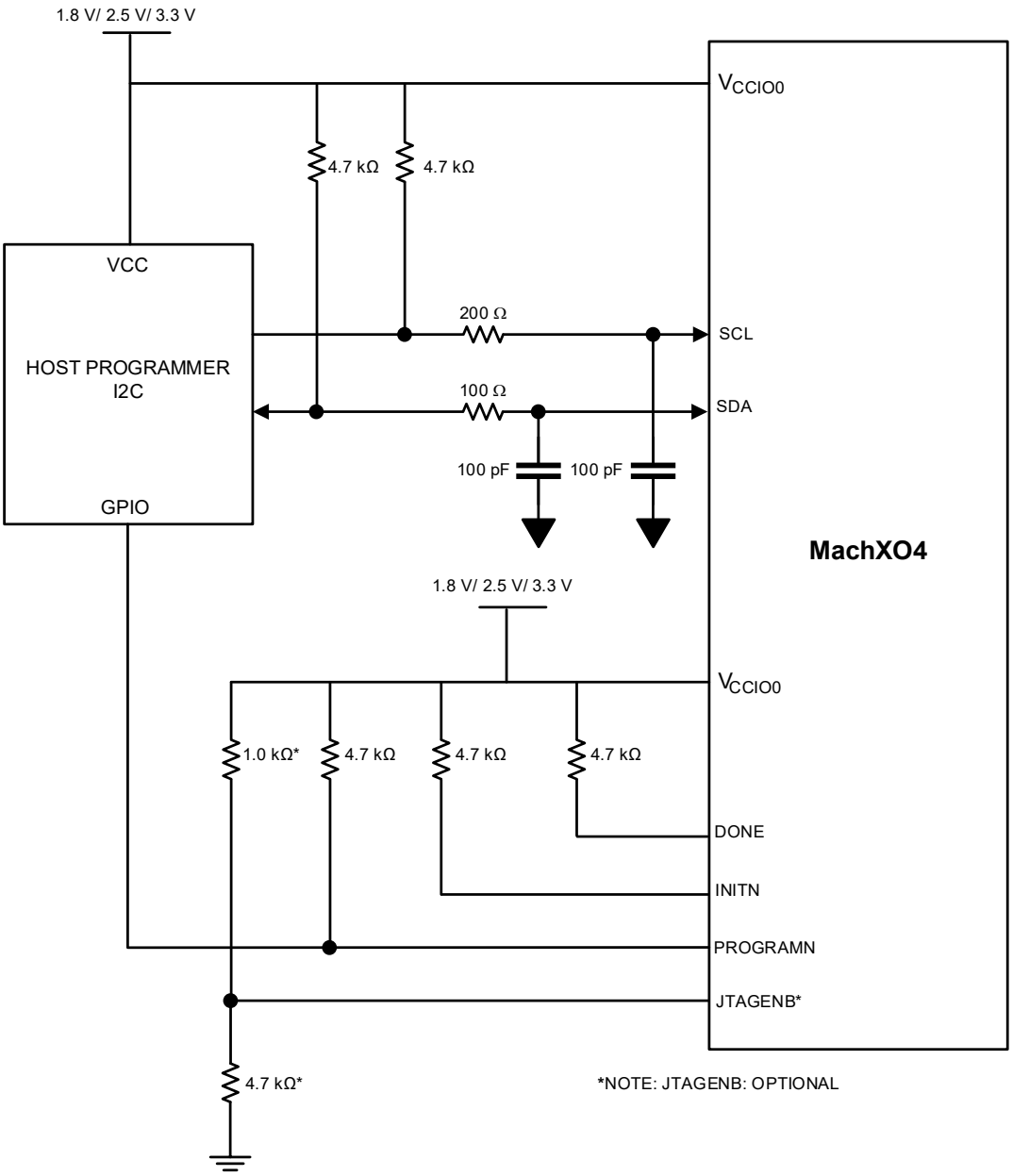


Figure 5.3. Typical Connections for Programming SRAM or Internal Flash via I2C

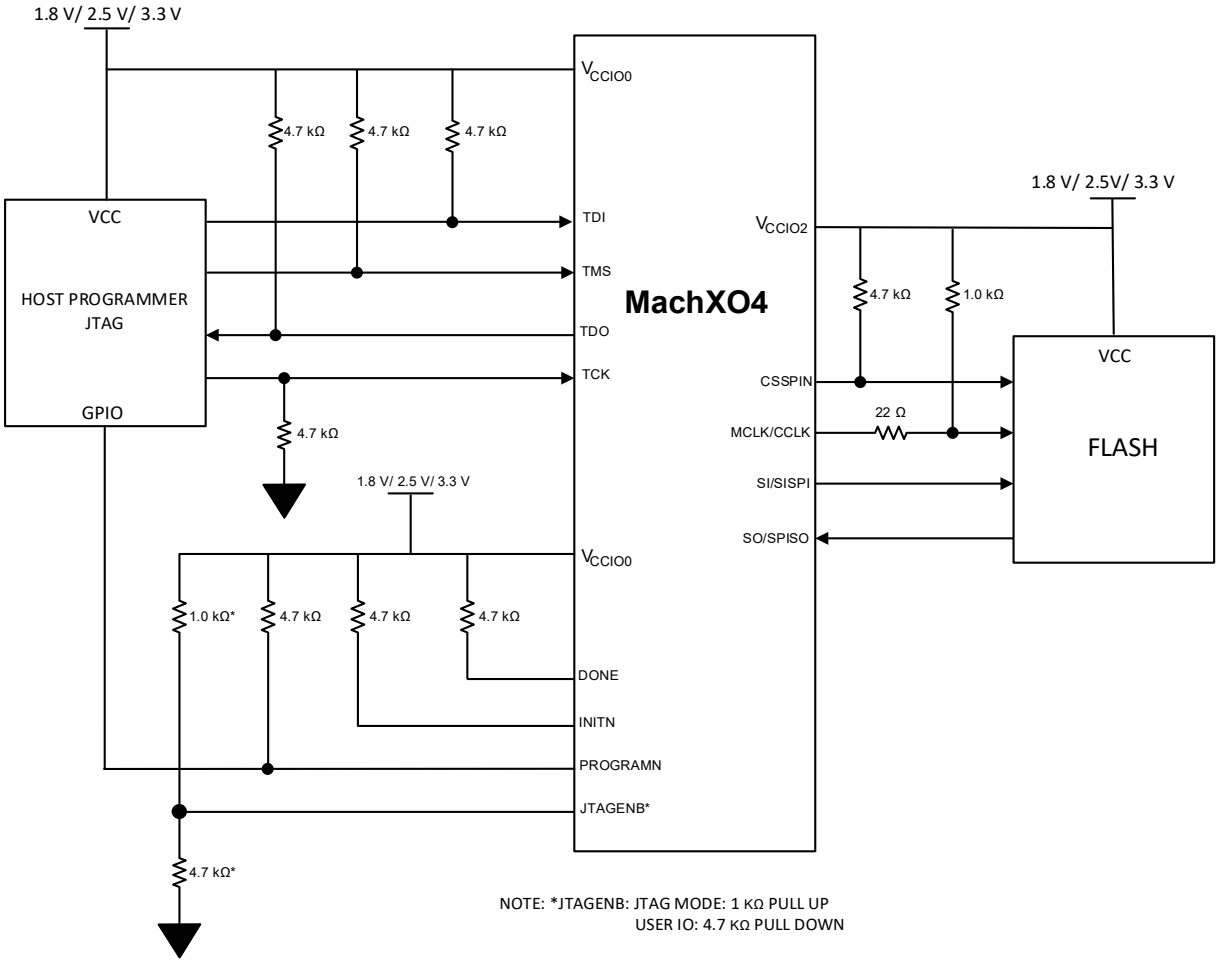


Figure 5.4. Typical Connections for Programming External Flash via JTAG

6. Controller SPI (MSPI)

When configuring from an external SPI Flash:

- The SPI Flash VCC and the MachXO4 device V_{CCIO2} must be at the same voltage level.
- Ensure the SPI Flash V_{CC} is within its recommended operating range. The SPI Flash should be supported in Lattice Radiant Programmer. To view the list of supported devices, open Lattice Radiant Programmer, select the **Help** menu, then search for **SPI Flash support**.
- For SPI Flash devices not listed under **SPI Flash Support**, the custom flash option may enable compatibility with unsupported devices.

7. PROGRAMN Initial Power Considerations

The MachXO4 PROGRAMN pin may be used as a general-purpose I/O in user run mode; however, it is recommended to use other GPIOs instead of PROGRAMN and JTAG pins for general-purpose I/O. The PROGRAMN pin becomes a general-purpose I/O only after the configuration bitstream is loaded. When power is applied to the MachXO4 device, the PROGRAMN input initially functions as PROGRAMN. It is critical that any signal input to the PROGRAMN exhibit high-to-low transition period longer than the time from V_{CC} (minimum) to INITN rising edge. Transitions faster than this period may prevent the MachXO4 from becoming operational. Refer to the description of PROGRAMN in the MachXO4 Programming and Configuration User Guide (FPGA-TN-02393).

8. Pinout Considerations

The MachXO4 device supports many applications with high-speed interfaces. These include various rule-based pinouts that must be understood before implementing the PCB design. Pinout selection should be based on a clear understanding of the FPGA fabric's interface building blocks, including IOLOGIC blocks such as DDR, clock resource connectivity, and PLL usage. Refer to Implementing High-Speed Interfaces with MachXO4 Devices (FPGA-TN-02410) for rules pertaining to these interface types.

8.1. Differential Pair Pin Connections

Differential pairs must use pin name pairs ending in either A and B or C and D. The positive side of a differential pair must connect to pins ending in A or C, and the negative side must connect to pins ending in B or D.

Examples

- PT23A DIFF_SIGNAL1+
- PT23B DIFF_SIGNAL1-
- PT23C DIFF_SIGNAL2+
- PT23D DIFF_SIGNAL2-

9. sysI/O

The MachXO4 device provides flexibility to configure each I/O according to user requirements. These pins can be configured as input, output, or tri-state. Additionally, attributes such as PULLMODE, CLAMP, HYSTERESIS, VREF, OPENDRAIN, SLEWRATE, DIFFRESISTOR, TERMINATION, and DRIVE STRENGTH can be set. Refer to the MachXO4 sysIO User Guide (FPGA-TN-02398) for more information.

For PULLMODE, pull-up and pull-down resistors can be configured. These resistors operate using a constant current with the following values:

Table 9.1. Weak Pull-up/Pull-down Current Specifications

	Parameter	Condition	Min	Max	Unit
Pull-up	I/O weak pull-up resistor current	0 ≤ VIN ≤ 0.7 × VCCIO	–26	–309	µA
Pull-down	I/O weak pull-down resistor current	VIL (max) ≤ VIN ≤ VCCIO	30	305	µA

These buffers are arranged around the periphery of the device in groups referred to as banks. Each bank is capable of supporting multiple I/O standards. Single-ended output buffers, ratioed input buffers (LVTTL, LVCMOS), differential (LVDS) input buffers are powered using I/O supply voltage (V_{CCIO}). Each sysI/O bank has its own V_{CCIO}.

There are three types of sysI/O buffer pairs:

- **Left and Right sysI/O Buffer Pairs**
  The sysI/O buffer pairs in the left and right banks of the device consist of two single-ended output drivers and two single-ended input buffers (for ratioed inputs such as LVCMOS and LVTTL). The I/O pairs on the left and right of the devices also have differential input buffers. The selective I/O pairs of Bank 3 support I3C dynamic pull up capability on MachXO4 RoT devices only.

- **Bottom sysI/O Buffer Pairs**
  The sysI/O buffer pairs in the bottom bank of the device consist of two single-ended output drivers and two single-ended input buffers (for ratioed inputs such as LVCMOS and LVTTL). The I/O pairs on the bottom also have differential input buffers. Only the I/O on the bottom banks have differential input termination. PCI clamps are available on the bottom I/O bank (Bank 2) of higher-density devices. When PCI clamps are required by the system design, assign these pins to I/O Bank 2. For the clamp characteristic, refer to the IBIS buffer models on the Lattice website or in the Lattice Radiant design software.

- **Top sysI/O Buffer Pairs**
  The sysI/O buffer pairs in the top bank of the device consist of two single-ended output drivers and two single-ended input buffers (for ratioed inputs such as LVCMOS and LVTTL). The I/O pairs on the top also have differential I/O buffers. Half of the sysI/O buffer pairs on the top edge have true differential outputs which support LVDS output buffers. When using LVDS outputs, connect a 2.5 V or 3.3 V supply to the Bank 0 V_{CCIO} supply rails. Refer to the MachXO4 sysIO User Guide (FPGA-TN-02398) for more information on this.

9.1. Typical I/O Behavior during Power-up

The default configuration of the I/O pins in a blank device is tri-state with a weak pull-down to GND (some pins such as PROGRAMN and the JTAG pins have weak pull-up to V_{CCIO} as the default functionality). The I/O takes on the user-configured settings only after a proper download/configuration.

10. Clock Inputs

The MachXO4 device provides certain pins for use as clock inputs in each I/O bank. These pins are shared and can alternately be used for general purpose I/O.

When these pins are used for clocking purposes, you need to pay attention to minimize signal noise on these pins.

These shared clock input pins, typically named GPLL and PCLK, can be found under the Dual Function column of the pin-list .csv file. High-speed differential interfaces (such as MIPI) received by the FPGA must route their differential clock pair into a pair of inputs that support differential clocking, labeled PCLKTx_y (+true) and PCLKCx_y (-complement).

Note: For single-ended I/Os, use only PCLKT pins as primary CLK pads.

When providing an external reference clock to the FPGA, ensure that the oscillator's output voltage to the FPGA does not exceed the bank's voltage. Good power supply decoupling of the clock oscillator is required to reduce clock jitter. A typical bypassing circuit is shown in Figure 10.1.

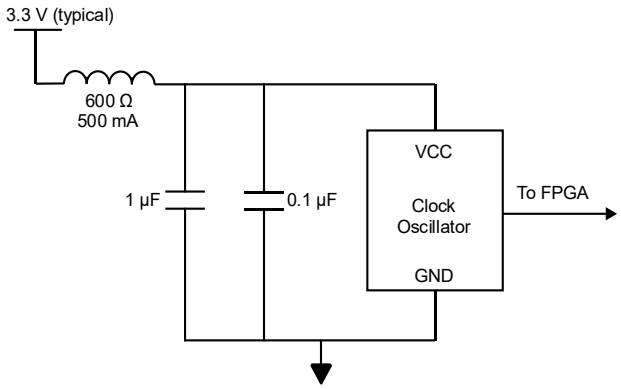


Figure 10.1. Clock Oscillator Bypassing

For differential clock inputs to banks with a V_{CCIO} voltage of 1.5 V or lower, it is recommended to use an HCSL oscillator to keep the clock voltage less than or equal to the bank's V_{CCIO}. An LVDS oscillator can also be used if AC is coupled and then DC is biased at half the VCCIO voltage. Example dual footprint design supporting HCSL and LVDS is shown below in Figure 10.2

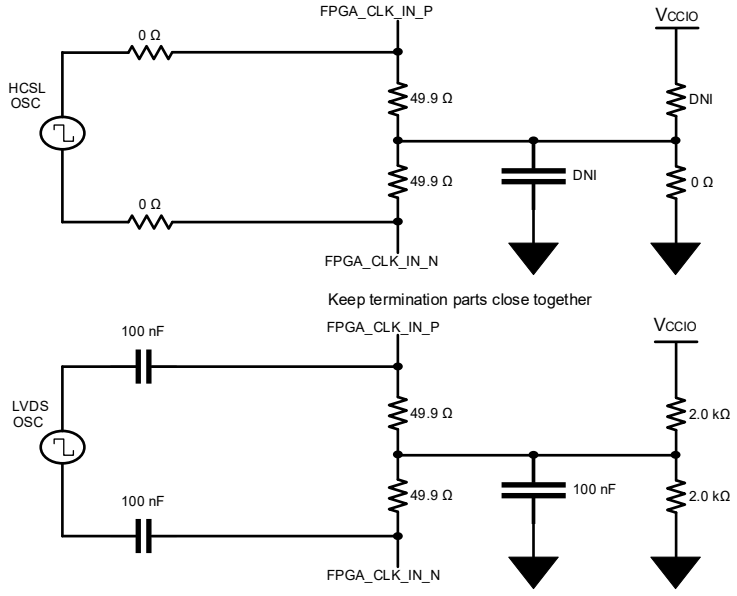


Figure 10.2. PCB Dual Footprint Supporting HCSL and LVDS Oscillators

10.1. PLL Reference Clock Locking

Reference clocks for PLLs must be stable before the PLL comes out of reset to guarantee proper PLL locking. PLLs should be held in reset using the PLL block's RST signal until the PLL's REFCLK signal is stable. See the Checklist section**.** The PLL reset procedure is usually required when an external oscillator or clock source becomes enabled or stable after the FPGA exits Power-On-Reset (POR). An example of a clock oscillator with a controlled enable pin is shown in Figure 10.3.

Note: External board oscillators typically require 5 to 10 ms for their outputs to stabilize after being enabled. Check the oscillator's data sheet for the exact number.

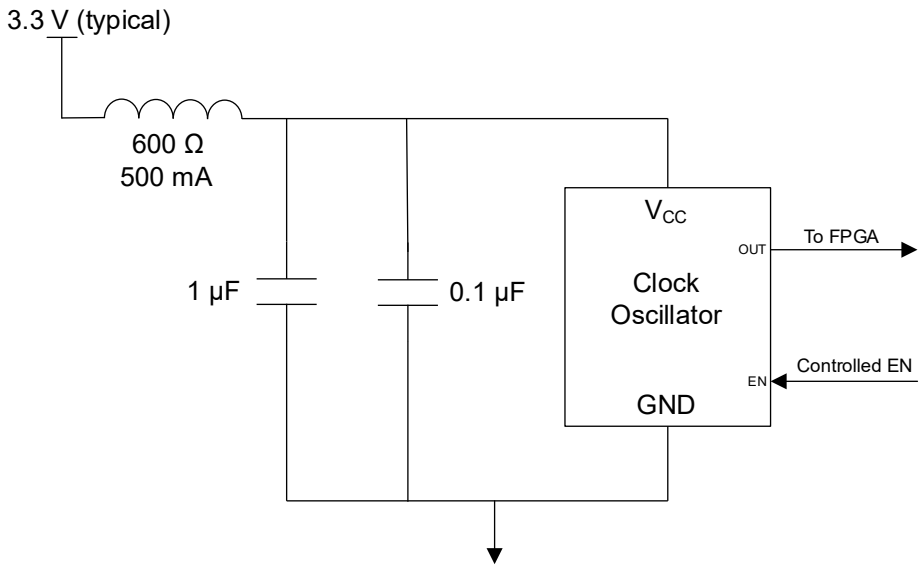


Figure 10.3. Clock Oscillator with Controlled Enable Pin

11. Issue: GPIO Input(s) Prevents Powering Down the FPGA

For HC and ZC devices where the design involves V_{CC} and bank V_{CCIOx} voltages that are the same (3.3 V or 2.5 V) and connected together, careful design consideration must be followed to avoid the FPGA not powering down fully and left operating in an undefined state.

Note: Chip failures can occur when the datasheet input current limits are exceeded.

11.1. GPIO Input Current Leakage Pathway

The FPGA is powered on, and the bit-stream program input CLAMPS ON.

While the FPGA powers down, the external circuit continues to drive input pins.

As the FPGA V_{CC} and V_{CCIOx} voltages drop, the GPIO input pins allow external devices to drive reverse current into the FPGA via the on-CLAMPs, and this current appears at the V_{CCIOx} pins, which are connected to V_{CC}, keeping the V_{CC} voltage high enough for the input CLAMPs to remain active.

Other devices, besides the FPGA, can be connected to the V_{CC} rail, with each device drawing current from the FPGA. As a result, the FPGA can pass enough reverse current to cause internal burnouts or failures to occur quickly or gradually, depending on the overcurrent of each pin and the number of pins involved.

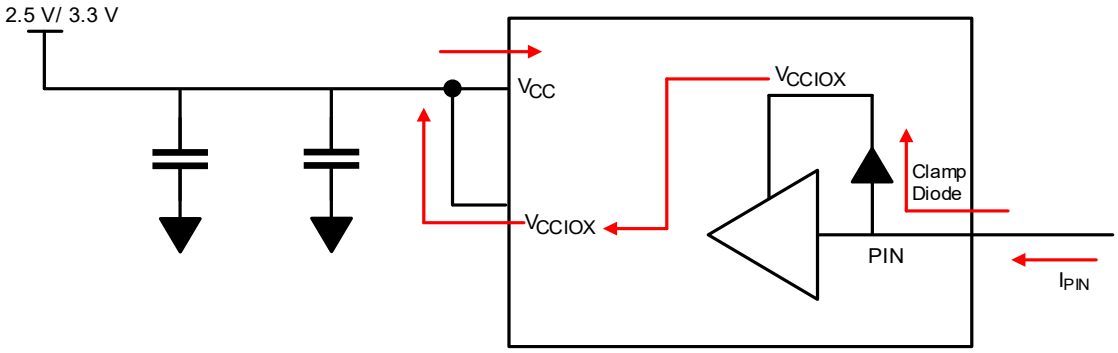


Figure 11.1. Potential Current Path for Powered Down FPGA with Driven Input

11.2. Workarounds

Workaround 1

- Turn off any external devices connected to the FPGA that are operating ≥ 2.5 V at the same time as the FPGA.

Workaround 2

- Configure software to keep GPIO CLAMPS OFF in the bitstream when CLAMPS are not required.

Workaround 3

- Ensure that external circuits do not exceed the datasheet I/O pad current limits for banks operating at ≥ 2.5 V.
- In each bank, the current should not exceed n × 8 mA. Where **n** represents the number of I/O pads in between two consecutive power pins. See below scenarios.
  - V_{CCIO} – I/O_1 – I/O_2 – I/O_x – V_{CCIO}
  - GND – I/O_1 – I/O_2 – I/O_x – GND
  - V_{CCIO} – I/O_1 – I/O_2 – I/O_x – GND

  The I/O groupings can be found in the pin tables generated by the Lattice Radiant software.

Example: Limit the pin current by connecting a series resistor to an FPGA GPIO input.

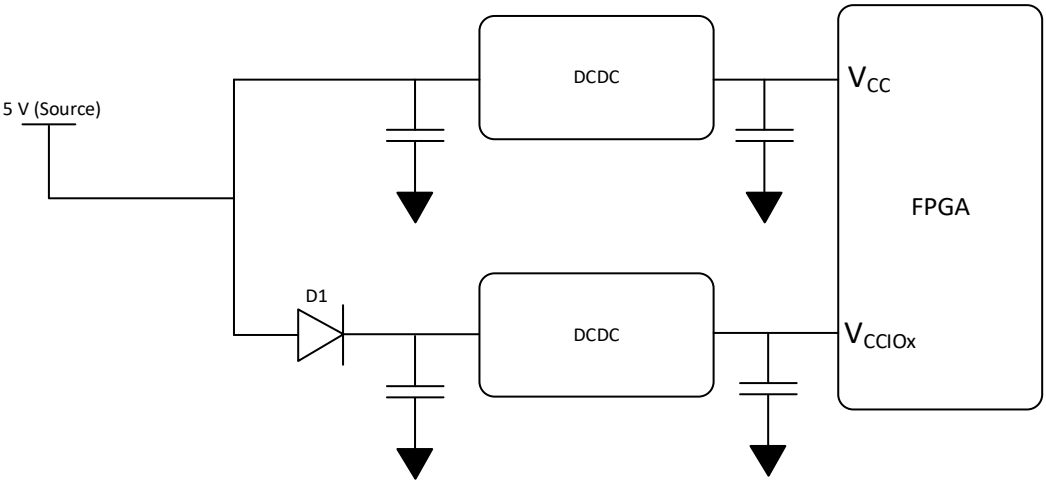
Most non-high-speed designs work well with a 200 Ω to 1 kΩ series resistor.

$$Math: R \times C \times 2.3\,Tau = Trise / Tfall$$

$$200\ \Omega\ series\ resistor\ at\ GPIO\ input \times 10\ pF\ etch\ and\ pin\ capacitance \times 2.3\,Tau = 4.6\ ns\ Trise / Tfall$$

Workaround 4

- For V_{CCIO}, use a separate voltage regulator with a diode (D1) connecting the voltage source to the input.



12. Layout Recommendations

A good design from a schematic should also reflect a good layout for the system design to work without any issues with noise or power distribution. Below are some of the recommended layouts in general.

1. All power should come from power planes. This is to ensure good power delivery and thermal stability.
2. Each power pin has its own decoupling capacitor, typically 100 nF, that should be placed as close as possible to each other.
3. The placement of analog circuits must be away from digital circuits or high switching components.
4. High-speed signals should have a clearance of five times the trace width of other signals.
5. High-speed signals that transition from one layer to another should have a corresponding transition ground if both reference planes are grounded. If the reference on the other layer is a V_{CC} plane, then a stitching capacitor should be used (ground to V_{CC}).

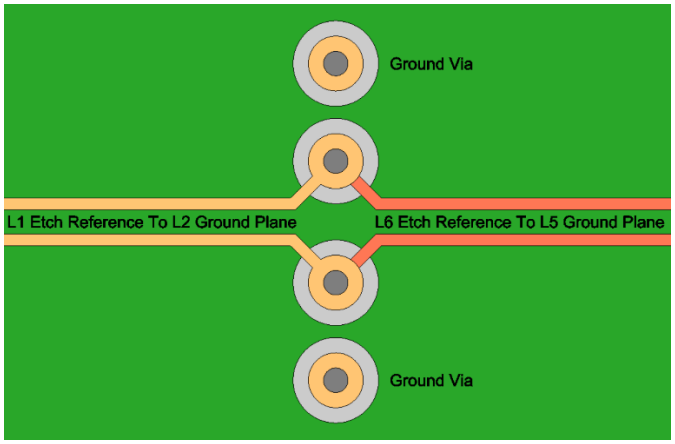


Figure 12.1. Ground Vias Implementation

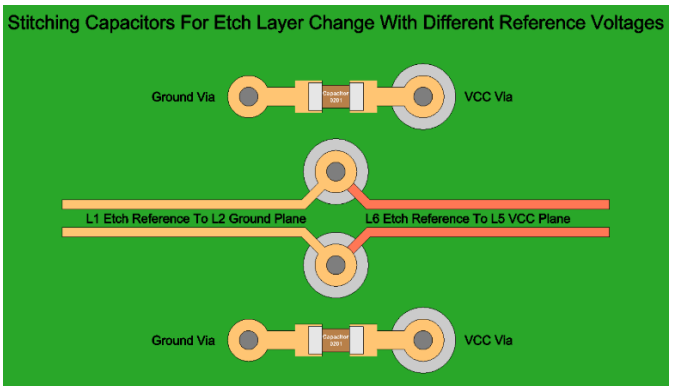


Figure 12.2. Stitching Vias Implementation

6. High-speed signals have a corresponding impedance requirement; calculate the necessary trace width and trace gap (differential gap) according to the desired stack-up. Verify trace dimensions with the PCB vendor.
7. For differential pairs, be sure to match the length as closely as possible. A good rule of thumb is to match up to ±5 mils.

For further information on layout recommendations, refer to:

- PCB Layout Recommendations for BGA Packages (FPGA-TN-02024)
- PCB Layout Recommendations for Leaded Packages (FPGA-TN-02160)

13. Simulation and Board Measurement of Critical Signals

To ensure a design is reliable and will have high manufacturing yield, critical signals should be simulated during the design phase and then measured on the PCB assembly to verify proper function.

13.1. Critical Signals

Signals sensitive to Signal Integrity (SI) degradation are considered critical signals which require extra design and verification attention.

Typical critical signals include:

- Differential Pairs (LVDS, MIPI, and the like)
- Clocks (Oscillator Inputs, Output Clocks)
- Data with embedded clocks
- Interrupts (Edge Triggered)
- Logic signals traveling long distances requiring termination

13.2. Simulation

Lattice Semiconductor supplies an IBIS (I/O Buffer Information Specification) file to be used with simulation tools. Popular simulations tools include:

- HyperLynx
- Sigrity
- SpectraQuest
- Micro-Cap (Free)

Most SI simulation tools are expensive and often have recurring subscription pricing. The expensive tools can import board design files and supply accurate simulations which include crosstalk and other SI degrading effects.

Free IBIS tools (for example Micro-Cap) can supply useful basic simulations, but take extra effort to set up SI effects for multiple signals with different transmission line lengths, lossy transmission lines, and crosstalk.

Simulation results should be used to optimize each critical signal for best signal integrity:

- Define output pin drive strength.
- Define output pin slew rate.
- Define output pin termination design (ex. output series termination resistor value).
- Define setting of internal pin pull-up and pull-down resistors.
- Improve PCB layout.

13.3. Board Measurements

Critical signals should be measured on the actual PCB assembly using an oscilloscope. Verify proper signaling function and signal integrity (that is, eye diagram, SI parameters).

Measurement results should be used to optimize each critical signal for best signal integrity:

- Adjust output pin drive strength.
- Adjust output pin slew rate.
- Adjust output pin termination design (ex. output series termination resistor value).
- Adjust the setting of internal pin pull-up and pull-down resistors.

Specification compliance testing is recommended for popular signaling methods (ex. USB, MIPI).

14. SSO (Simultaneous Switching Output) Design Check

Users should verify designs that will not have functional failures due to SSO voltage drops (sometimes called SSO Noise, Ground Bounce, or Power Bounce).

SSO voltage drops are mainly caused by package inductance combined with dynamic switching current causing Ldi/dt voltage drops.

The Lattice SSO Tool should be used to provide SSO voltage drop estimates.

14.1. SSO Failures – Each of the following can lead to SSO failures

1. Many simultaneous switching outputs in the same I/O bank.
   The more simultaneous switching outputs in a bank the greater the 'di' current, and thus greater Ldi/dt voltage drops.
2. I/Os slew rates set to FAST (and sometimes MEDIUM).
   Faster slew rates reduce the 'dt' time, and thus increase the Ldi/dt voltage drops.
3. I/Os output current set high (ex. 8mA – 16mA).
   The greater the I/O output current the greater the 'di' current, and thus greater Ldi/dt voltage drops.
4. I/Os capacitive loading is relatively high (especially > 15pF)
   High capacitance loading increases the 'di' current, and thus increases Ldi/dt voltage drops.
5. I/O Banks with low voltage rails (ex. LVCMOS 1.0V – LVCMOS 1.5V) have small voltage margins and are more susceptible to Ldi/dt ground & power violations.

14.2. SSO Mitigations

1. Split up simultaneous switching outputs into multiple banks (where timing permits.)
   The fewer simultaneous switching outputs in a bank the lower the 'di' current, and thus lower Ldi/dt voltage drops.
2. Reduce I/O slew rates to MEDIUM or even better SLOW if timing allows.
   The increase in slew time increases ‘dt’ and thus reduces Ldi/dt voltage drops.
3. Reduce I/Os output current (ex. 4mA), where timing and signal quality permit.
   Reducing the I/O output current reduces 'di' current, and thus reduces Ldi/dt voltage drops.
4. Reduce I/Os capacitive loading (this usually requires PCB design changes).
   Reducing capacitive loading reduces 'di' current, and thus reduces Ldi/dt voltage drops.
5. Increase I/O Bank voltage rails (this often requires PCB design changes). When above mitigations do not provide enough design margin, then increasing I/O Bank voltage can increase absolute voltage margins and provide enough design margin for reliable operation.

15. Checklist

Table 15.1 Hardware Checklist

	MachXO4 Hardware Checklist Item	OK	N/A
1	**Power Supply**		
1.1	Core Supply VCC at 1.2 V for HE device		
1.2	Core Supply VCC at 2.5 V or 3.3 V for HC device		
1.3	I/O power supply VCCIO[0-5] at 1.2 V to 3.3 V		
1.4	On HC and ZC devices, like power supplies must be tied together. For example, if V_{CCIO} and V_{CC} are both the same voltage, they must also be the same supply.		
1.5	On HE devices, VCC needs to be powered up prior to VCCIO with fast ramp rate applied on V_{CC} and at least 20 ms delay before V_{CCIO} is powered up.		
1.6	Power Estimation		
1.7	Follow the recommended power filtering groups and components in Table 3.1. Recommended Power Filtering Groups and Components.		
1.8	All ground pins need to be connected to the board's ground plane.		
1.9	For the TQFP-144 package, the EPAD pin must be connected to the board ground plane as described in the Ground Pins section.		
1.10	Bank I/O supplies.		
1.11	Connect the unused VCCIOx to a power rail. Do not leave it open.		
1.12	All configurations of V_{CCIO} (Banks 0,2), when used with the configuration interfaces (example: SPI Flash Memory Devices), need to match the voltage specifications.		
2	**Configuration**		
2.1	Configuration options		
2.2	Apply pull-up resistor on PROGRAMN, INITN, and DONE as described in the Configuration Considerations section.		
2.3	Pull-up on SPI mode pins, per Configuration Considerations section.		
2.4	Pull-up on I2C mode pins, per Configuration Considerations section.		
2.5	Ensure the JTAG_EN pin remains accessible on the PCB to allow JTAG port recovery, particularly during development.		
2.6	Apply a pull-up or pull-down resistor to the JTAG_EN pin.		
2.7	Apply pull-down resistor to JTAG TCK as specified in the Configuration Considerations section.		
2.8	Pull-up on TMS, TDI, and TDO.		
2.9	Add a source series termination resistor close to the driver of TDO (and TCK if buffered on the PCB). Tune the combined output impedance of the driver plus resistor to equal the characteristic impedance of the transmission line (PCB or wires). Often a value from 22 Ω to 33 Ω works well.		
2.10	PROGRAMN high-to-low transition time period is larger than the V_{CC} (min) to INITN rising edge time period.		
2.11	The Controller SPI (MSPI) voltage should match V_{CCIO2} voltage.		
3	**I2C Filter**		
3.1	RC filter for I2C bus, per Table 5.1. Default States of the sysCONFIG Pins1.		
4	**I/O pin assignment**		
4.1	Differential pairs must use pin name pairs ending in A and B or C and D. The positive side of a differential pair connects to pins ending in A or C. The negative side of a differential pair connects to pins ending in B or D.		
4.2	True LVDS output pin assignments use Bank 0 with V_{CCIO0} connected to a 2.5 V or 3.3 V supply.		
4.3	PCI clamp available on Bottom Bank 2.		

	MachXO4 Hardware Checklist Item	OK	N/A
4.4	Connect single-ended clock inputs to the FPGA using the PCLKTx_y pins, which support low skew routing throughout the FPGA fabric.		
4.5	Connect differential clock inputs to the FPGA using the PCLKTx_y and PCLKCx_y pins, which support low skew routing throughout the FPGA fabric.		
5	**Miscellaneous**		
5.1	Verify that no GPIO clamp issues exist, as described in the Issue: GPIO Input(s) Prevents Powering Down the FPGA section.		
5.2	Run SSO tool as required per SSO (Simultaneous Switching Output) Design Check section.		
5.3	Run simulations per Simulation and Board Measurement of Critical Signals section.		

References

- MachXO4 web page
- MachXO4 Family Data Sheet (FPGA-DS-02125)
- MachXO4 Programming and Configuration User Guide (FPGA-TN-02393)
- MachXO4 sysIO User Guide (FPGA-TN-02398)
- Implementing High-Speed Interfaces with MachXO4 Devices (FPGA-TN-02410)
- Using Hardened Control Functions in MachXO4 Devices (FPGA-TN-02403)
- Power and Thermal Estimation and Management for MachXO4 Devices (FPGA-TN-02409)
- PCB Layout Recommendations for BGA Packages (FPGA-TN-02024)
- PCB Layout Recommendations for Leaded Packages (FPGA-TN-02160)
- Lattice Radiant FPGA design software
- Lattice Insights for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at https://www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 1.1, September 2026

Section	Change Summary
All	• Updated document title from *MachXO4 Hardware Checklist* to *MachXO4 Family Hardware Checklist*. • Minor editorial fixes.
Abbreviations in This Document	• Added DDR, FPGA, I3C, LVCMOS, LVDS, MIPI, SI, and USB to the list. • Corrected the GPLL acronym from *Global Phase-Locked Loop* to *General Purpose PLL*.
Introduction	• Added terminology definitions for MachXO4 and MachXO4 RoT device references. • Added the ZC device variant to the MachXO4 family description, including its power characteristics, built-in regulator support, and industrial-temperature speed grades.
Power Supply	• Extended Table 2.1. Power Supply Description and Voltage Levels to include the new ZC device as also using the 2.5 V/3.3 V core supply. • Added a Power Regulator Derating section.
Power	• Merged the former *Power section (power sequencing and power estimation)* into the *Power Supply Filtering* section and renamed the combined section Power. • Added a new grounding requirement for the TQFP-144 package, specifying low-inductance EPAD connection using a 1.5 mm ground-via grid. • Added power-up sequencing requirements distinguishing HC/ZC (tied supplies) from HE (VCC-before-VCCIO with a 20 ms minimum delay) under the Power Sequencing section. • Added Table 3.2. Power Supply Ramp Rates, a new ramp-rate specification table (0.01 to 40 V/ms).
Power Supply Filtering	Removed this section and merged to the new Power section.
Configuration Considerations	• Renamed *I2C Primary Port* to *I2C Controller* port in the configuration arbitration priority list. Aligning I2C terminology with the Controller/Target naming. • Added JTAG pull-resistor selection guidance for TMS, TDI, TCK, and TDO. • Added JTAG signal-integrity guidance, including a series termination value and a TCK trace-spacing recommendation.
True-LVDS Output Pin Assignments	Removed the *True-LVDS Output Pin Assignments* section and merged its guidance into the new Top sysI/O Buffer Pairs description under the sysI/O section.
PCI Clamp Pin Assignment	Removed the *PCI Clamp Pin Assignment* section and merged its guidance into the new *Bottom sysI/O Buffer Pairs* description under sysI/O section.
sysI/O	Added this new section.
Issue: GPIO Input(s) Prevents Powering Down the FPGA	Extended the GPIO-clamp power-down caution to also apply to ZC devices.
Checklist	• Added a new checklist item 1.9 for *TQFP-144 EPAD grounding*. • Added checklist item 1.4, covering the HC/ZC tied-supply requirement and checklist item 1.5, covering the HE VCC-before-VCCIO sequencing with a 20 ms minimum delay. • Added a checklist item 2.9, requiring JTAG TDO/TCK series termination. • Updated the PCI clamp checklist item, identifying Bank 2 as the clamp location.

Revision 1.0, December 2025

Section	Change Summary
All	Initial release

www.latticesemi.com