I/O Interface IP

IP Version: v1.1.0

User Guide

FPGA-IPUG-02292-1.1

December 2025

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This document was created consistent with Lattice Semiconductor’s inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice’s inclusive language FAQ 6878 for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

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Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviations	Definition
AHB	Advanced High-performance Bus
AXI4	Advanced eXtensible Interface 4
CPU	Central Processing Unit
CSR	Control and Status Register
FPGA	Field Programmable Gate Array
GPI	General Purpose Input
GPIO	General Purpose I/O
GPO	General Purpose Output
GUI	Graphical User Interface
IP	Intellectual Property
KiB	Kibibyte (1024 bytes)
I/O	Input/ Output
LSE	Lattice Synthesis Engine
LUT	Look Up Table
PDC	Physical Design Constraint
PLL	Phase-Locked Loop
SoC	System-on-a-Chip

1. Introduction

1.1. Overview of the IP

The I/O Interface IP provides a set of I/O functions that enable access to external modules through standard interfaces such as Advanced High-performance Bus Lite (AHB-Lite) and Advanced eXtensible Interface Lite (AXI4-Lite). This IP supports up to 256 bits of general-purpose input and output ports.

1.2. Quick Facts

Table 1.1. Summary of the I/O Interface IP

IP Requirements	Supported Devices	All
	IP Changes	For a list of changes to the IP, refer to the I/O Interface IP Release Notes (FPGA-RN-02084).
	Supported User Interface	AHB-Lite, AXI4-Lite
Design Tool Support	Lattice Implementation	IP v1.1.0 – Lattice Radiant Software 2025.2
	Synthesis	Lattice Synthesis Engine (LSE) Synopsys® Synplify Pro® for Lattice
	Simulation	For the list of supported simulators, see the Lattice Radiant Software User Guide.

Note:

1. In some instances, the IP may be updated without changes to the user guide. This user guide may reflect an earlier IP version but remains fully compatible with the later IP version. Refer to the IP Release Notes for the latest updates.

1.3. IP Support Summary

Table 1.2. I/O Interface IP Support Readiness

Device Family	Interface	Radiant Timing Model	Hardware Validated
CertusPro™-NX	AHB-Lite	Final	Yes
	AXI4-Lite	Final	No
Certus™-NX MachXO5™-NX Lattice Avant™ Certus™-N2	AHB-Lite	Preliminary	No
	AXI4-Lite	Preliminary	No
CrossLink™-NX MachXO4™	AHB-Lite	Final	No
	AXI4-Lite	Final	No

1.4. Features

Key features of the I/O Interface IP include:

- Supports either AHB-Lite or AXI4-Lite interface to I/O Bus Interface.
- Supports 8, 16, or 32-bit data access for the AHB-Lite interface. For the AXI4-Lite interface, the data access is fixed at 32 bits.
- Supports up to 256 bits of general purpose input and output ports that can be programmed and sampled.

1.5. Licensing and Ordering Information

The I/O Interface IP is provided at no additional cost with the Lattice Radiant software.

1.6. Hardware Support

Refer to the Example Design section for more information on the boards used.

1.7. Minimum Device Requirements

There are no minimum device requirements for the I/O Interface IP.

1.8. Naming Conventions

1.8.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.8.2. Signal Names

- _n are active low, asserted when value is logic 0.
- _i are input signals.
- _o are output signals.

2. Functional Description

2.1. IP Architecture Overview

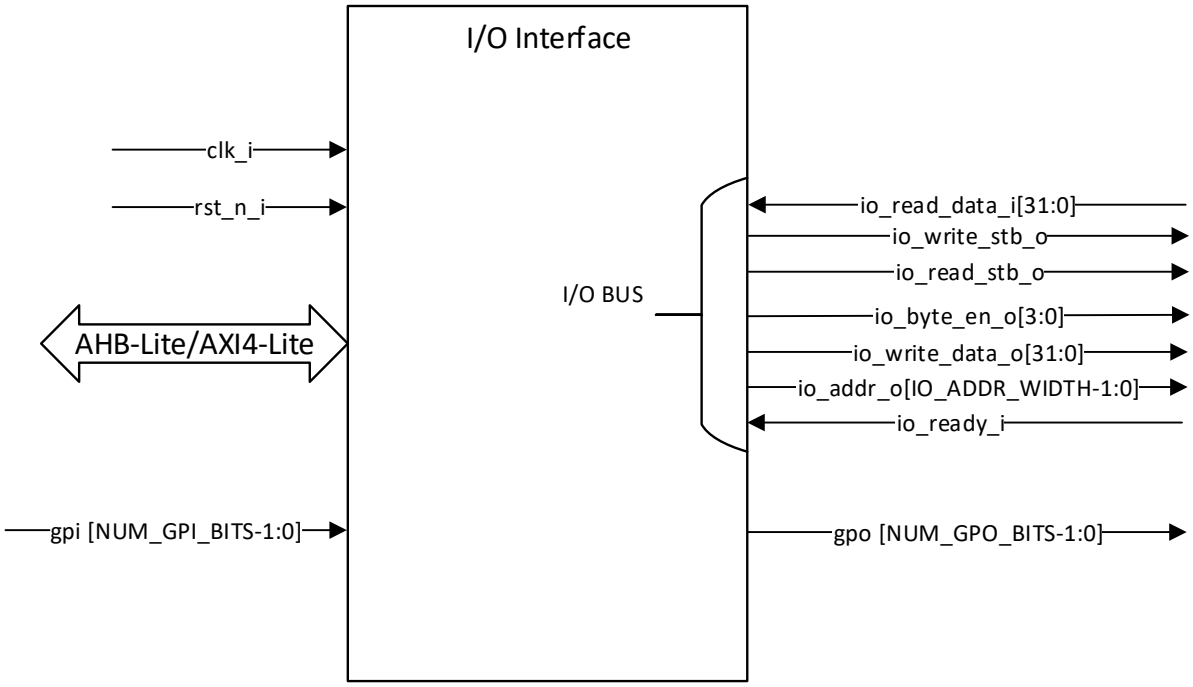


Figure 2.1. I/O Interface Block Diagram

2.2. Functional Overview

The Interface attribute functions as memory interface when accessing valid register addresses which can program the GPO registers and read the GPI registers. In addition, it can function as a bridge to interface the I/O bus, given that the registers being accessed are valid I/O addresses.

2.3. Clocking

The clock source of the I/O Interface IP is synchronous to clk_i.

2.4. Reset

There is one hardware reset for the I/O Interface IP.

rst_n_i: An asynchronous active low reset.

Note: This asynchronous reset is synchronized with the system clock. Upon the de-assertion of rst_n_i, three (3) clock cycles are needed to propagate the reset in the IP core blocks.

2.5. User Interfaces

Table 2.1 shows the user interfaces and supported protocols.

Table 2.1. User Interfaces and Supported Protocols

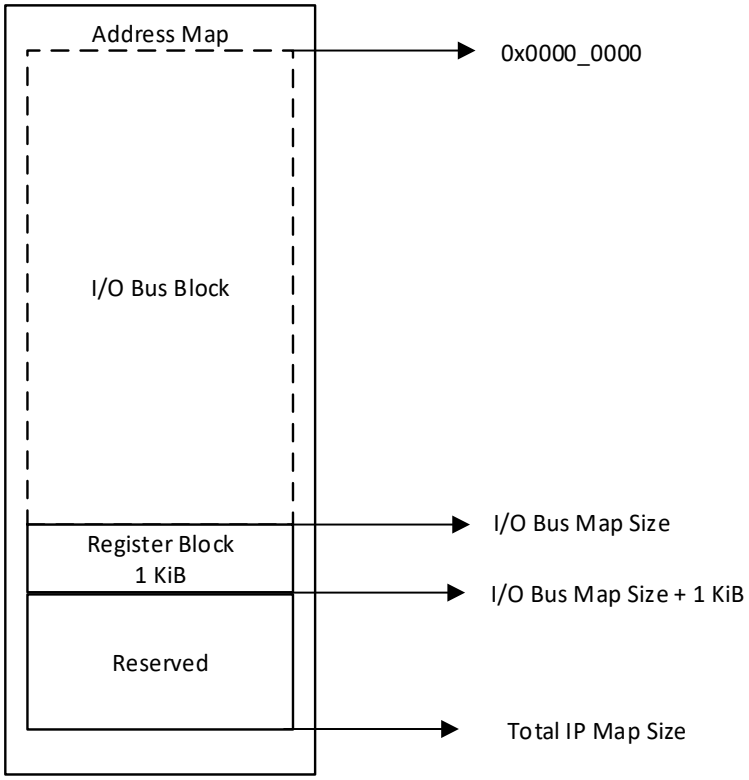
Interface	Supported Protocols	Description
I/O Bus	AHB-Lite	The following describes the read and write transactions of the

Interface	Supported Protocols	Description
		AHB-Lite interface given that there is no wait states in I/O bus interface: • Write transaction has three wait states; • Read transaction has two wait states. For more information about AHB-Lite APB interface and the timing diagrams, refer to the AMBA 3 AHB-Lite Protocol Specification.
	AXI4-Lite	For more information about AXI4-Lite interface and the timing diagrams, refer to the AMBA AXI Protocol Specification.
CSR Interface	AHB-Lite	The following describes the read and write transactions of the AHB-Lite interface: • Write transaction has one wait state; • Read transaction has one wait state. For more information about AHB-Lite APB interface and the timing diagrams, refer to the AMBA 3 AHB-Lite Protocol Specification.
	AXI4-Lite	For more information about AXI4-Lite interface and the timing diagrams, refer to the AMBA AXI Protocol Specification.

2.5.1. Address Space Mapping

The I/O bus address starts at 0x0000_0000 up to the configured I/O bus map size. The size of the register block is 1 KiB. The unused addresses in the register block up to the Total IP Map Size, are treated as reserved, read-only access.

The valid writable block is from the offset, 0x0000_0000, to GPO registers. The valid readable block is from the offset, 0x0000_0000, to IO Bus Map Size, and the range of the GPI registers.



2.6. I/O Bus Transactions

2.6.1. AHB-Lite Transfers

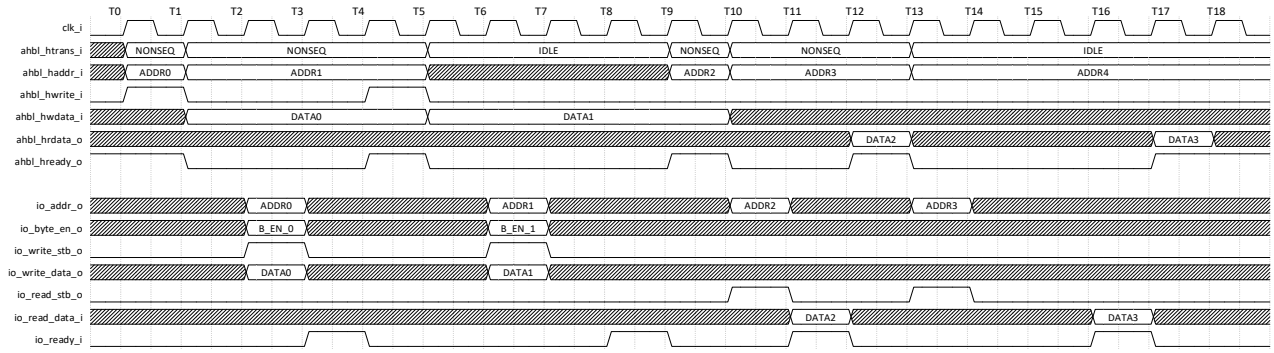


Figure 2.2. AHB-Lite I/O Bus Transfers

Figure 2.2 shows the AHB-Lite I/O Bus transfers.

- T0-T4: Write transfer without wait state
  I/O bus write strobe asserts one cycle after the data phase.
  AHB-Lite ready out signal asserts one cycle after the assertion of I/O bus ready.
- T4: Interface ready for next transfer
- T4-T9: Write transfer with one (1) wait state
- T9: Interface ready for next transfer
- T9-T12: Read transfer without wait state
  I/O bus read strobe asserts one cycle after the address phase.
  AHB-Lite ready out signal asserts one cycle after the assertion of I/O bus ready with the AHB-Lite read data.
- T12: Interface ready for next transfer
- T12-T17: Read transfer with two (2) wait states
- T17-T18: Interface not ready for transfer
  AHB-Lite transfer type signal is in IDLE. Despite AHB-Lite ready out signal being asserted, no transfer proceeds.

2.6.2. AXI4-Lite Transfers

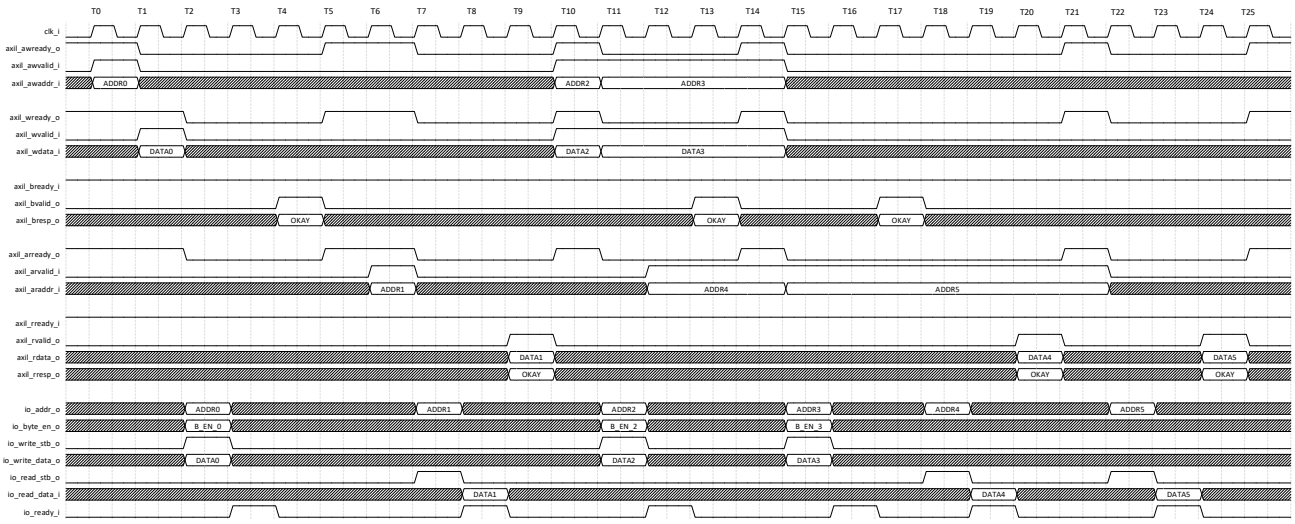


Figure 2.3. AXI4-Lite I/O Bus Transfers

Figure 2.3 shows the AXI4-Lite I/O Bus transfers.

- T0-T4: Single write transfer
  The I/O bus write strobe asserts one cycle after the handshakes of the write address and write data channels.
  AXI4-Lite write response valid asserts one cycle after the assertion of I/O bus ready.
- T5: Interface ready for next transfer
- T6-T9: Single read transfer
  I/O bus read strobe asserts one cycle after the handshake of the read address channel.
  AXI4-Lite read data valid and read response assert one cycle after the assertion of I/O bus ready. Read data is sampled upon the assertion of I/O bus ready.
- T10: Interface ready for next transfer
- T10-T16: Back-to-back write transfer
  After the assertion of AXI4-Lite write response valid, the next write transfer proceeds.
- T12-T24: Back-to-back read transfer
  After the assertion of AXI4-Lite read response and read data valid, the next read transfer proceeds.
- T14-T20: Simultaneous write-read transfer
- Write and read requests assert at the same time. Write transfer has a priority over read transfer. The read address received is stored while the read transfer is pended.
- T15-T17: Write transfer proceeds.
- T18-T20: After the assertion of AXI4-Lite write response valid, interface ready signals remain de-asserted and the previously pending read transfer proceeds.
- T21: Interface ready for the next transfer
- T25: Interface ready for the next transfer

3. IP Parameter Description

The configurable attributes of the I/O Interface IP are shown in the following tables. You can configure the IP by setting the attributes accordingly in the IP Catalog's Module/IP wizard of the Lattice Radiant software.

Wherever applicable, default values are in bold.

3.1. General

Table 3.1. General Attributes

Attribute	Selectable Values	Description
Interface Setting		
Interface	AXI4L, **AHBL**	Selects the interface.
General Purpose Pins Setting		
GPI Enable	Checked, **Unchecked**	Enables General Purpose Input.
Number of GPI Bits	**1**–128	Size of the General Purpose Input Applicable when GPI Enable is Checked.
GPO Enable	Checked, **Unchecked**	Enables General Purpose Output.
Number of GPO Bits	**1**–128	Size of the General Purpose Output Applicable when GPO Enable is Checked.
Address Map Setting		
I/O Bus Map Size (KiB)	**1**–<Maximum Selectable Size> The maximum selectable size is power of 2.	Size of the I/O Bus Note that if the GPI Enable and GPO Enable attributes are unchecked, the maximum selectable size is 4,194,304. Otherwise, the maximum selectable size is 2,097,152.
Total IP Map Size (KiB)	—	Informational only. Specifies the total size of both register space and I/O bus space.

4. Signal Description

This section describes the I/O Interface IP ports.

Table 4.1. Ports Descriptions

Port	Type	Description
System Clock and Reset		
clk_i	Input	System clock
rst_n_i	Input	Active low system reset
AXI4-Lite[1]		
axil_awready_o	Output	AXI4-Lite Write Address Ready Signal The default value of this signal is 1.
axil_awprot_i[2:0]	Input	AXI4-Lite Write Address Privilege and Security Level Signal Not supported.
axil_awvalid_i	Input	AXI4-Lite Write Address Valid Signal
axil_awaddr_i[31 :0]	Input	AXI4-Lite Write Address Signal
axil_wready_o	Output	AXI4-Lite Write Data Ready Signal The default value of this signal is 1.
axil_wvalid_i	Input	AXI4-Lite Write Data Valid Signal
axil_wdata_i[31:0]	Input	AXI4-Lite Write Data Signal
axil_wstrb_i[3:0]	Input	AXI4-Lite Write Data Strobe Signal
axil_bready_i	Input	AXI4-Lite Write Response Ready Signal
axil_bvalid_o	Output	AXI4-Lite Write Response Valid Signal
axil_bresp_o[1:0]	Output	AXI4-Lite Write Response Identification Signal • 2'b00 – Normal access success • 2'b11 – Decode error
axil_arready_o	Output	AXI4-Lite Read Address Ready Signal The default value of this signal is 1.
axil_arprot_i[2:0]	Input	AXI4-Lite Read Address Privilege and Security Level Signal Not supported.
axil_arvalid_i	Input	AXI4-Lite Read Address Valid Signal
axil_araddr_i[31:0]	Input	AXI4-Lite Read Address Signal
axil_rready_i	Input	AXI4-Lite Read Data Ready Signal
axil_rvalid_o	Output	AXI4-Lite Read Data Valid Signal
axil_rdata_o[31:0]	Output	AXI4-Lite Read Data Signal
axil_rresp_o[1:0]	Output	AXI4-Lite Read Data Response Signal • 2'b00 – Normal access success • 2'b11 – Decode error
AHB-Lite[2]		
ahbl_haddr_i[31:0]	Input	AHB-Lite Address Signal
ahbl_hburst_i[2:0]	Input	AHB-Lite Burst Type Signal Only supports single burst transaction which has the value of 3'b000.
ahbl_htrans_i[1:0]	Input	AHB-Lite Transfer Type Signal SEQ and BUSY are not supported. • 2'b00 – IDLE • 2'b10 – NONSEQ
ahbl_hsize_i[2:0]	Input	AHB-Lite Transfer Size Signal. Allowed values for 32-bit data bus are: • 3'b000 – Byte (8-bit) • 3'b001 – Halfword (16-bit) • 3'b010 – Word (32-bit)
ahbl_hwdata_i[31:0]	Input	AHB-Lite Write Data Signal

Port	Type	Description
ahbl_hwrite_i	Input	AHB-Lite Direction Signal If the signal is high, it indicates a write transfer. Otherwise, it is a read transfer.
ahbl_hready_i	Input	AHB-Lite Ready Input Signal
ahbl_hsel_i	Input	AHB-Lite Select Signal
ahbl_hrdata_o[31:0]	Output	AHB-Lite Read Data Signal
ahbl_hready_o	Output	AHB-Lite Ready Output Signal This signal indicates that the transfer is finished and is ready to accept another transfer request. The default value of this signal is 1.
ahbl_hresp_o	Output	AHB-Lite Transfer Response Signal This signal indicates the success or failure of the transfer. When the signal is LOW, it indicates the transfer status is OKAY. Otherwise, it indicates ERROR.
ahbl_hmasterlock_i	Input	AHB-Lite Locked Sequence Transfer Signal Not supported.
ahbl_hprot_i[3:0]	Input	AHB-Lite Protection Control Signal Not supported.
General Purpose Input/Output		
gpi[Number of GPI Bits-1:0]	Input	General Purpose Input The width of this signal is set by the Number of Bits attribute under GPI, NUM_GPI_BITS.
gpo[Number of GPO Bits-:0]	Output	General Purpose Output The width of this signal is set by the Number of Bits attribute under GPO, NUM_GPO_BITS.
I/O Bus		
io_read_stb_o	Output	I/O Bus Read Strobe Signal
io_write_stb_o	Output	I/O Bus Write Strobe Signal
io_addr_o[IO_ADDR_WIDTH-1 :0]	Output	I/O Bus Address Signal The width of this signal is based on the configured I/O bus map size where IO_ADDR_WIDTH = $\log_2$(I/O Bus Map Size).
io_read_data_i[31 :0]	Input	I/O Bus Read Data Signal
io_write_data_o[31 :0]	Output	I/O Bus Write Data Signal
io_byte_en_o[3:0]	Output	I/O Bus Byte Enable Signal
io_ready_i	Input	I/O Bus Data Ready Handshake Signal This signal indicates that the current transaction is done and the I/O bus is ready to receive new transaction.

Notes:

2. AXI4-Lite Interface is selected in the Interface parameter.
3. AHB-Lite Interface is selected in the Interface parameter.

5. Register Description

Table 5.1. Register Access Types

Access Type	Access Type Abbreviation	Behavior on Read Access	Behavior on Write Access
Read-Only	RO	Returns register value.	Ignores write access.
Write-Only	WO	Returns 0.	Updates register value.

Table 5.2. Register Address Map

Offset Address[1]	Register Name	Access Type	Description
0x000-0x00C	GPO	WO	General Purpose Output Registers It is applicable if GPO Enable is checked and depends on the Number of GPO Bits attribute. All unused bits are reserved.
0x010-0x01C	GPI	RO	General Purpose Input Registers It is applicable if GPI Enable is checked and depends on the Number of GPI Bits attribute. All unused bits are reserved.

Note:

1. The register starting offset is I/O Bus Map Size.

5.1. General Purpose Output Register (Address: 0x000)

Table 5.3. General Purpose Output Register

Field	Name	Access	Width	Reset
[31:0]	GPO	WO	32	0x0000

General Purpose Output Register holds the data corresponding to the GPO port.

5.2. General Purpose Input Register (Address: 0x010)

Table 5.4. General Purpose Input Register

Field	Name	Access	Width	Reset
[31:0]	GPI	RO	32	0x0000

General Purpose Input Register holds the data corresponding to the GPI port.

6. Example Design

The I/O Interface example design allows you to compile, simulate, and test the I/O Interface IP on the following Lattice evaluation board:

CertusPro-NX Evaluation Board, with the ordering part number LFCPNX-EVN

6.1. Example Design Supported Configuration

Note: In the table below, ✓ refers to a checked option in the I/O Interface IP example design.

Table 6.1. I/O Interface IP Configuration Supported by the Example Design

I/O Interface IP GUI Parameter	I/O Interface IP Configuration Supported in Example Demo Design
Interface Settings	
Interface	AHBL
General Purpose Pins Setting	
GPI Enable	✓
Number of GPI Bits	4
GPO Enable	✓
Number of GPO Bits	4
Address Map Setting	
I/O Bus Map Size (KiB)	1
Total IP Map Size (KiB)	2 (display-only)

6.2. Overview of the Example Design and Features

The example design discussed in this section is created using the RISC-V MC SoC project template in the Lattice Propel Development Suite. The generated project includes the following components:

- Processor – RISC-V MC with PIC and Timer
- GPIO
- Asynchronous SRAM
- UART – Serial port
- Phase-Locked Loop (PLL)
- Glue Logic

6.3. Example Design Components

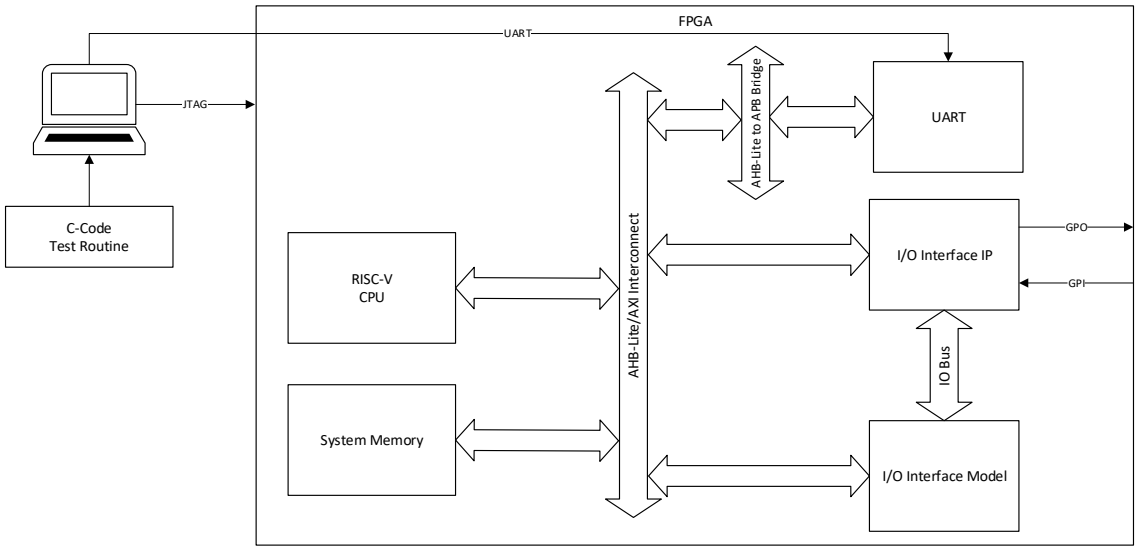
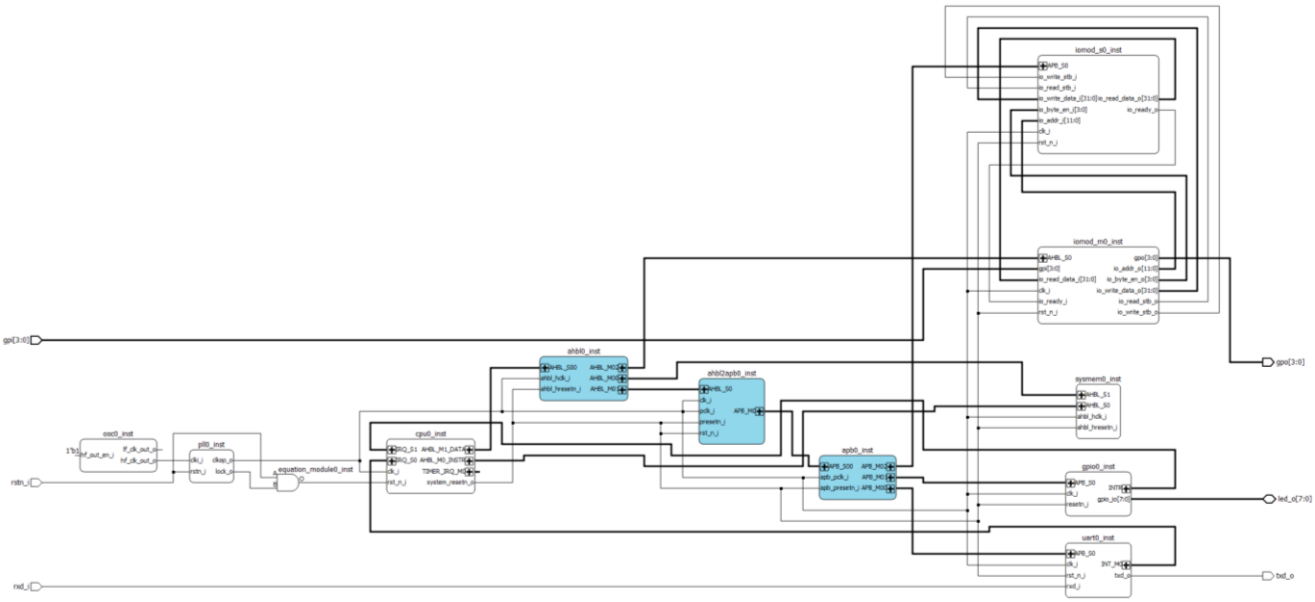


Figure 6.1. I/O Interface Example Design Block Diagram

The I/O Interface example design includes the following blocks:

- RISC-V CPU – Passes the C-Code Test Routing from the system memory to system bus and handles interrupts.
- Memory module – Contains commands to be done for testing.
- System bus – AHB-Lite system bus for transfers between memory and IP.
- I/O Interface IP – the design under test
- I/O Interface model – Communicates with the I/O Interface IP.



6.4. Simulating the Example Design

The Lattice Propel Builder software also has a verification project mode that can be used to generate a simulation environment. The procedure for generating a verification project for the I/O Interface IP is described in the following section.

To simulate the example design, follow these steps:

1. From the SoC project, perform the pre-simulation requirements enumerated in the Verification Project Flow section of the A Step-By-Step Approach to Lattice Propel Application Note (FPGA-AN-02052).
2. Click on the **Switch Verification and SoC Design** icon to switch to the verification project.
3. Reload dut_inst by double clicking on it. The **Reload sbx** window displays, as shown in Figure 6.2. Click **Yes** to continue. Figure 6.3 shows the verification project schematic.

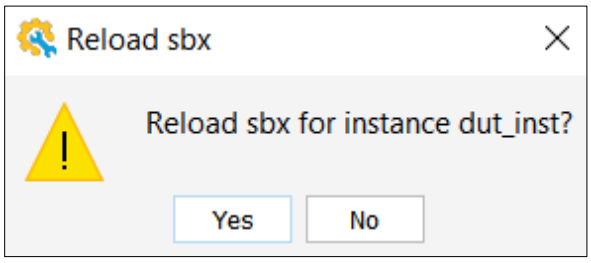


Figure 6.2. Reload sbx

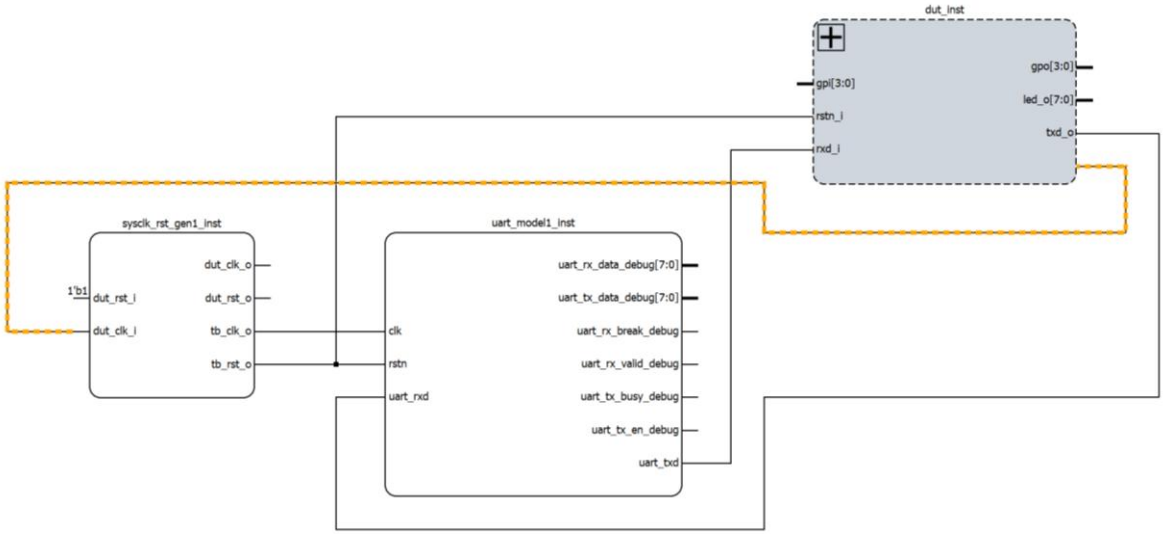


Figure 6.3. Verification Project Schematic

4. Click the **Generate** icon to generate the simulation environment. The testbench files, including scripts for the chosen simulator, file lists, and other files, are generated in the verification folder of the SoC project.
5. To see the full IP simulation behavior for this example design, connect your own I/O Interface model to the IP instance in the generated testbench file, as shown in the following figure and add the I/O Interface simulation model in the generated file list.
6. Click the Launch Simulation icon to run the simulation.

6.5. Hardware Testing

The generated bitstream file in the Radiant Project Flow section of the A Step-By-Step Approach to Lattice Propel Application Note (FPGA-AN-02052) document is downloaded to the CertusPro-NX Versa Evaluation Board through Radiant Programmer. The Reveal analyzer is added to the Radiant software project to verify the output behavior of the IP.

7. Designing with the IP

This section provides information on how to generate the IP using the Lattice Radiant software and how to run simulation and synthesis. For more details on the Lattice Radiant software, refer to the Lattice Radiant Software User Guide.

7.1. Generating and Instantiating the IP

You can use the Lattice Radiant software to generate IP modules and integrate them into the device architecture. The steps below describe how to generate the I/O Interface IP in the Lattice Radiant software.

To generate the I/O Interface IP:

1. Create a new Lattice Radiant software project or open an existing project.
2. In the **IP Catalog** tab, double-click **I/O Interface** of the **Processors_Controllers_and_Peripherals** category under **IP**. The **Module/IP Block Wizard** opens, as shown in Figure 7.1. Enter values in the **Component name** and the **Create in** fields and click **Next**.

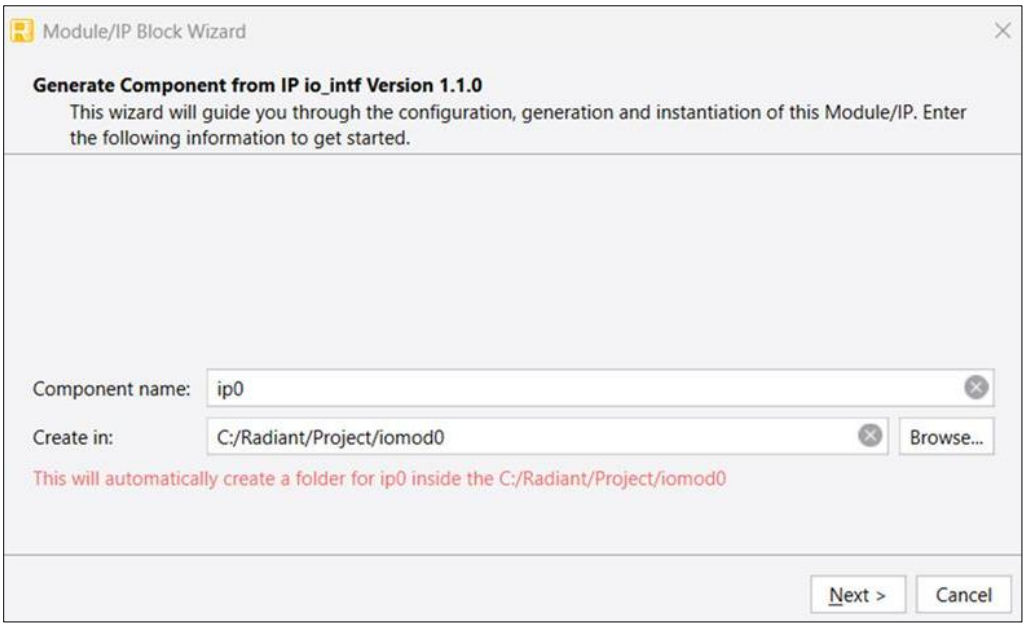


Figure 7.1. Module/IP Block Wizard

3. In the next **Module/IP Block Wizard** window, customize the selected I/O Interface IP using drop-down lists and check boxes. Figure 7.2 shows an example configuration of the I/O Interface IP. For details on the configuration options, refer to the IP Parameter Description section.

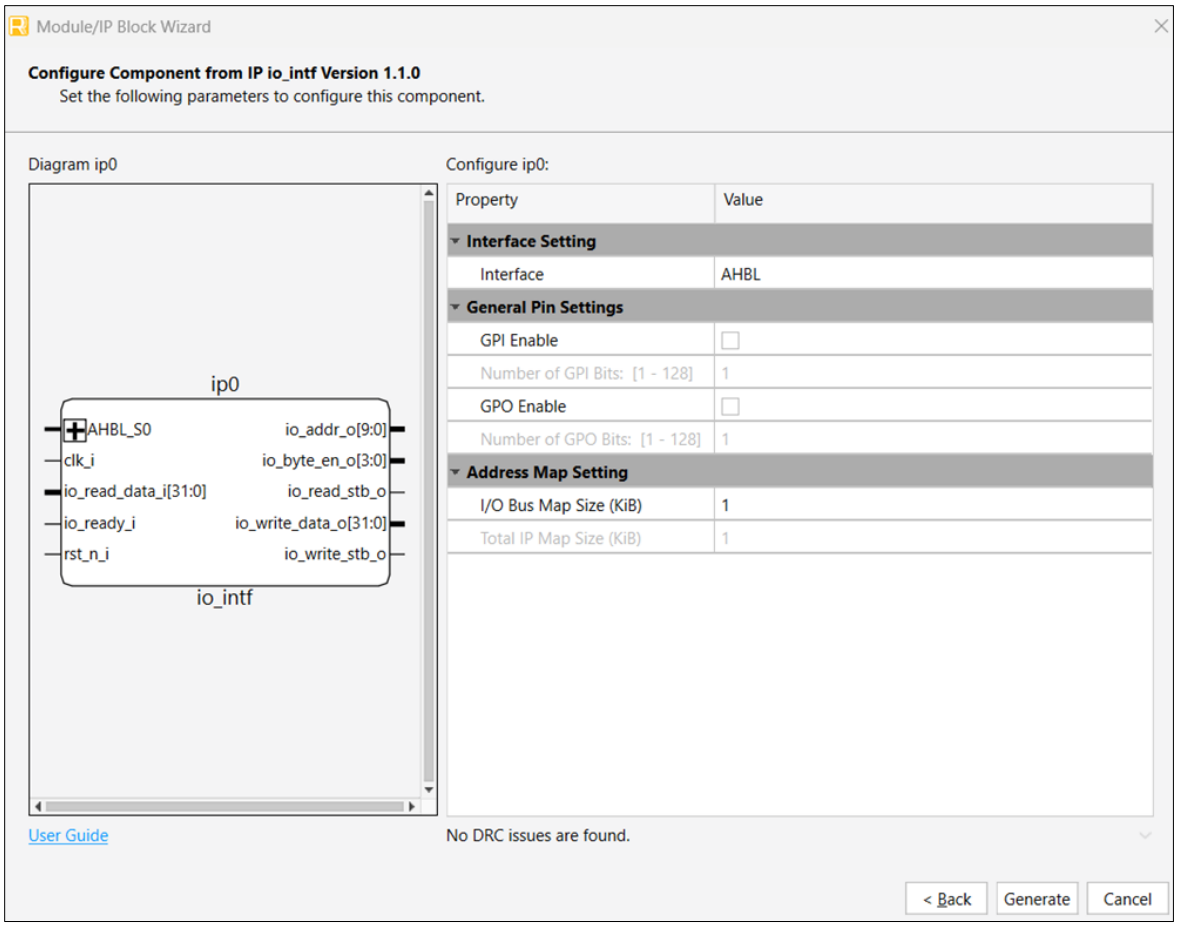


Figure 7.2. IP Configuration

4. Click **Generate**. The **Check Generated Result** dialog box opens, showing design block messages and results (Figure 7.3).

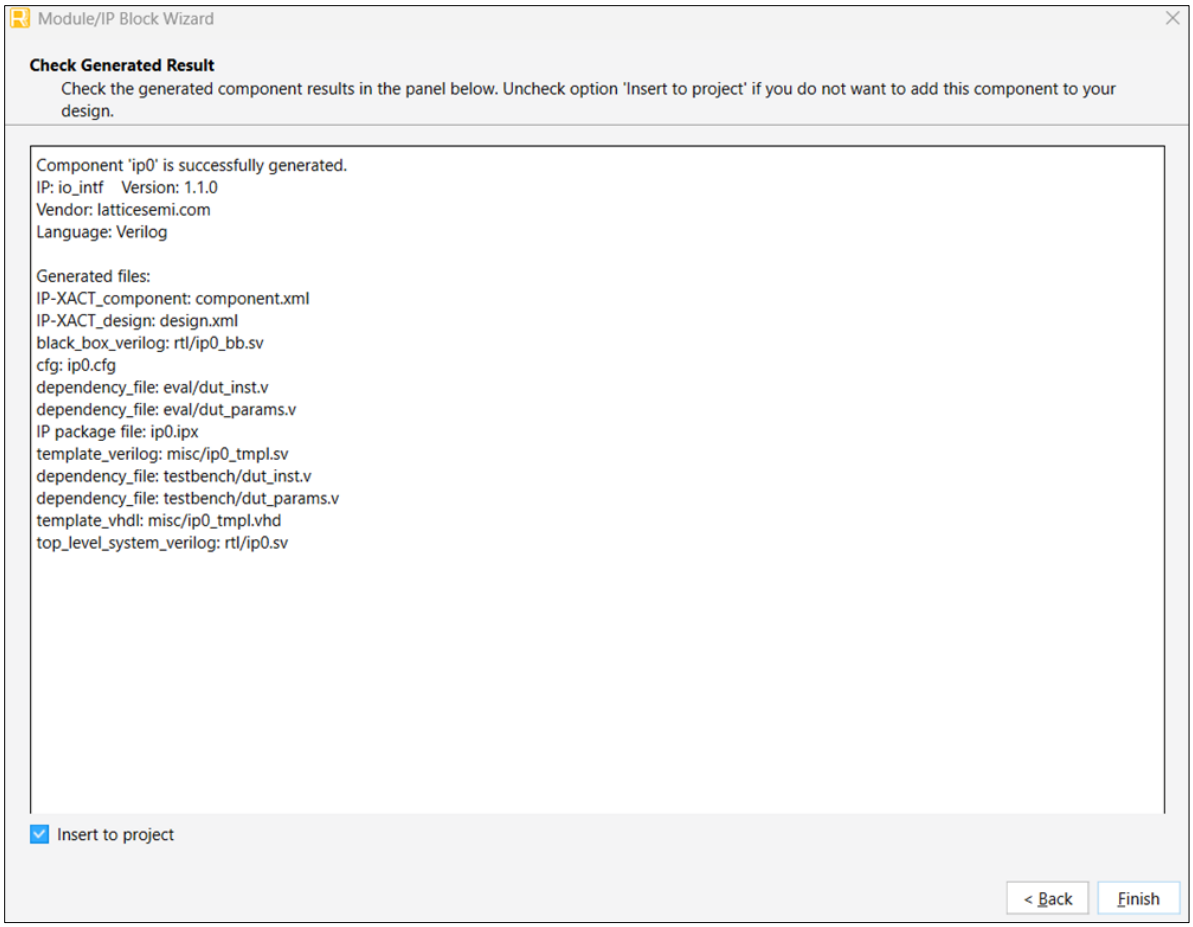


Figure 7.3. Check Generated Result

5. Click **Finish**. All the generated files are placed under the directory paths in the **Create in** and the **Component name** fields shown in Figure 7.1.

7.1.1. Generated Files and File Structure

The generated I/O Interface package includes the closed-box (<Component name>_bb.v) and instance templates (<Component name>_tmpl.v/vhd) that can be used to instantiate the core in a top-level design. An example RTL top-level reference source file (<Component name>.v) that can be used as an instantiation template for the module is also provided. You may also use this top-level reference as the starting template for the top-level for your complete design. The generated files are listed in Table 7.1.

Table 7.1. Generated File List

Attribute	Description
<Component name>.ipx	This file contains the information on the files associated to the generated IP.
<Component name>.cfg	This file contains the parameter values used in IP configuration.
component.xml	Contains the ipxact: component information of the IP.
design.xml	Documents the configuration parameters of the IP in IP-XACT 2014 format.
rtl/<Component name>.v	This file provides an example RTL top file that instantiates the module.
rtl/<Component name>_bb.v	This file provides the synthesis closed-box.
testbench/dut_inst.v testbench/dut_params.v	These files are the generated instances and parameters of the module.
testbench/tb_common.v testbench/tb_models.v	These files provide a simple testbench for the module.

Attribute	Description
testbench/tb_tests.v testbench/tb_top.v testbench/tb_util_task.v	
misc/<Component name>_tmpl.v misc /<Component name>_tmpl.vhd	These files provide instance templates for the module.

7.2. Timing Constraints

You must provide proper timing and physical design constraints to ensure that your design meets the desired performance goals on the FPGA. Add the content of the following IP constraint file to your design constraints: *<IP_Instance_Path>/<IP_Instance_Name>/eval/constraint.pdc.*

The constraint file has been verified during IP evaluation with the IP instantiated directly in the top-level module. You can modify the constraints in this file with thorough understanding of the effect of each constraint.

To use this constraint file, copy the content of *constraint.pdc* to the top-level design constraint for post-synthesis.

For more information on how to constraint your design, refer to the Lattice Radiant Timing Constraints Methodology Application Note (FPGA-AN-02059).

7.3. Running Functional Simulation

You can run functional simulation after the IP is generated.

To run functional simulation:

1. Click the  button located on the **Toolbar** to initiate the **Simulation Wizard** shown in Figure 7.4.

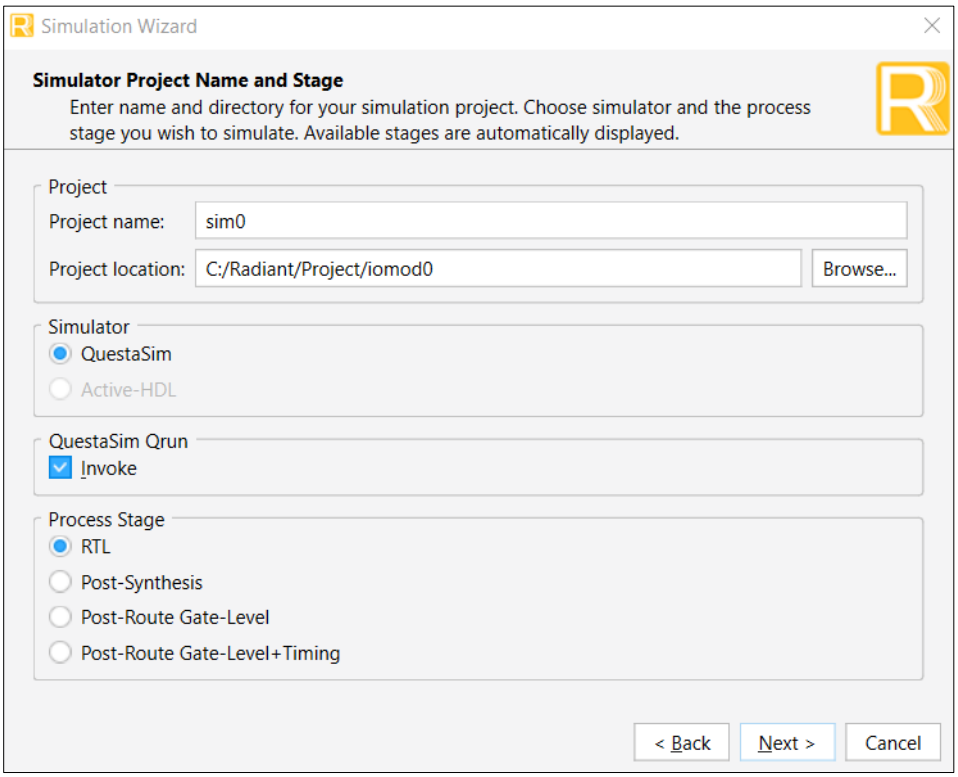


Figure 7.4. Simulation Wizard

2. Click **Next**. The **Add and Reorder Source** window opens, as shown in Figure 7.5.

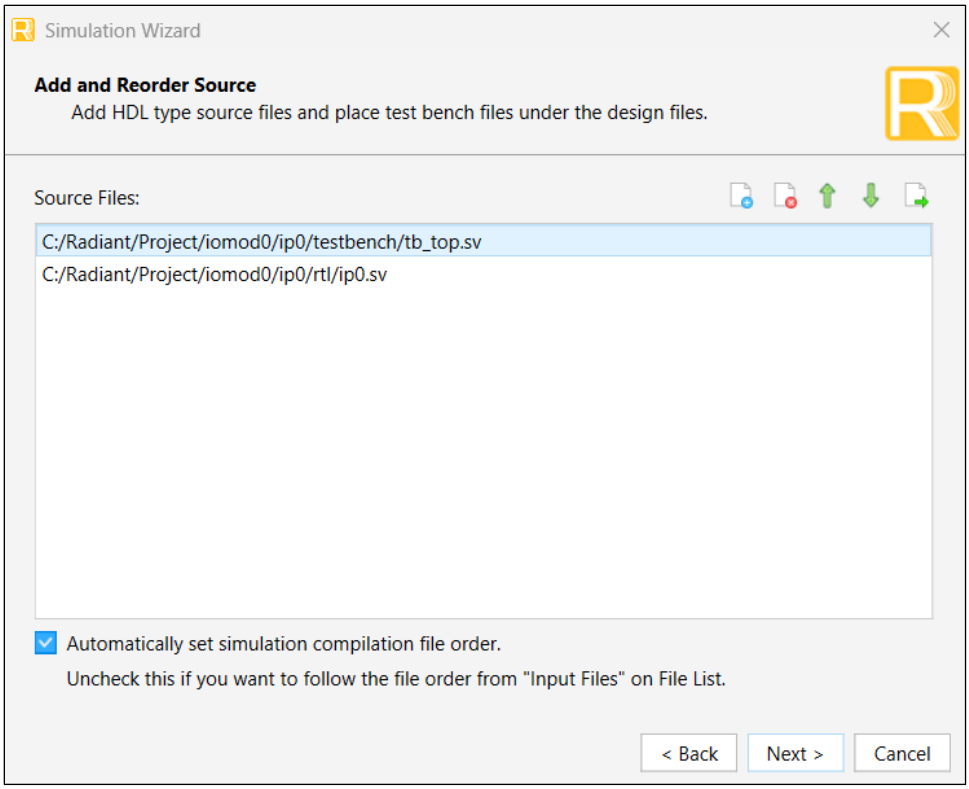


Figure 7.5. Add and Reorder Source

3. Click **Next**. The **Summary** window is shown (Figure 7.5).

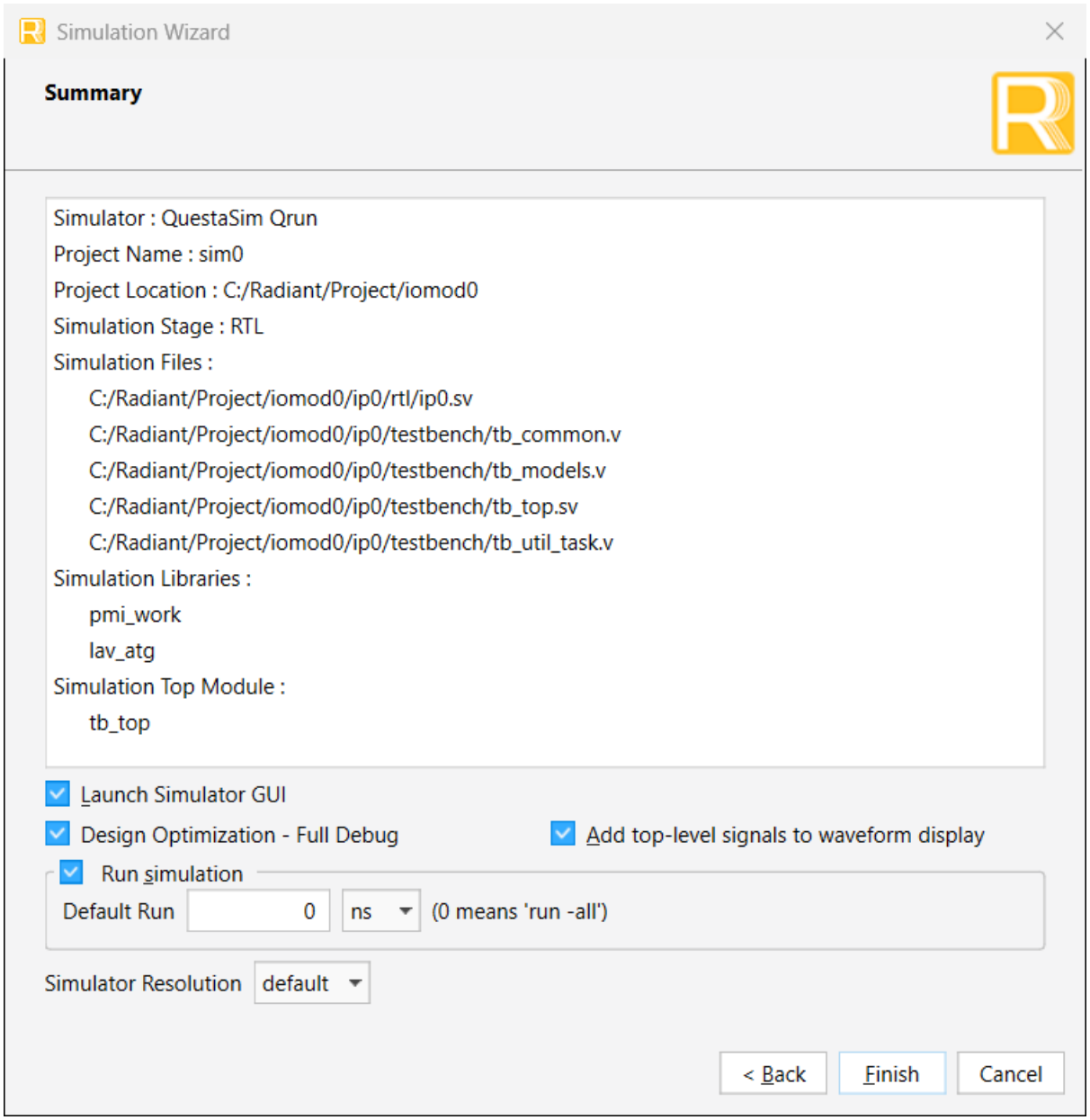


Figure 7.6. Summary Window

4. Click **Finish** to run the simulation.

The waveform in Figure 7.7 shows an example simulation result.

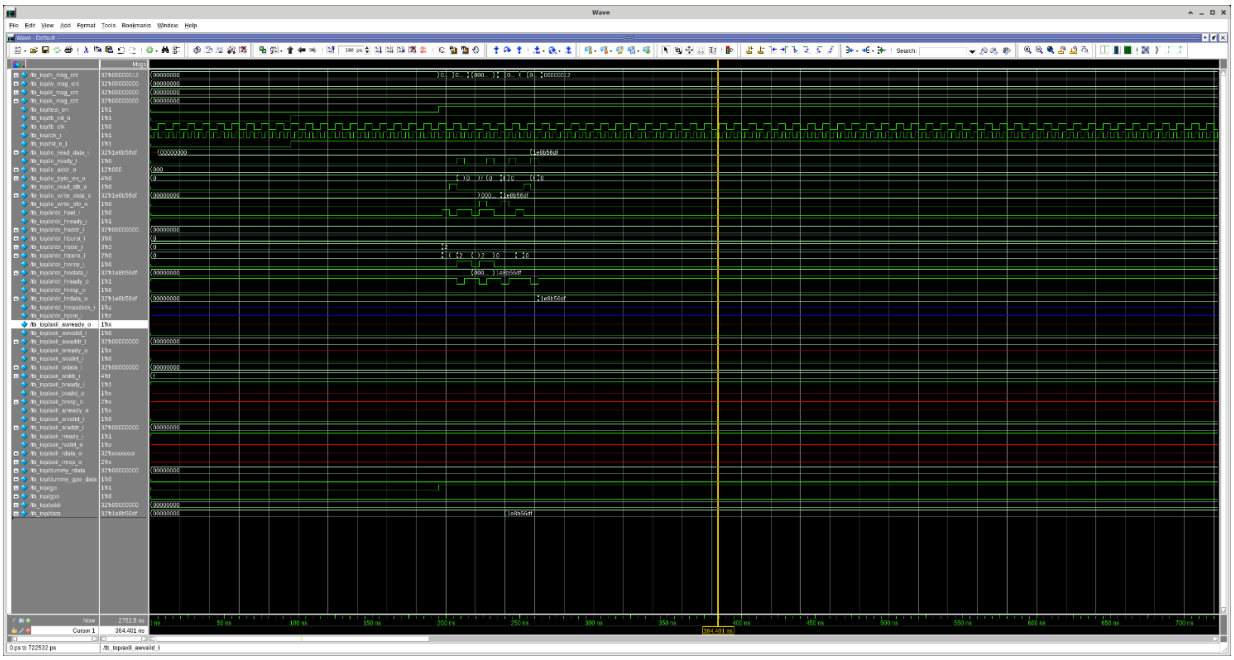


Figure 7.7. Simulation Waveform

Appendix A. Resource Utilization

Table A.1 shows a sample resource utilization of the I/O Interface IP using the LFD2NX-35-7BG400I device with the Synplify Pro synthesis tool in the Lattice Radiant software 2025.1. The default configuration is used, and some attributes are changed from the default value to show the effect on the resource utilization.

Table A.1. Resource Utilization for LFD2NX-35-7BG400I[1] Device

IP Configuration	LUTs	Registers	EBR	DSP
Default	231	81	0	0
Interface = AHBL	289	105	0	0
Interface = AHBL GPI Enable = Checked Number of GPI Bits = 1 GPO Enable = Checked Number of GPO Bits = 1	277	98	0	0
Interface = AHBL GPI Enable = Checked Number of GPI Bits = 128 GPO Enable = Checked Number of GPO Bits = 128	925	225	0	0
Interface = AXI4L GPI Enable = Checked Number of GPI Bits = 1 GPO Enable = Checked Number of GPO Bits = 1	299	109	0	0
Interface = AXI4L GPI Enable = Checked Number of GPI Bits = 128 GPO Enable = Checked Number of GPO Bits = 128	902	236	0	0

Note:

1. To get the resource utilization of some of the configurations of this device, virtual I/O constraints are declared to map the design.

Table A.2 shows a sample resource utilization of the I/O Interface IP using the LFCPNX-50-7ASG256I device with the Synplify Pro synthesis tool in the Lattice Radiant software 2025.1. The default configuration is used, and some attributes are changed from the default value to show the effect on the resource utilization.

Table A.2. Resource Utilization for LFCPNX-50-7ASG256I[1] Device

IP Configuration	LUTs	Registers	EBR	DSP
Default	231	81	0	0
Interface = AHBL	289	105	0	0
Interface = AHBL GPI Enable = Checked Number of GPI Bits = 1 GPO Enable = Checked Number of GPO Bits = 1	277	98	0	0
Interface = AHBL GPI Enable = Checked Number of GPI Bits = 128 GPO Enable = Checked Number of GPO Bits = 128	925	225	0	0

IP Configuration	LUTs	Registers	EBR	DSP
Interface = AXI4L GPI Enable = Checked Number of GPI Bits = 1 GPO Enable = Checked Number of GPO Bits = 1	299	109	0	0
Interface = AXI4L GPI Enable = Checked Number of GPI Bits = 128 GPO Enable = Checked Number of GPO Bits = 128	902	236	0	0

Note:

1. To get the resource utilization of some of the configurations of this device, virtual I/O constraints are declared to map the design.

Table A.3 shows a sample resource utilization of the I/O Interface IP using the LN2-CT-20ES-1ASG410I device with the Synplify Pro synthesis tool in the Lattice Radiant software 2025.1. Default configuration is used, and some attributes are changed from the default value to show the effect on the resource utilization.

Table A.3. Resource Utilization for LN2-CT-20ES-1ASG410I[1] Device

IP Configuration	LUTs	Registers	EBR	DSP
Default	229	81	0	0
Interface = AHBL	289	105	0	0
Interface = AHBL GPI Enable = Checked Number of GPI Bits = 1 GPO Enable = Checked Number of GPO Bits = 1	277	98	0	0
Interface = AHBL GPI Enable = Checked Number of GPI Bits = 128 GPO Enable = Checked Number of GPO Bits = 128	916	225	0	0
Interface = AXI4L GPI Enable = Checked Number of GPI Bits = 1 GPO Enable = Checked Number of GPO Bits = 1	303	109	0	0
Interface = AXI4L GPI Enable = Checked Number of GPI Bits = 128 GPO Enable = Checked Number of GPO Bits = 128	907	236	0	0

Note:

1. To get the resource utilization of some of the configurations of this device, virtual I/O constraints are declared to map the design.

Table A.4 shows a sample resource utilization of the I/O Interface IP using the LFMXO5-35T-7BBG484I device with the Synplify Pro synthesis tool in the Lattice Radiant software 2025.1. The default configuration is used, and some attributes are changed from the default value to show the effect on the resource utilization.

Table A.4. Resource Utilization for LFMXO5-35T-7BBG484I[1] Device

IP Configuration	LUTs	Registers	EBR	DSP
Default	229	81	0	0
Interface = AHBL	289	105	0	0
Interface = AHBL GPI Enable = Checked Number of GPI Bits = 1 GPO Enable = Checked Number of GPO Bits = 1	277	98	0	0
Interface = AHBL GPI Enable = Checked Number of GPI Bits = 128 GPO Enable = Checked Number of GPO Bits = 128	925	225	0	0
Interface = AXI4L GPI Enable = Checked Number of GPI Bits = 1 GPO Enable = Checked Number of GPO Bits = 1	299	109	0	0
Interface = AXI4L GPI Enable = Checked Number of GPI Bits = 128 GPO Enable = Checked Number of GPO Bits = 128	902	236	0	0

Note:

1. To get the resource utilization of some of the configurations of this device, virtual I/O constraints are declared to map the design.

References

- I/O Interface IP Release Notes (FPGA-RN-02084)
- Lattice Certus-N2 Family Devices web page
- Lattice Avant-E Family Devices web page
- Lattice Avant-G Family Devices web page
- Lattice Avant-X Family Devices web page
- MachXO5-NX Family Devices web page
- Certus-NX Family Devices web page
- CertusPro-NX Family Devices web page
- Lattice Radiant FPGA design software
- Lattice Radiant Software User Guide
- Lattice Radiant Timing Constraints Methodology (FPGA-AN-02059)
- Lattice Insights for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, please refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Note: In some instances, the IP may be updated without changes to the user guide. The user guide may reflect an earlier IP version but remains fully compatible with the later IP version. Refer to the IP Release Notes for the latest updates.

Revision 1.1, IP v1.1.0, December 2025

Section	Change Summary
All	Updated I/O Interface IP version to 1.1.0.

Introduction	• Table 1.1. Summary of the I/O Interface IP:
	  • updated Supported Devices to *All*;
	  • added the following table note, *In some instances, the IP may be updated without changes to the user guide. The user guide may reflect an earlier IP version but remains fully compatible with the later IP version. Refer to the IP Release Notes for the latest updates*.
	• Updated Table 1.2. I/O Interface IP Support Readiness to include CrossLink-NX and MachXO4 related information.

IP Parameter Description	• In Table 3.1. General Attributes, removed *since there is an allocated 1 KiB for the register space* from the description of the I/O Bus Map Size (KiB) attribute. • In Table 3.1. General Attributes, removed *Note that the allocated register space is 1 KiB if either GPI Enable or GPO Enable attribute is checked* from the description of the Total IP Map Size (KiB) attribute.
Designing with the IP	• Updated Figure 7.1. Module/IP Block Wizard, Figure 7.2. IP Configuration, and Figure 7.3. Check Generated Result. • In Table 7.1. Generated File List, added the following files: testbench/dut_inst.v testbench/dut_params.v testbench/tb_common.v testbench/tb_models.v testbench/tb_tests.v testbench/tb_top.v testbench/tb_util_task.v • Removed the original section 7.2. Design Implementation. • Added Figure 7.5. Add and Reorder Source.
Revision History	Added the note: *In some instances, the IP may be updated without changes to the user guide. The user guide may reflect an earlier IP version but remains fully compatible with the later IP version. Refer to the IP Release Notes for the latest updates*.

Revision 1.0, IP v1.0.0, June 2025

Section	Change Summary
All	Production release.

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