APB Interconnect Module

IP Version: v1.5.0

Release Notes

FPGA-RN-02077-1.2

June 2026

Disclaimers

Lattice makes no warranty, representation, or guarantee regarding the accuracy of information contained in this document or the suitability of its products for any particular purpose. All information herein is provided AS IS, with all faults, and all associated risk is the responsibility entirely of the Buyer. The information provided herein is for informational purposes only and may contain technical inaccuracies or omissions, and may be otherwise rendered inaccurate for many reasons, and Lattice assumes no obligation to update or otherwise correct or revise this information. Products sold by Lattice have been subject to limited testing and it is the Buyer's responsibility to independently determine the suitability of any products and to test and verify the same. LATTICE PRODUCTS AND SERVICES ARE NOT DESIGNED, MANUFACTURED, OR TESTED FOR USE IN LIFE OR SAFETY CRITICAL SYSTEMS, HAZARDOUS ENVIRONMENTS, OR ANY OTHER ENVIRONMENTS REQUIRING FAIL-SAFE PERFORMANCE, INCLUDING ANY APPLICATION IN WHICH THE FAILURE OF THE PRODUCT OR SERVICE COULD LEAD TO DEATH, PERSONAL INJURY, SEVERE PROPERTY DAMAGE OR ENVIRONMENTAL HARM (COLLECTIVELY, "HIGH-RISK USES"). FURTHER, BUYER MUST TAKE PRUDENT STEPS TO PROTECT AGAINST PRODUCT AND SERVICE FAILURES, INCLUDING PROVIDING APPROPRIATE REDUNDANCIES, FAIL-SAFE FEATURES, AND/OR SHUT-DOWN MECHANISMS. LATTICE EXPRESSLY DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY OF FITNESS OF THE PRODUCTS OR SERVICES FOR HIGH-RISK USES. The information provided in this document is proprietary to Lattice Semiconductor, and Lattice reserves the right to make any changes to the information in this document or to any products at any time without notice.

Inclusive Language

This document was created consistent with Lattice Semiconductor’s inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice’s inclusive language FAQ 6878 for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

Contents

1. Introduction

This document contains the Release Notes for the APB Interconnect Module. For specific details about the IP, refer to the following:

- APB Interconnect Module User Guide (FPGA-IPUG-02054)

APB Interconnect Module v1.5.0

Software	Software Version	Summary of Changes
Lattice Propel Builder Lattice Radiant	2026.1	• Added support for LN2-CT-20, LN2-CT-20ES1, LFD2NX-15P, LFD2NX-25P, and LFMXO5-25P devices. • Fixed completer address conflict in IP GUI. • Updated the GUI to hide the **Main Settings** tab when *Total APB Completers* = 1. • Updated the highest priority index of APB requester from 1 to 0.

APB Interconnect Module v1.4.0

Software	Software Version	Summary of Changes
Lattice Propel Builder Lattice Radiant	2025.2	Added support for LFMXO4 device.

APB Interconnect Module v1.3.0

Software	Software Version	Summary of Changes
Lattice Propel Builder Lattice Radiant	2025.1	• Corrected the AMBA terminology from *Requestor* to *Requester*. • Added support for LFD2NX-15, LFD2NX-25, LFD2NX-35, and LFD2NX-65 devices. • Added support for LFMXO5-35, LFMXO5-35T, LFMXO5-65, and LFMXO5-65T devices. • Documented the changes for earlier IP versions in the IP Release Notes.

APB Interconnect Module Earlier Versions

IP Version	Summary of Changes
1.2.1	• Adopted AMBA new inclusive terminology. • Removed the *Weighted Round Robin* option from the *Arbiter Scheme* property.
1.2.0	Resolved synthesis errors.
1.1.0	Extended support to all FPGA devices.
1.0.6	Added support for MachXO3L and MachXO3LF devices.
1.0.5	Added support for MachXO2 devices.
1.0.4	Added support for Mach-NX devices.
1.0.3	Added an explicit definition of port type for the clock and reset ports.
1.0.2	Added support for IP generation with the Lattice Radiant software.
1.0.1	Added support for CrossLink-NX and Certus-NX devices.
1.0.0	Initial release.

References

- APB Interconnect Module User Guide (FPGA-IPUG-02054)
- CrossLink-NX web page
- CertusPro-NX web page
- Certus-NX web page
- Certus-N2 web page
- Mach-NX web page
- MachXO2 web page
- MachXO3 web page
- MachXO3D web page
- MachXO4 web page
- MachXO5-NX web page
- iCE40 UltraPlus web page
- Avant-E web page
- Avant-G web page
- Avant-X web page
- APB Interconnect Module web page
- Lattice Radiant Software web page
- Lattice Propel Design Environment web page
- Lattice Diamond Software web page
- Lattice Insights for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

www.latticesemi.com