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Green FPGA: The Role of FPGA in Waveform Agnostics Radio Unit (RU) for 5G and 6G Applications

Green FPGA

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***Abstract*— One of the key goals of the ORAN architecture is to support waveform agnostic Radio Units (RU). This allows RUs to be software-defined and adaptable to various waveform technologies, including but not limited to 4G (LTE), 5G New Radio (NR), and eventually 6G. Waveform agnostic RU represents a significant advantage, offering unprecedented levels of modularity, adaptability, scalability, interoperability, customization, and enabling operators to deploy mixed-generation networks and dynamically allocate bandwidth based on demand and network conditions. This enables operators to more efficiently reuse the spectrum from one RAT to another as technology evolves and tune it to fit the economics of mobile users.**

This paper delves into critical aspects of designing and implementing a waveform agonistic RU system. The system is implemented on a reference hardware architecture consisting of a host and baseband CPUs, FPGA, and analog RF Frontend (RFFE). It contains cellular L3/L2/L1 stack, Serializer Deserializer (SERDES)-to-JESD204 bridging with deterministic latency, analog RF and antennas for different MIMO configurations. The system shows an innovative design and high modularity by creating a unified flexible, scalable, and customizable system that is used for the current 4G/5G Releases and 6G Terahertz waveform. The use of FPGA offers unparalleled reconfigurability, extremely low power consumption, and high security. The performance of such system supports up to 16T16R MIMO, meets 3GPP 5G/6G waveform specification, and industry standards for data throughput, low latency, low power consumption, and ultra compact footprint. It supports 5G sidelink and V2X use cases.

Keywords—5G, ORAN, FPGA, JESD204B, L1, SERDES, small cell

I. INTRODUCTION

One of the key features of the ORAN architecture is its support for waveform agnostic Radio Units (RU). This allows RUs to be software-defined and adaptable to various waveform technologies, including but not limited to LTE, 5G NR and 6G. Waveform agnostic RUs enhance flexibility, scalability, and interoperability, enabling operators to deploy mixed-generation mobile networks and dynamically allocate bandwidth based on demand, network use cases, and network conditions. 5G networks reuse spectrum by using the same frequency band in multiple cells, sharing spectrum with 4G networks, and dynamically allocating spectrum. This allows 5G networks to use spectrum more efficiently, which increases capacity, data rates, and improves the economics for both mobile operators and mobile users.

The choice between ASIC and FPGA to be used in the ORAN is a fundamental aspect of modularization. ASIC, such as baseband CPU, offers high performance and efficiency but at the cost of flexibility and reconfigurability. FPGA, on the other hand, provide unparalleled flexibility and reconfigurability, making them ideal for rapidly changing protocol stack and best suited for performance enhancement and tuning. 5G protocol stack has a large number of configurations and each is suited for specific use case and scenario. Unlike traditional fixed-function ASIC hardware, FPGAs can be reprogrammed on-the-fly to adapt to evolving 5G standards, waveform, protocols, and applications. This adaptability empowers mobile operators to swiftly implement new functionalities, optimize algorithms, and tailor the network infrastructure to specific needs. Consequently, this adaptability leads to increased operational efficiency, improved performance, and a competitive edge in the rapidly changing modern telecommunication landscape.

FPGA also contributes to fortifying the security and resiliency of 5G. With the rise of cyberattacks and threats and vulnerabilities in 5G infrastructures, FPGA offers inherent

security features such as Root of Trust (RoT), encryption and decryption, secure boot mechanism, mutual-authentication between the different nodes of eNodeB (base station), and tamper-resistant designs. By integrating FPGA-based security measures, 5G networks can mitigate cybersecurity risks, safeguard sensitive data, and ensure uninterrupted service delivery to users.

FPGA also has a small footprint and extremely low power consumption makes it ideal for radio units (RU), small base station like femto-cell, pico-cell, or small cell. The latter can be powered by battery and mounted on streetlights, outdoor venues such as bus stations, public transportation, or shopping malls.

A hybrid use of ASIC and FPGA can yield the maximum benefits of high performance CPUs and reconfigurability and programmability. Such a platform will be able to address the rapidly sophisticated and changing 5G and toward 6G protocol stacks.

I. 6G System Model

6G is announced by ITU and is part of the IMT-2030 which aims at connecting humans, machines, and software. 6G aims at multiple goals and among them are these most important aspects to achieve waveform agnostic capability [1]:

1) **Peak data rate**: Maximum achievable data rate under ideal conditions per device. The research target of peak data rate would be 50, 100, 200 Gbit/s.
2) **Latency**: Latency over the air interface target (over the air interface) could be 0.1 – 1 ms.

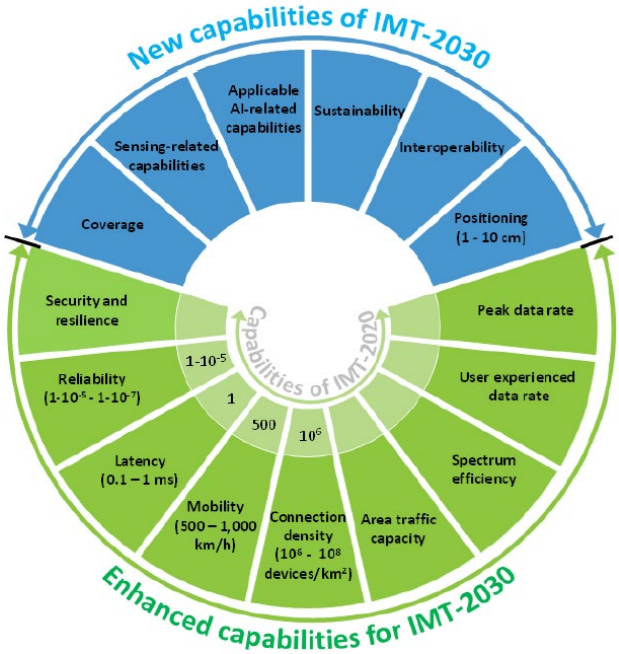

Figure 1. IMT-2030 (6G) Capabilities,

3) **Security and resilience**: Preservation of confidentiality, integrity, and availability of information, such as user data and signaling, and protection of networks, devices and systems against cyberattacks such as hacking, distributed denial of service, man in the middle attacks, etc. Resilience refers to capabilities of the networks and systems to continue operating correctly during and after a natural or man-made disturbance, such as the loss of primary source of power, etc.
4) **Sustainability (low power consumption)**: Refers to the ability of both the network and devices to minimize greenhouse gas emissions and other environmental impacts throughout their life cycle. Important factors include improving energy efficiency, minimizing energy consumption and the use of resources.
5) **Interoperability** (**waveform Agnostics**): Refers to the radio interface being based on member-inclusivity and transparency, so as to enable functionalities between different entities of the system.

It is important to note that the radio unit system architecture proposed in this paper aims at achieving the above goals including peak data rate, latency, security, sustainability, and interoperability.

II. 5G System Model

A. 5G NR Frame Structure

In 5G NR, downlink and uplink transmissions are organized into frames with each frame is 10 ms in duration, consisting of ten subframes. Each subframe is 1ms and the number of slots per subframe vary from 1 slot to 64 slots per subframe depending on the numerology used.

Table 1 summarize the 5G NR numerology. A slot has 14 OFDM symbols; each symbol has a normal Cyclic Prefix (CP). The new feature in 5G NR is that it supports multiple different types of Sub-carrier Spacing (SCS). Each numerology is labeled as a parameter (μ). The numerology (μ=0) represents 15 kHz. Slot length has different durations depending on numerology.

Table 1 5G NR Numerology.

Numerology μ	Subcarrier Spacing $\Delta f = 2^{\mu} \cdot 15$ kHz	Resource block bandwidth $\Delta f . 12$	OFDM symbol duration (us)
0	15	180 kHz	66.67
1	30	360 kHz	33.33
2	60	720 kHz	16.67
3	120	1440 kHz	8.633
4	240	2880 kHz	4.17
5	480	5760 kHz	2.23
6	960	11520 kHz	1.12

5G NR includes several low and mid-frequency bands in the sub-7 GHz range, defined as FR1, as well as higher frequency

bands above 24 GHz, defined as FR2 (mmWave). 5G frequency includes all previous cellular spectrum and additional spectrum in the sub-7 GHz frequency range and beyond. This is shown in Figure 2.

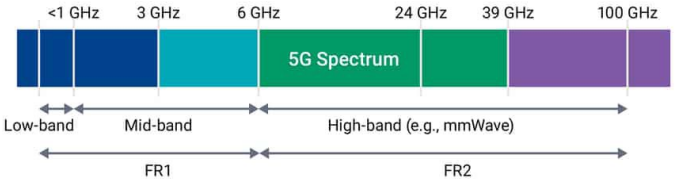

Figure 2 5G Spectrum

B. *JESD204 Protocol*

JESD204 is a high-speed serial interface used between data converters, such as analog-to-digital converters (ADCs) and digital-to-analog converters (DACs), and logic devices such as the FPGA to replace traditional interfaces, such as CMOS and LVDS. With converter sampling rates and data throughput increasing, the JESD204 interface offers advantages in terms of size, cost, and speed.

One version of JES204 is JESD204B. JESD204B key component is the ability to provide deterministic latency. It supports data rate up to 12.5 Gbps per lane and up to 12 lanes per link. JESD204C supports up to 32 Gbps per lane and up to 32 lanes.

The JESD204B provides a mechanism to ensure that, from power-up cycle and across link re-synchronization events, the latency is repeatable and deterministic. The JESD204B has three device subclasses: Subclass 0—no support for deterministic latency, Subclass 1— deterministic latency using SYSREF, and Subclass 2— deterministic latency using SYNC~. Subclass 0 can simply be compared to a JESD204A link. Subclass 1 is primarily intended for converters operating at or above 500 MSPS while Subclass 2 is primarily for converters operating below 500 MSPS.

Figure 3 shows the JESD204B interface working between FPGA and RFFE.

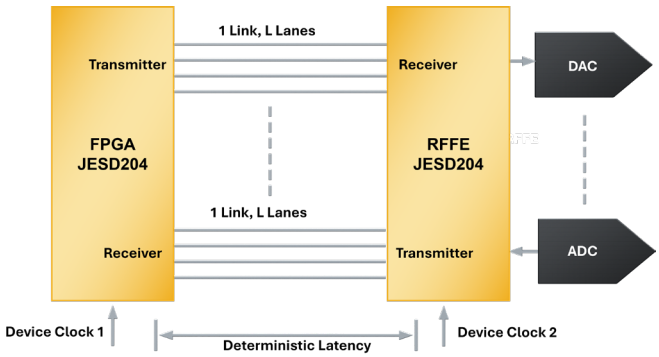

Figure 3. JESD204 Protocol.

C. *FPGA SERDES*

SERDES, as shown in Figure 4, is an electronic circuit designed to transform serial data into parallel data and vice versa, commonly found in high-speed communications applications. SERDES mainly consists of two parts:

- **Serializer**: A serializer is responsible for converting parallel data into serial data. It receives data in the form of parallel bits and converts them into a stream of serial bits that can be transmitted over a communication channel.
- **Deserializer**: A deserializer is responsible for converting serial data into parallel data. It receives serial data and converts it back into parallel bits that can be used by the receiving system.

SERDES technology includes a transmitter (TX) block, which serializes the parallel data, and a receiver (RX) block, which deserializes the serial data back into parallel form. In addition, SERDES circuits often include clock and data recovery (CDR) circuits, equalizers, data alignment, and error detection and correction mechanisms to ensure accurate and reliable data transmission over a communication channel.

SERDES serial I/O technology enables data transmission across a channel (PCB trace, cable) at high rates that can exceed 2000 - 3000 times faster than what can be achieved with parallel transmission techniques.

SERDES can reduce the intricacy, cost, and usage linked with applying wide parallel data buses when moving large amounts of data. It is specifically beneficial when frequency rates of parallel data move past 500 MHz

SERDES also allow significant savings in the number of I/O required to move large amounts of data across a channel compared to parallel techniques. Reducing I/O saves on cost and board area.

SERDES speed is essential in realizing 5G/6G goals of high peak data rate and low latency. SERDES is often used in 5G systems such as to exchange data to/from baseband CPU and RFFE. SERDES can be used as plain bidirectional channels or can be used in other forms such as Peripheral Component Interconnect Express (aka PCI Express® or PCIe®) or Ethernet interface. JESD204 uses SERDES to communicate with external CPUs and RFFE.

The Lattice CertusPro™-NX FPGAs feature up to 8 embedded 10 Gbps each SERDES channels. CertusPro-NX SERDES are organized in quads of four. Each CertusPro-NX SERDES quad includes four dedicated SERDES for high speed, full duplex serial data transfer.

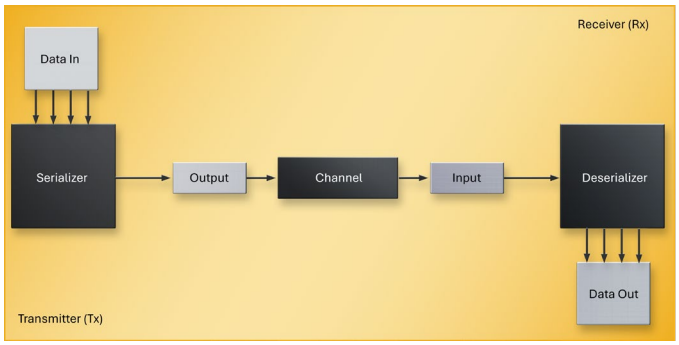

Figure 4. SERDES Interface.

The CertusPro-NX SERDES supports a range of popular serial protocols including: PCI Express Gen1 (2.5 Gbps), Gen 2 (5.0 Gbps), and Gen3 (8.0 Gbps), Ethernet, 10GBASE-R at 10.3125 Gbps, 1000BASE-X, SGMII, QSGMII, XAUI at 3.125 Gbps per lane, SLVS-EC at 1.25 Gbps, 2.5 Gbps and 5 Gbps, DisplayPort/eDP at 1.62 Gbps (RBR), 2.7 Gbps (HBR), 5.4 Gbps (HBR2), and 8.1 Gbps (HBR3), and CoaXPress at 1.25 Gbps, 2.5 Gbps, 3.125 Gbps, 5 Gbps, and 6.25 Gbps [3] .

JESD204C is another version of JESD204 protocol operating at even higher speeds and number of lanes than JESD204B. JESD204B/C utilizes the FPGA SERDES. Table 2 lists SERDES lane rates for the JESD204B/C interface required by 5G eNodeB [4]. The final column provides a count of the number of Antenna Carriers (AxC) operating at RF bandwidth of 100MHz each with a sampling frequency of 122.88 MHz that can be supported over a single JESD204B/C lane. For example, at SERDES lane rate of 4.9152 Gbps it supports one AxC per JESD204B/C lane.

Lattice CertusPro-NX FPGA supports 8 SERDES channels; each up to 10.3125 Gbps [5] while the Lattice Avant™-X FPGA supports 28 SERDES channels; each up to 25 Gbps [6]. Both FPGAs are suitable for supporting JESD204B and JESD204C with up to 8 lanes and 28 lanes respectively. If spare SERDES are needed for other SERDES interface such as PCIe Gen 3 with 4 lanes; The remaining SERDES can support JESD204B up to 4 lanes and JESD204C up to 24 lanes.

Table 2 FPGA SERDES Lane Rate.

JESD204B/C SERDES lane rate	Encoding	# of AxC at RF bandwidth = 100 MHz and F_s is 122.88 MHz
2.4576G	8B/10B	0.5
4.9152G	8B/10B	1
9.8304G	8B/10B	2
19.6608G	8B/10B	4
8.11008G	64B/66B	2
16.22016G	64B/66B	4
24.33024G	64B/66B	6

From Table 2, four JESD204B/C lanes operating at 9.8304G per lane, can support up to two AxC per lane or up to a total of eight AxC. This can be utilized as follows:

- Single RF bandwidth of 100 MHz component carrier for each AxC thus having eight component carriers for eight antennas.
- Two RF bandwidth of 100 MHz component carriers occupying a total 200 MHz in the same band for each AxC thus having four pairs of component carriers across four antennas.
- Two 100 MHz component carriers deployed in separate bands; each for each AxC thus having four pairs of component carriers across four antennas.

D. FPGA Security

5G ORAN can experience security vulnerabilities as they are often deployed at physically insecure sites and may even be a target for physical and cyberattacks by users trying to circumvent financial or technical restrictions. O-RAN Alliance has published a comprehensive threat model analysis of the 5G RAN segment [6] and is working towards a complete set of implementations requirements to mitigate the security risks. There are three aspects to consider with 5G ORAN security:

- **Hardware feature support** including key generation and storage and disabling physical interfaces
- **Software support** including hardened operating system and network protocol stack, standards defined authentication processes, interface input validation and protocol security
- **Operational security** including supply chain, secure firmware updates, mutual-authentication, and certificate management and monitoring.

Table 3 summarizes the hardware feature requirements that help create a secure 5G ORAN platform.

Table 3 FPGA Security Features.

FPGA security Feature	Description
Root of trust	A unique hardware identity for each device, an immutable first stage boot loader, and secure storage for root cryptographic keys and certificates
Cryptographic accelerators and trusted platform modules	speeding up cryptographic operations, provide key generation and storage so that keys are never visible to software
Secure processing features	Trusted execution environments isolate sensitive code. NX (no execute) mapping prevents execution of code hiding in data. Hardware stack protection and pointer authentication counter some of the most prevalent software attacks

E. 5G NR Traffic Digitization and Sampling

Figure 5 shows the functional split between baseband CPU (BB), FPGA, and RF Front End (RFFE). All the operations above the physical layer, and most of the physical layer are performed by the BB, which generates the radio signal, samples it, and sends the resulting data to the FPGA. The FPGA performs multiple functions such as FIR (Finite Impulse Response), MIMO multiplexing and processing, RFFE preprocessing, arithmetic and logic (ALU), bridging (such as converting from/to SERDES to/from JESD204B/C). RFFE usually has a JESD204B interface while ASIC baseband can have PCIe, Ethernet, or SERDES interfaces. An important function of FPGA is to translate, bridge, and process the digital samples from the BB and to convert it into the required 5G/6G waveform and then to the RFFE. In a simplest function, FPGA can act as a bridge between the BB PCIe/Ethernet/SERDES interface and JESD2024B/C RFFE interface.

The digitized samples are processed and transported by the FPGA from BB to RFFE. The RFFE has ADCs/DACs and is responsible for the on-air 5G waveform generation, transmission, and reception. BB, FPGA and RFFE collectively work in both downlink and uplink directions. The main benefit of this split is that the reconfigurable FPGA is tasked at processing and translating digital samples into required 5G/6G waveform. In addition, FPGA can be used to offload BB and RFFE of any digital processing (e.g. FIRs) making RFFE small and cheap. This architecture makes it suitable to do many 5G performance tuning, adaptation, and meets the changing 5G requirements and upgrades. In addition, the centralization of 5G L3/L2/L1 stack with most of the static PHY functionalities that require high-performance in the BB, simplifies the adoption of complicated 5G scenarios and uses cases such as V2X.

In downlink direction, FPGA receives In-Phase and Quadrature (I/Q) samples from the BB, performs DSP processing (e.g. FIR, MIMO, arithmetic & logic operations) and bridges the I/Q samples from SERDES interface over JESD204B/C interface to RFFE. RFFE does the final 5G on-air waveform construction and transmission over the antenna. In the uplink direction, FPGA receives the I/Q samples from RFFE, performs DSP functions (e.g. noise filtration), and bridges the samples from the JESD204B/C interface to the SERDES interface to the BB.

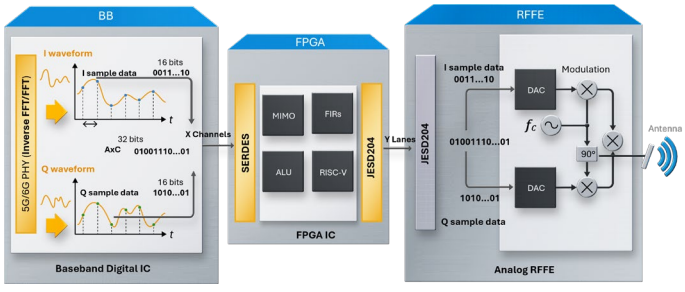

Figure 5. Functional split between Baseband CPU (BB), FPGA, and RF Front End (RFFE).

Sampling of the radio signal is done at the BB. Typical sampling rates for ORAN are derived for the channel bandwidths listed in Table 4 and Table 5. For each channel bandwidth, the total number of sub-carriers in downlink can be computed by the formula:

$$N_{subcarriers} = N_{RB} \text{ x } N_{sc}^{RB}, \quad \text{where } N_{sc}^{RB} \text{ is equal to 12. [8]}$$

The size N_{FFT} of the IFFT or FFT operations is chosen greater than the number of sub-carriers. Typical values are listed in Table 4 and Table 5. The sampling frequency F_S can be computed using the formula:

$$F_S = \Delta f \text{ x } N_{FFT},$$

where Δf is the sub-carrier spacing as per [8].

F. Transmission of 5G NR Control- and User-plane Data

The transmission of user plane data is based on the concept of Antenna Carrier (AxC). Given that the 5G NR radio signal is first sampled and then quantized, the amount of information carried by an AxC depends on two parameters:

- The sampling frequency F_s which is a multiple of the nominal chip rate $F_c = 3.84$ MHz (see Table 4).
- The number of bits, M, used in the quantization process of the I and Q radio signals. In 5G NR, M = 8, … , 20 either DL or UL. Actual baseband, FPGA, and RFFE implementation consider M = 16 for each of the I and Q samples for capacity efficiency.

For example, in a configuration with M = 16 bits/sample, one AxC contains 16 + 16 = 32 bits per IQ sample, which are transmitted in the following interleaved sequence:

$$I_0Q_0I_1Q_1 \ldots I_{M-1}Q_{M-1}.$$

That is, from the Least Significant Bit (LSB) to the Most Significant Bit (MSB).

To be compatible with eCPRI specifications, one Basic Frame is created and transmitted every $T_c = 260.416$ ns which is based on the UMTS clock rate, namely 3.84 MHz [7]. Such duration remains constant for all eCPRI line bit rate options [8]. The value of T_c is designed to transport, two samples for the 5G NR bandwidth of 5 MHz, 4 samples for the 10 MHz bandwidth, 8 samples for the 20 MHz bandwidth, etc as shown in the F_s row in Table 4 and Table 5.

In eCPRI, The duration of the hyperframe is 66.67 us which is one OFDM symbol time in 5G NR for numerology $\mu = 0$ (SCS of 15 kHz) , two OFDM symbol time for $\mu = 1$ (SCS of 30 kHz), four OFDM symbol time for $\mu = 2$, eight OFDM symbol time for $\mu = 3$, 16 OFDM symbol time for $\mu = 4$. Thus, a hyperframe carries all the FFT samples required to decode the whole OFDM symbol (or multiple of them).

G. General Data Rate Dimensioning GuideLine

One of the common RF bandwidths used in 5G NR is RF bandwidth of 100 MHz .

Serial protocols are protected by parity bits to protect the integrity of serial data bits. When the FPGA transports digital samples from baseband to RFFE, the digital samples go through the SERDES and then JESD204B/C and then finally to RFFE. JESD204B/C uses a 10B/8B or 64B/66B encoding rate.

In the case of an RF channel bandwidth of 100 MHz, a 30 kHz SCS, N_{FFT} is 4096 as shown in the 100 MHz column in Table 4. The sampling frequency, F_s, is set to 32 x 3.84 = 122.88 MHz.

Sampling and quantization of a single AxC requires an I/Q data bit rate of $B_{AxC} = 2M \times F_s$ bit/s, expanded by a factor of 10B/8B for the JESD204B or a factor of 66B/64B for JESD204C. Accordingly, a 100 MHz RF channel bandwidth requires 2 x 16 x 122.88 x 10/8 = 4.9152 Gbps. If JESD204C interface is used, it requires a 2 x 16 x 122.88 x 66/64 = 4.055 Gbps.

The I/Q data rate of 4.9152 Gbps contains 64QAM modulated symbols where each 64QAM symbol is carried on each subcarrier. Thus, the useful throughput (useful data) at a 100 MHZ RF bandwidth can be calculated as the total numbers of 64QAM modulated bits over all subcarriers divided by the OFDM symbol and cyclic prefix duration. Thu, for a 100 MHz RF bandwidth, L1 throughput would be 6 (6 bits for 64QAM) x 3276 (number of subcarriers in 100 MHz RF bandwidth at 30 kHz SCS) / (33.33 + 2.3) (OFDM symbol duration plus the cyclic prefix) = 551.67 Mbps. This is shown in the 100 MHz column in Table 4 for single AxC. This data rate represents the required data rate at the FPGA and the JESD204B data rate per lane.

If four antennas are used, e.g., four AxC, the required FPGA data rate and JESD204B per lane data rate is four times that of the "JESD204B per Lane Rate" row in Table 4.

The "JESD204B per lane rate" row in Table 4 shows the required data rate at the FPGA for each of the RF channel bandwidth and is the required JESD204B per lane data rate. It is calculated as the I/Q data rate expanded by JESD204B encoding factor of 10B/8B. When using MIMO at an RF bandwidth of 100 MHz, the number of Tx or Rx antennas can be 2, 4, 8, 12, or 16 antennas in each direction; thus, this requires 2, 4, 8, 12, or 16 times the "JESD204B per lane rate". With JESD204B supporting up to 12 lanes, 12 AxC at 100 MHz bandwidth each can be used where each AxC is carried over a single JESD204B lane.
If JESD204C is used, the I/Q data rate is expanded by a factor of 66B/64B. With JESD204C supporting 16 lanes, 16 AxC at 100 MHz bandwidth each can be used where each AxC is carried over a single JESD204C lane.

Table 5 shows also the "JESD204B per lane rate" with FR2 for each antenna. In FR2, the SCS can be 60 kHz, 120 kHz, 480 kHz, or 960 kHz and the RF bandwidth can be as wide as 50 MHz, 100 MHz, 200 MHz, 800 MHz, 1600 MHz, or 2000 MHz. In FR2 and for high RF bandwidth of 800 MHz, 1600 MHz, or 2000 MHz, they require multiple lanes to aggregate the required I/Q data rata at 39.3216 Gbps or 78.6432 Gbps.

It is worth noting that the number of AxC used in 5G NR frame can be used for FDD or TDD configuration. JESD204B/C interface is not aware of FDD or TDD being used as JESD204B/C is an always-on protocol meaning that it is continuously transmitting or receiving data from/to ADC/DACs. Single AxC can be used for FDD for both directions. If TDD is used, then either a pause in data or zero bits are transmitted/received over the JESD204B/C interface.

H. Example Use Case of a 4x4 MIMO , FDD, 100 MHz Channel Bandwidth

Consider the four-antenna scenario operating as 5G NR FDD, 4x4 MIMO channel of 100 MHz bandwidth. This scenario requires the multiplexing and transmission of four AxC (for the 4 x 4 MIMO) whereas 4 antennas are used for downlink and uplink. According to Table 4, each IQ sample is 2M=32 bits. The "JESD204B per lane rate" required for each antenna is 4.9152 Gbps and JESD204B bidirectional four lanes are required to support 4.9152 Gbps per each AxC.

I. Basband, FPGA, and RFFE Functional Split

Table 6 summarizes the functional splits between the BB, FPGA, and RF front end. BB ASIC has a limited configuration of SERDES (e.g. PCIe or Ethernet) that are not compatible with the RFFE interface and thus require bridging functionality so that the BB and RFFE can communicate to each other. In addition, FPGA hosts other functionalities such as bit-format conversion (one's complement or two's complement conversion), FIR for signal filtering and shaping, MIMO multiplexing, demultiplexing, or proprietary DSP algorithms to enhance the 5G RF waveform.

Table 4 FPGA and L1 Data Rate for FR1 per Antenna (AxC).

Bandwidth (B)	Subcarrier Spacing (SCS)	5 MHz	10 MHz	20 MHz	30 MHz	50 MHz	60 MHz	80 MHz	90 MHz	100 MHz
Number of subcarriers	15 kHz	300	624	1272	1920	3240	NA	NA	NA	NA
	30 kHz	132	288	612	936	1596	1944	2604	2940	3276
	60 kHz	NA	132	288	456	780	948	1284	1452	1620
Number of PRB (N_{prb})	15 kHz	25	52	106	160	270	NA	NA	NA	NA
	30 kHz	11	24	51	78	133	162	217	245	273
	60 kHz	NA	11	24	38	65	79	107	121	135
FFT size (N_{fft})	15 kHz	512	1024	2048	3072	4096	NA	NA	NA	NA
	30 kHz	256	512	1024	1536	2048	3072	4096	4096	4096
	60 kHz	NA	256	512	768	1024	1536	2048	2048	2048
Sampling Freq (MHz)	15 kHz	7.68	15.36	30.72	46.08	61.44	NA	NA	NA	NA
	30 kHz	7.68	15.36	30.72	46.08	61.44	92.16	122.88	122.88	122.88
	60 kHz	NA	15.36	30.72	46.08	61.44	92.16	122.88	122.88	122.88
F_s = SCS X N_{fft}	15 kHz	2 x 3.84 MHz	4 x 3.84 MHz	8 x 3.84 MHz	12 x 3.84 MHz	16 x 3.84 MHz	24 x 3.84 MHz	32 x 3.84 MHz	32 x 3.84 MHz	32 x 3.84 MHz
	30 kHz									
	60 kHz									
OFDM symbol duration (T_s) (us)	15 kHz	66.67								
	30 kHz	33.33								
	60 kHz	16.67								
Cyclic Prefix duration (T_{cp}) (us)	15 kHz	4.7								
	30 kHz	2.3								
	60 kHz	1.2								
Modulation Constellation	64QAM	6								
No. of bits for I and Q (2M)		32								
I/Q Data Rate		0.24576	0.49152	0.98304	1.47456	1.96608	2.94912	3.93216	3.93216	3.93216
JESD204B per Lane Rate		0.3072	0.6144	1.2288	1.8432	2.4576	3.6864	4.9152	4.9152	4.9152
L1 Throughput (64QAM)	15 kHz	0.0252207	0.052459	0.1069357	0.1614124	0.2723834	NA	NA	NA	NA
	30 kHz	0.0222285	0.0484985	0.1030592	0.15762	0.2687623	0.3273646	0.4385069	0.4950884	0.5516699
	60 kHz	NA	0.0443201	0.0966984	0.1531058	0.2618914	0.3182988	0.4311136	0.487521	0.5439284

Table 5 FPGA and L1 Data Rate for FR2 per Antenna (AxC).

Bandwidth (B)	Subcarrier Spacing (SCS)	50 MHz	100 MHz	200 MHz	400 MHz	800 MHz	1600 MHz	2000 MHz
Number of subcarriers	60 kHz	792	1584	3168	NA			
	120 kHz	384	792	1584	3168			
	480 kHz				792	1488	2976	
	960 kHz				396	744	1488	1776
Number of PRB (N_{prb})	60 kHz	66	132	264	NA			
	120 kHz	32	66	132	264			
	480 kHz				66	124	248	
	960 kHz				33	62	124	148
FFT size (N_{fft})	60 kHz	1024	2048	4096	NA			
	120 kHz	512	1024	2048	4096			
	480 kHz				1024	2048	4096	
	960 kHz				512	1024	2048	2048
Sampling Freq (MHz)	60 kHz	61.44	122.88	245.76	NA			
	120 kHz	61.44	122.88	245.76	491.52			
	480 kHz				491.52	983.04	1966.08	
	960 kHz				491.52	983.04	1966.08	1966.08
F_s = SCS X N_{fft}	60 kHz	16 x 3.84 MHz	32 x 3.84 MHz	64 x 3.84 MHz	128 x 3.84 MHz	256 x 3.84 MHz	512 x 3.84 MHz	512 x 3.84 MHz
	120 kHz							
	480 kHz							
	960 kHz							
OFDM symbol duration (T_s) (us)	60 kHz	16.67						
	120 kHz	8.3						
	480 kHz	2.08						
	960 kHz	1.04						
Cyclic Prefix duration (T_{cp}) (us)	60 kHz	1.2						
	120 kHz	0.6						
	480 kHz	0.15						
	960 kHz	0.07						
Modulation Constellation	64QAM	6						
No. of bits for I and Q (2M)		32						
I/Q Data Rate		1.96608	3.93216	7.86432	15.72864	31.45728	62.91456	62.91456
JESD204B/C per Lane Rate		2.4576	4.9152	9.8304	19.6608	39.3216	78.6432	78.6432
L1 Throughput (64QAM)	60 kHz	0.265921	0.531841	1.063682				
	120 kHz	0.258876	0.533933	1.067865	2.13573			
	480 kHz				2.130942	4.003587	8.007175	
	960 kHz				2.140541	4.021622	8.043243	9.6

Table 6 BB, FPGA, and RFFE Functional Split.

Functions of BB		Functions of FPGA		Functions of RFFE	
Downlink	**Uplink**	**Downlink**	**Uplink**	**Downlink**	**Uplink**
Radio base station control & management				Channel Filtering	
Backhaul transport		SERDES to JESD204B/C	JESD204B/C to SERDES	D/A conversion	A/D conversion
MAC layer				Up Conversion	Down Conversion
Channel Coding, Interleaving, Modulation	Channel De-coding, De-Interleaving, Demodulation	Finite Impulse Response (FIRs)		ON/OFF control of each carrier	Automatic Gain Control
IFFT	FFT	Bit-format conversion and representation (One's or two's complement conversion)		Carrier Multiplexing	Carrier De-multiplexing
Add CP (optional)	Remove CP	MIMO Multiplexing and Processing		Power amplification and limiting	Low Noise Amplification
Signal aggregation from signal processing units		Proprietary DSP algorithms		Digital Pre-Distortion (DPD)	
Transmit Power Control of each physical channel	Signal distribution to signal processing units			RF filtering	
Frame and slot signal generation (including clock stabilization)	Transmit Power Control & Feedback Information detection			TDD switching in case of TDD mode	
Measurements				Measurements	

III. 5G HARDWARE REFERENCE ARCHITCTURE

Figure 6 depicts a hardware reference architecture that is used to host 5G NR protocol stack consisting of TCP/IP, L3/L2 (RRC, PDCP, RLC), L1 (MAC/PHY), and a configuration of 4Tx4Rx antennas. MIMO unit can be used to process SU-MIM, MU-MIMO, Arithmetic and Logic Unit (ALU) for math computation such as two's complement, floating-point arithmetic, and FIR for frequency-domain processing of the 5G waveform (such as filtering, repeater). The reference architecture can be used for TDD or FDD modes and can be used with a single-sector or multiple-sector eNodeB. If a multiple-sector scenario is used, the baseband CPU communicates with multiple FPGAs/RFFEs where each single unit of FPGA/RFFE is used for each sector.

The FPGA interfaces with the baseband CPU through SERDES interface. The FPGA SERDES supports up to 8 or 28 embedded channels and each channel can run at a maximum speed of 10.3125 Gbps or 25 Gbps respectively. The FPGA interfaces with the RFFE is through JESD204B/C. The FPGA JESD204B/C supports up to x8 lanes (or x24 lanes). The SERDES and JESD204B/C per lane speed can support all the SERDES speeds as specified in Table 2. Table 2 SERDES speeds are the basic speeds that can be used to support "JESD204B/C per lane rate" for 5G FR1 and FR2 as in Table 4 and Table 5.

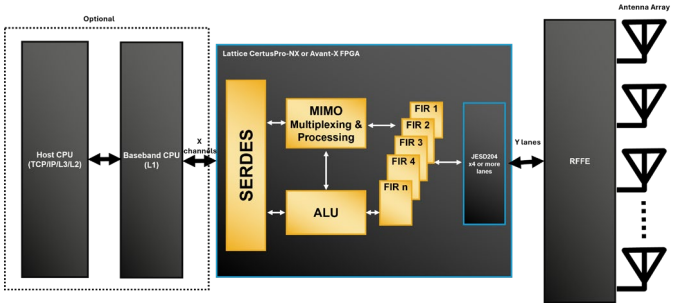

Figure 6: Hardware Reference Architecture for 5G 4Tx4Rx ORAN.

In some 5G applications such as 5G repeater, the hardware reference architecture does not need Host/Baseband CPUs and instead only the FPGA and RFFE are used. This is because for

a 5G repeater, only 5G waveform needs to be processed such as amplification and filtering. In 5G repeater, 5G L1/L2/L3 protocol stack is not required.

Figure 7 depicts a detailed hardware reference architecture scenario where BB, FPGA, and RFFE are used to host a complete 5G protocol stack consisting of TCP/IP/L3/L2/L1.
The baseband can host the L2/L1 (MAC and PHY) layers of the 5G NR. FPGA can host other L1 functionalities to offload the baseband CPU for custom L1 functionalities. RFFE is responsible for on-air 5G waveform analog functionalities.

Baseband CPU has multiple cores, floating arithmetic unit, DDR4 interface, PCIe Gen3/4 interface, 10G/25G Ethernet interfaces.

FPGA has SERDES interface, DDR4/DDR5, Flash, and embedded memory interfaces, DSP slices, LUTs, 10/25G Ethernet interfaces, secure booting, and SPI/I2C interfaces.

The RFFE contains ADCs/DACs, JESD204B/C interfaces, decimation and programmable FIRs, automatic gain control (AGC), PLLs, tunning and interpolation engines, power control, synthesizers, and SPI interface.

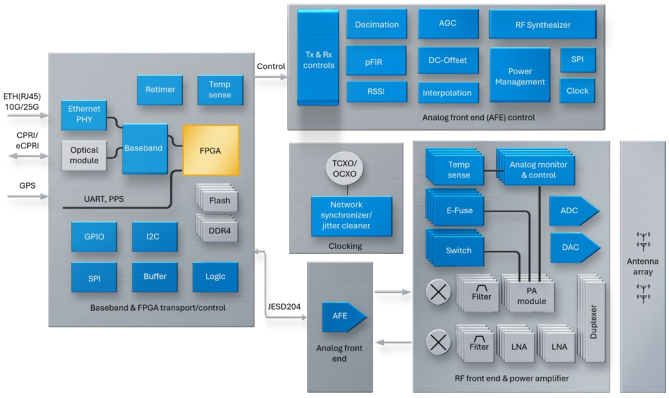

Figure 7: Hardware Reference Architecture.

I. DEMO OF THE HARDWARE REFERENCE ARCHITECTURE

The 5G ORAN design in Figure 6 and Figure 7 are implemented and validated. Please refer to Lattice website for more technical details about the hardware reference architecture [11]. The RF bandwidth of 100 MHz configuration as in Table 4 is used and a 4Tx4Rx antenna system is used. Baseband CPU runs 5G L1 and has an OFDM modulator and demodulator. The OFDM modulator generates 64QAM modulated symbols, performs IFFT, and transfers the 16-bits I and Q samples to the FPGA over four SERDES channels. The FPGA process and transmits the I/Q samples to RFFE over JESD204B four lanes. Since this is a 4Tx4Rx system, the SERDES has four channels and JESD24B has four lanes, and each lane runs at 4.9125 Gbps as in Table 4 (RF bandwidth =100 MHz).
The RFFE has four Tx ports and four Rx ports. RFFE uses a carrier frequency of 1 GHz. One Tx port is connected to a spectrum analyzer, and an OFDM spectral power density signal shows up as in Figure 8. In the figure, the OFDM spectrum mask is at bandwidth of 100 MHz and centered at the carrier frequency of 1 GHz.

Four OFDM signals on the four Tx ports also looped-back to the Rx ports. The signal received on the Rx port propagates over the four lanes JESD204B to the FPGA and then over four SERDES channels to the BB CPU. On the BB, OFDM demodulator performs FFT and demodulates the 64QAM symbols. 64QAM symbols are obtained and match with the same original and transmitted 64 modulated symbols.

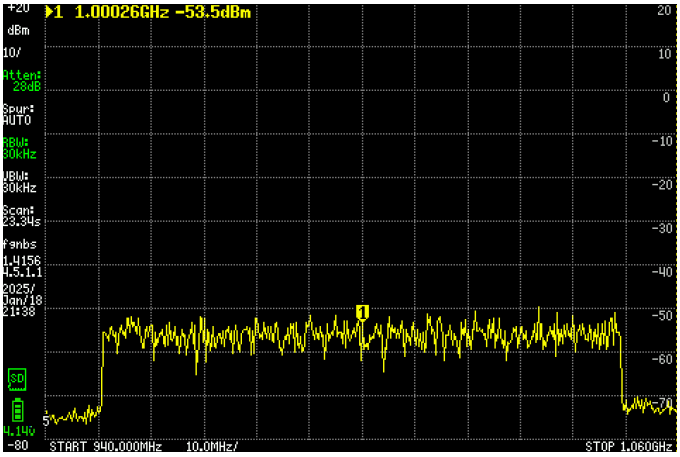

Figure 8: OFDM Spectral Mask.

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