# DDR Memory Module IP

IP Version: v2.3.0

# Release Notes

FPGA-RN-02080-1.2

June 2026

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# Contents

# 1. Introduction

This document contains the Release Notes for the DDR Memory Module IP. For specific details about the IP, refer to the following:

- DDR Memory Module IP User Guide (FPGA-IPUG-02060)

## DDR Memory Module IP v2.3.0

| Software | Software Version | Summary of Changes |
|---|---|---|
| Lattice Radiant | 2026.1 | • Tri-stated the DM signals on the memory interface when there are no active transactions.<br>• Added device support for LFD2NX-15P, LFD2NX-25P, and LFMXO5-25P, including usage of the PLLD primitive for these devices. |

## DDR Memory Module IP v2.2.0

| Software | Software Version | Summary of Changes |
|---|---|---|
| Lattice Radiant | 2025.2 | • Fixed the testbench to align with the software model's timing fix.<br>• Updated the SIM_FLOAT_PRECISION parameter for the internal PLL to a value of 0.625.<br>• Removed support for LPDDR3 for all devices except ECP5.<br>• Updated the DELAY element for CK, commands, and DQ from DELAYB to DELAYA.<br>• Improved write leveling stability by stopping the DQSBUF internal clocks with the PAUSE signal during delay code updates. |

## DDR Memory Module IP v2.1.0

| Software | Software Version | Summary of Changes |
|---|---|---|
| Lattice Radiant | 2025.1 | • Added delay configuration for clock, command, and address lines<br>• Updated PLL<br>• Added support for constraints to be consumed by the Radiant Constraint Propagation Engine<br>• Added DRC on unsupported configurations |

## DDR Memory Module IP Earlier Versions

| IP Version | Summary of Changes |
|---|---|
| 2.0.0 | Modified DDR clock from differential to two single-ended complementary signals |
| 1.4.0 | Added UT24C and UT24CP support |
| 1.3.0 | • Added LFMXO5 support<br>• Updated calculation of PLL settings |
| 1.2.0 | • Added LFCPNX support<br>• Updated PLL instance |
| 1.1.0 | • Added LFD2NX support<br>• Improved selectable values in GUI<br>• Updated PLL instance |
| 1.0.1 | • Added optional PLL<br>• Improved implementation of X4 gearing ratio |
| 1.0.0 | Initial release |

# References

- DDR Memory Module IP User Guide (FPGA-IPUG-02060)
- CertusPro-NX web page
- Certus-NX web page
- CrossLink-NX web page
- IP Core for Nexus Devices
- Lattice Radiant Software web page
- Lattice Insights for Lattice Semiconductor training courses and learning plans

# Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, please refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.


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