MachXO4 EFB Module IP

IP Version: v1.3.0

User Guide

FPGA-IPUG-02287-1.2

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Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviation	Definition
ACK	Acknowledgement
APB	Advanced Peripheral Bus
CFG	Configuration
CTCM	Clear Timer on Compare Match
DUT	Device Under Test
EFB	Embedded Functional Block
FIFO	First In, First Out
FPGA	Field Programmable Gate Array
GUI	Graphical User Interface
GPIO	General-Purpose Input/Output
I/O	Input/Output
I2C	Inter-Integrated Circuit
ID	Identification
IP	Intellectual Property
IRQ	Interrupt Request
ISC	In-System Configuration
JTAG	Joint Test Action Group
LSE	Lattice Synthesis Engine
LSB	Least Significant Bit
LUT	Look-Up Table
MDF	Mode Fault
MSB	Most Significant Bit
NACK	No Acknowledgement
NVR	Non-Volatile Registers
OEM	Original Equipment Manufacturer
PFCPWM	Phase/Frequency Correct Pulse Width Modulation
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation
RO	Read-Only
RoT	Root of Trust
RW	Read-Write
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
UFM	User Flash Memory
WO	Write-Only

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1. Introduction

1.1. Overview of the IP

The embedded functional block (EFB) module provides a soft-IP implementation of the hardened control functions in the Lattice MachXO4™ FPGA devices. These hardened control functions ease design implementation and conserve general-purpose resources like LUTs, registers, clocks, and routing. The hardened control functions are physically located in the EFB.

The EFB includes the following control functions:

- Two I2C cores
- One SPI core
- One 16-bit Timer/Counter
- Interface to flash memory, which includes:
  - User Flash memories
  - Configuration logic
  - Feature row and security blocks, which are available only for MachXO4 Root of Trust (RoT) devices
- Interface to dynamic phase-locked loop (PLL) configuration settings
- Interface to the on-chip power controller through I2C and SPI

1.2. Quick Facts

Table 1.1. Summary of the EFB Module IP

IP Requirements	Supported Devices	MachXO4™
	IP Changes	For a list of changes to the IP, refer to the MachXO4 EFB Module IP Release Notes (FPGA-RN-02079).
Resource Utilization	Supported User Interface	WISHBONE, APB, I2C, and SPI
	Resources	Refer to Appendix A. Resource Utilization
Design Tool Support	Lattice Implementation	IP Core v1.3.0 – Lattice Radiant™ software 2026.1.1
	Synthesis	Lattice Synthesis Engine (LSE)
		Synplify Pro®
	Simulation	Questa Lattice OEM

Notes:

1. In some instances, the IP may be updated without changes to the user guide. This user guide may reflect an earlier IP version but remains fully compatible with the later IP version. Refer to the IP Release Notes for the latest updates.
2. In this document, *MachXO4* refers to both LFMXO4 and LFMXO4D unless explicitly identified as MachXO4 (LFMXO4). *MachXO4 RoT* refers to only *LFMXO4D*.

1.3. IP Support Summary

Table 1.2. EFB Module IP Support Readiness

Device Family	Feature	Radiant Timing Model
MachXO4	I2C	Final
	SPI	Final
	Timer/Counter	Final
	PLL (dynamic configuration)	Final
	CFG/UFM	Final
	Tamper Detect/Response	Final

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1.4. Features

Key features of the EFB Module IP include:

- Provides an interface to user logic through the WISHBONE interface.
- Two I2C cores:
  - Operate as both controller and target.
  - Support configurable 7-bit and 10-bit addressing.
  - Support 50 kHz, 100 kHz, and 400 kHz data transfer speed.
  - The primary I2C core can access either flash memory or user logic.
- One SPI core:
  - Configurable as either SPI controller/target or SPI target.
  - When configured as controller/target, the IP core can control up to eight other SPI target devices.
  - Provides an interface to flash memory or user logic through the WISHBONE interface.
  - Includes a Mode Fault Error flag with CPU interrupt.
  - Features a double-buffered data register for increased throughput.
  - Supports serial clock with programmable polarity and phase.
  - Supports both LSB-first and MSB-first data transfers.
- Various Timer/Counter modes of operation:
  - Clear Timer on Compare Match (CTCM)
  - Watchdog Timer
  - Fast Pulse-Width Modulation (PWM)
  - Phase and Frequency Correct PWM
- Dynamic PLL configuration.
- Interface to flash memory, which includes:
  - User flash memory
  - Configuration logic
  - Feature row and security blocks (available only for MachXO4 RoT devices)
- APB interface for bridging to the WISHBONE user interface.

1.5. Licensing and Ordering Information

The EFB Module IP is provided at no additional cost with the Lattice Radiant software.

1.6. Minimum Device Requirements

The EFB Module IP has no device speed-grade limitation. Refer to Appendix A. Resource Utilization for minimum required resources to instantiate this IP and maximum clock frequency supported.

1.7. Naming Conventions

1.7.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

1.7.2. Signal Names

- *_n* are active low (asserted when value is logic 0)
- *_i* are input signals
- *_o* are output signals

1.7.3. Attribute Names

Attribute names in this document are formatted in title case and italicized (*Attribute Name*).

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2. Functional Description

2.1. IP Architecture Overview

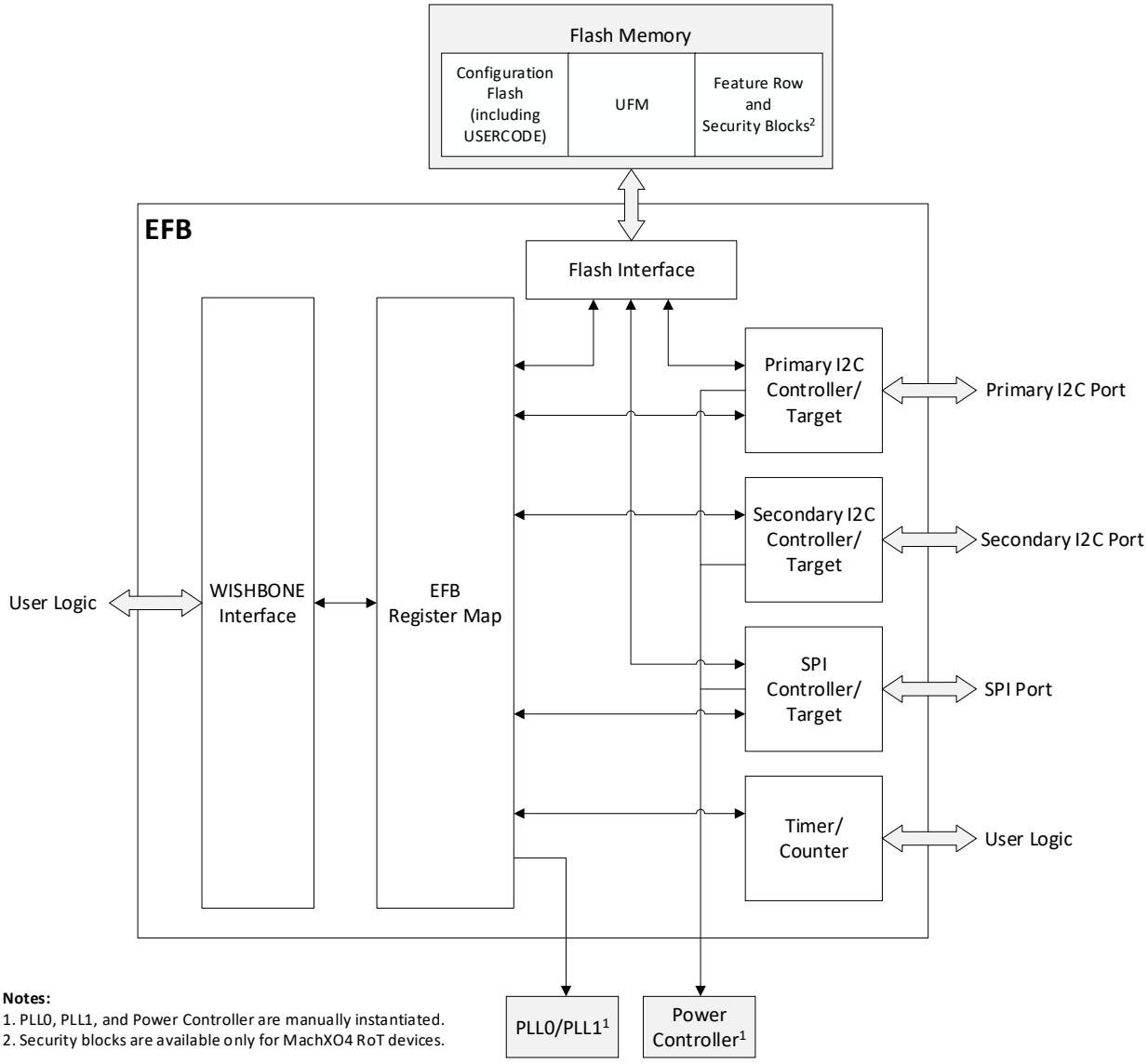


Figure 2.1. EFB Module IP Block Diagram

The hardened control function of MachXO4 devices is contained inside the EFB. You can interface with the logic through the WISHBONE interface to the EFB register map. Each hardened function can be controlled through these registers.

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2.2. Clocking

2.2.1. Clocking Overview

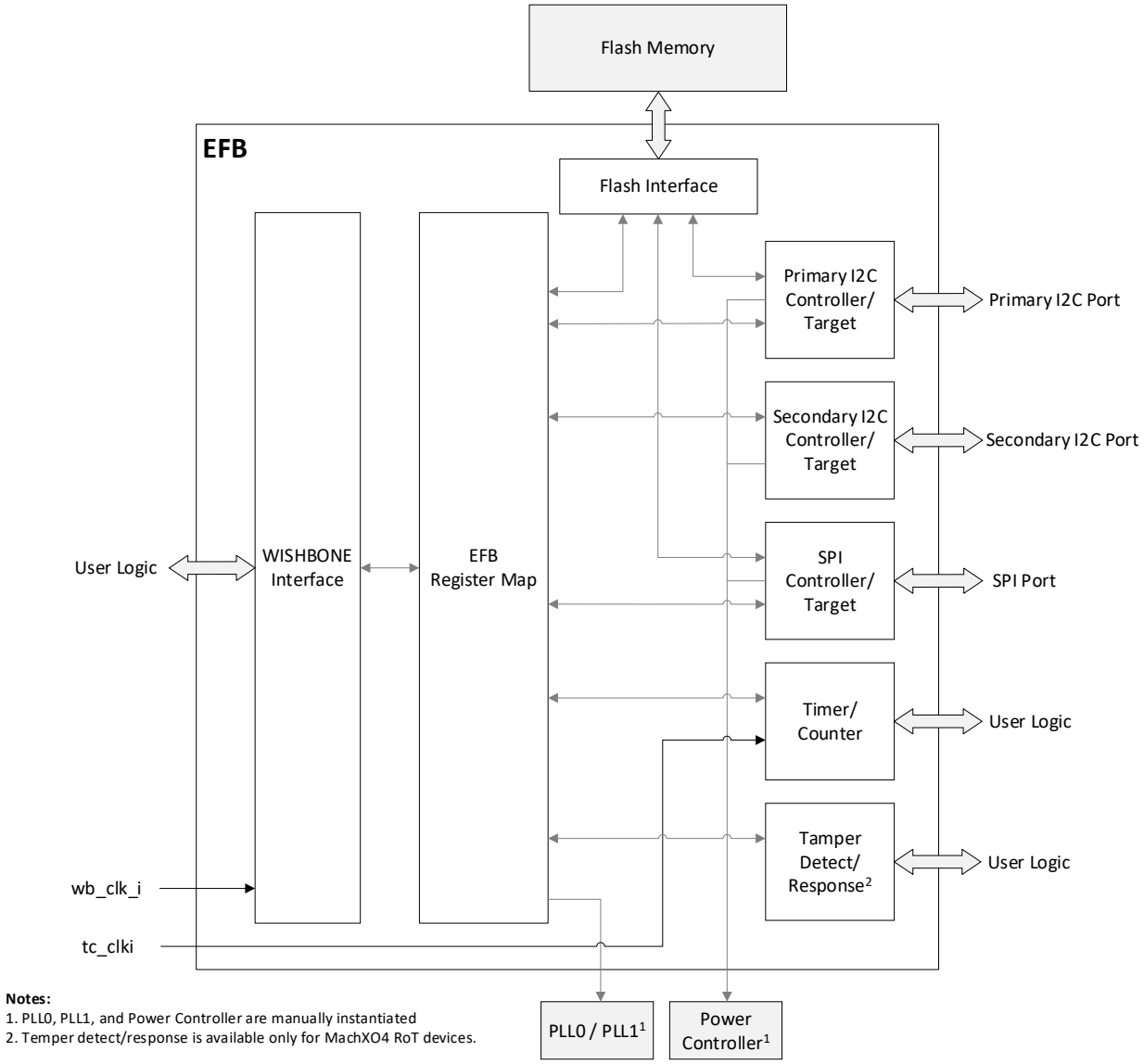


Figure 2.2. EFB Module IP Clock Overview

The WISHBONE interface clock is used by the WISHBONE interface logic and control registers.

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2.3. Reset

2.3.1. Reset Overview

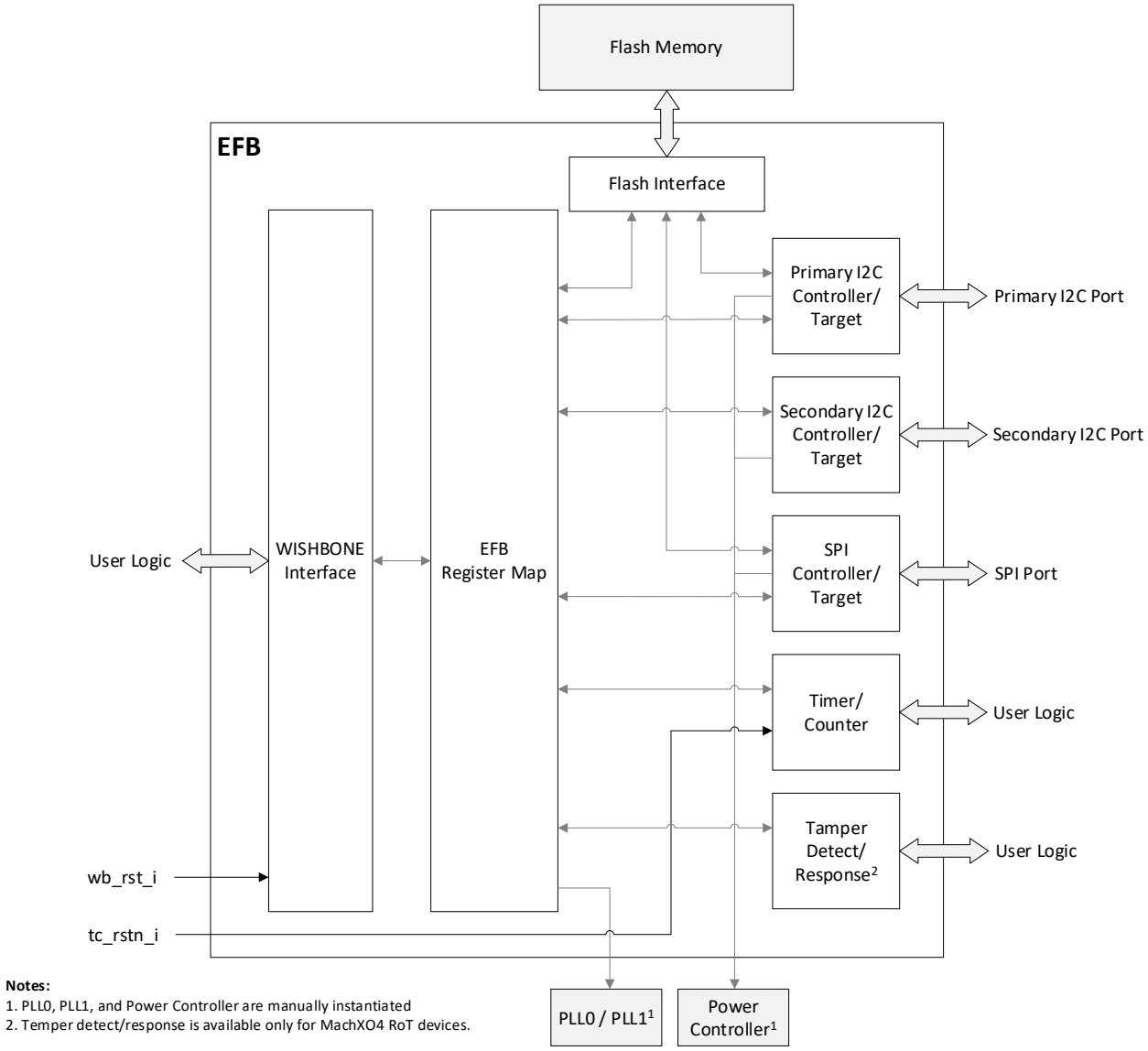


Figure 2.3. EFB Module IP Reset Overview

The WISHBONE interface reset signal only resets the WISHBONE interface logic.

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2.4. User Interfaces

Table 2.1. User Interfaces and Supported Protocols

User Interface	Supported Protocol	Description
Data/Control	WISHBONE (Target)	Provides connectivity between user logic and the EFB functional blocks. The user logic must include a WISHBONE initiator interface to communicate with the WISHBONE target of the EFB.
	I2C	Each MachXO4 device contains two hardened I2C IP cores, designated as primary and secondary. Both can operate as an I2C controller or target.
	SPI	Hardened SPI core, which can operate as both SPI controller and target, or solely as an SPI target device.
	APB	AMBA APB 3 protocol-compliant interface can be enabled to bridge transactions from a system bus to the WISHBONE target of the EFB.
	WISHBONE (Initiator)	Provides WISHBONE transactions for the dynamic reconfiguration of PLL configurations.

2.4.1. WISHBONE Bus Interface (Register Access)

The WISHBONE bus in this IP is compliant with the WISHBONE standard from OpenCores. The bus provides connectivity between the FPGA user logic and EFB functional blocks. You can implement a WISHBONE controller interface to interact with the EFB WISHBONE target interface. Table 4.1 provides a detailed definition of the WISHBONE signals.

The EFB WISHBONE bus supports the classic version of the WISHBONE standard. Because the WISHBONE bus is an open-source standard, not all features of the standard are implemented or required:

- Tags are not supported in the WISHBONE target interface of the EFB module. Because the EFB is a hardened block, you cannot add these signals.
- The target WISHBONE bus interface of the EFB module does not require the byte select signals (sel_i or sel_o), since the data bus is only a single byte wide.
- The EFB WISHBONE target interface does not support the optional error and retry access termination signals. The IP does not guarantee the WISHBONE behavior if it receives access to an invalid register. You need to stay within the valid address range detailed in the Register Description section.
- If the EFB WISHBONE input signals are not used, they must be connected to 0.
- To ensure correct operation, wb_cyc_i must be asserted for the entire WISHBONE transaction. For the EFB WISHBONE interface, wb_cyc_i and wb_stb_i may be connected together.

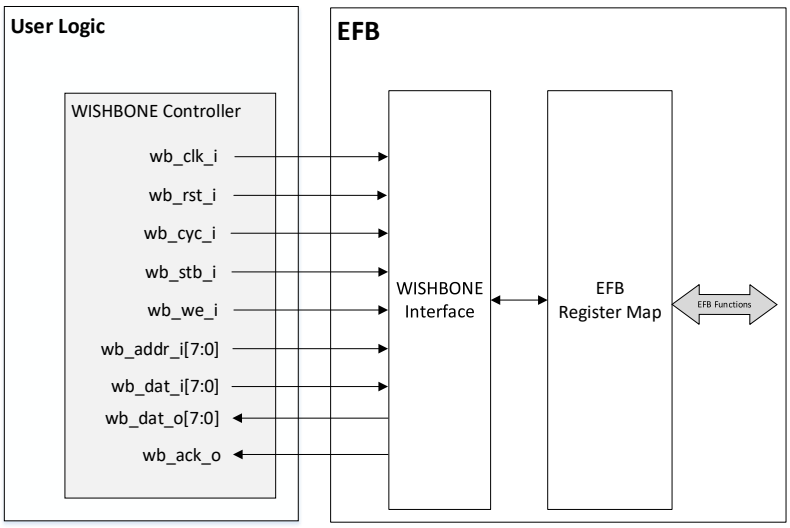


Figure 2.4. EFB Module WISHBONE Interface

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2.4.2. I2C IP Cores

I2C is a widely used two-wire serial bus for communication between devices on the same board. Every MachXO4 device contains two hardened I2C IP cores, designated as the primary and secondary I2C IP cores. Either of the two cores can operate as an I2C controller or I2C target. The difference between the two cores is that the primary core has pre-assigned I/O pins, while the ports of the secondary core can be assigned to any general-purpose I/O (GPIO).

When instantiating the hardened I2C IP cores for target operations, the EFB *wb_clk_i* input must be connected to a valid clock source of at least 7.5 × the I2C bus rate. For example, >3.0 MHz when I2C rate = 400 kHz.

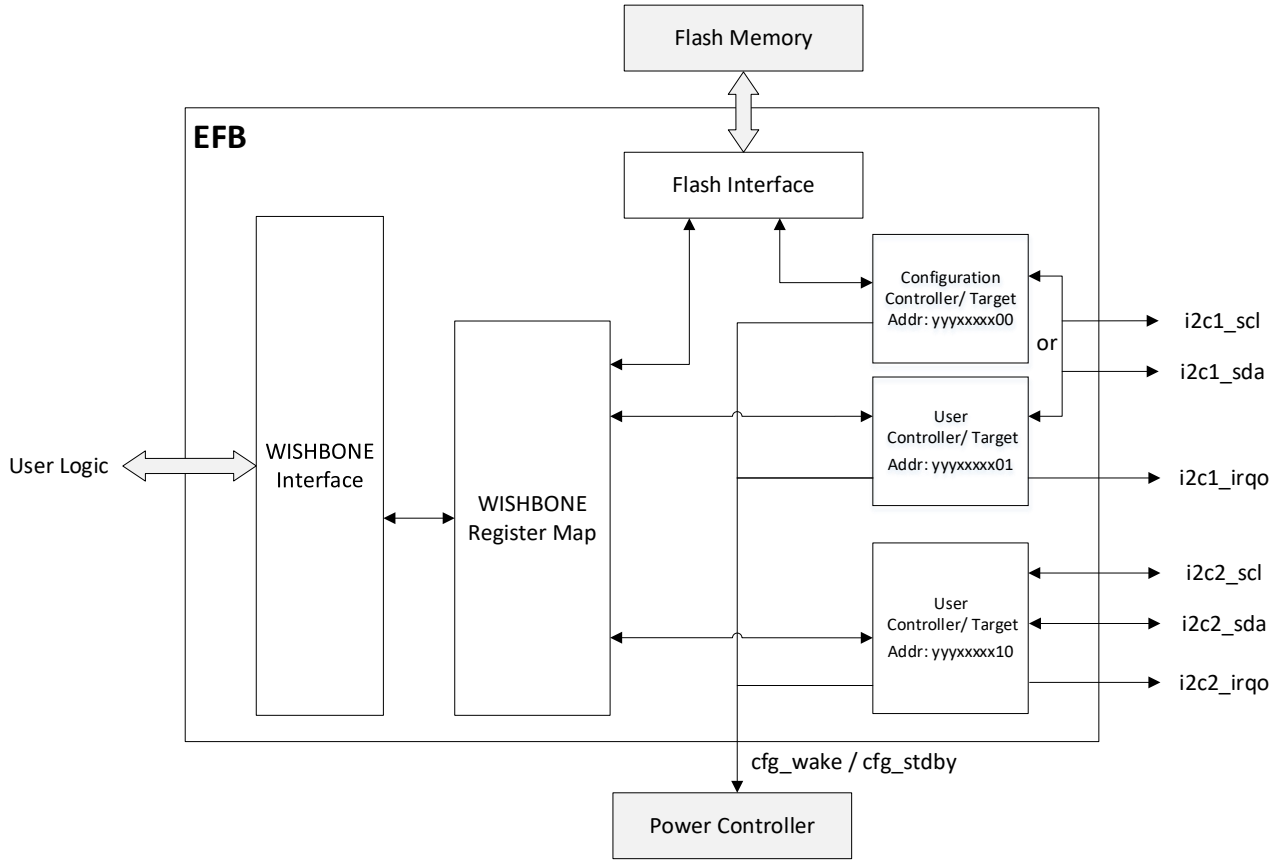


Figure 2.5. EFB Module I2C Core Interface

2.4.2.1. Primary I2C

The main functions of the primary controller are:

- Either:
  - I2C configuration target provides access to the flash; or
  - I2C user target provides access to the user logic.
- I2C user controller provides access to peripherals attached to the MachXO4 device.

The primary I2C core can access the flash memory. However, the primary I2C port cannot be used for both flash access and user functions in the same design. Figure 2.5 shows an interface between the I2C block and the flash access.

The I2C controller accesses target I2C peripherals on a bus by calling the unique addresses of the target. The primary configuration address is yyyxxxxx00 and the primary user address is yyyxxxxx01, where y and x are user programmable from IP generation.

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2.4.2.2. Secondary I2C

The secondary I2C controller in a MachXO4 device provides the same functionality as the primary I2C controller with the exception of access to the flash memory. The i2c2_scl and i2c2_sda ports are routed through the general purpose routing of the FPGA fabric and you can assign them to any GPIO.

Target I2C peripherals on a bus are accessed by the user controller I2C calling the unique addresses of the target. The secondary user address is yyyxxxxx10, where y and x are user programmable from IP generation.

2.4.3. SPI IP Core

SPI is a widely used four-wire serial bus that operates in full-duplex mode for communication between devices. The MachXO4 EFB includes an SPI controller that can be configured either as both an SPI controller/target, or solely as an SPI target.

When configured as a controller/target, the IP core can control up to eight other devices with SPI target interfaces. When configured as a target, the IP core can interface to an external SPI controller device.

The SPI core interfaces with either the configuration logic of the MachXO4 device or other user logic. The functionality and block diagram of the hardened SPI IP core are shown below.

Table 2.2. Hardened SPI Functionality

Feature	Configuration SPI	User SPI
SPI target port	Yes	Yes
SPI controller port	No	Yes
Access to Flash memory	Yes	No
Requires dedicated I/O	Yes	Yes
Wake Power Controller from Standby Mode	Yes	Yes
Enter Power Controller Standby Mode	No	Yes

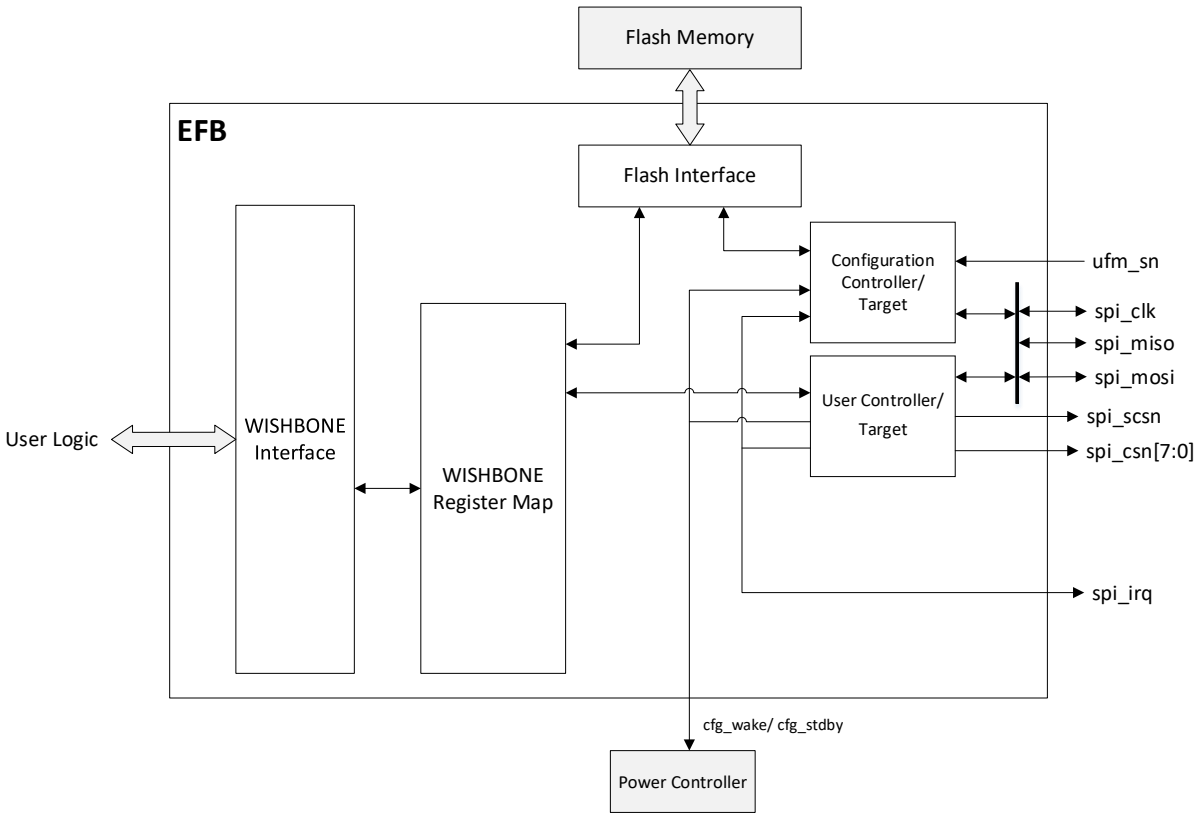


Figure 2.6. EFB Module SPI Core Interface

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2.4.4. APB

By default, EFB module registers are accessed through the native WISHBONE interface. When APB is selected as the user interface, an APB-to-WISHBONE bridge is automatically included, allowing APB requesters to access the EFB register map. The APB interface complies with the AMBA APB3 protocol. The EFB register map remains internally connected through the WISHBONE interface.

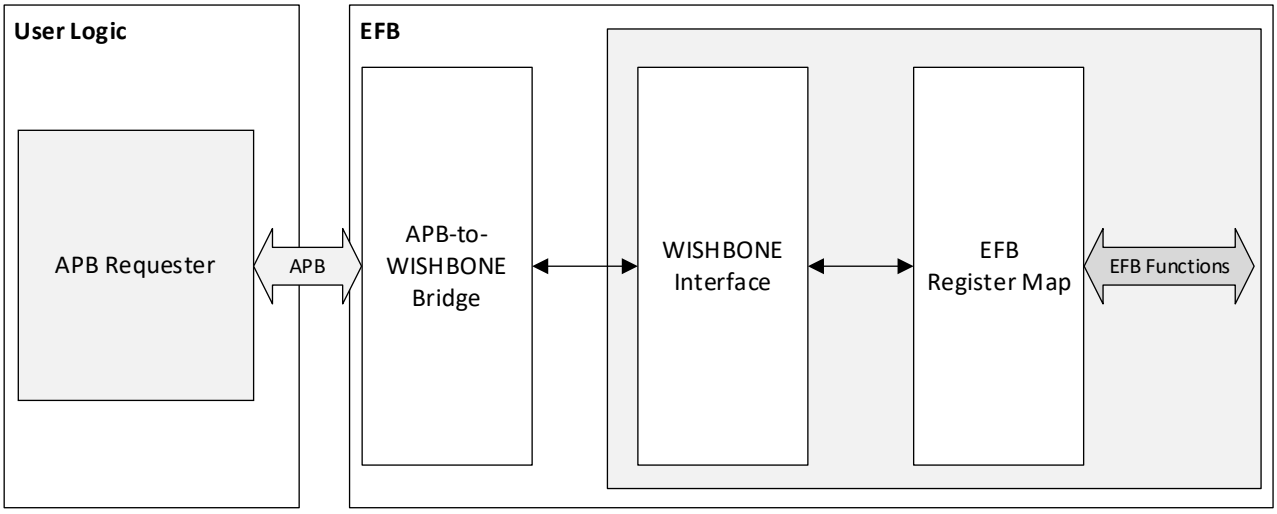


Figure 2.7. EFB Module APB Interface

2.4.5. WISHBONE Controller (for PLL)

The WISHBONE interface of the EFB module can be used to dynamically update the configurable settings of the PLL IPs in MachXO4 devices. Each MachXO4 device supports up to two PLLs.

By connecting the EFB WISHBONE interface to the PLL interface, PLL0 has an address range from 0x00 to 0x1F, while PLL1 (if applicable) has an address range from 0x20 to 0x3F in the EFB register map.

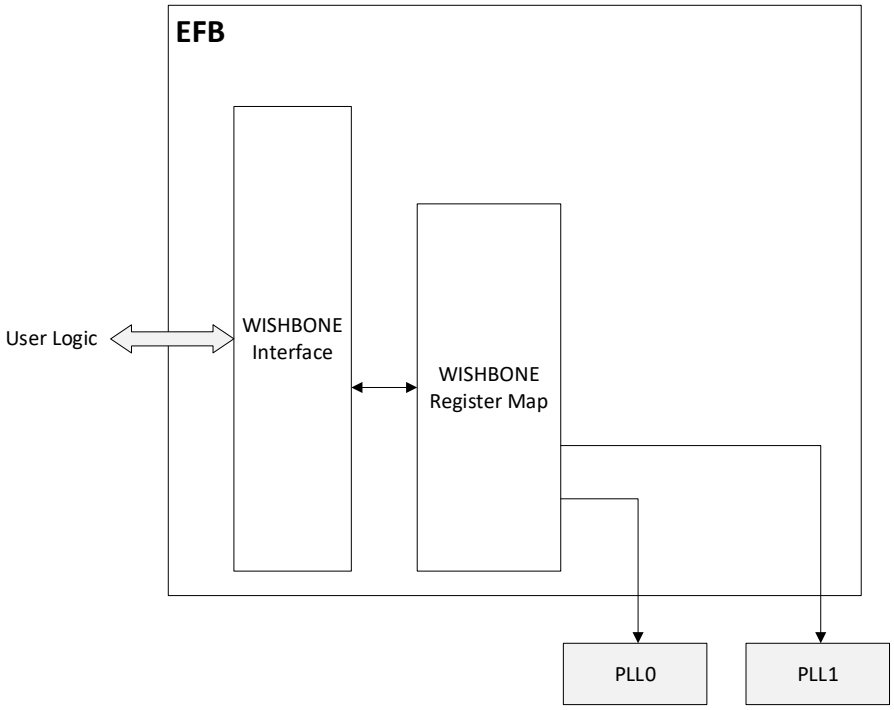


Figure 2.8. EFB Interface to Dynamic PLL

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2.5. Flash Access Interface

You can access the flash logic interface using the JTAG, SPI, I2C, or WISHBONE interfaces.

The MachXO4 flash memory consists of three sectors:

- Configuration flash (Sector 0)
- UFM (Sector 1)
- Feature Row

The MachXO4 RoT flash memory consists of multiple subsectors:

- Two configuration memory sectors (CFG0 and CFG1)
- Four user flash memory sectors (UFM0, UFM1, UFM2, and UFM3)
- One feature row sector (FEA)
- One public key sector (PUBKEY)
- One Advanced Encryption Standard key sector (AESKEY)
- One configuration security setting sector (CSEC)
- One user security setting sector (USEC)

Refer to the MachXO4 Programming and Configuration User Guide (FPGA-TN-02393) for more implementation details.

The ports used to access the flash memory are shown in the table below.

Table 2.3. Flash Memory (UFM/Configuration) Access

Interface	UFM	Configuration Flash
JTAG	Yes	Yes
Target SPI Port with Chip Select (ufm_sn)	Yes	Yes
Target SPI Port with Chip Select (spi_scsn)	No	No
Primary Target I2C Port address (yyyxxxxx00)	Yes	Yes
Primary Target I2C Port address (yyyxxxxx01)	No	No
Secondary Target I2C Port address (yyyxxxxx10)	No	No
WISHBONE	Yes	Yes

The flash memory is organized in pages and is not byte addressable. Each page has 128 bits (16 bytes).

The configuration logic arbitrates access from the interfaces according to the following priority. When higher priority ports are enabled, flash access by lower priority ports is blocked:

- JTAG port – All MachXO4 devices include a JTAG port that supports read/write operations to Flash. The JTAG port complies with IEEE 1149.1 and IEEE 1532 specifications. JTAG port has the highest priority for Flash operations.
- SPI target port – All MachXO4 devices include an SPI target port that supports read/write operations to Flash. Asserting the UFM/Flash target chip select (ufm_sn) enables access.
- I2C primary port – All MachXO4 devices include an I2C port that supports read/write operations to Flash. The primary configuration I2C address is yyyxxxxx00, where *y* and *x* are user-programmable bits.
- WISHBONE target interface – The WISHBONE interface of the EFB module enables designers to access the UFM/Flash from FPGA user logic by creating a WISHBONE controller.

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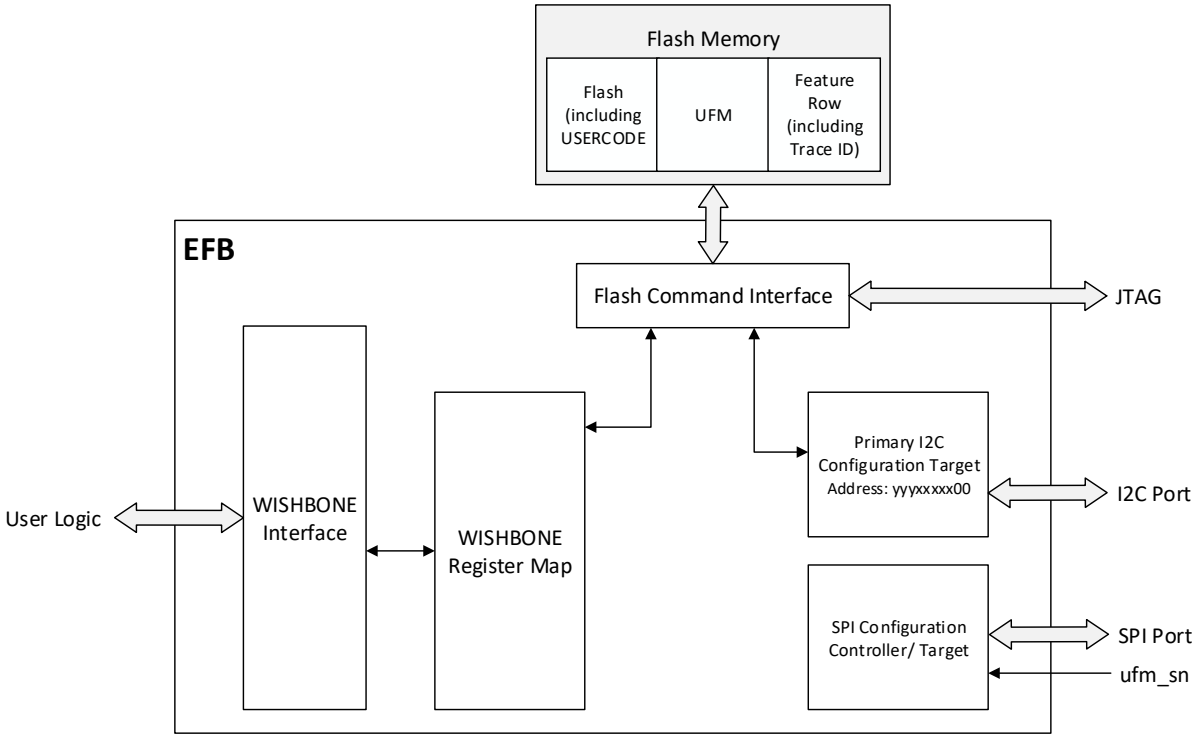


Figure 2.9. EFB Module Flash Interface

The WISHBONE interface of the EFB module allows a WISHBONE host to access the configuration resources of MachXO4 devices. This is useful for reading data from configuration resources such as USERCODE and Trace ID. Most importantly, this feature allows you to update the flash array of the devices while the device is in operation mode. This is a self-configuration operation. Upon power-up or a configuration refresh operation, the new content of the CFG flash is loaded into the configuration SRAM, and the device continues operation with the new configuration.

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3. IP Parameter Description

The configurable attributes of the EFB Module IP are shown in the following tables. You can configure the IP by setting the attributes accordingly in the IP Catalog's Module/IP wizard of the Lattice Radiant software.

Wherever applicable, default values are in **bold**.

3.1. EFB Enables

Table 3.1. EFB Enables Attributes

Attribute	Selectable Values	Description
User Interface Options		
Enable User Interface	**Checked,** Unchecked	Enables the selected user interface for user logic. Some EFB features require a user interface to be enabled.
User Interface	WISHBONE, APB	Configures either the default WISHBONE interface or the AMBA APB-compliant protocol interface to bridge WISHBONE transactions.
APB Data Width	**8**, 32	Configures the APB data bus width (apb_pwdata_i, apb_prdata_o). When *APB Data Width* is 32, only the lower 8 bits are used.
APB Address Width	**8**–32	Configures the APB address bus width (apb_addr_i). When *APB Data Width* is 32, the EFB register addressing is 4-byte aligned (minimum width is 10).
User Interface Clock Frequency	1 MHz – 133 MHz, **50 MHz**	Specifies the input value for the WISHBONE interface clock frequency. This value also affects the required clock prescale, depending on the selected I2C bus performance.
I2C Options		
Primary I2C	**Checked,** Unchecked	Enables access to the primary I2C (I2C1) ports.
Primary I2C Access Type (if Primary I2C Enabled)	**User Function,** Flash Access	Configures whether primary I2C (I2C1) access is assigned to user functions/logic or to UFM/configuration. This setting affects the primary I2C target address.
Secondary I2C	Checked, **Unchecked**	Enables access to the secondary I2C (I2C2) ports.
SPI Options		
SPI	Checked, **Unchecked**	Enables access to the SPI core ports.
Timer/Counter Options		
Timer/Counter	Checked, **Unchecked**	Enables the Timer/Counter features.
Allow Dynamic Register Changes (via User Interface)	Checked, **Unchecked**	Enables dynamic control of the Timer/Counter registers.
PLL Options		
PLL (Dynamic Access)	Checked, **Unchecked**	Enables the WISHBONE ports for dynamic control of the PLL registers. PLL must be included in the design, and WISHBONE ports must be enabled.
Number of PLLs for dynamic access	**1**,2	Configures the number of PLLs for dynamic access. The number of available PLLs depends on the specific MachXO4 device.
UFM Options		
User Flash Memory	Checked, **Unchecked**	Enables user flash memory access through the EFB, allowing access from user logic through the WISHBONE bus, primary configuration I2C, or configuration SPI.
Boot Settings[1]	**Internal Boot**, External Boot	Configures whether flash sectors are reserved for boot images (internal boot) or not (external boot).
Internal Boot Settings[1]	**Single Boot**, Dual Boot	Configures the reservation of flash memory for one or two boot images.
Image0 Options[1, 2]	**CFG0 only**, CFG0 and UFM0	Configures the flash sectors used for Image0.

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Attribute	Selectable Values	Description
Image1 Options[1, 2]	**CFG1 only**, CFG1 and UFM1	Configures the flash sectors used for Image1.
Total available UFM[1]	(Display only)	Displays the total number of usable UFM pages.
UFM used in EFB[1]	(Display only)	Displays the total number of UFM pages configured for EFB usage.
Enable UFM CFG0 – located at FLASH-A[1]	Checked, **Unchecked**	Enables access to the CFG0 sector.
UFM CFG0 located at FLASH-A total number of pages[1]	(Display only)	Displays the number of usable pages for the CFG0 sector.
Enable UFM UFM0 – located at FLASH-A[1]	Checked, **Unchecked**	Enables access to the UFM0 sector.
UFM UFM0 – located at FLASH-A[1]	(Display only)	Displays the number of usable pages for the UFM0 sector.
Enable UFM CFG1 – located at FLASH-B[1]	Checked, **Unchecked**	Enables access to the CFG1 sector.
UFM CFG1 located at FLASH-B total number of pages[1]	(Display only)	Displays the number of usable pages for the CFG1 sector.
Enable UFM UFM1 – located at FLASH-B[1]	Checked, **Unchecked**	Enables access to the UFM1 sector.
UFM UFM1 – located at FLASH-B[1]	(Display only)	Displays the number of usable pages for the UFM1 sector.
Enable UFM UFM2 – located at FLASH-A[1]	Checked, **Unchecked**	Enables access to the UFM2 sector.
UFM UFM2 located at FLASH-B total number of pages[1]	(Display only)	Displays the number of usable pages for the UFM2 sector.
Enable UFM UFM3 – located at FLASH-C[1]	Checked, **Unchecked**	Enables access to the UFM3 sector.
UFM UFM3 - located at FLASH-C[1]	(Display only)	Displays the number of usable pages for the UFM3 sector.
Tamper Detect/Response Options[1]		
Enable Tamper Detection/Response	Checked, **Unchecked**	Enables Tamper Detection/Response features

Notes:

1. Available only for MachXO4 RoT devices.
2. Available only when *Boot Settings* = *Internal Boot*.

3.2. I2C

Table 3.2. I2C Attributes

Attribute	Selectable Values	Description
Primary I2C (Primary I2C = Enabled)		
General Call Enable	Checked, **Unchecked**	Enables general call response for the primary I2C target. The general call address is *0000000* for both 7-bit and 10-bit addressing.
Wakeup Enable	Checked, **Unchecked**	Enables the Wakeup (cfg_wake) and Standby (cfg_stdby) signals from the primary I2C for the Power Controller.
I2C Bus Performance	50 kHz, **100 kHz,** 400 kHz	Specifies the input configuration for the primary I2C clock frequency as the controller.

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Attribute	Selectable Values	Description
Clock Pre-scale Value	(Display only) **125**	Displays the initial configuration of the clock prescale based on the set user interface (WISHBONE) clock frequency and primary I2C bus performance. The WISHBONE clock frequency is divided by the prescale value × 4 to produce the primary I2C controller clock frequency.
I2C Addressing	**7-bit,** 10-bit	Configures whether the primary I2C uses a 7-bit or 10-bit addressing scheme on the bus.
I2C Device Address	**10000**	The input address (in binary) for the primary I2C target.
Primary I2C/Flash Access Device Address	(Display only) **0b1000001** (User)/0b1000000 (Flash)	Displays the address of the primary I2C based on the input device address and the primary I2C access type.
Secondary I2C (Secondary I2C = Enabled)		
General Call Enable	Checked, **Unchecked**	Enables general call response for the secondary I2C target. The general call address is *0000000* for both 7-bit and 10-bit addressing.
Wakeup Enable	Checked, **Unchecked**	Enables the Wakeup (cfg_wake) and Standby (cfg_stdby) signals from the secondary I2C for the Power Controller.
I2C Bus Performance	50 kHz, **100 kHz,** 400 kHz	Specifies the input configuration for the secondary I2C clock frequency as the controller.
Clock Pre-scale Value	(Display only) **125**	Displays the initial configuration of the clock prescale based on the set user interface (WISHBONE) clock frequency and secondary I2C bus performance. The WISHBONE clock frequency is divided by the prescale value × 4 to produce the secondary I2C controller clock frequency.
I2C Addressing	**7-bit,** 10-bit	Configures whether the secondary I2C uses a 7-bit or 10-bit addressing scheme on the bus.
I2C Device Address (shows only if Primary I2C is Disabled)	**10000**	The input address (in binary) for the secondary I2C target.
Secondary I2C Device Address	(Display only) **0b1000010** (User)	Displays the address of the secondary I2C based on the input device address.

3.3. SPI

Table 3.3. SPI Attributes

Attribute	Selectable Values	Description
General (SPI = Enabled)		
SPI Mode	**Target**, Controller and Target	Selects either target mode, or both controller and target modes for the initial mode of the SPI core. Selecting controller and target modes enables SPI Controller settings, which include Controller Clock Rate and Controller Chip Selects. This option can be updated dynamically by modifying the MSTR bit in the SPICR2 register.
Wakeup Enable	Checked, **Unchecked**	Enables the SPI core to send Wakeup signals (cfg_wake and cfg_stdby) to the Power Controller, allowing the device to exit standby mode when the user target SPI chip select (spi_csn[0]) is driven low. This option can be updated dynamically by modifying the WKUPEN_USER bit in the SPICR1 register.

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Attribute	Selectable Values	Description
Controller Clock Rate (SPI = Enabled AND SPI Mode = *Controller and Target*)		
Desired (MHz)	1-**45**	Specifies the input configuration for the SPI core clock when operating as a controller.
Actual (MHz)	(Display only) **1**	Displays the actual SPI core clock based on the desired input frequency. The actual clock frequency is determined by the nearest whole prescale value.
Clock Pre-scale Value	(Display only) **50**	Displays the initial prescale value configuration set in the registers, based on the actual SPI core clock.
Controller Chip Selects (SPI = Enabled AND SPI Mode = *Controller and Target*)		
Number of Chip Selects	**1**-8	Configures the number of SPI targets that can be connected to the SPI core when operating as a controller. This setting affects the bit width of the spi_csn signal.
Protocol Options (SPI = Enabled)		
LSB First	Checked, **Unchecked**	Specifies the order of the serial shift of a byte of data. The data order (MSB-first or LSB-first) is programmable within the SPI core. This option can be updated dynamically by modifying the LSBF bit in the SPICR2 register.
Inverted Clock	Checked, **Unchecked**	When enabled, the clock edge changes from rising to falling edge. This option can be updated dynamically by accessing the CPOL bit of the SPICR2 register.
Phase Adjust	Checked, **Unchecked**	Specifies the phase change to match the application. This option can be updated dynamically by accessing the CPHA bit in the SPICR2 register.
Target Handshake Mode	Checked, **Unchecked**	Enables Lattice proprietary extension to the SPI protocol. Use this option when an internal support circuit (such as a WISHBONE host) cannot respond with initial data within the required time; it ensures the SPI target read-out data is predictably available at high SPI clock rates. This option can be updated dynamically by accessing the SDBRE bit in the SPICR2 register.
SPI – Interrupts		
Enable Port	Checked, **Unchecked**	Enables the interrupt request output signal (spi_irq) from the SPI core. This signal is intended to be connected to a WISHBONE controller and to request an interrupt when a specific condition is met.
Tx Ready	Checked, **Unchecked**	An interrupt that indicates the SPI transmit data register (SPITXDR) is empty. When enabled, indicates TRDY is asserted. This option can be changed dynamically by modifying the IRQTRDYEN bit in the SPICSR register.
Rx Ready	Checked, **Unchecked**	An interrupt that indicates the receive data register (SPIRXDR) contains valid receive data. When enabled, indicates RRDY is asserted. This option can be changed dynamically by modifying the IRQRRDYEN bit in the SPICSR register.
Tx Overrun	Checked, **Unchecked**	An interrupt that indicates the target SPI chip select (spi_scsn) is driven low while being transacted by the SPI Controller. When enabled, indicates MDF (Mode Fault) is asserted. This option can be changed dynamically by modifying the IRQMDFEN bit in the SPICSR register.

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Attribute	Selectable Values	Description
Rx Overrun	Checked, **Unchecked**	An interrupt that indicates SPIRXDR received new data before the previous data is captured. When enabled, indicates ROE is asserted. This option can be changed dynamically by modifying the IRQROEEN bit in the SPICSR register.

3.4. Timer/Counter

Table 3.4. Timer/Counter Attributes

Attribute	Selectable Values	Description
Mode Selection		
Timer/Counter Mode	Watchdog Timer, **Clear Timer on Compare Match (CTCM)**, Fast PWM, Phase/Freq Correct PWM (PFCPWM)	Configures between different Timer/Counter modes of operation. Refer to the following subsections for a detailed discussion of each mode.
Output Function	Static, **Toggle**, Wave Generator, Inverted Wave Generator	Configures the function of the output signal (tc_oc) of the Timer/Counter IP. The available functions are: • Static – output is static low. • Toggle – output toggles based on conditions defined by the Timer/Counter settings. • Wave Generator – generates a waveform based on Set/Clear conditions defined by the Timer/Counter settings. • Inverted Wave Generator – generates an inverted waveform.
Clock Selection		
Clock Edge Selection	**Positive**, Negative	Selects the edge of the input clock source.
Use On-chip Oscillator	Checked, **Unchecked**	Enables the use of the on-chip oscillator.
Prescale Divider Value	0, **1**, 8, 64, 256, 1024	Configures the prescale value to divide the input clock prior to reaching the 16-bit counter. This option can be updated dynamically by modifying the PRESCALE[2:0] bits of the TCCR1 register.
Enable Interrupt Register		
Overflow	Checked, **Unchecked**	Enables an interrupt that indicates the counter matches the TCTOP0/1 register value. When enabled, indicates OVF is asserted. This option can be updated dynamically by modifying the IRQOVFEN bit of the TCIRQEN register. Available if *Allow Dynamic Register Changes (via User Interface)* is enabled.
Output Compare Match	Checked, **Unchecked**	Enables an interrupt that indicates when counter matches the TCOCR0/1 register value. When enabled, indicates OCRF is asserted. This option can be updated dynamically by modifying the IRQOCRFEN bit of the TCIRQEN register. Available if *Allow Dynamic Register Changes (via User Interface)* is enabled.

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Attribute	Selectable Values	Description
Input Compare	Checked, **Unchecked**	Enables an interrupt that indicates the TC_IC input signal is asserted. When enabled, indicates ICRF is asserted. This option can be updated dynamically by modifying the IRQICRFEN bit of the TCIRQEN register. Available if *Allow Dynamic Register Changes (via User Interface)* is enabled.
Standalone Overflow (no User Interface)	Checked, **Unchecked**	Enables the overflow interrupt without the user interface and serves as the only available interrupt request. Available only if *Allow Dynamic Register Changes (via User Interface)* is disabled.
Counter Values		
Set Top Counter Value	Checked, **Unchecked**	Enables setting a specific Timer/Counter top value, other than the maximum.
Timer/Counter Top	0–**65535**	Configures the top value of the Timer/Counter.
Output Compare Value	0–65535, **32767**	Configures the compare value of the Timer/Counter for PWM modes.

3.4.1. Watchdog Timer Mode

Watchdog timers monitor operating behavior of a system and provide a reset or interrupt when the microcontroller of the system or embedded state machine is no longer operational.

One use case is for a microcontroller to reset the Watchdog Timer to 0x0000 before starting a process. The microcontroller must complete the process and reset the Watchdog Timer again before the timer reaches its terminal count. If the microcontroller fails to clear the timer in time, the Watchdog Timer asserts a strobe signal indicating that the time has expired. The system uses this strobe to gracefully recover the system.

Another use case is to periodically turn off system modules to save power. The Watchdog Timer can also be used to interact with the on-chip power controller of a MachXO4 device.

The most commonly used ports of the Timer/Counter in Watchdog Timer mode are the clock, reset, and interrupt.

Optionally, the user interface can be used to read time stamps from the TCICR register and update the top value of the counter.

3.4.2. Clear Timer on Compare Match Mode

CTCM (Clear Timer on Compare Match) operates as a basic counter with interrupt capability. The counter automatically clears to 0x0000 when the counter value in the TCCNT register matches the value in the TCTOP register.

The TCTOP register value can be dynamically updated through the WISHBONE interface or assigned as a static value during IP generation. By default, the TCTOP register holds the value 0xFFFF.

The data loaded into the timer counter to define the top counter value is double-registered. The user interface controller writes the data to the TCTOPSET register, which is then automatically loaded into the TCTOP register at the moment of auto-clear. Therefore, a new top value can be written to the TCTOPSET register after the overflow flag asserts and during the counting-up to the top value.

Updating the value of the TCTOP register changes the frequency of the Timer/Counter output signal.

Refer to the following figure for the Timer/Counter CTCM output waveform.

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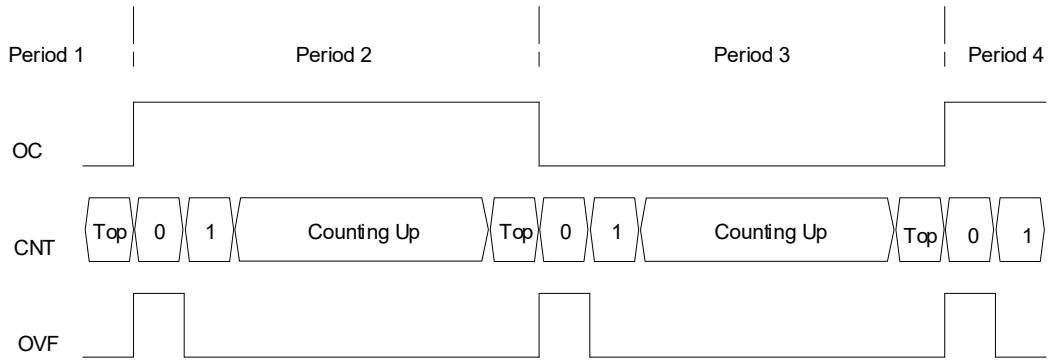


Figure 3.1. Timer/Counter CTCM Output Waveform

3.4.3. Fast PWM Mode

PWM is a widely used technique to digitally control analog circuits. PWM uses a rectangular pulse wave whose pulse width is modulated, resulting in the variation of the average value of the waveform.

The period and the duty cycle of the waveform can be varied by loading 16-bit digital values into:

- the TCTOP register to define the top value of the counter, and
- the TCOCR register to provide a compare value for the output of the counter.

The Timer/Counter output is cleared when the counter value matches the top value that is loaded into the TCTOP register. The output is set when the value of the counter matches the compare value that is loaded into the TCOCR register. These clear/set functions can be inverted, allowing the output of the Timer/Counter to be set when the counter value matches the top value and cleared when the value of the counter matches the compare value.

The interrupt line can be used for Overflow Flag (OVF) and Output Compare Flag (OCRF).

Refer to the following figure for the PWM waveform generation, where the Timer/Counter output is configured to be set when the counter matches the top value and cleared when the counter matches the compare value.

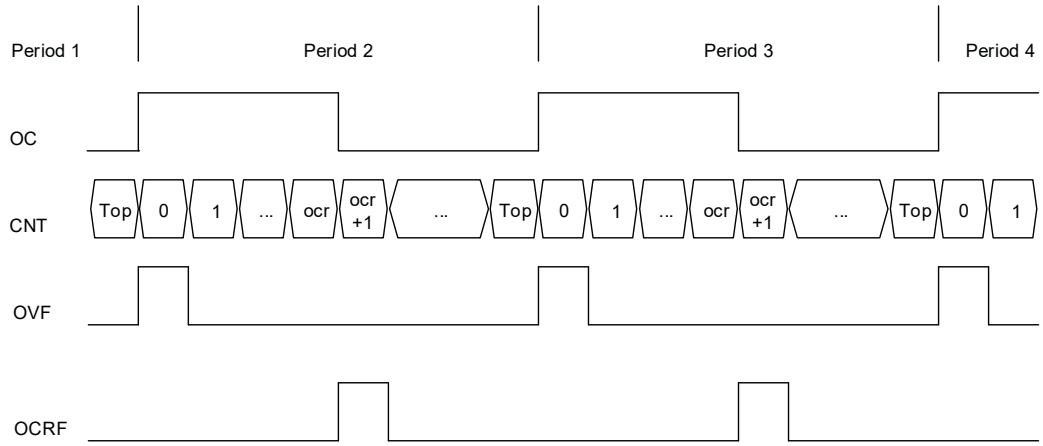


Figure 3.2. Fast PWM Mode Waveform Generation

3.4.4. Phase and Frequency Correct PWM Mode

In phase and frequency correct PWM mode, the counting direction changes from up to down when the counter is incrementing to the top value (top value minus 1). When the counter is decrementing from 0x0001 to 0x0000, the following occurs:

- The TCTOP register is updated with the value loaded in the TCTOPSET register.
- The TCOCR register is updated with the value loaded in the TCOCRSET register.
- The Overflow Flag TCSR[OVF] is asserted for one clock cycle.

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The output of the Timer/Counter is updated only when the counter value matches the compare value in the TCOCR register. This match occurs twice within one period:

- The first match occurs when the counter is counting up.
- The second match occurs when the counter is counting down.

The Output Compare Flag TCSR[OCRF] is asserted when both matches occur.

The output of the Timer/Counter is set on the first compare match and cleared on the second compare match.

The order of set and clear can be inverted.

This mode allows you to adjust the frequency (based on the top value) and phase (based on the compare value) of the generated waveform.

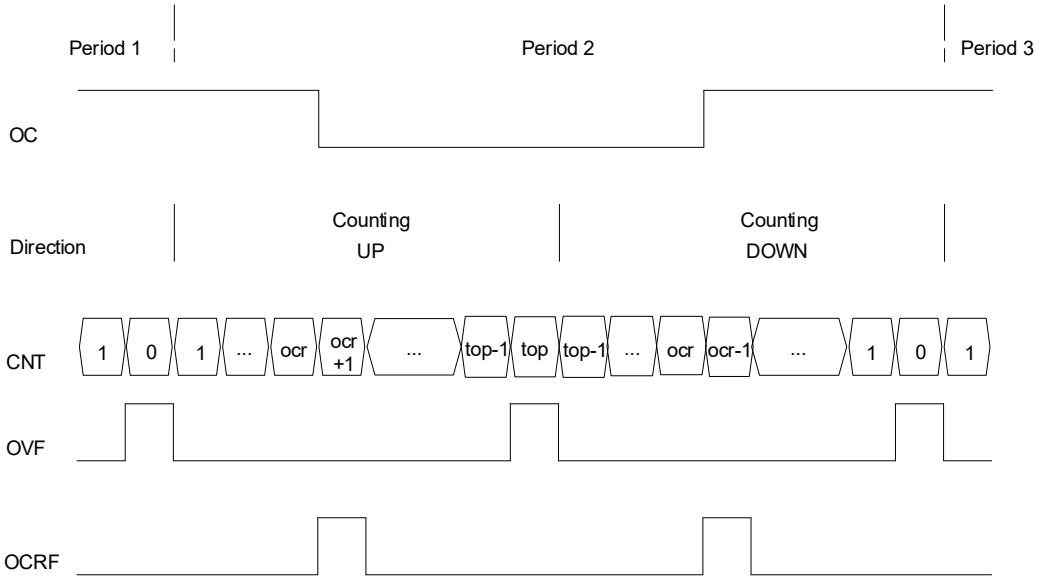


Figure 3.3. Phase/Frequency Correct PWM Mode Waveform Generation

3.5. CFG/UFM

Table 3.5. UFM Attributes

Attribute	Selectable Values	Description
User Flash Memory (User Flash Memory = Enabled)		
Number of Pages	**1**–<sector max pages>	The input value to indicate the start page of the flash memory initialization. The range is calculated based on the available device UFM resource.
Initialization Data Start Page	(Display only)	Calculated based on the available device UFM resource.
Initialize Flash Memory with All 0s	**Checked,** Unchecked	Enables initialization of the flash memory to all zeroes.
UFM Initialization Data File	**<file>**	Specifies the input file containing initialization data for the flash memory.
UFM/CFG Initialization Data File Format	**Hexadecimal,** Binary	Configures whether the input file format is hexadecimal or binary.

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3.5.1. Initializing UFM

You can initialize the UFM sector with system-level non-volatile data during IP generation. Each flash sector options tab appears when the sector is enabled. The *Number of Pages* attribute defines the number of pages to be preloaded with initialization data. Because the initialization data is bottom-justified, the *Initialization Data Start Page* attribute indicates the address of the first page initialized with the contents of the memory file.

For more information on programming MachXO4 devices, refer to the following documents:

- MachXO4 Hardened Control Functions User Guide (FPGA-TN-02403)
- MachXO4 Hardened Control Functions Reference Guide (FPGA-TN-02404)

3.6. Tamper

This section applies only to MachXO4 RoT devices.

Table 3.6. Tamper Attributes

Attribute	Selectable Values	Description
Tamper Type Register		
Password Protection	Checked**, Unchecked**	Enables the Password Protection Access Detect feature.
Locked Flash or SRAM	Checked**, Unchecked**	Enables the Memory (Flash/SRAM) Tampering Detect feature.
Manufacture Mode	Checked**, Unchecked**	Enables the Manufacturing Access Tampering Detect feature.
Tamper Source Register		
JTAG Port	Checked**, Unchecked**	Enables monitoring and reporting with JTAG as the tamper source.
SSPI Port	Checked**, Unchecked**	Enables monitoring and reporting with Target SPI as the tamper source
SI2C Port	Checked**, Unchecked**	Enables monitoring and reporting with Target I2C as the tamper source
WB Port	Checked**, Unchecked**	Enables monitoring and reporting with WISHBONE as the tamper source
Tamper Port Lock		
Port Lock	Checked**, Unchecked**	Enables the port lock feature for a configuration interface after a tamper event is detected.

For a detailed description of the Tamper Detect feature, refer to the MachXO4 Root of Trust Tamper Detection/Response (FPGA-TN-02434).

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4. Signal Description

This section describes the EFB Module IP ports.

Table 4.1. EFB Module IP Ports

Port	Type	Description
Wishbone Interface (Available when User Interface = WISHBONE)		
wb_clk_i	Input	The positive-edge clock used by the WISHBONE interface registers and hardened functions, supporting speeds up to 133 MHz.
wb_rst_i	Input	The synchronous reset signal for the WISHBONE interface. This reset terminates the active bus cycle. Wait 1 µs after deassertion before starting a WISHBONE transaction. This reset does not reset the contents of any registers.
wb_cyc_i	Input	Indicates a valid bus cycle on the WISHBONE interface.
wb_stb_i	Input	The strobe signal indicating the WISHBONE is the target for the current transaction on the bus. The wb_ack_o signal asserts an acknowledgment in response to the assertion of the strobe.
wb_we_i	Input	The write/read control signal. Logic low indicates a read operation, while logic high indicates a write operation.
wb_adr_i[7:0]	Input	The address signal for the WISHBONE interface, which is used to select a specific EFB register during write cycles.
wb_dat_i[7:0]	Input	The data signal for the WISHBONE interface, which writes data to the addressed EFB register during write cycles.
wb_dat_o[7:0]	Output	The read data signal for the WISHBONE interface, which outputs the data from the addressed EFB register during read cycles.
wb_ack_o	Output	Signals that the WISHBONE cycle is complete; data written to the EFB is accepted, and data read from the EFB is valid.
APB Interface (Available when User Interface = APB)		
clk_i	Input	APB interface clock. All APB signals are timed against the positive edge of this clock.
rstn_i	Input	APB interface reset. An active-low reset signal that is typically connected to the system reset.
apb_psel_i	Input	APB select. Indicates that this APB completer is selected and that a data transfer is required.
apb_penable_i	Input	APB enable. Indicates the subsequent cycles of an APB transfer.
apb_pwrite_i	Input	APB write. Indicates an APB write when high and an APB read operation when low.
apb_paddr_i	Input	APB address bus. The bit width is set by the *APB Data Width* attribute.
apb_pwdata_i	Input	APB write data bus. The bit width is set by the *APB Data Width* attribute.
apb_pready_o	Output	APB ready. Used to extend an APB transfer.
apb_prdata_o	Output	APB read data bus. The bit width is set by the *APB Data Width* attribute.
apb_pslverr_o	Output	APB transfer error. An optional signal that asserts high to indicate an error condition.
int_o	Output	EFB interrupt request. When the User Interface is set to APB, this signal represents the combined interrupts from the I2C1, I2C2, SPI, and Flash Memory interfaces.
Flash Memory		
wbc_ufm_irq	Output	The interrupt request output of the user flash memory.
I2C Interface		
i2c1_scl	Input/ Output	The open-drain serial clock of the primary I2C core. This signal is an output if the I2C core is performing a controller operation and an input during target operations. This signal must be brought to the top level of the user RTL design. The Radiant software automatically routes this signal to its pre-assigned pin (no user pin location constraint is necessary).
i2c1_sda	Input/ Output	The open-drain serial data line of the primary I2C core. The signal is an output when data is transmitted from the I2C core and an input when data is received into the I2C core. This signal must be brought to the top level of the user RTL design. The Radiant software automatically routes this signal to its pre-assigned pin (no user pin location constraint is necessary).
i2c1_irqo	Output	The interrupt request output signal of the primary I2C core. Connect this signal to a WISHBONE controller to request an interrupt when a specific condition is met. These conditions are described in the Flash Access Registers section.

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Port	Type	Description
i2c2_scl	Input/ Output	The open-drain serial clock line of the secondary I2C core. This signal is an output if the I2C core is performing a controller operation and an input during target operations. This signal can be routed to any GPIO of the MachXO4 device.
i2c2_sda	Input/ Output	The open-drain data line of the secondary I2C core. This signal is an output when data is transmitted from the I2C core and an input when data is received into the I2C core. This signal can be routed to any GPIO of the MachXO4 device.
i2c2_irqo	Output	The interrupt request output signal of the secondary I2C core. Connect this signal to a WISHBONE controller to request an interrupt when a specific condition is met. These conditions are described in the Flash Access Registers section.
SPI Interface		
spi_clk	Input/ Output	Serial Clock of the SPI core. The signal is an output if the SPI core is a controller (MCLK) and an input if the SPI core is a target (CCLK). This signal must be brought to the top level of the user RTL design. The Radiant software automatically routes this signal to its pre-assigned pin (no user pin location constraint is necessary).
spi_miso	Input/ Output	The signal is an output if the SPI core is a controller (SPISO) and an input if the SPI core is a target (SO). This signal must be brought to the top level of the user RTL design. The Radiant software automatically routes this signal to its pre-assigned pin (no user pin location constraint is necessary).
spi_mosi	Input/ Output	The signal is an output if the SPI core is a controller (SISPI) and an input if the SPI core is a target (SI). This signal must be brought to the top level of the user RTL design. The Radiant software automatically routes this signal to its pre-assigned pin (no user pin location constraint is necessary).
spi_scsn	Input	User Target Chip Select (Active Low). An external SPI controller asserts this signal to transfer data to/from the SPI Controller Transmit Data/Receive Data registers. The signal can be routed to any GPIO of the MachXO4 device.
ufm_sn	Input	Configuration Logic Chip Select (Active Low). It is dedicated to selecting the UFM/Flash sectors. Radiant software automatically routes this signal to its pre-assigned pin (no user pin location constraint is necessary).
spi_csn	Output	Controller Chip Select (Active Low). Up to eight independent Target SPI devices can be accessed using the SPI Controller when it is in controller/target SPI mode. The signal spi_csn[0] must be brought to the top level of the user RTL design. The Radiant software automatically routes this signal to its pre-assigned pin (no user pin location constraint is necessary). The other bits (spi_csn[7:1]) can be routed to any GPIO of the MachXO4 device.
spi_irq	Output	Interrupt request output signal of the SPI core. This signal is connected to a WISHBONE controller. It is asserted when specific conditions are met. These conditions are controlled using the SPI register settings.
Timer/Counter		
tc_clki	Input	Timer/Counter input clock signal. Can be connected to the on-chip oscillator. The clock signal is limited to 133 MHz.
tc_rstn	Input	Active-low reset signal, which resets the 16-bit counter.
tc_ic	Input	Active-high input capture trigger event, applicable for non-PWM modes with WISHBONE interface. If enabled, a rising edge of this signal is detected and synchronized to capture the counter value (TCCNT Register) and make the value accessible to the WISHBONE interface by loading it into TCICR register. The common usage is to perform a time-stamp operation with the counter.
tc_int	Output	Interrupt signal, indicating the occurrence of a specific event such as Overflow, Output Compare Match, or Input Capture.
tc_oc	Output	Timer/Counter output signal.
PLL0 (WISHBONE)		
pll0_ack_i	Input	Acknowledgment signal from the WISHBONE Target. You must connect only to a PLL component that is instantiated in the design.
pll0_dati_i[7:0]	Input	Data output bus from the WISHBONE Target. You must connect only to a PLL component that is instantiated in the design.
pll0_clk_o	Output	Clock generated by the WISHBONE Controller for the WISHBONE Target.

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Port	Type	Description
		You must connect only to a PLL component that is instantiated in the design.
pll0_rst_o	Output	Reset output generated by the WISHBONE Controller for the WISHBONE Target. You must connect only to a PLL component that is instantiated in the design.
pll0_addr_o[7:0]	Output	Address bus from the WISHBONE Controller for the WISHBONE Target. You must connect only to a PLL component that is instantiated in the design.
pll0_dato_o[7:0]	Output	Data bus from the WISHBONE Controller for the WISHBONE Target. You must connect only to a PLL component that is instantiated in the design.
pll0_we_o	Output	Write/read control signal generated for the WISHBONE Target. You must connect only to a PLL component that is instantiated in the design.
pll0_stb_o	Output	Strobe signal generated for the WISHBONE Target. You must connect only to a PLL component that is instantiated in the design.
PLL1 (WISHBONE)		
pll1_ack_i	Input	Acknowledgment signal from the WISHBONE Target. You must connect only to a PLL component that is instantiated in the design.
pll1_dati_i[7:0]	Input	Data output bus from the WISHBONE Target. You must connect only to a PLL component that is instantiated in the design.
pll1_clk_o	Output	Clock generated by the WISHBONE Controller for the WISHBONE Target. You must connect only to a PLL component that is instantiated in the design.
pll1_rst_o	Output	Reset output generated by the WISHBONE Controller for the WISHBONE Target. You must connect only to a PLL component that is instantiated in the design.
pll1_addr_o[7:0]	Output	Address bus from the WISHBONE Controller for the WISHBONE Target. You must connect only to a PLL component that is instantiated in the design.
pll1_dato_o[7:0]	Output	Data bus from the WISHBONE Controller for the WISHBONE Target. You must connect only to a PLL component that is instantiated in the design.
pll1_we_o	Output	Write/read control signal generated for the WISHBONE Target. You must connect only to a PLL component that is instantiated in the design.
pll1_stb_o	Output	Strobe signal generated for the WISHBONE Target. You must connect only to a PLL component that is instantiated in the design.
Power Controller		
cfg_wake	Output	Wakeup signal – Hardwired signal to be connected ONLY to the Power Controller of the MachXO4 device for functional simulation support. This signal is enabled only if the Wakeup Enable feature has been set by the I2C or SPI core settings.
cfg_stdby	Output	Stand-by signal – Hardwired signal to be connected ONLY to the Power Controller of the MachXO4 device for functional simulation support. This signal is enabled only if the Wakeup Enable feature has been set by the I2C or SPI core settings.
Tamper Detect/Response (for MachXO4 RoT Devices Only)		
tamper_detect_clk	Input	Tamper detection module clock. This clock signal must remain uninterrupted for the module to function at all times. All tamper detect/response output signals operate in this clock domain.
tamper_detect_in	Input	Tamper detection enable/disable. Drive this signal high (1) to enable the Tamper Detection module. Setting this signal to low (0) also resets the tamper_detect output signal.
tamper_src_lock	Input	Tamper detection configuration ports lock. Once tamper is detected, the user logic can lock the configuration ports to prevent further attack. Drive this signal high (1) to enable the pre-selected configuration ports.
tamper_detect	Output	Tamper detection signal. This signal goes to high (1) to indicate that tamper is detected.
tamper_src[1:0]	Output	Tamper detection source. This signal reports the source of the detected tamper: • 00 – WISHBONE (WB) • 01 – Target SPI (SSPI) • 10 – Target I2C (SI2C) • 11 – JTAG
tamper_type[1:0]	Output	Tamper detection type. This signal provides the information about the detected tamper: • 00 – Reserved

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Port	Type	Description
		• 01 – Password Protection • 10 – Locked Flash/SRAM • 11 – Manufacture Mode

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5. Register Description

The following subsections provide summary descriptions of the registers for the I2C, SPI, Timer/Counter, Flash Access, and EFB Interrupt Source IP blocks. For detailed register information, refer to the MachXO4 Hardened Control Functions Reference Guide (FPGA-TN-02404).

5.1. I2C Registers

Both I2C cores communicate with the EFB WISHBONE interface through a set of control, command, status, and data registers.

Table 5.1. I2C Functions Register Map

Offset	Register Name	Description	Access	Default
0x40	I2C_1_CR	Primary I2C Control	RW	0x00
0x41	I2C_1_CMDR	Primary I2C Command	RW	0x00
0x42	I2C_1_BR0	Primary I2C Clock Prescale 0	RW	0x00[1]
0x43	I2C_1_BR1	Primary I2C Clock Prescale 1	RW	0x00[1]
0x44	I2C_1_TXDR	Primary I2C Transmit Data	WO	—
0x45	I2C_1_SR	Primary I2C Status	RO	0x00
0x46	I2C_1_GCDR	Primary I2C General Call	RO	—
0x47	I2C_1_RXDR	Primary I2C Receive Data	RO	—
0x48	I2C_1_IRQ	Primary I2C IRQ	RW	—
0x49	I2C_1_IRQEN	Primary I2C IRQ Enable	RW	0x00
0x4A	I2C_2_CR	Secondary I2C Control	RW	0x00
0x4B	I2C_2_CMDR	Secondary I2C Command	RW	0x00
0x4C	I2C_2_BR0	Secondary I2C Clock Prescale 0	RW	0x00[1]
0x4D	I2C_2_BR1	Secondary I2C Clock Prescale 1	RW	0x00[1]
0x4E	I2C_2_TXDR	Secondary I2C Transmit Data	WO	—
0x4F	I2C_2_SR	Secondary I2C Status	RO	0x00
0x50	I2C_2_GCDR	Secondary I2C General Call	RO	—
0x51	I2C_2_RXDR	Secondary I2C Receive Data	RO	—
0x52	I2C_2_IRQ	Secondary I2C IRQ	RW	—
0x53	I2C_2_IRQEN	Secondary I2C IRQ Enable	RW	0x00

Note:

1. The hardware default is overridden by parameter configurations.

5.2. SPI Registers

Table 5.2. SPI Functions Register Map

Offset	Register Name	Description	Access	Default
0x54	SPICR0	Control Register 0	RW	0x00
0x55	SPICR1	Control Register 1	RW	0x00[1]
0x56	SPICR2	Control Register 2	RW	0x00[1]
0x57	SPIBR	Clock Prescale	RW	0x00[1]
0x58	SPICSR	Controller Chip Select	RW	0x00
0x59	SPITXDR	Transmit Data	WO	—
0x5A	SPISR	Status	RO	—
0x5B	SPIRXDR	Receive Data	RO	—
0x5C	SPIIRQ	Interrupt Request	RW	—
0x5D	SPIIRQEN	Interrupt Request Enable	RW	0x00

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Note:
1. The hardware default is overridden by parameter configurations.

5.3. Timer/Counter Registers

Table 5.3. Timer/Counter Functions Register Map

Offset	Register Name	Description	Access	Default
0x5E	TCCR0	Control Register 0	RW	0x00[1]
0x5F	TCCR1	Control Register 1	RW	0x00[1]
0x60	TCTOPSET0	Set Top Counter Value [7:0]	WO	0x00[1]
0x61	TCTOPSET1	Set Top Counter Value [15:8]	WO	0x00[1]
0x62	TCOCRSET0	Set Compare Counter Value [7:0]	WO	0x00[1]
0x63	TCOCRSET1	Set Compare Counter Value [15:8]	WO	0x00[1]
0x64	TCCR2	Control Register 2	RW	0x00[1]
0x65	TCCNT0	Counter Value [7:0]	RO	—
0x66	TCCNT1	Counter Value [15:8]	RO	—
0x67	TCTOP0	Current Top Counter Value [7:0]	RO	—
0x68	TCTOP1	Current Top Counter Value [15:8]	RO	—
0x69	TCOCR0	Current Compare Counter Value [7:0]	RO	—
0x6A	TCOCR1	Current Compare Counter Value [15:8]	RO	—
0x6B	TCICR0	Current Capture Counter Value [7:0]	RO	—
0x6C	TCICR1	Current Capture Counter Value [15:8]	RO	—
0x6D	TCSR0	Status Register	RW	—
0x6E	TCIRQ	Interrupt Request	RW	—
0x6F	TCIRQEN	Interrupt Request Enable	RW	0x00[1]

Note:
1. The hardware default is overridden by parameter configurations.

5.4. Flash Access Registers

The WISHBONE target interface of the EFB module enables you to access the flash interface directly from the FPGA core logic. The WISHBONE bus signals are used by a WISHBONE host that you can implement using the general-purpose FPGA resources.

The WISHBONE interface communicates to the configuration logic through a set of data, control, and status registers.

Table 5.4. Flash Memory Functions Register Map

Offset	Register Name	Description	Access	Default
0x70	CFGCR	Control	RW	0x00
0x71	CFGTXDR	Transmit Data	WO	0x00
0x72	CFGSR	Status	RO	0x00
0x73	CFGRXDR	Receive Data	RO	0x00
0x74	CFGIRQ	Interrupt Request	RW	0x00
0x75	CFGIRQEN	Interrupt Request Enable	RW	0x00

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5.5. EFB Interrupt Source

Table 5.5. Unused (Reserved) Register

Offset	Register Name	Description	Access	Default
0x76	UNUSED	Reserved Registers	—	0x00
0x77	EFBIRQ	EFB Interrupt Source	RO	0x00

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6. Command and Data Transfers to Flash Space

The command and data transferred to the flash memory are identical for all the access ports, regardless of their different physical interfaces. The flash memory is organized in pages. Therefore, you address a specific page for read or write operations to that page. Each page has 128 bits (16 bytes). Transfers are based on a set of instructions and page addresses. Erase operations are sector based (Configuration Flash, UFM, or Feature Row).

6.1. Command Summary

Table 6.1. MachXO4 (LFMXO4) Flash Command

Command	SVF Name	Opcode	Applies To	Description
Read Status Register	LSC_READ_STATUS	0x3C	CFG, UFM	Reads the 4-byte configuration status register.
Check Busy Flag	LSC_CHECK_BUSY	0xF0	CFG, UFM	Reads the Configuration Busy Flag status.
Bypass	ISC_NOOP	0xFF	CFG, UFM	Performs a null operation.
Enable Configuration Interface (Transparent Mode)[1]	ISC_ENABLE_X	0x74	CFG, UFM	Enables transparent UFM access. The device remains in user mode.
Enable Configuration Interface (Offline Mode)[1]	ISC_ENABLE	0xC6	CFG, UFM	Enables offline access.
Disable Configuration Interface	ISC_DISABLE	0x26	CFG, UFM	Disables the configuration UFM access.
Set Address	LSC_WRITE_ADDRESS	0xB4	CFG, UFM	Sets the UFM sector 14-bit address register.
Reset UFM Address	LSC_INIT_ADDR_UFM	0x47	UFM	Resets the address to UFM Sector 1, Page 0.
Read UFM	LSC_READ_TAG	0xCA	UFM	Reads UFM data. The operand specifies the number of pages to read. The address register is post-incremented.
Erase UFM	LSC_ERASE_TAG	0xCB	UFM	Erases the UFM sector.
Program UFM Page	LSC_PROG_TAG	0xC9	UFM	Writes one page of data to the UFM. The address register is post-incremented.
Read Device ID	IDCODE_PUB	0xE0	CFG	Reads the 4-byte device ID. For the expected device IDs, refer to the device ID information in the MachXO4 Hardened Control Functions Reference Guide (FPGA-TN-02404).
Read USERCODE	USERCODE	0xC0	CFG	Reads the 32-bit USERCODE.
Refresh	LSC_REFRESH	0x79	CFG	Launches the boot sequence.
STANDBY	LSC_DEVICE_CTRL	0x7D	CFG	Triggers the Power Controller to enter or wake from standby mode.
Verify Device ID	VERIFY_ID	0xE2	CFG	Verifies the device ID against a 32-bit input and sets the fail flag if mismatched.
Reset Configuration Flash Address	LSC_INIT_ADDRESS	0x46	CFG	Resets the address to Sector 0, Page 0 of the Configuration Flash.
Read Flash	LSC_READ_INCR_NV	0x73	CFG	Reads flash data. The operand specifies the number of the pages to read. The address register is post-incremented.
Erase	ISC_ERASE	0x0E	CFG, UFM	Erases the configuration flash, UFM, Feature Row, FEABITS, DONE bit, Security bits, and USERCODE.
Program Page	LSC_PROG_INCR_NV	0x70	CFG	Writes one page of data to the flash. The address register is post-incremented.

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Command	SVF Name	Opcode	Applies To	Description
Program DONE	ISC_PROGRAM_DONE	0x5E	CFG	Programs the DONE bit.
Program SECURITY[2]	ISC_PROGRAM_SECURITY	0xCE	CFG	Programs the Security bit to secure the configuration flash sector.
Program SECURITY PLUS[2]	ISC_PROGRAM_SECPLUS	0xCF	CFG	Programs the Security Plus bit to secure configuration flash and UFM sectors.
Program USERCODE	ISC_PROGRAM_USERCODE	0xC2	CFG	Programs the 32-bit USERCODE.
Read Feature Row	LSC_READ_FEATURE	0xE7	CFG	Reads the Feature Row.
Program Feature Row	LSC_PROG_FEATURE	0xE4	CFG	Programs the Feature Row.
Read FEABITS	LSC_READ_FEABITS	0xFB	CFG	Reads the FEA bits.
Program FEABITS	LSC_PROG_FEABITS	0xF8	CFG	Programs the FEA bits.

Notes:

1. The configuration interface must be enabled before issuing the subsequent commands listed in this table:
   - In transparent mode, user I/O (except primary user ports) remain controlled by user logic.
   - In offline mode, user I/O (except persisted ports) are tri-stated, and user logic stops functioning while UFM remains accessible.
2. SECURITY and SECURITY PLUS commands are mutually exclusive.

Table 6.2. MachXO4 RoT (LFMXO4D) Flash Commands

Command	SVF Name	Opcode	Applies To	Description
Read Status, Busy, Bypass, Read Device ID, and Refresh				
Read Status Register 0	LSC_READ_STATUS0	0x3C	CFG, UFM, Feature, Security Policy, Security Keys	Reads the 4-byte configuration status register.
Read Status Register 1	LSC_READ_STATUS1	0x3D	CFG, UFM, Feature, Security Policy, Security Keys	Reads the 4-byte configuration status register.
Check Busy Flag	LSC_CHECK_BUSY	0xF0	CFG, UFM, Feature, Security Policy, Security Keys	Reads the configuration busy flag status.
Bypass	ISC_NOOP	0xFF	CFG, UFM, Feature, Security Policy, Security Keys	Performs a null operation.
Read Device ID	IDCODE_PUB	0xE0	CFG	Reads the 4-byte device ID.
Read USERCODE	USERCODE	0xC0	CFG	Reads the 32-bit USERCODE.
Read USERCODE_DRYRUN	USERCODE_DRYRUN	0xC1	CFG	Reads the 32-bit dry-run USERCODE for bitstream testing.
Address Location for USERCODE (Dry-Run)	LSC_PROG_DRYRUN_ADDR	0xFC	CFG	Specifies the address location of the external flash for dry-run.
Refresh	LSC_REFRESH	0x79	—	Launches the boot sequence, which is the same as toggling the PROGRAMN pin.
Bitstream Check	LSC_DEVICE_CTRL	0x7D	—	Enables bitstream checking options (dry-run, SED, or others) and device operations such as standby, wakeup, and reset.
Verify Device ID	LSC_VERIFY_ID	0xE2	CFG	Verifies the device ID against a 32-bit input and sets the fail flag if mismatched.

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Command	SVF Name	Opcode	Applies To	Description
Enable Configuration (Transparent Mode), Enable (Offline Mode)				
Enable Configuration Interface (Transparent Mode)[1]	ISC_ENABLE_X	0x74	CFG, UFM, Feature, Security Policy, Security Keys	Enables transparent CFG, UFM, FEABITS, Security Policy, or Security Keys access. The device remains in user mode.
Enable Configuration Interface (Offline Mode)[1]	ISC_ENABLE	0xC6	CFG, UFM, Feature, Security Policy, Security Keys	Enables offline UFM access.
Disable Configuration Interface	ISC_DISABLE	0x26	CFG, UFM, Feature, Security Policy, Security Keys	Disables the configuration (UFM) access.
Set and Reset Address				
Reset Configuration Flash Address	LSC_INIT_ADDRESS	0x46	CFG, UFM, Feature, Security Policy, Security Keys	Resets the address to Sector 0, Page 0 of the active flash sector.
Reset UFM Address	LSC_INIT_ADDR_UFM	0x47	UFM	Resets the address to UFM Sector 1, Page 0.
Set Address	LSC_WRITE_ADDRESS	0xB4	CFG, UFM	Sets the UFM sector 14-bit address.
Read, Program, and Erase				
Read Flash	LSC_READ_INCR_NV	0x73	CFG, UFM, Feature, Security Policy, Security Keys	Reads flash data. The operand specifies the number of pages to read.
Erase Flash	ISC_ERASE	0x0E	CFG, UFM, Feature, Security Policy, Security Keys	Erases the configuration flash, UFM, Feature Row, FEABITS, DONE bit, Security setting bits, Security keys, and USERCODE.
Program Page	LSC_PROG_INCR_NV	0x70	CFG, UFM, Feature, Security Policy, Security Keys	Writes one page of data to the flash memory (configuration or UFM). The address register is post-incremented.
Program DONE	ISC_PROGRAM_DONE	0x5E	CFG	Programs the DONE bit.
Read UFM	LSC_READ_TAG	0xCA	UFM	Reads UFM data. The operand specifies the number of pages to read.
Erase UFM	LSC_ERASE_TAG	0xCB	UFM	Erases the UFM sector.
Program UFM Page	LSC_PROG_TAG	0xC9	UFM	Writes one page of data to the UFM. The address register is post-incremented.
Program USERCODE	ISC_PROGRAM_USERCODE	0xC2	CFG	Programs the 32-bit USERCODE.
Feature and Feature Bits Keys				
Read Feature Row	LSC_READ_FEATURE	0xE7	Feature, Security Policy	Reads the Feature Row.
Program Feature Row	LSC_PROG_FEATURE	0xE4	Feature, Security Policy	Programs the Feature Row.
Read FEABITS	LSC_READ_FEABITS	0xFB	Feature, Security Policy	Reads the FEA bits.
Program FEABITS	LSC_PROG_FEABITS	0xF8	Feature, Security Policy	Programs the FEA bits.

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Command	SVF Name	Opcode	Applies To	Description
Security Keys				
Program ECDSA Public Key 0	LSC_PROG_ECDSA_PUBKEY0	0x59	Security Keys	Programs ECDSA public key bits [127:0].
Program ECDSA Public Key 1	LSC_PROG_ECDSA_PUBKEY1	0x5B	Security Keys	Programs ECDSA public key bits [255:128].
Program ECDSA Public Key 2	LSC_PROG_ECDSA_PUBKEY2	0x61	Security Keys	Programs ECDSA public key bits [383:256].
Program ECDSA Public Key 3	LSC_PROG_ECDSA_PUBKEY3	0x63	Security Keys	Programs ECDSA public key bits [511:384].
Read ECDSA Public Key 0	LSC_READ_ECDSA_PUBKEY0	0x5A	Security Keys	Reads ECDSA public key bits [127:0].
Read ECDSA Public Key 1	LSC_READ_ECDSA_PUBKEY1	0x5C	Security Keys	Reads ECDSA public key bits [255:128].
Read ECDSA Public Key 2	LSC_READ_ECDSA_PUBKEY2	0x62	Security Keys	Reads ECDSA public key bits [383:256].
Read ECDSA Public Key 3	LSC_READ_ECDSA_PUBKEY3	0x64	Security Keys	Reads ECDSA public key bits [511:384].
Program AES Key 0	LSC_PROG_CIPHER_KEY0	0xF3	Security Keys	Programs AES key bits [127:0].
Program AES Key 1	LSC_PROG_CIPHER_KEY1	0xFD	Security Keys	Programs AES key bits [255:128].
Read AES Key 0	LSC_READ_CIPHER_KEY0	0xF4	Security Keys	Reads AES key bits [127:0].
Read AES Key 1	LSC_READ_CIPHER_KEY1	0xFE	Security Keys	Reads AES key bits [255:128].

Note:

1. The configuration interface must be enabled before issuing the subsequent commands listed in this table.
   - In transparent mode, user I/O (except hardened user SPI and primary user I2C ports) remain controlled by user logic.
   - In offline mode, user I/O (except persisted sysCONFIG ports) are tri-stated, and user logic stops functioning while UFM remains accessible.

Table 6.3. Non-Volatile Register (NVR) Commands

Command Name	SVF Name	Opcode	Description
Read Trace ID code	UIDCODE_PUB	0x19	Read 64-bit Trace ID.

When using the WISHBONE bus interface, the commands, operand, and data are written to the CFGTXDR register. The target SPI or I2C interface shifts the most significant bit (MSB) first into the MachXO4 device. This is required only when communicating with the configuration logic inside the MachXO4 device.

6.2. Command Descriptions

For more details, refer to the command descriptions by command code information in the MachXO4 Hardened Control Functions Reference Guide (FPGA-TN-02404).

6.3. Command Framing

For more details, refer to the command framing information in the MachXO4 Hardened Control Functions Reference Guide (FPGA-TN-02404).

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7. Designing with the IP

This section provides information on how to generate the IP core using the Lattice Radiant software and how to run simulation and synthesis. For more details on the Lattice Radiant software, refer to the Lattice Radiant Software User Guide.

Note: The screenshots provided are for reference only. Details may vary depending on the version of the IP or software being used. If there have been no significant changes to the GUI, a screenshot may reflect an earlier version of the IP.

7.1. Generating and Instantiating the IP

You can use the Lattice Radiant software to generate IP modules and integrate them into the device architecture. The steps below describe how to generate the EFB Module IP in the Lattice Radiant software.

To generate the EFB Module IP:

1. Create a new Lattice Radiant software project or open an existing project.
2. In the **IP Catalog** tab, double-click **Embedded Functional Block** under **IP, Architecture Modules** category. The **Module/IP Block Wizard** opens as shown in Figure 7.1. Enter values in the **Component name** and the **Create in** fields and click **Next**.

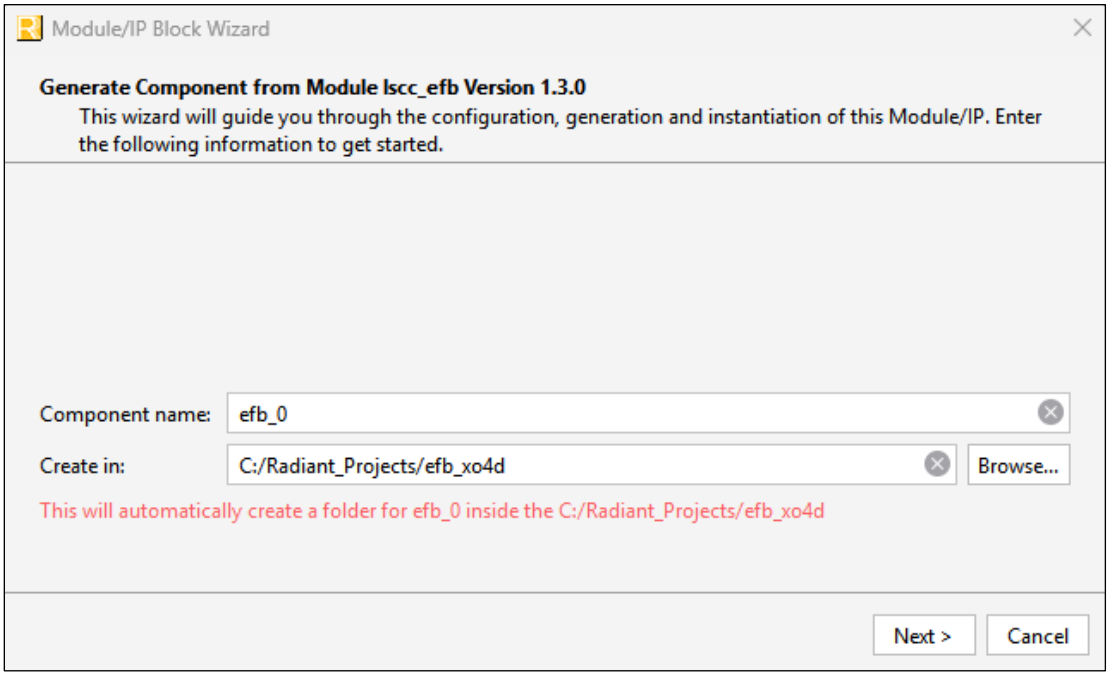


Figure 7.1. Module/IP Block Wizard

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3. In the next **Module/IP Block Wizard** window, customize the selected EFB Module IP using drop-down lists and check boxes. Figure 7.2 shows an example configuration of the EFB Module IP. For details on the configuration options, refer to the IP Parameter Description section. For sample configurations relating to the EFB features, specifically for I2C and UFM functionality, refer to the Running Functional Simulation section.

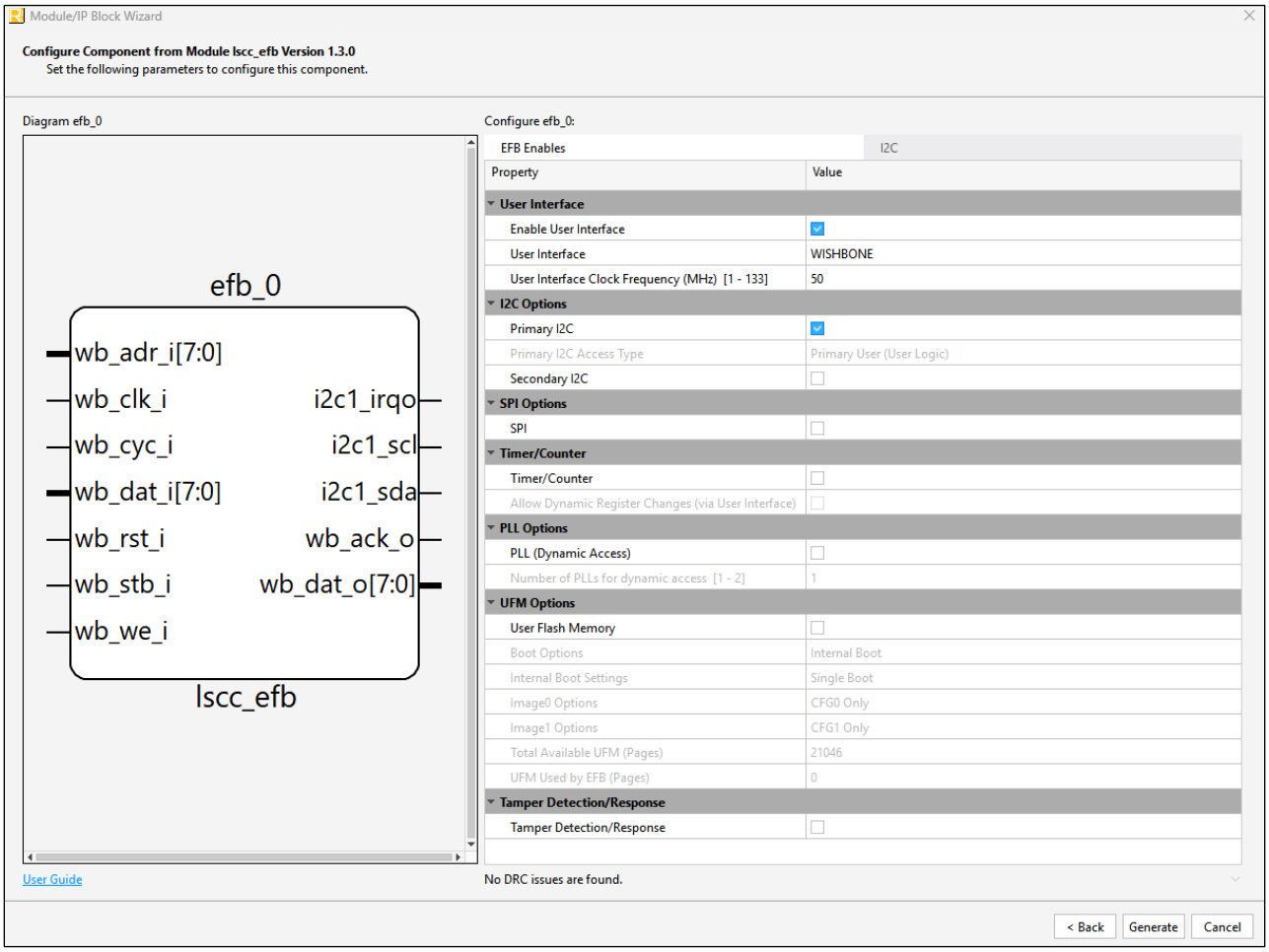


Figure 7.2. IP Configuration

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4. Click **Generate**. The **Check Generated Result** dialog box opens, showing design block messages and results as shown in Figure 7.3.

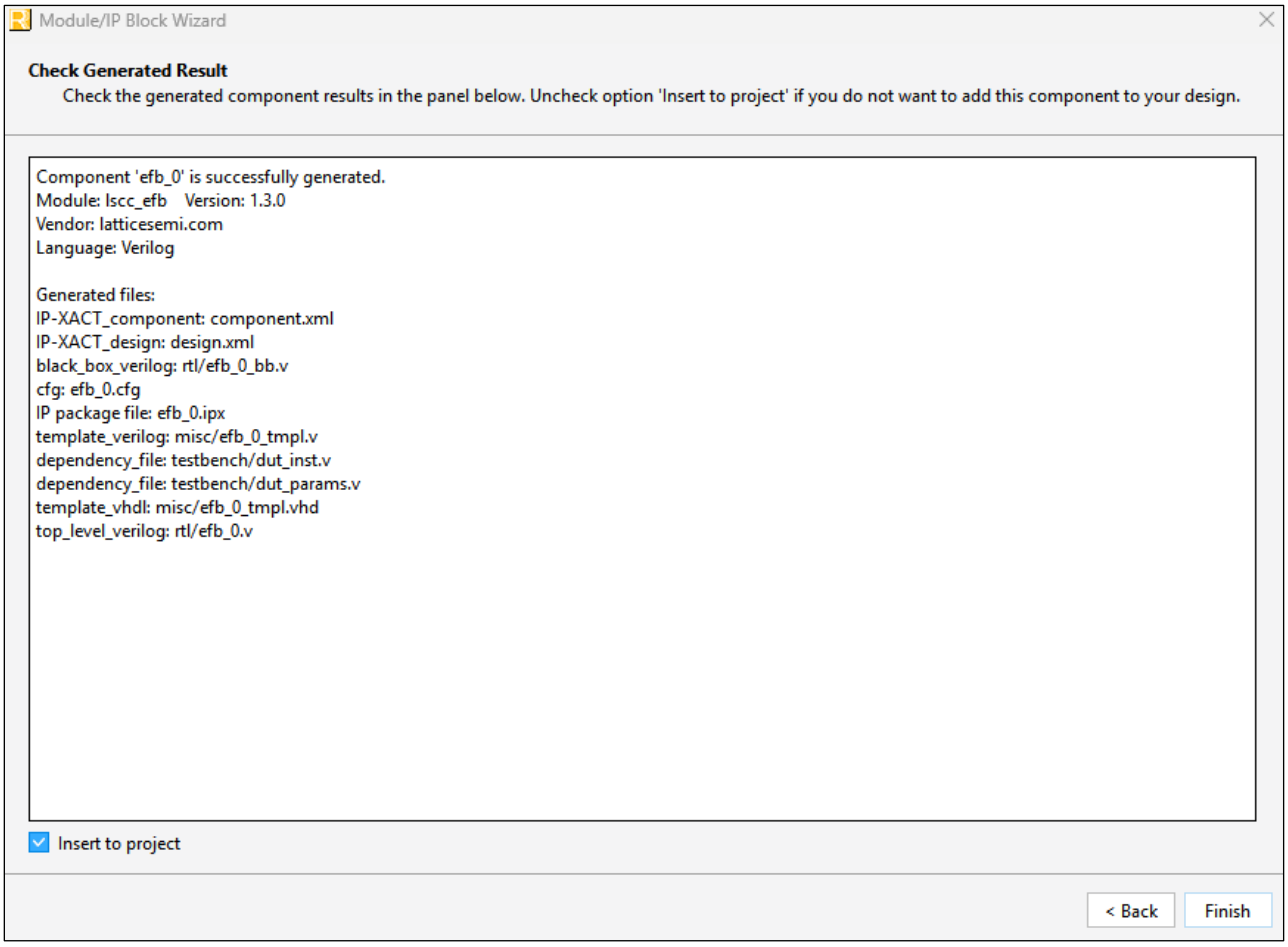


Figure 7.3. Check Generated Result

5. Click **Finish**. All the generated files are placed under the directory paths in the **Create in** and the **Component name** fields shown in Figure 7.1.

7.1.1. Generated Files and File Structure

The generated EFB module package includes the closed-box (<Component name>_bb.v) and instance templates (<Component name>_tmpl.v/vhd) that can be used to instantiate the core in a top-level design. An example RTL top-level reference source file (<Component name>.v) that can be used as an instantiation template for the module is also provided. You may also use this top-level reference as the starting template for the top-level for your complete design. The generated files are listed in Table 7.1.

Table 7.1. Generated File List

Attribute	Description
<Component name>.ipx	This file contains the information on the files associated to the generated IP.
<Component name>.cfg	This file contains the parameter values used in IP configuration.
component.xml	Contains the ipxact: component information of the IP.
design.xml	Documents the configuration parameters of the IP in IP-XACT 2014 format.
rtl/<Component name>.v	This file provides an example RTL top file that instantiates the module.
rtl/<Component name>_bb.v	This file provides the synthesis closed-box.

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7.2. Design Implementation

Completing your design includes additional steps to specify analog properties, pin assignments, and timing and physical constraints. You can add and edit the constraints using the Device Constraint Editor or by manually creating a PDC File.

Post-Synthesis constraint files (.pdc) contain both timing and non-timing *constraint.pdc* source files for storing logical timing/physical constraints. Constraints that are added using the Device Constraint Editor are saved to the active .pdc file. The active post-synthesis design constraint file is then used as input for post-synthesis processes.

Refer to the relevant sections in the Lattice Radiant Software User Guide for more information on how to create or edit constraints and how to use the Device Constraint Editor.

7.3. Timing Constraints

The timing constraints are based on the clock frequency used. The timing constraints for the IP are defined in relevant constraint files. The example below shows the IP timing constraints generated for the EFB Module IP.

```
create_clock -name {wb_clk_i} -period 20 [get_ports wb_clk_i]
```

7.4. Physical Constraints

For the primary I2C core signals (i2c1_scl and i2c1_sda), the Radiant software tool automatically routes these signals to their pre-assigned pins (no user pin location constraint is necessary). However, for the secondary I2C core signals (i2c2_scl and i2c2_sda), these can be routed to any GPIO of the MachXO4 device.

The SPI core signals (spi_clk, spi_miso, spi_mosi, spi_csn[0], and ufm_sn) are also automatically routed by the Radiant software tool to their pre-assigned pins. The remaining SPI signals (spi_csn[7:1]) can be routed to any GPIO on the MachXO4 device.

7.5. Specifying the Strategy

The Radiant software provides two predefined strategies: Area and Timing. It also enables you to create customized strategies. For details on how to create a new strategy, refer to the *Strategies* section in the Lattice Radiant Software user guide.

7.6. Running Functional Simulation

You can run functional simulation after the IP is generated.

To run functional simulation:

1. Click the  button located on the **Toolbar** to initiate the **Simulation Wizard** shown in Figure 7.4.

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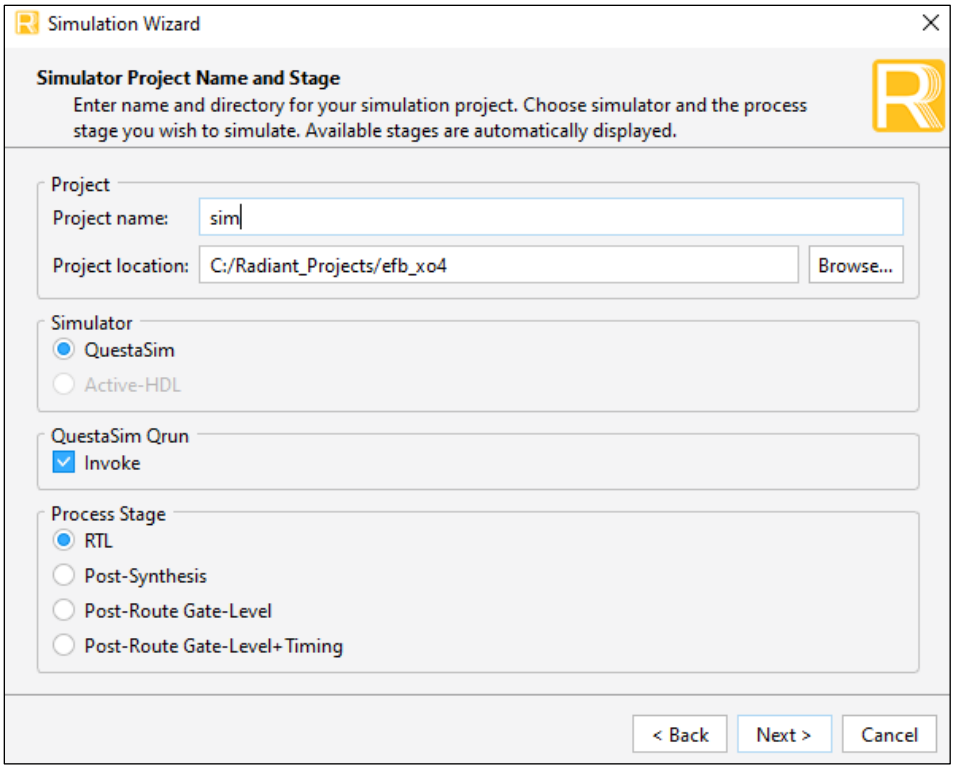


Figure 7.4. Simulation Wizard

2. Click **Next** to open the **Add and Reorder Source** window as shown in Figure 7.5.

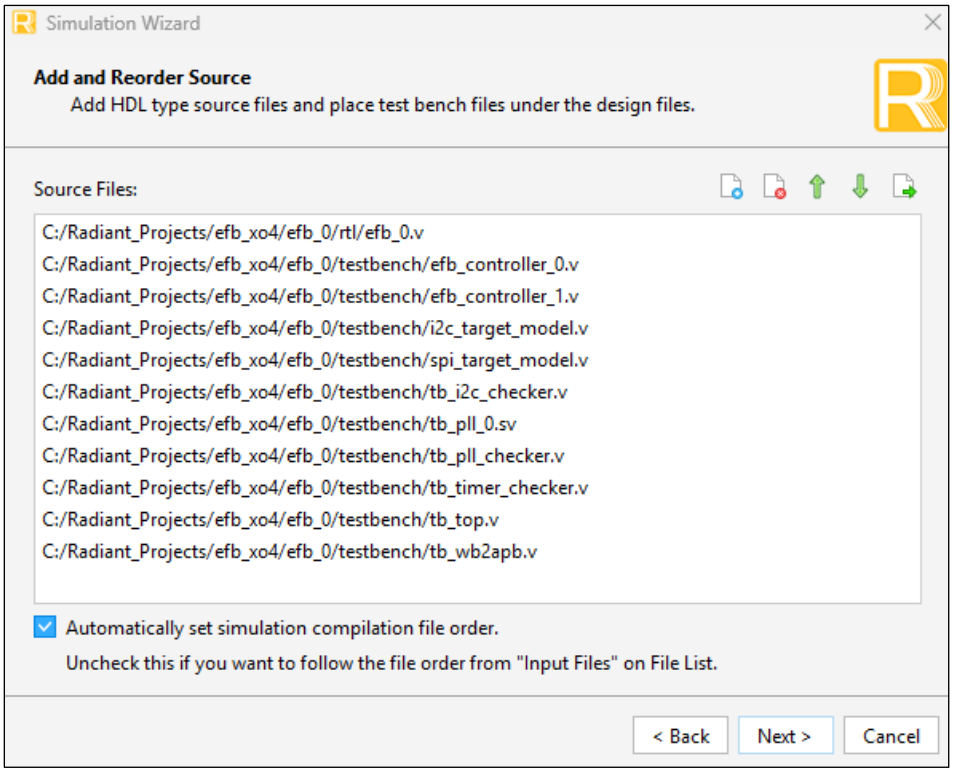


Figure 7.5. Add and Reorder Source

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3. Click **Next**. The **Summary** window is shown.
4. Click **Finish** to run the simulation.

The waveform in Figure 7.6 shows an example simulation result.

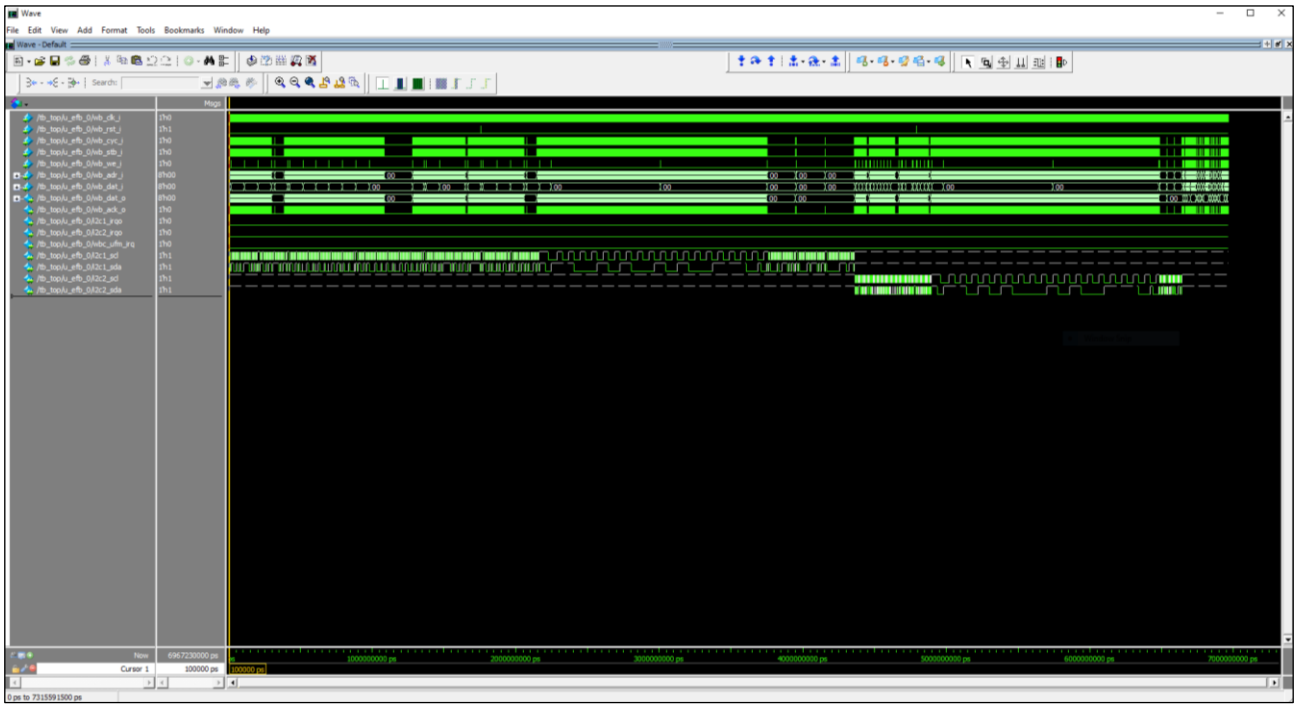


Figure 7.6. Simulation Waveform

7.6.1. Simulation Results

The provided testbench includes basic functional tests for all EFB features. A WISHBONE controller is used to access registers and generate the required sequences. If APB support is enabled, a WISHBONE-to-APB bridge is included to interface with the EFB.

The following describe how each EFB feature is exercised and checked through simulation using the provided testbench:

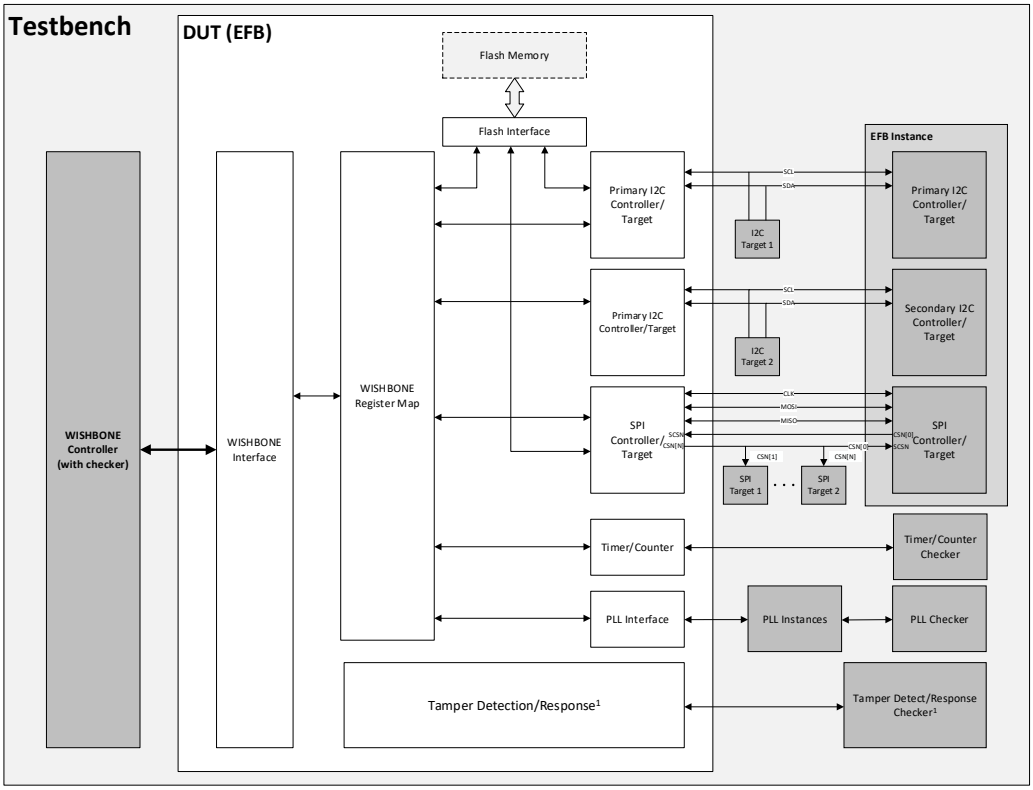
- I2C Core Simulation:
  - Controller Mode – A custom I2C target module with simple memory is used to confirm basic write and read behavior.
  - Target Mode – An EFB instance with I2C enabled acts as the controller to exercise target functionality.
- SPI Core Simulation:
  - Controller Mode – A custom SPI target module is connected to observe basic controller behavior.
  - Target Mode – An EFB instance with SPI enabled is used to simulate a controller and check target-side operation.
- Timer/Counter Simulation:
  - Timer/Counter functionality is exercised by:
    - Observing output timing and interrupt signals.
    - Accessing Timer/Counter registers to adjust and monitor behavior dynamically.
- PLL Interface Simulation:
  - The PLL interface is exercised by:
    - Instantiating a PLL IP in the testbench.
    - Observing clock timing behavior.

    Note: Only basic PLL configuration changes are included in the simulation.

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- CFG/UFM Access:
  - Basic flash memory operations are performed using WISHBONE register access:
    - Initialization
    - Erase operation
    - Status flag checking
    - Write and read operations
  - Additionally, read and write operations through SPI interface are included if enabled.
- Tamper Detect/Response:
  - Basic sequence of tamper assertion through WISHBONE (assertion not simulated).

The following figure provides an overview of a sample testbench.



Note:
1. Temper detect/response is available only for MachXO4 RoT devices.

Figure 7.7. Sample Testbench Overview

Depending on the features enabled during IP configuration, the corresponding test is included in the simulation. The simulation logs are expected to indicate **SIMULATION PASSED**, along with the corresponding waveform behavior.

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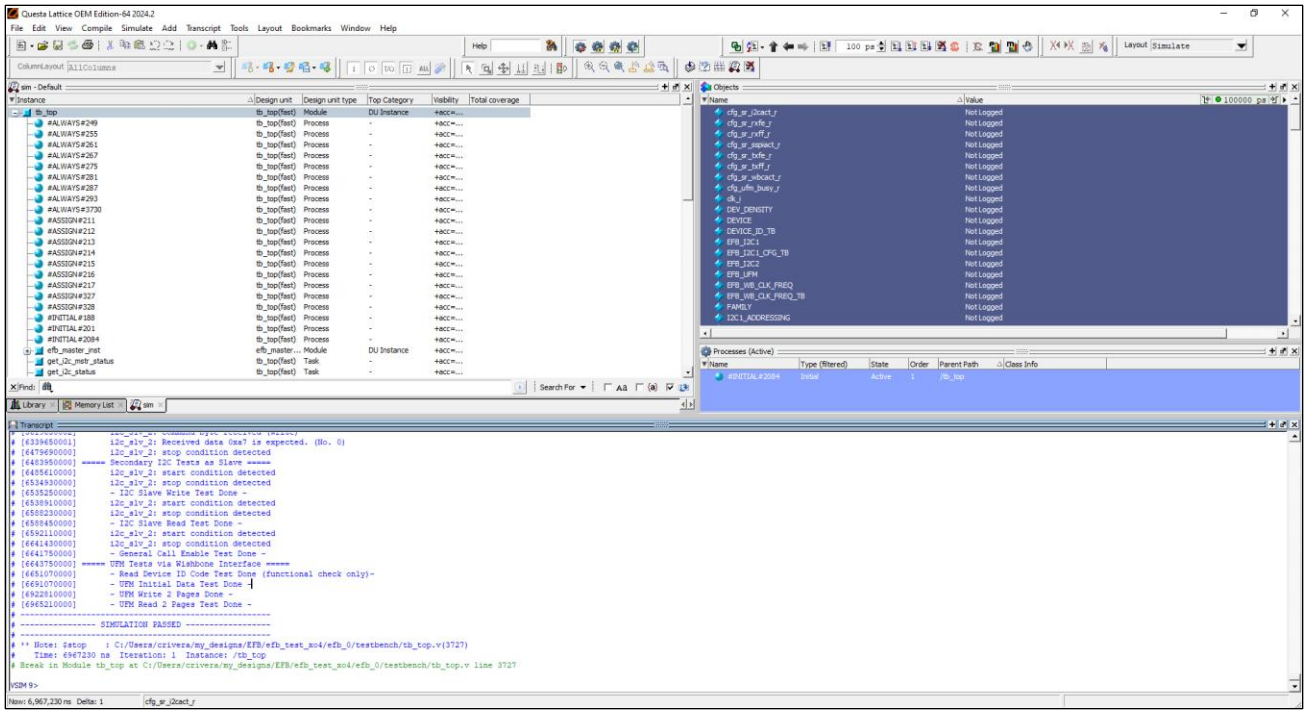


Figure 7.8. Sample Testbench Output

7.7. Example Designs (Simulation)

7.7.1. I2C Core Transaction Example

Figure 7.9 and Figure 7.10 show flow diagrams for controlling and receiving I2C reads and writes initiated through the WISHBONE interface. The following sequence is for the primary I2C, but the same sequence applies to the secondary I2C. This sequence is implemented in the included sample testbench to confirm the basic operations of the Primary and Secondary I2C. Figure 7.11 shows an example configuration to enable both Primary and Secondary I2C.

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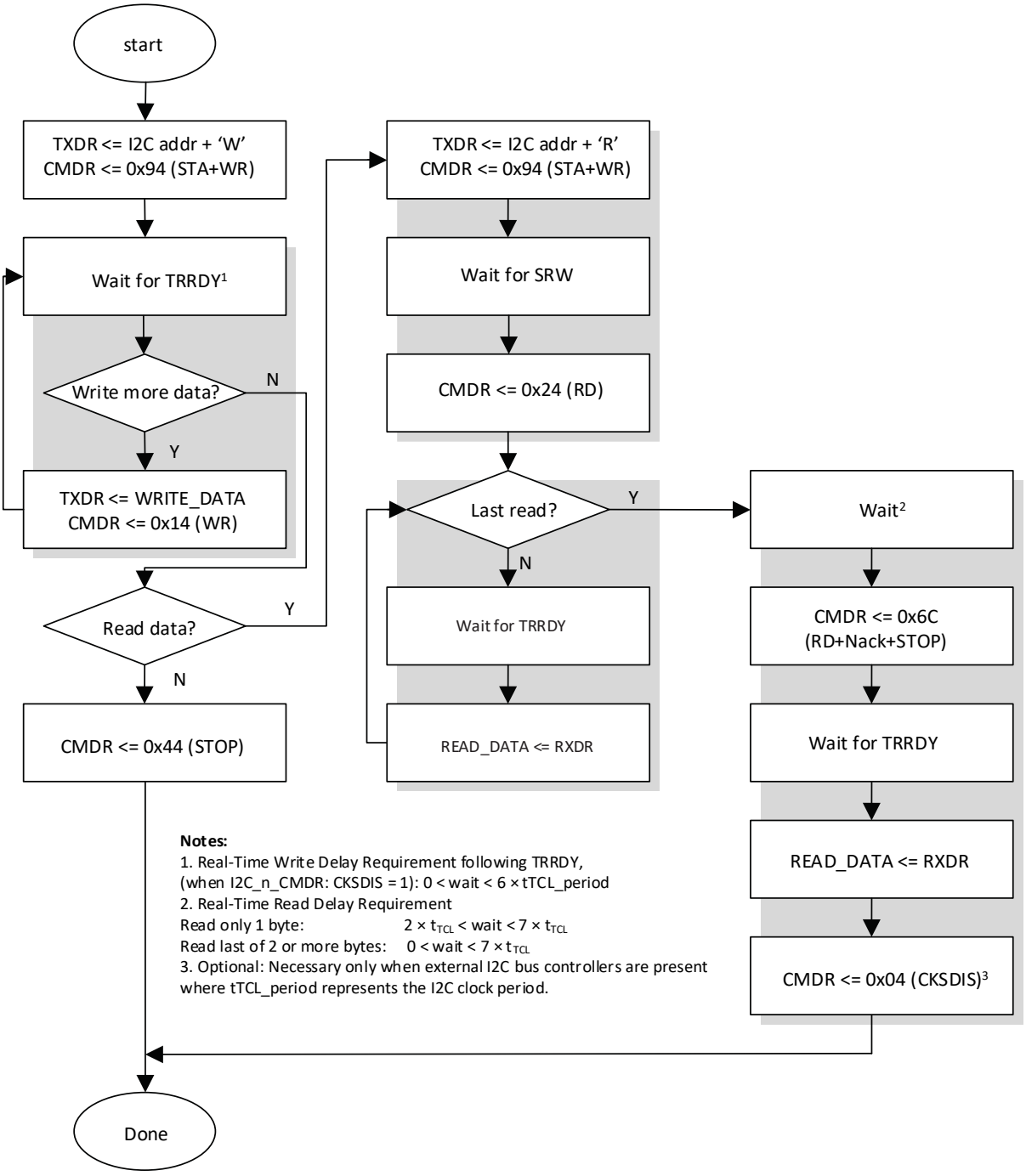


Figure 7.9. I2C Controller Read/Write Example (through WISHBONE)

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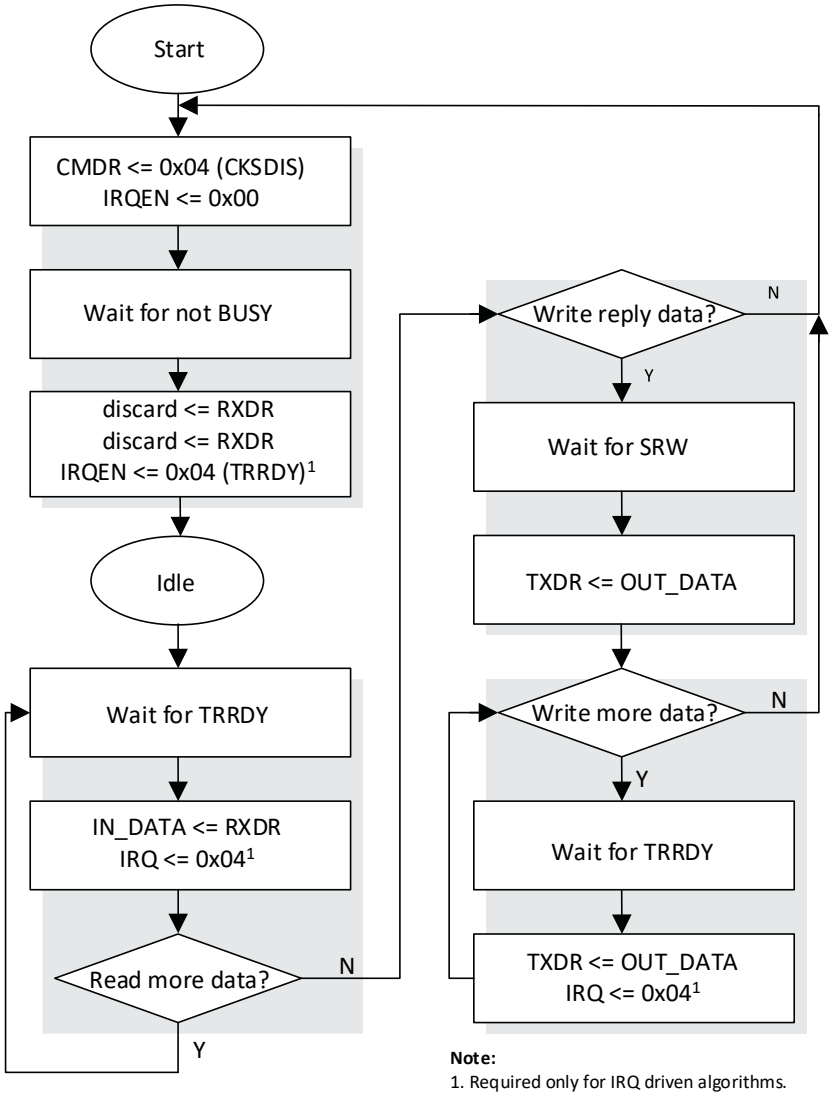


Figure 7.10. I2C Target Read/Write Example (through WISHBONE)

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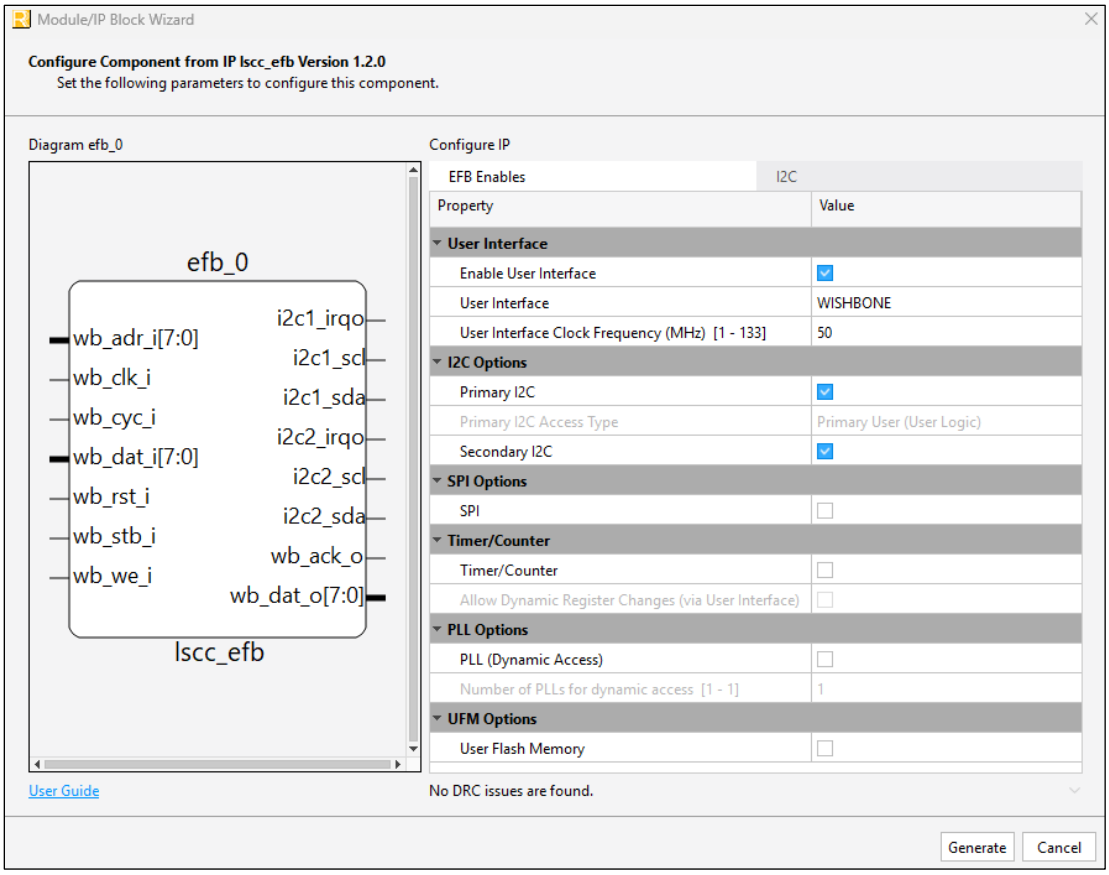


Figure 7.11. I2C Sample Configuration (Primary and Secondary I2C Enabled)

7.7.2. Flash Write and Read Example

Table 7.2, Table 7.3, and Table 7.4 show example write, erase, and read operations on a flash sector. The following sequence is for UFM access, but similar sequences can be followed for other sectors using their corresponding commands. This is implemented in the included sample testbench to confirm the basic operations of the UFM.

Table 7.2. Write Two UFM Pages (WISHBONE)

Instruction Number	R/W1	CMD2	Operand	Data	**Comment**
—	—	—	—	—	Open frame
1	W	74	08 00 00	—	Enable Configuration Interface
—	—	–	—	—	Close frame
—	—	+	—	—	—
2	W	3C	00 00 00	—	Poll Configuration Status Register
—	R	—	—	xx xx bx xx	—
—	—	–	—	—	(Repeat until Busy Flag not set, or wait 5 µs if not polling.)
—	—	+	—	—	—
3	W	47	00 00 00	—	Init UFM Address to 0000
—	—	–	—	—	—
—	—	+	—	—	—
4	W	C9	00 00 01	00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F	Write UFM Page 0 Data

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Instruction Number	R/W1	CMD2	Operand	Data	**Comment**
—	—	–	—	—	—
—	—	+	—	—	—
5	W	3C	00 00 00	—	Poll Configuration Status Register
—	R	—	—	xx xx bx xx	—
—	—	–	—	—	(Repeat until Busy Flag not set)
—	—	+	—	—	—
6	W	C9	00 00 01	10 11 12 13 14 15 16 17 18 19 1A 1B 1C 1D 1E 1F	Write UFM Page 1 Data **Note:** Address automatically incremented
—	—	–	—	—	—
—	—	+	—	—	—
7	W	3C	00 00 00	—	Poll Configuration Status Register
—	R	—	—	xx xx bx xx	—
—	—	–	—	—	(poll until Busy Flag clear)
—	—	+	—	—	—
8	W	26	00 00	—	Disable Configuration Interface
—	—	–	—	—	—
—	—	+	—	—	—
9	W	FF	—	—	Bypass (NOP)
—	—	–	—	—	—

Notes:

- When accessing the flash through WISHBONE, use CFGTXDR (0x71) to write data and CFDRXDR (0x73) to read data.
- + and – refer to the command framing protocol appropriate for the interface discussed in the Command Framing section.

Table 7.3. Read One UFM Page (WISHBONE)

Instruction Number	**R/W1**	**CMD2**	**Operand**	**Data**	**Comment**
—	—	+	—	—	Open frame
1	W	74	08 00 00	—	Enable Configuration Interface
—	—	–	—	—	Close frame
—	—	+	—	—	—
2	W	3C	00 00 00	—	Poll Configuration Status Register
—	R	—	—	xx xx bx xx	—
—	—	–	—	—	(Repeat until Busy Flag not set)
—	—	+	—	—	—
3	W	B4	00 00 00	40 00 00 01	Set UFM Address to 0001
—	—	–	—	—	—
—	—	+	—	—	—
4	W	CA	10 00 01	—	Read one page UFM (page 1) data
—	R	—	—	10 11 12 13 14 15 16 17 18 19 1A 1B 1C 1D 1E 1F	—
—	—	–	—	—	—
—	—	+	—	—	—
5	W	26	00 00	—	Disable Configuration Interface
—	—	–	—	—	—

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Instruction Number	R/W1	CMD2	Operand	Data	Comment
—	—	+	—	—	—
6	W	FF	—	—	Bypass (NOP)
—	—	–	—	—	—

Notes:

- When accessing the Flash through WISHBONE, use CFGTXDR (0x71) to write data and CFDRXDR (0x73) to read data.
- + and – refer to the command framing protocol appropriate for the interface discussed in the Command Framing section.

Table 7.4. Read Two UFM Pages (WISHBONE)

Instruction Number	R/W1	CMD2	Operand	Data	**Comment**
—	—	+	—	—	Open frame
1	W	74	08 00 00	—	Enable Configuration Interface
—	—	–	—	—	Close frame
—	—	+	—	—	—
2	W	3C	00 00 00	—	Poll Configuration Status Register
—	R	—	—	xx xx bx xx	—
—	—	–	—	—	(Repeat until Busy Flag not set, or wait 5 µs if not polling.)
—	—	+	—	—	—
3	W	47	00 00 00	—	Init UFM address to 0000
—	—	–	—	—	—
—	—	+	—	—	—
4	W	CA	10 00 03	—	Read two pages of UFM data, after one page of dummy bytes.3.
—	R	—	—	xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx 00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F 10 11 12 13 14 15 16 17 18 19 1A 1B 1C 1D 1E 1F	—
—	—	–	—	—	—
—	—	+	—	—	—
5	W	26	00 00	—	Disable Configuration Interface
—	—	–	—	—	—
—	—	+	—	—	—
6	W	FF	—	—	Bypass (NOP)
—	—	–	—	—	—

Notes:

- When accessing the Flash through WISHBONE, use CFGTXDR (0x71) to write data and CFDRXDR (0x73) to read data.
- + and – refer to the command framing protocol appropriate for the interface.
- num_pages count must include dummy page.

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To use the I2C ports to access the flash memory, both *Primary I2C* and *User Flash Memory* must be enabled. Then, select *Primary Config (Flash Access)* as the *Primary I2C Access Type*. This sets the Primary I2C Address to *0bxxxxx00*. Figure 7.12 shows an example configuration to enable Flash Access, through both WISHBONE Access and Primary I2C ports.

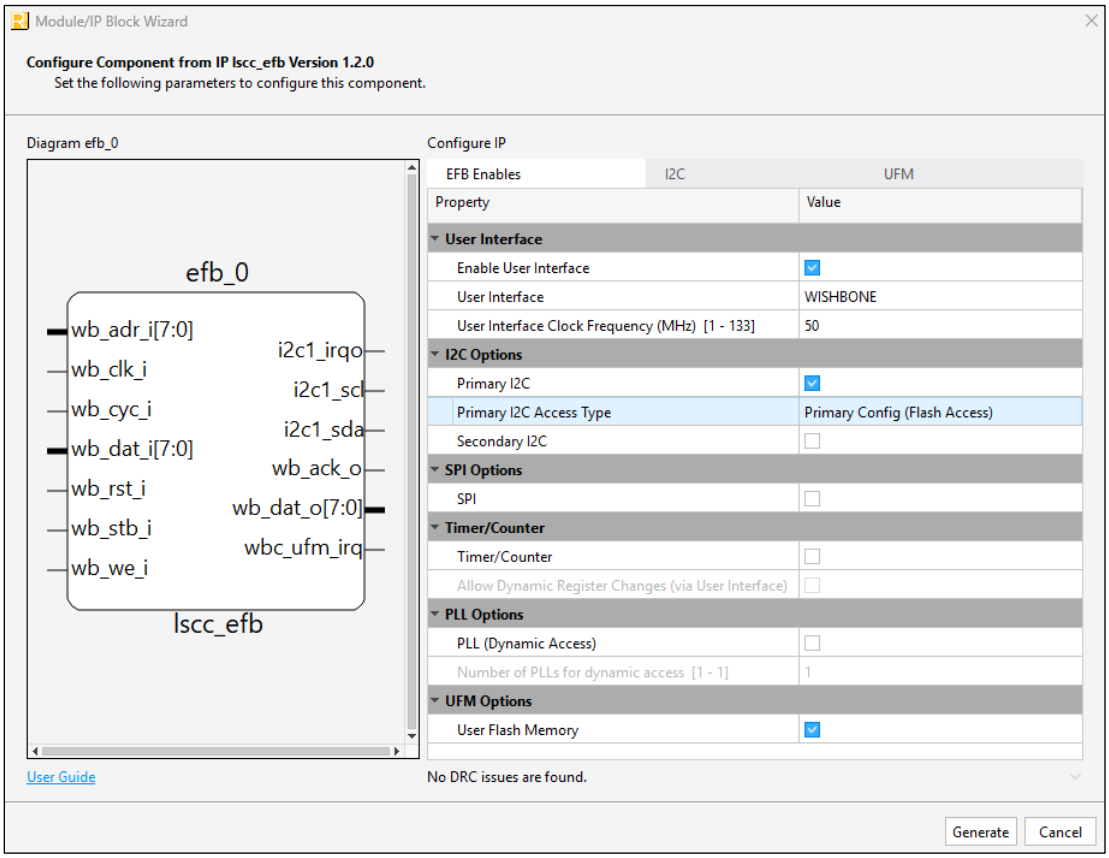


Figure 7.12. UFM Access Sample Configuration (through WISHBONE and I2C Access)

7.7.3. SPI Core Transaction Example

Figure 7.13 shows flow diagrams for controlling and receiving SPI reads and writes initiated through the WISHBONE interface. This sequence is implemented in the sample testbench to confirm the basic operations of the SPI core.

Figure 7.14 shows an SPI example configuration.

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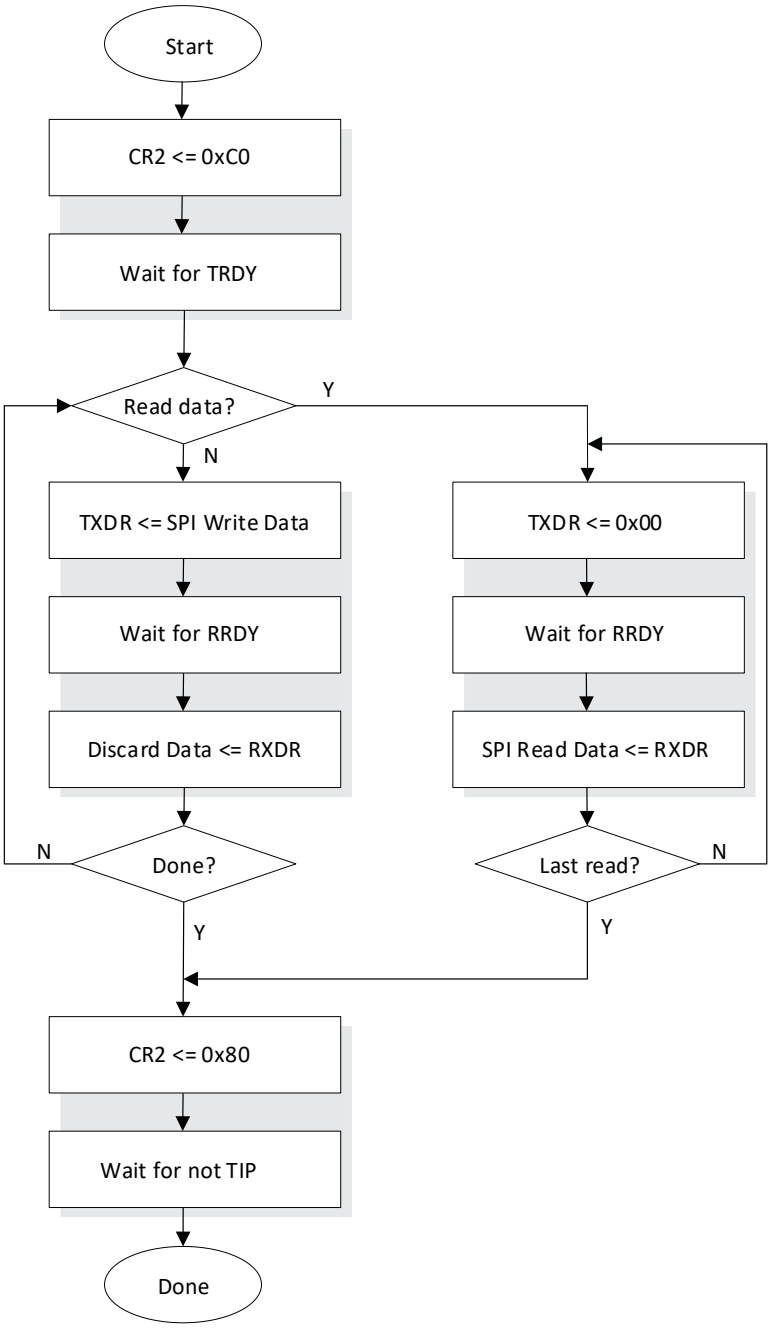


Figure 7.13. SPI Controller Read/Write Example (through WISHBONE)

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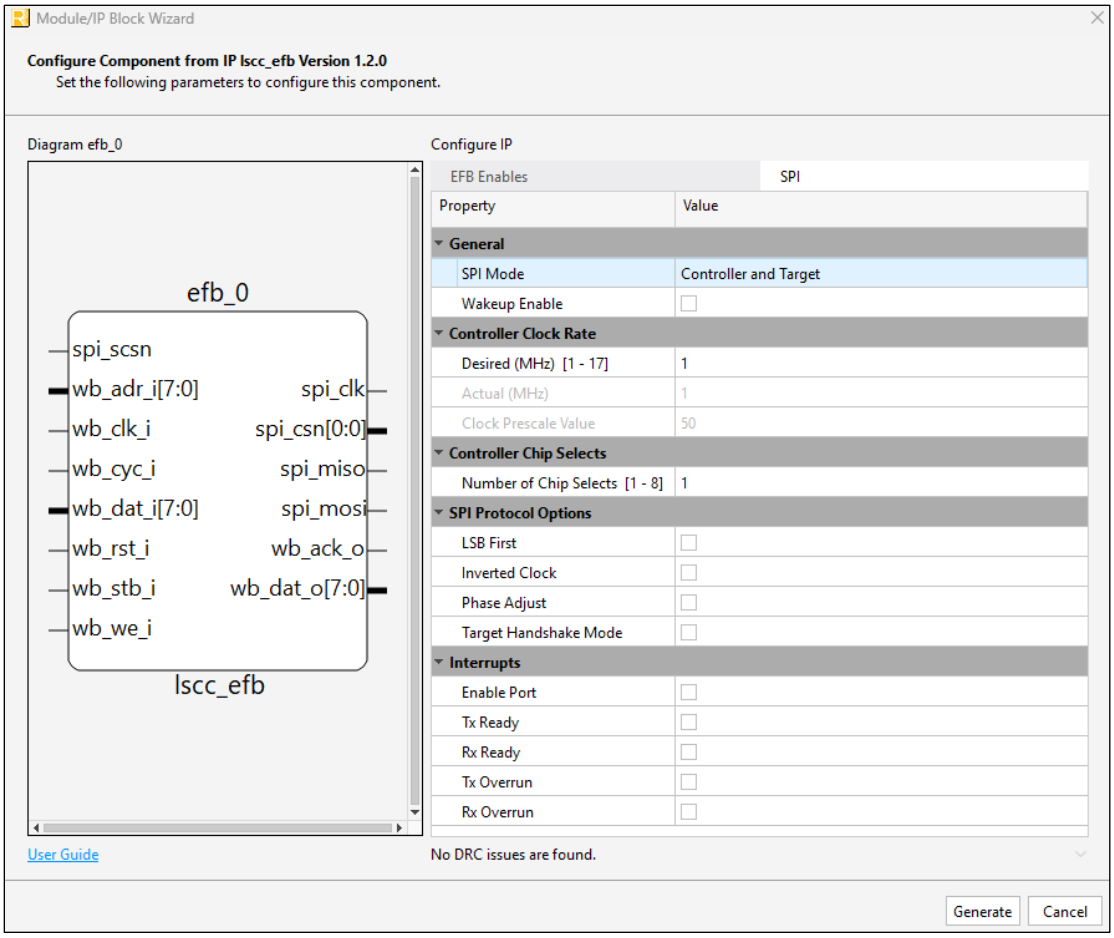


Figure 7.14. SPI Sample Configuration

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8. Design Considerations

Refer to the design tips in the MachXO4 Hardened Control Functions User Guide (FPGA-TN-02403) for suggestions on using the various MachXO4 EFB functions.

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Appendix A. Resource Utilization

Table A.1 shows a sample resource utilization of the EFB Module IP core on the LFMXO4-110HE-6BBG484I device.

Table A.1. LFMXO4-110HE-6BBG484I Device Resource Utilization

IP Configuration	Registers	LUTs	EFB	Fmax (MHz)[1]
(Default) User Interface Enabled (WISHBONE) • Interface Clock: 133 MHz I2C Cores Enabled (Primary I2C: Flash Access) User Flash Memory Enabled	0	0	1	133.014 (wb_clk_i)
User Interface Enabled (WISHBONE) • Interface Clock: 133 MHz SPI Core Enabled (Controller and Target) • SPI Clock: 45 MHz • CS Pins: 8 User Flash Memory Enabled	0	0	1	133.014 (wb_clk_i)
User Interface Disabled Timer/Counter Enabled Prescale Divider Value: 8	0	0	1	133.014 (tc_clki)

Note:

1. The maximum WISHBONE clock that can be configured is 133 MHz. Fmax is generated when the FPGA design contains only the EFB Module IP core and the target frequency is 133 MHz. These values may be reduced when user logic is added to the FPGA design.

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References

- MachXO4 EFB Module IP Release Notes (FPGA-RN-02079)
- MachXO4 Hardened Control Functions User Guide (FPGA-TN-02403)
- MachXO4 Hardened Control Functions Reference Guide (FPGA-TN-02404)
- Lattice Radiant Timing Constraints Methodology (FPGA-AN-02059)
- MachXO4 Root of Trust Tamper Detection/Response (FPGA-TN-02434)
- MachXO4 web page
- Lattice Radiant Software web page
- Lattice Solutions IP Cores web page
- Lattice Solutions Reference Designs web page
- Lattice Insights web page for Lattice Semiconductor training courses and learning plans

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Revision History

Note: In some instances, the IP may be updated without changes to the user guide. The user guide may reflect an earlier IP version but remains fully compatible with the later IP version. Refer to the IP Release Notes for the latest updates.

Revision 1.2, IP v1.3.0, October 2026

Section	Change Summary
All	Made editorial fixes.
Abbreviations in This Document	Added *ISC*, *RoT*.

Introduction	• Expanded the flash memory interface control functions in the Overview of the IP section.
	• In Table 1.1. Summary of the EFB Module IP:
	  • Updated *Lattice Implementation*.
	  • Added a table note for the MachXO4 device family.
	• In Table 1.2. EFB Module IP Support Readiness:
	  • Removed the *Hardware Validated* column.
	  • Added the *CFG* and *Tamper Detect/Response* features.
	• Added the MachXO4 RoT feature row and security blocks feature in the Features section.

Functional Description	• Updated Figure 2.1. EFB Module IP Block Diagram, Figure 2.2. EFB Module IP Clock Overview, and Figure 2.3. EFB Module IP Reset Overview. • Updated the WISHBONE Bus Interface (Register Access), I2C IP Cores, and Primary I2C sections. • Added the APB section. • Added MachXO4 RoT flash architecture to the Flash Access Interface section.
IP Parameter Description	• Updated Table 3.1. EFB Enables Attributes. • Updated the selectable values for the *Timer/Counter Mode* attribute in Table 3.4. Timer/Counter Attributes. • Updated the selectable values for the *Number of Pages* attribute in Table 3.5. UFM Attributes. • Updated the Clear Timer on Compare Match Mode and CFG/UFM sections. • Added the Initializing UFM and Tamper sections.
Signal Description	In Table 4.1. EFB Module IP Ports: • Moved the *wb_clk_i* and *wb_rst_i* signals to the WISHBONE Interface port group. • Added bit width annotations for the *wb_adr_i*, *wb_dat_i*, *wb_dat_o*, *pll0_dati_i*, *pll0_addr_o*, *pll0_dato_o*, *pll1_dati_i*, *pll1_addr_o*, and *pll1_dato_o* signals. • Added the *APB Interface* and *Tamper Detect/Response* port groups.
Register Description	Updated this section.
Command and Data Transfers to Flash Space	Updated this section.
Designing with the IP	• Updated Figure 7.1. Module/IP Block Wizard, Figure 7.2. IP Configuration, Figure 7.3. Check Generated Result, Figure 7.5. Add and Reorder Source, and Figure 7.7. Sample Testbench Overview. • Updated the reference for the I2C and UFM sample configurations in the Generating and Instantiating the IP section. • Removed the template files in Table 7.1. Generated File List. • Updated the *CFG/UFM* feature description and added the *Tamper Detect/Response* feature to the Simulation Results section.
References	Added *MachXO4 Root of Trust Tamper Detection/Response (FPGA-TN-02434)*.

Revision 1.1, IP v1.2.0, December 2025

Section	Change Summary
Register Description	Updated the *DIVIDER* description for Table 5.16. SPI Clock Prescale.

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Revision 1.0, IP v1.2.0, December 2025

Section	Change Summary
All	• Updated the IP version information on the cover page. • Added a note on the IP version in the *Quick Facts* and *Revision History* sections. • Made editorial fixes.
Abbreviations in This Document	Added *ACK*, *APB*, *CTCM*, *GUI*, *GPIO*, *LSE*, *MDF*, *NACK*, *PFCPWM*, *PLL*, and *PWM*.

Introduction	• In the Overview of the IP section, added the following control functions:
	  • One SPI core
	  • One 16-bit Timer/Counter
	  • Interface to the dynamic PLL configuration settings
	  • Interface to the on-chip power controller through I2C and SPI
	• Updated *Resource Utilization* and *Lattice Implementation* in Table 1.1. Summary of the EFB Module IP.
	• Updated Table 1.2. EFB Module IP Support Readiness.
	• Updated the Features section and added the Attribute Names section.

Functional Description	• Updated Figure 2.1. EFB Module IP Block Diagram – Figure 2.5. EFB Module I2C Core Interface and Figure 2.8. EFB Module Flash Interface. • Updated Table 2.1. User Interfaces and Supported Protocols. • Added Register Access to the WISHBONE Bus Interface (Register Access) section title. • Added SPI IP Core and WISHBONE Controller (for PLL) sections. • Updated the Flash Access Interface section.
IP Parameter Description	Updated this section.
Signal Description	• Replaced the *Interrupt Ports* subtable header with *Flash Memory*. • Added *SPI Interface*, *Timer/Counter*, *PLL0 (WISHBONE)*, *PLL1 (WISHBONE)*, and *Power Controller* ports.
Register Description	Added the SPI Registers and Timer/Counter Registers sections.
Command and Data Transfers to Flash Space	Added the SPI Framing section.

Designing with the IP	• Added a note on screenshots in this section.
	• Updated the Simulation Results section.
	• Added SPI core signals description to the Physical Constraints section.
	• Add the SPI Core Transaction Example section.
	• Updated the following figures:
	  • Figure 7.1. Module/IP Block Wizard
	  • Figure 7.2. IP Configuration
	  • Figure 7.3. Check Generated Result
	  • Figure 7.5. Add and Reorder Source
	  • Figure 7.7. Sample Testbench Overview
	  • Figure 7.11. I2C Sample Configuration (Primary and Secondary I2C Enabled)
	  • Figure 7.12. UFM Access Sample Configuration (through Wishbone and I2C Access)

Design Considerations	Added this section.
Resource Utilization	Updated this section.
References	Added *MachXO4 EFB Module IP Release Notes (FPGA-RN-02079)*, *MachXO4 Hardened Control Functions User Guide (FPGA-TN-02403)*, *MachXO4 Hardened Control Functions Reference Guide (FPGA-TN-02404)*, and *MachXO4 web page*.

Revision 0.80, IP v1.0.0, June 2025

Section	Change Summary
All	Initial release.

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