Lattice Sentry I2C Filter IP

IP Version: v1.4.1

Release Notes

FPGA-RN-02070-1.1

June 2026

Disclaimers

Lattice makes no warranty, representation, or guarantee regarding the accuracy of information contained in this document or the suitability of its products for any particular purpose. All information herein is provided AS IS, with all faults, and all associated risk is the responsibility entirely of the Buyer. The information provided herein is for informational purposes only and may contain technical inaccuracies or omissions, and may be otherwise rendered inaccurate for many reasons, and Lattice assumes no obligation to update or otherwise correct or revise this information. Products sold by Lattice have been subject to limited testing and it is the Buyer's responsibility to independently determine the suitability of any products and to test and verify the same. LATTICE PRODUCTS AND SERVICES ARE NOT DESIGNED, MANUFACTURED, OR TESTED FOR USE IN LIFE OR SAFETY CRITICAL SYSTEMS, HAZARDOUS ENVIRONMENTS, OR ANY OTHER ENVIRONMENTS REQUIRING FAIL-SAFE PERFORMANCE, INCLUDING ANY APPLICATION IN WHICH THE FAILURE OF THE PRODUCT OR SERVICE COULD LEAD TO DEATH, PERSONAL INJURY, SEVERE PROPERTY DAMAGE OR ENVIRONMENTAL HARM (COLLECTIVELY, "HIGH-RISK USES"). FURTHER, BUYER MUST TAKE PRUDENT STEPS TO PROTECT AGAINST PRODUCT AND SERVICE FAILURES, INCLUDING PROVIDING APPROPRIATE REDUNDANCIES, FAIL-SAFE FEATURES, AND/OR SHUT-DOWN MECHANISMS. LATTICE EXPRESSLY DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY OF FITNESS OF THE PRODUCTS OR SERVICES FOR HIGH-RISK USES. The information provided in this document is proprietary to Lattice Semiconductor, and Lattice reserves the right to make any changes to the information in this document or to any products at any time without notice.

Inclusive Language

This document was created consistent with Lattice Semiconductor’s inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice’s inclusive language FAQ 6878 for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

© 2025 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Contents

Contents 3
1. Introduction 4
Lattice Sentry I2C Filter IP v1.4.1 4
Lattice Sentry I2C Filter IP v1.4.0 4
Lattice Sentry I2C Filter IP Earlier Versions 4
References 5
Technical Support Assistance 6

© 2025 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

1. Introduction

This document contains the Release Notes for the Lattice Sentry I2C Filter IP. For specific details about the IP, refer to the following:

- Lattice Sentry I2C Filter IP User Guide (FPGA-IPUG-02166)

Lattice Sentry I2C Filter IP v1.4.1

Software	Software Version	Summary of Changes
Lattice Radiant Lattice Propel Builder	2026.1	Fixed the dual-port RAM implementation to ensure correct operation on MachXO4 devices. **Note:** There are no updates to the IP user guide for this release. Refer to the Lattice Sentry I2C Filter IP User Guide (FPGA-IPUG-02166, v1.4) for the applicable documentation.

Lattice Sentry I2C Filter IP v1.4.0

Software	Software Version	Summary of Changes
Lattice Radiant Lattice Propel Builder	2025.2	• Added support for MachXO4 devices. • Updated GUI to remove tool selection.

Lattice Sentry I2C Filter IP Earlier Versions

IP Version	Summary of Changes
1.3.0	Fixed glitch filter when clock stretching is enabled.
1.2.0	Fixed handling of clock stretching.
1.1.0	• Added SCL speed select port to control output SCL frequency. • Improved clock stretching feature. • Added support for MachXO5-NX devices.
1.0.0	Initial release.

© 2025 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

References

- Lattice Sentry I2C Filter IP User Guide (FPGA-IPUG-02166)
- Mach-NX web page
- MachXO3D web page
- MachXO4 web page
- MachXO5-NX web page
- Lattice Sentry I2C Filter IP Core web page
- Lattice Diamond Software web page
- Lattice Propel Design Environment web page
- Lattice Radiant Software web page
- Lattice Solutions IP Cores web page
- Lattice Solutions Reference Designs web page
- Lattice Insights web page for Lattice Semiconductor training courses and learning

© 2025 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

© 2025 Lattice Semiconductor Corp. All Lattice trademarks, registered trademarks, patents, and disclaimers are as listed at www.latticesemi.com/legal.
All other brand or product names are trademarks or registered trademarks of their respective holders. The specifications and information herein are subject to change without notice.



www.latticesemi.com