Lattice Radiant 2024.2.1 Software Release Notes

Welcome to Lattice Radiant® software, the complete design environment for Lattice Semiconductor Field Programmable Gate Arrays (FPGAs).

What's New in Radiant 2024.2.1 Software

- **Radiant Installer**
  - A new version of the Radiant installer has been uploaded to the Lattice website, solving a potential error encountered when running PAR on Windows. Installing the latest 2024.2.1.330.0 version is recommended if you are currently using the 2024.2.1.327.3 version.

    Note: If you encounter an issue, reinstall the 2024.2.0.3.4 base version and then install version 2024.2.1.330.

  - **Installation Instructions:**

    Refer to the list below for the instructions to install the new version of the Radiant software. Also ensure that no instances of Radiant are running before attempting to install the new version.

    To install the new version on Windows:

    1. Extract the zip file and navigate to the location where you want to save it.
    2. Double-click the 2024.2.1.330.0_Radiant.exe file to install the software.

    To install the new version on Linux:

    1. Extract the zip file and navigate to the location where you want to save it.
    2. Execute the Radiant run file as follows:

       % cd <directory_with_RUN>

       % ./ 2024.2.1.330.0_Radiant_lin.run

- **Device Support:**
  - Lattice Avant™ (LAV-AT)
    - E50 (-1/-2/-3) 0.82V (COM/IND) – CBG484
    - E70 (-1/-2/-3) 0.82V (COM/IND) – CBG484, LFG676, CSG841, LFG1156

- **Tool and Other Enhancements:**
  - **Device –** Security bitstream and GUI, Programming, and Reveal Debugger have been updated to support the LAV-AT-E50 and LAV-AT-E70 devices.
  - **Reveal**
    - Reveal debugger (Logic Analyzer and Controller) supports the latest Avant-E70 and Avant-E50 silicon.
    - For Avant devices, Reveal supports SerDes debugging with IBERT (Integrated Bit Error Tester) and the optimization of transceiver channels.

Updating Projects from an Earlier Version

If you want to work on a design project created with an earlier version of Radiant software, it may be necessary to re-create some IP, per the procedures described in the following table.

These procedures adapt the project for the changes in Radiant software.

Versions	IP			IP Regeneration Procedures
	Avant (LAV-AT)	**CrossLink-NX (LIFCL), Certus-NX (LFD2NX), Certus-NX-RT (UT24C), CertusPro-NX (LFCPNX), and CertusPro-NX-RT (UT24CP), MachXO5-NX (LFMXO5)**	**iCE40UP**	
2024.2.1	FIFO_DC MPPHY	N/A	N/A	These IP used in designs created in Radiant 2024.2 or earlier must be re-generated in Radiant 2024.2.1.
2024.2	DDR Generic DDR 7:1 SDR	DDR Memory PLL SDR	N/A	These IP used in designs created in

Versions	IP			IP Regeneration Procedures
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	PLL	Barrel Shifter		Radiant 2024.1.1 or earlier must be re-generated in Radiant 2024.2.
	DDRPHY	FIFO		
	MIPI DPHY	FIFO_DC		
	MPPHY	RAM_DP		
	SEDC	RAM_DP_True		
	Barrel Shifter	RAM_DQ		
	FIFO	ROM		
	FIFO_DC			
	RAM_DP			
	RAM_DP_True			
	RAM_DQ			
	ROM			

Supported Devices

Lattice Radiant software can be used with either a free license or a subscription license. The two licenses provide access to different device families.

Device Family	Free License	Subscription License
iCE40 UltraPlus (iCE40UP)	◀	
Lattice Avant (LAV-AT-E)		◀
CertusPro™-NX (LFCPNX)	Evaluation Mode	◀
Certus™-NX (LFD2NX)	◀	
Certus™-N2 (LN2-CT-ES)	Evaluation Mode	◀
MachXO5™-NX (LFMXO5)	Evaluation Mode	◀
CrossLink-NX (LIFCL)	◀	
Certus™-NX-RT (UT24C)		RT Subscription

Device Family	Free License	Subscription License
CertusPro™-NX-RT (UT24CP)		RT Subscription

Support for Third-Party Synthesis and Simulator Tools

The Synopsys Synplify Pro® for Lattice synthesis tool and the Siemens QuestaSim® Lattice Edition simulator tools are included in the Radiant software.

- **Synopsys Synplify Pro FPGA synthesis software version V-2023.09LR-2**
  - Release Notes for Synplify Pro are located in ..\<*install_directory*>\radiant\2024.2\synpbase\doc\. The file name is release_notes.pdf.
  - A full set of documents for Synplify Pro are also located in \<*install_directory*>\radiant\2024.2\synpbase\doc\.
- **Siemens QuestaSim Lattice Edition 2024.2**
  - Release Notes for QuestaSim Lattice Edition are located in <install_directory>\radiant\2024.2\questasim\. The file names are RELEASE_NOTES.html or RELEASE_NOTES.txt.
  - A full set of documents for QuestaSim Lattice Edition are located in <install_directory>\radiant\2024.2\questasim\docs\pdfdocs.
- **Siemens Questa® 2022.3**
- **Cadence Xcelium® 24.09.005**
- **Synopsys VCS® U-2023.12-SP2**

Help Resources

- Online Help updated with CertusPro-NX (LFCPNX), Certus-NX (LFD2NX), Certus-N2 (LN2-CT-ES), MachXO5-NX (LFMXO5), CrossLink-NX (LIFCL), Certus-NX-RT (UT24C), CertusPro-NX-RT (UT24CP), and Lattice Avant (LAV-AT) content.
- To view the Online Help, start the Lattice Radiant software and select the 

"Getting Started" icon under Information Center.

  Note: The Firefox Snap install is not supported if you are using Ubuntu 20.04 or 18.04 to access the Radiant Help. This is a result of the snap install's inability to open local HTML pages. You may reinstall the latest version of Firefox using Apt install. For installation instructions, please refer to this guide.

System Requirements

The following shows the basic system requirements for Radiant software:

- Intel x86 64-bit or 64-bit-compatible PC
- OS Support:

64-bit OS	Radiant	Synplify Pro	QuestaSim
Windows 10	✓	✓	✓
Windows 11	✓	✓*	✓*
Red Hat Enterprise Linux 7.9	✓	✓	✓
Red Hat Enterprise Linux 8.8	✓	✓	✓
Ubuntu version 20.04 LTS	✓	✓*	✓*
Ubuntu version 22.04 LTS	✓	✓*	✓*

***Note**: The third-party tools have been tested by Lattice on the listed platforms, but the vendors do not officially support them.

- Approximately 50 GB free disk space
- Computer Memory Requirement:
  - Nexus – 16GB
  - LAV-AT– 32GB Recommended for running a single project. If running multiple projects, the memory requirement will be higher.
- 1024 X 768 graphics display
- Network adapter for license and network connectivity
- A Web browser with JavaScript capability
- Acrobat Reader

Issues Fixed in this Release

The following known issues are fixed in this release. Their workarounds are no longer needed.

The DDRPHY64D, DDRPHY64E, and DDRPHY72D primitives are incompatible with the LN2-CT-20 device.

Devices affected: Certus-N2 (LN2-CT)

Bug number: DNG-24598

Place and Route outputs high CLK/CE/SR utilization, resulting to the following error: “ERROR <63101006> - Cannot place all instances into the device. Please increase all region constraints (if any) by at least 1 PLCs.”

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-25194

The datasheet link for the Certus-N2 device is incorrect.

Devices affected: Certus-N2 (LN2-CT)

Bug number: DNG-24786

Issue in handling differential I/O in Place & Route results in “ERROR <61293290> - par: This design requires at least 413 HPIO pins to be placed, but only 412 HPIO pins are available”.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-25135

When using the Programmer tool, the Program and Verify option may fail, displaying a "Split_Verify" error message.

Device affected: CertusPro-NX (LFCPNX)

Bug number: DNG-24900

PLL with REFCLK locked at "C17" can be placed at any available PLL site, and the REFCLK input can be routed to the PCLK tree.

Device affected: Lattice Avant (LAV-AT)

Bug number: DNG-24812

When running the PAR process, “netcheck: Signal found floating net segments” error occurs. This error may occur when one IO is driving multiple PLL clock inputs, and when IO is manually located by the user at a dedicated pin.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-24766

Incorrect clock pin causes internal fatal error on PAR in Certus-NX device.

Devices affected: Certus-NX (LFD2NX)

Bug Number: DNG-24440

FIFO DC Mixed width configuration has incorrect read data.

Devices affected: CertusPro-NX (LFCPNX)

Bug Number: DNG-24678

You may encounter an issue when using Place & Route due to the Radiant version 2024.2 causing hardware failure in iCE40 devices.

Devices affected: iCE40UP (iCE40 UltraPlus)

Bug Number: DNG-25165

Potential Synplify synthesis crash in Avant projects that include LPDDR4.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-24791

When using Synplify Pro, you may encounter the following error during macro reuse: “Synthesis exit by 9. Child process exited abnormally. Done: error code 1.”

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-20116

The PDPSC32K primitive does not have an output path despite outreg being used.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-20772

Known Issues for Radiant 2024.2.1

The following are known issues for the Radiant Software 2024.2.1. For assistance with these issues, please contact Lattice Technical support.

In the Bitstream Security GUI settings, you can see all options for ECDSA and RSA being active. However, there should be no RSA option and ECDSA should be limited to EDSA521 for the LN2-C20ES and LAV-AT-E70ES1 devices.

The Bitgen tool does not prohibit the bitstream generation for these options, and if you generate the bitstream, it will not work on the board.

Devices affected: Certus-N2 (LN2-C20ES), Lattice Avant (LAV-AT-E70ES1)

Bug number: DNG-26309

MPPHY (IP, JESD204C) RTL simulation failed, Error: Data mismatch detected.

All configurations are failing for normal transactions due to testbench limitations.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-25991

MPPHY (IP, Ethernet, 25GBASE-R_RSFEC) Post-Synthesis simulation failed, Error: Data mismatch detected, received data is not installing.

Failed pma_rxdata_o check due to testbench updates.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-25990

MPPHY (IP, Ethernet, SyncE_10G) RTL simulation failed, Error: Data mismatch detected.

All configurations are failing for normal transactions due to testbench limitations.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-25989

The LAV-AT-X50 Device Folder under Primitives Template in Radiant GUI is missing.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-25633

Programming File Utility cannot switch windows when multiple files are open.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-25746

The Area-Optimized (HW) setting on the FIFO_DC IP catalog encounters a configuration issue in Avant.

Devices affected: Lattice Avant (LAV-AT), Certus-N2 (LN2-CT)

Bug number: DNG-25669

The Pinout by Pin Number section in the PAD report is missing nine pins when compared to the DCE pins spreadsheet view.

Devices affected: Certus-N2 (LN2-CT)

Bug number: DNG-25644, DNG-25642

The Power Calculator's Power File Revision for Avant-E70/50 should be marked as "Preliminary," not "Advanced."

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-25577

SEI Editor shows incorrect behavior for different devices.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-25902

Errors may occur when compiling the Lattice encrypted device library with Questa on Ubuntu systems.

Workaround: The environment variable LD_PRELOAD needs to be unset and/or the /etc/ld.so.preload file should be deleted or empty before using Questa to compile the library.

Devices affected: MachXO5-NX (LFMXO5)

Bug number: DNG-25863

Avant devices have missing SSO feature in Device Constraint Editor.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-25701

The PMI and Primitive templates do not include the LN2-CT device.

Devices affected: Certus-N2 (LN2-CT)

Bug number: DNG-25693

The location for a secured component (Hard DPHY) cannot be changed.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-24746

The expected behavior of Write Enable in a FIFO/EBR for Avant Simulation models was not captured with the WrEn assertion.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-24347

Unsupported components may still pass synthesis when using both Synplify Pro and LSE.

SEDCA, UMXSPI, and UXSPI are not available for the E30ES device, but the synthesis step in Radiant project flow may still pass.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-24562

IDDRX2 has exceptionally large C2INP_DEL value.

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-24167

CONFIG_LMMIE and CONFIG_LMMIB RTL simulation fails.

Devices affected: MachXO5-NX (LFMXO5)

Bug number: DNG-22187

The clock, using pclk routing and connected only to fabric registers, has a lower clock MPW at the higher speed grade (-8).

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-21315

The “Trace_Length” and “Package_Delay” data of LFD2NX-9/17's CABGA196 package is missing in the .pkt file.

Devices affected: Certus-NX (LFD2NX)

Bug number: DNG-23568

Synplify Pro fails in FSM with initial value case and reports an error instead of a warning.

Workaround: Remove the initial value since this value can be assigned during reset (the 'reset' signal in this design") task.

Devices affected: CertusPro-NX (LFCPNX), Certus-NX (LFD2NX), MachXO5-NX (LFMXO5), CrossLink-NX (LIFCL), Certus-NX-RT (UT24C), CertusPro-NX-RT (UT24CP)

Bug number: DNG-24118

MPPHY (IP, Generic G8B10B, X1_5X4, G70) RTL simulation failed, Error: Found MPPHY Clock Out mismatched .= 2

Device affected: Lattice Avant (LAV-AT)

Bug number: DNG-23343

Power Calculator resource usage reporting is incorrect.

The report shows that MPP is utilized at 100% regardless of the number of lanes used, due to the current power modeling treating the entire IP as a single unit.

Device affected: Lattice Avant (LAV-AT)

Bug number: DNG-23785

Synplify Pro incorrectly removes virtual wire signals that were preserved using the "syn_rvl_debug" attribute.

Devices affected: All devices

Bug number: DNG-21236

Synplify Pro does not report an error or warning for clocks that are driven by logic.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-21048

The PDPSC32K primitive does not have an output path despite outreg being used.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-20772

You may encounter an issue with CONFIG_LMMI and CONFIG_LMMA's lmmi_ready signal during simulation.

Devices affected: Certus-NX (LFD2NX), CrossLink-NX (LIFCL)

Bug number: DNG-20717

CONFIG_LMMI RTL simulation error occurs and data missing in output ports.

Devices affected: Certus-NX (LFD2NX), CrossLink-NX (LIFCL)

Bug number: DNG-20543

Synplify Pro does not correctly process macro creation constraints with escape characters.

Devices affected: CertusPro-NX (LFCPNX), Certus-NX (LFD2NX), CrossLink-NX (LIFCL), Certus-NX-RT (UT24C), CertusPro-NX-RT (UT24CP)

Bug number: DNG-20134

IBIS reports I/O models of some sysCONFIG pins even if they are used as GPIO.

Workaround: Remove duplicated pins in IBIS file.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-19646

Simulation with XCELIUM may fail when simulating projects using the CNTL_LR_U_POWER primitive due to incorrect compilation order of cmpl_libs.

Devices affected: CrossLink-NX (LIFCL-33U)

Bug number: DNG-19623

Cannot assign input ports as MIPI_DPHY type for Avant.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-19199

Reveal Power-on Reset (POR) Debug function does not work when using LSE with only one Trigger Unit (TU).

Workaround: Add another Trigger Unit (TU) that can be unrelated to POR Debug.

Devices affected: All devices except iCE40UP

Bug number: DNG-13901

The CSI-2/DSI D-PHY Transmitter and Receiver Soft IP simulations fail when using Synopsys VCS as simulation tool.

Devices affected: CertusPro-NX (LFCPNX), Certus-NX (LFD2NX), CrossLink-NX (LIFCL), Certus-NX-RT (UT24C), CertusPro-NX-RT (UT24CP)

Bug number: DNG-13225

Post-route simulation error when using GDDR for Nexus devices due to parameters not being passed correctly from the original RTL.

Workaround: Intrinsic delay similar to the delay value on the vo.vo file needs to be added to the IP testbench.

Devices affected: CertusPro-NX (LFCPNX), Certus-NX (LFD2NX), MachXO5-NX (LFMXO5), CrossLink-NX (LIFCL), Certus-NX-RT (UT24C), CertusPro-NX-RT (UT24CP)

Bug number: DNG-9639

MAP incorrectly reports number of DPHY and PCIE/ADC resources for CrossLink-NX (LIFCL) QFN72 package.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-8297