



Lattice Avant/Nexus 2 PLL Module

IP Version: v2.7.1

Release Notes

FPGA-RN-02066-1.1

October 2026

Disclaimers

Lattice makes no warranty, representation, or guarantee regarding the accuracy of information contained in this document or the suitability of its products for any particular purpose. All information herein is provided AS IS, with all faults, and all associated risk is the responsibility entirely of the Buyer. The information provided herein is for informational purposes only and may contain technical inaccuracies or omissions, and may be otherwise rendered inaccurate for many reasons, and Lattice assumes no obligation to update or otherwise correct or revise this information. Products sold by Lattice have been subject to limited testing and it is the Buyer's responsibility to independently determine the suitability of any products and to test and verify the same. LATTICE PRODUCTS AND SERVICES ARE NOT DESIGNED, MANUFACTURED, OR TESTED FOR USE IN LIFE OR SAFETY CRITICAL SYSTEMS, HAZARDOUS ENVIRONMENTS, OR ANY OTHER ENVIRONMENTS REQUIRING FAIL-SAFE PERFORMANCE, INCLUDING ANY APPLICATION IN WHICH THE FAILURE OF THE PRODUCT OR SERVICE COULD LEAD TO DEATH, PERSONAL INJURY, SEVERE PROPERTY DAMAGE OR ENVIRONMENTAL HARM (COLLECTIVELY, "HIGH-RISK USES"). FURTHER, BUYER MUST TAKE PRUDENT STEPS TO PROTECT AGAINST PRODUCT AND SERVICE FAILURES, INCLUDING PROVIDING APPROPRIATE REDUNDANCIES, FAIL-SAFE FEATURES, AND/OR SHUT-DOWN MECHANISMS. LATTICE EXPRESSLY DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY OF FITNESS OF THE PRODUCTS OR SERVICES FOR HIGH-RISK USES. The information provided in this document is proprietary to Lattice Semiconductor, and Lattice reserves the right to make any changes to the information in this document or to any products at any time without notice.

Inclusive Language

This document was created consistent with Lattice Semiconductor's inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice's inclusive language [FAQ 6878](#) for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

Contents

Contents 3

1. Introduction 4

 PLL Module v2.7.1 4

 Corrections to Previous Release Notes..... 4

 PLL Module v2.7.0 4

 PLL Module v2.6.1 4

 PLL Module v2.6.0 4

 Lattice Avant PLL Module Earlier Versions 4

References 6

Technical Support Assistance 7

1. Introduction

This document contains the Release Notes for the PLL Module. For specific details about the IP, refer to the following:

- [Lattice Avant/Nexus 2 PLL Module User Guide \(FPGA-IPUG-02220\)](#)

PLL Module v2.7.1

Software	Software Version	Summary of Changes
Lattice Radiant	2026.1.1	• Removed the SIMULATION flag guard from the initial block that initializes rst_n_reg, bw_usr_regval, and nf_usr_regval. Enabled the registers by default in simulation. • Added the EN_PARAM_CHECK guard to make parameter checking optional in the testbench. In the GUI, use the Simulation Type option only for parameter checking. • Updated the width of the APB Write Data signal and the APB Read Data signal.

Corrections to Previous Release Notes

- In IP version 2.6.0, support for Certus-N2 and Mach-N2 devices was omitted from the release notes.

PLL Module v2.7.0

Software	Software Version	Summary of Changes
Lattice Radiant	2026.1	Updated the LMMI read-back path (RDATA, RDATAVALID, READY) to route through PLL_LMMI_MUX for LMMI register interface mode.

PLL Module v2.6.1

Software	Software Version	Summary of Changes
Lattice Radiant	2025.2.1	Annotated clock output ports with frequency values for the Lattice Propel clock DRC.

PLL Module v2.6.0

Software	Software Version	Summary of Changes
Lattice Radiant	2024.2	• De-feature Config wait for lock. • Updated constraint. • Added limitation on maximum VCO when using dynamic phase shift with phase advance. • Updated CLKPHY output divider range up to 256.

Lattice Avant PLL Module Earlier Versions

IP Version	Summary of Changes
2.5.0	Added bandwidth initialization logic.
2.4.0	• Set the LOSS_LOCK_DETECTION parameter to disable. • Updated device name.
2.3.0	Restricted feedback divider to integer only when using external clock as feedback.
2.2.0	Updated VCO range and parameter optimization calculation.
2.1.0	• Updated port name in constraint file. • Added the CONFIG_WAIT_FOR_LOCK parameter.

IP Version	Summary of Changes
2.0.0	Added support for Lattice Avant devices.

References

- [Lattice Avant/Nexus 2 PLL Module User Guide \(FPGA-IPUG-02220\)](#)
- [Avant-E](#) web page
- [Avant-G](#) web page
- [Avant-X](#) web page
- [Certus-N2](#) web page
- [Mach-N2](#) web page
- [Lattice Radiant Software](#) web page
- [Lattice Insights](#) for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.



www.latticesemi.com