



System Memory Module

IP Version: v2.6.0

Release Notes

FPGA-RN-02065-1.5

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Inclusive Language

This document was created consistent with Lattice Semiconductor's inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice's inclusive language [FAQ 6878](#) for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

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1. Introduction

This document contains the Release Notes for the System Memory Module. For specific details about the IP, refer to the following:

- [System Memory Module User Guide \(FPGA-IPUG-02073\)](#)

System Memory Module v2.6.0

Software	Software Version	Summary of Changes
Lattice Propel	2026.1	Added support for the AHB-Lite low-latency mode.

System Memory Module v2.5.1

Software	Software Version	Summary of Changes
Lattice Propel	2025.2	Fixed bug for MachXO4 devices. Note: There are no updates to the IP user guide for this release. Refer to the <i>System Memory Module User Guide (FPGA-IPUG-02073, v2.4)</i> for the applicable documentation.

System Memory Module v2.5.0

Software	Software Version	Summary of Changes
Lattice Propel	2025.2	<ul style="list-style-type: none"> • Added the AXI4 atomic access feature. • Added support for MachXO4 devices.

System Memory Module v2.4.0

Software	Software Version	Summary of Changes
Lattice Propel	2025.1	<ul style="list-style-type: none"> • Added AXI interface support for ECP5 devices. • Added support for 64-bit data width on the AXI interface.

System Memory Module v2.3.1

Software	Software Version	Summary of Changes
Lattice Propel	2024.2.1	Fixed the Memory Address Depth parameter in the graphical user-interface (GUI).

System Memory Module Earlier Versions

IP Version	Summary of Changes
2.3.0	<ul style="list-style-type: none"> • Added LN2-CT support. • Enhancements with AXI4 performance. • Disabled output register for AXI4.
2.2.0	<ul style="list-style-type: none"> • Added ECP5 support and other enhancements.
2.1.0	<ul style="list-style-type: none"> • Support Read Pipeline for timing enhancement.
2.0.0	<ul style="list-style-type: none"> • Added AXI4 Interface support.
1.1.2	<ul style="list-style-type: none"> • Support for LAV-AT devices.
1.1.1	<ul style="list-style-type: none"> • Support for 208 EBRs in CertusPro-NX devices.

IP Version	Summary of Changes
1.1.0	<ul style="list-style-type: none"><li data-bbox="428 235 1019 262">• Added support for up to 7 LRAMs in CertusPro-NX devices.
1.0.4	<ul style="list-style-type: none"><li data-bbox="428 270 1284 298">• Support for MachXO2, MachXO3L and improved timing for LRAM implementations.
1.0.3	<ul style="list-style-type: none"><li data-bbox="428 306 688 333">• Support for Mach-NX.
1.0.2	<ul style="list-style-type: none"><li data-bbox="428 342 732 369">• Support for CertusPro-NX.
1.0.1	<ul style="list-style-type: none"><li data-bbox="428 378 829 405">• Support for Crosslink-NX, Certus-NX.
1.0.0	<ul style="list-style-type: none"><li data-bbox="428 413 613 441">• Initial release.

References

- [System Memory Module User Guide \(FPGA-IPUG-02073\)](#)
- [iCE40 UltraPlus](#) web page
- [LatticeECP3](#) web page
- [ECP5 / ECP5-5G](#) web page
- [CrossLink-NX](#) web page
- [Certus-NX](#) web page
- [Certus-N2](#) web page
- [CertusPro-NX](#) web page
- [Mach-NX](#) web page
- [MachXO2](#) web page
- [MachXO3](#) web page
- [MachXO3D](#) web page
- [MachXO4](#) web page
- [MachXO5-NX](#) web page
- [Avant-E](#) web page
- [Avant-G](#) web page
- [Avant-X](#) web page
- [System Memory Module IP Core](#) web page
- [Lattice Radiant Software](#) web page
- [Lattice Propel Design Environment](#) web page
- [Lattice Diamond Software](#) web page
- [Lattice Insights](#) for Lattice Semiconductor training courses and learning plans

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For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.



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