Lattice Radiant 2024.2 Software Release Notes

Welcome to Lattice Radiant® software, the complete design environment for Lattice Semiconductor Field Programmable Gate Arrays (FPGAs).

What's New in Radiant 2024.2 Software

- **Device Support:**
  - Certus™-N2 (LN2-CT-ES)
    - 22K (-1/-2/-3) 0.82V (COM/IND) – ASG410, CBG484
- **Tool and Other Enhancements:**
  - **Design Rule Checking** – Lattice Synthesis Engine (LSE) now supports a standalone design rule checking flow to lint user RTL.
  - **Power Calculator**
    - The User Entered Tj has been added to Power Calculator Environment section allowing users to enter junction temperature directly.
    - Utilization table for each tab has been added to show the percentage of resources used for each IP after power calculations.
    - For devices that supports boundary scanning, a radio option has been added at the top of the I/O tab allowing users to enable or disable boundary scanning.
  - **General Options –** The Check Controlled Device License is enabled by default if Radiant is newly installed. You have to manually enable it if you are using previous Radiant versions.
  - **Reports –** The Radiant Report Summary now includes the IP Summary Report, which displays the Lattice IP utilized in the design.
  - **Timing Analyzer –** The Waveform tab provides a visual reference to the Data Path, demonstrating how and where the constraints have been applied.
  - **Reveal –** Reveal now supports beta version of post-PAR Reveal debugger.

Updating Projects from an Earlier Version

If you want to work on a design project created with an earlier version of Radiant software, it may be necessary to re-create some IP, per the procedures described in the following table.

These procedures adapt the project for the changes in Radiant software.

Versions	IP			IP Regeneration Procedures
	Avant (LAV-AT)	**CrossLink-NX (LIFCL), Certus-NX (LFD2NX), Certus-NX-RT (UT24C), CertusPro-NX (LFCPNX), and CertusPro-NX-RT (UT24CP), MachXO5-NX (LFMXO5)**	**iCE40UP**	
2024.2	DDR Generic	DDR Memory		These IP used in designs created in Radiant 2024.1 or earlier must be re-generated in Radiant 2024.2.
	DDR 7:1	PLL		
	SDR	SDR		
	PLL	Barrel Shifter		
	DDRPHY	FIFO		
	MIPI DPHY	FIFO_DC		
	MPPHY	RAM_DP		
	SEDC	RAM_DP_True		
	Barrel Shifter	RAM_DQ		
	FIFO	ROM		
	FIFO_DC			
	RAM_DP			
	RAM_DP_True			
	RAM_DQ			
	ROM			

Supported Devices

Lattice Radiant software can be used with either a free license or a subscription license. The two licenses provide access to different device families.

Device Family	Free License	Subscription License
iCE40 UltraPlus (iCE40UP)	◀	
Lattice Avant (LAV-AT-E)		◀
CertusPro™-NX (LFCPNX)	Evaluation Mode	◀

Device Family	Free License	Subscription License
Certus™-NX (LFD2NX)	◄	
Certus-N2 (LN2-CT-ES)	Evaluation Mode	◄
MachXO5™-NX (LFMXO5)	Evaluation Mode	◄
CrossLink-NX (LIFCL)	◄	
Certus™-NX-RT (UT24C)		RT Subscription
CertusPro™-NX-RT (UT24CP)		RT Subscription

Support for Third-Party Synthesis and Simulator Tools

The Synopsys Synplify Pro® for Lattice synthesis tool and the Siemens QuestaSim® Lattice Edition simulator tools are included in the Radiant software.

- **Synopsys Synplify Pro FPGA synthesis software version V-2023.09LR-2**
  - Release Notes for Synplify Pro are located in ..\<*install_directory*>\radiant\2024.2\synpbase\doc\. The file name is release_notes.pdf.
  - A full set of documents for Synplify Pro are also located in \<*install_directory*>\radiant\2024.2\synpbase\doc\.
- **Siemens QuestaSim Lattice Edition 2024.2**
  - Release Notes for QuestaSim Lattice Edition are located in <install_directory>\radiant\2024.2\questasim\. The file names are RELEASE_NOTES.html or RELEASE_NOTES.txt.
  - A full set of documents for QuestaSim Lattice Edition are located in <install_directory>\radiant\2024.2\questasim\docs\pdfdocs.
- **Siemens Questa® 2022.3**
- **Cadence Xcelium® 23.03.003**
- **Synopsys VCS® U-2023.03-SP2**

Help Resources

- Online Help updated with CertusPro-NX (LFCPNX), Certus-NX (LFD2NX), MachXO5-NX (LFMXO5), CrossLink-NX (LIFCL), Certus-NX-RT (UT24C), CertusPro-NX-RT (UT24CP), and Lattice Avant (LAV-AT) content.
- To view the Online Help, start the Lattice Radiant software and select the  "Getting Started" icon under Information Center.

  Note: The Firefox Snap install is not supported if you are using Ubuntu 20.04 or 18.04 to access the Radiant Help. This is a result of the snap install's inability to open local HTML pages. You may reinstall the latest version of Firefox using Apt install. For installation instructions, please refer to this guide.

System Requirements

The following shows the basic system requirements for Radiant software:

- Intel x86 64-bit or 64-bit-compatible PC
- OS Support:

64-bit OS	Radiant	Synplify Pro	QuestaSim
Windows 10	✓	✓	✓
Windows 11	✓	✓*	✓*
Red Hat Enterprise Linux 7.9	✓	✓	✓
Red Hat Enterprise Linux 8.8	✓	✓	✓
Ubuntu version 20.04 LTS	✓	✓*	✓*
Ubuntu version 22.04 LTS	✓	✓*	✓*

***Note**: The third-party tools have been tested by Lattice on the listed platforms, but the vendors do not officially support them.

- Approximately 50 GB free disk space
- Computer Memory Requirement:
  - Nexus – 16GB
  - LAV-AT– 32GB Recommended for running a single project. If running multiple projects, the memory requirement will be higher.
- 1024 X 768 graphics display
- Network adapter for license and network connectivity
- A Web browser with JavaScript capability

Issues Fixed in this Release

The following known issues are fixed in this release. Their workarounds are no longer needed.

An error occurs during Place & Route due to the code referencing a null clock pin.

Devices affected: Certus-NX (LFD2NX)

Bug number: DNG-24440

Place & Route error occurs when PLL version 2.6 is used.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-23731

LUT4 resource usage is different when using Synplify Pro and LSE synthesis tools.

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-23772

When using MPCS IP V1.6.0 in PMA-only mode, no transactions are seen on the Tx side, and the pcsdata input differs from the serialized sd[x]txp_o.

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-23708

PCIe fails during MAP stage.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-23456

An error occurs when Reveal Analyzer continuously triggers and when the Start Polling button of virtual LED is clicked.

Devices affected: All Nexus devices

Bug number: DNG-23417

PLL Foundation IP encounters timing issue when using the *Select Register Interface* = APB attribute

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-23345

PLL Foundation IP has a chance of having a timing issue when the attribute *Select Register Interface* = None

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-23312

The bit location in SEI GUI is inconsistent with the bit location read from SEDC

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-21154

Known Issues for Radiant 2024.2

The following are known issues for the Radiant Software 2024.2. For assistance with these issues, please contact Lattice Technical support.

Potential Synplify synthesis crash in Avant projects that include LPDDR4.

In rare cases, projects including Avant LPDDR4 IP may trigger a crash in the Synplify synthesis tool.

Workaround: On impacted projects, use Lattice Synthesis Engine.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-24791

The datasheet link for the Certus-N2 device is incorrect.

Devices affected: Certus-N2 (LN2-CT)

Bug number: DNG-24786

The location for a secured component (Hard DPHY) cannot be changed.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-24746

The expected behavior of Write Enable in a FIFO/EBR for Avant Simulation models was not captured with the WrEn assertion.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-24347

The DDRPHY64D, DDRPHY64E, and DDRPHY72D primitives are incompatible with the LN2-CT-20 device.

It is not advisable to use these primitives as they are not supported by the LN2-CT-20 device even though they may be selectable in IP generation. For DDRPHY IP, the supported configurations are limited to x16, x32, and x40.

Devices affected: Certus-N2 (LN2-CT)

Bug number: DNG-24598

Unsupported components may still pass synthesis when using both Synplify Pro and LSE.

SEDCA, UMXSPI, and UXSPI are not available for the E30ES device, but the synthesis step in Radiant project flow may still pass.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-24562

IDDRX2 has exceptionally large C2INP_DEL value.

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-24167

CONFIG_LMMIE and CONFIG_LMMIB RTL simulation fails.

Devices affected: MachXO5-NX (LFMXO5)

Bug number: DNG-22187

The clock, using pclk routing and connected only to fabric registers, has a lower clock MPW at the higher speed grade (-8).

Devices affected: CertusPro-NX (LFCPNX)

Bug number: DNG-21315

The “Trace_Length” and “Package_Delay” data of LFD2NX-9/17's CABGA196 package is missing in the .pkt file.

Devices affected: Certus-NX (LFD2NX)

Bug number: DNG-23568

Synplify Pro fails in FSM with initial value case and reports an error instead of a warning.

Workaround: Remove the initial value since this value can be assigned during reset (the 'reset' signal in this design") task.

Devices affected: CertusPro-NX (LFCPNX), Certus-NX (LFD2NX), MachXO5-NX (LFMXO5), CrossLink-NX (LIFCL), Certus-NX-RT (UT24C), CertusPro-NX-RT (UT24CP)

Bug number: DNG-24118

MPPHY (IP, Generic G8B10B, X1_5X4, G70) RTL simulation failed, Error: Found MPPHY Clock Out mismatched .= 2

Device affected: Lattice Avant (LAV-AT)

Bug number: DNG-23343

Power Calculator resource usage reporting is incorrect.

The report shows that MPP is utilized at 100% regardless of the number of lanes used, due to the current power modeling treating the entire IP as a single unit.

Device affected: Lattice Avant (LAV-AT)

Bug number: DNG-23785

Synplify Pro incorrectly removes virtual wire signals that were preserved using the "syn_rvl_debug" attribute.

Devices affected: All devices

Bug number: DNG-21236

Synplify Pro does not report an error or warning for clocks that are driven by logic.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-21048

The PDPSC32K primitive does not have an output path despite outreg being used.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-20772

You may encounter an issue with CONFIG_LMMI and CONFIG_LMMA's lmmi_ready signal during simulation.

Devices affected: Certus-NX (LFD2NX), CrossLink-NX (LIFCL)

Bug number: DNG-20717

CONFIG_LMMI RTL simulation error occurs and data missing in output ports.

Devices affected: Certus-NX (LFD2NX), CrossLink-NX (LIFCL)

Bug number: DNG-20543

Synplify Pro does not correctly process macro creation constraints with escape characters.

Devices affected: CertusPro-NX (LFCPNX), Certus-NX (LFD2NX), CrossLink-NX (LIFCL), Certus-NX-RT (UT24C), CertusPro-NX-RT (UT24CP)

Bug number: DNG-20134

When using Synplify Pro, you may encounter the following error during macro reuse: “Synthesis exit by 9. Child process exited abnormally. Done: error code 1.”

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-20116

IBIS reports I/O models of some sysCONFIG pins even if they are used as GPIO.

Workaround: Remove duplicated pins in IBIS file.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-19646

Simulation with XCELIUM may fail when simulating projects using the CNTL_LR_U_POWER primitive due to incorrect compilation order of cmpl_libs.

Devices affected: CrossLink-NX (LIFCL-33U)

Bug number: DNG-19623

Cannot assign input ports as MIPI_DPHY type for Avant.

Devices affected: Lattice Avant (LAV-AT)

Bug number: DNG-19199

Reveal Power-on Reset (POR) Debug function does not work when using LSE with only one Trigger Unit (TU).

Workaround: Add another Trigger Unit (TU) that can be unrelated to POR Debug.

Devices affected: All devices except iCE40UP

Bug number: DNG-13901

The CSI-2/DSI D-PHY Transmitter and Receiver Soft IP simulations fail when using Synopsys VCS as simulation tool.

Devices affected: CertusPro-NX (LFCPNX), Certus-NX (LFD2NX), CrossLink-NX (LIFCL), Certus-NX-RT (UT24C), CertusPro-NX-RT (UT24CP)

Bug number: DNG-13225

Post-route simulation error when using GDDR for Nexus devices due to parameters not being passed correctly from the original RTL.

Workaround: Intrinsic delay similar to the delay value on the vo.vo file needs to be added to the IP testbench.

Devices affected: CertusPro-NX (LFCPNX), Certus-NX (LFD2NX), MachXO5-NX (LFMXO5), CrossLink-NX (LIFCL), Certus-NX-RT (UT24C), CertusPro-NX-RT (UT24CP)

Bug number: DNG-9639

MAP incorrectly reports number of DPHY and PCIE/ADC resources for CrossLink-NX (LIFCL) QFN72 package.

Devices affected: CrossLink-NX (LIFCL)

Bug number: DNG-8297