Timer/Counter IP

IP Version: v1.5.0

Release Notes

FPGA-RN-02022-1.1

June 2026

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This document was created consistent with Lattice Semiconductor’s inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice’s inclusive language FAQ 6878 for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

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1. Introduction

This document contains the Release Notes for the Timer/Counter IP. For specific details about the IP and driver, refer to the following:

- Timer/Counter IP User Guide (FPGA-IPUG-02139)
- Timer/Counter Driver API Reference (FPGA-TN-02425)

Timer/Counter IP v1.5.0

Software	Software Version	Summary of Changes

Lattice Radiant	2026.1	• Fixed an issue where the internal counter did not reset when a timeout was asserted while the prescaler was disabled.
		• Added device-specific clock frequency constraints for MachXO4 devices.
		• Updated testbench files to fix a simulation hang issue that occurred when *SWTRIG_EN_TEST_0* was the selected test in configurations where the number of timers is fewer than 4.
		• Driver update v26.01.00:
		  • Simplified the *gp_timer_config* function.
		  • Removed the dependency on *reg_access.h*.
		  • Added macros for register access.
		  • Removed the unused prescaler ratio macro.
		  • Added *gp_timer_enable_interrupt* and *gp_timer_disable_interrupt*.
		  • Enabled calling *gp_timer_start* without passing a callback function.

Timer/Counter IP v1.4.0

Software	Software Version	Summary of Changes
Lattice Radiant	2024.2	Fixed the bug where the timeout is asserted when Software-Controlled Retrigger is disabled.

Timer/Counter IP Earlier Versions

IP Version	Summary of Changes
1.3.1	Fixed an issue where the interrupt did not assert in some configurations and addressed the missing AHBL memory map.
1.3.0	• Fixed an issue where the PREADY response was not generated for all addresses, causing the internal counter to become stuck. • Updated the driver.
1.2.2	Fixed GUI settings issues.
1.2.1	Fixed the Python script issue when the number of timers equals 1.
1.2.0	• Added AHB-Lite support. • Updated the prescaler ratio to 1:2 to avoid IP generation issues.
1.1.1	Added the driver folder.
1.1.0	• Fixed the SNAPSHOT register readback. • Fixed an issue with updating the internal counter reload value through the PERIOD register.
1.0.0	Initial release.

References

- Timer/Counter IP User Guide (FPGA-IPUG-02139)
- Timer/Counter Driver API Reference (FPGA-TN-02425)
- Avant-E web page
- Certus-N2 web page
- Certus-NX web page
- CrossLink web page
- Timer/Counter IP Core web page
- Lattice Propel Design Environment web page
- Lattice Radiant Software web page
- Lattice Insights web page for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

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