



SPI Target IP

IP Version: v2.4.0

Release Notes

FPGA-RN-02014-1.1

July 2025

Disclaimers

Lattice makes no warranty, representation, or guarantee regarding the accuracy of information contained in this document or the suitability of its products for any particular purpose. All information herein is provided AS IS, with all faults, and all associated risk is the responsibility entirely of the Buyer. The information provided herein is for informational purposes only and may contain technical inaccuracies or omissions, and may be otherwise rendered inaccurate for many reasons, and Lattice assumes no obligation to update or otherwise correct or revise this information. Products sold by Lattice have been subject to limited testing and it is the Buyer's responsibility to independently determine the suitability of any products and to test and verify the same. LATTICE PRODUCTS AND SERVICES ARE NOT DESIGNED, MANUFACTURED, OR TESTED FOR USE IN LIFE OR SAFETY CRITICAL SYSTEMS, HAZARDOUS ENVIRONMENTS, OR ANY OTHER ENVIRONMENTS REQUIRING FAIL-SAFE PERFORMANCE, INCLUDING ANY APPLICATION IN WHICH THE FAILURE OF THE PRODUCT OR SERVICE COULD LEAD TO DEATH, PERSONAL INJURY, SEVERE PROPERTY DAMAGE OR ENVIRONMENTAL HARM (COLLECTIVELY, "HIGH-RISK USES"). FURTHER, BUYER MUST TAKE PRUDENT STEPS TO PROTECT AGAINST PRODUCT AND SERVICE FAILURES, INCLUDING PROVIDING APPROPRIATE REDUNDANCIES, FAIL-SAFE FEATURES, AND/OR SHUT-DOWN MECHANISMS. LATTICE EXPRESSLY DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY OF FITNESS OF THE PRODUCTS OR SERVICES FOR HIGH-RISK USES. The information provided in this document is proprietary to Lattice Semiconductor, and Lattice reserves the right to make any changes to the information in this document or to any products at any time without notice.

Inclusive Language

This document was created consistent with Lattice Semiconductor's inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice's inclusive language [FAQ 6878](#) for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

Contents

Contents 3

1. Introduction 4

 SPI Target IP v2.4.0 4

 SPI Target IP v2.3.0 4

 SPI Target IP Earlier Versions 4

References 5

Technical Support Assistance 6

1. Introduction

This document contains the Release Notes for the SPI Target IP. For specific details about the IP, refer to the following:

- [SPI Target IP User Guide \(FPGA-IPUG-02070\)](#)

SPI Target IP v2.4.0

Software	Software Version	Summary of Changes
Lattice Radiant™	2025.1	<ul style="list-style-type: none"> • Added support for LFMXO5-35, LFMXO5-35T, LFMXO5-65, and LFMXO5-65T devices. • Added support for LFD2NX-15, LFD2NX-25, LFD2NX-35, and LFD2NX-65 devices.

SPI Target IP v2.3.0

Software	Software Version	Summary of Changes
Lattice Radiant	2024.2	<ul style="list-style-type: none"> • Added support for Certus™-N2 device (LN2-CT-20). • Added support for Certus-NX devices (LFD2NX-9 and LFD2NX-28). • Added timing requirement from ss_i assertion to first edge of sclk_o in testbench and IP User Guide.

SPI Target IP Earlier Versions

IP Version	Summary of Changes
2.1.0	Increased FIFO depth. Added Avant™ G/X support.
2.0.0	Changed terminology to Target.
1.5.1	Added driver version number and inline comments.
1.5.0	Added Avant support.
1.4.0	Added IP driver and Propel™ 2.2 support.
1.3.0	<ul style="list-style-type: none"> • Modified minimum value of Tx/Rx_FIFO_Almost_Full/Empty_Flag to 1. • Added static value attributes for setting the miso_o to a static value when Tx_FIFO is empty.
1.2.0	Added LFMXO5 support.
1.1.0	Added LFCPNX support.
1.0.1	<ul style="list-style-type: none"> • Added LFD2NX support. • Fixed RTL Bug related to Daisy Chain. • Reduced AHB-Lite and APB Read Latency from 2 to 1 clock cycle.
1.0.0	Initial release.

References

- [SPI Target IP User Guide \(FPGA-IPUG-02070\)](#)
- [Avant-E](#) web page
- [Avant-G](#) web page
- [Avant-X](#) web page
- [Certus-N2](#) web page
- [Certus-NX](#) web page
- [CertusPro-NX](#) web page
- [CrossLink-NX](#) web page
- [MachXO5-NX](#) web page
- [SPI Target IP Core](#) web page
- [Lattice Radiant Software](#) web page
- [Lattice Propel Design Environment](#) web page
- [Lattice Solutions IP Cores](#) web page
- [Lattice Solutions Reference Designs](#) web page
- [Lattice Insights](#) for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, please refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase



www.latticesemi.com