SPI Controller IP

IP Version: v2.4.1

Release Notes

FPGA-RN-02015-1.2

June 2026

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Inclusive Language

This document was created consistent with Lattice Semiconductor's inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice's inclusive language FAQ 6878 for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

Contents

1. Introduction

This document contains the Release Notes for the SPI Controller IP. For specific details about the IP, refer to the following:

- SPI Controller IP User Guide (FPGA-IPUG-02069)

SPI Controller IP v2.4.1

Software	Software Version	Summary of Changes
Lattice Radiant™ Lattice Propel™	2026.1	Fixed FIFO status check timing in the testbench. **Note:** There are no updates to the IP user guide for this release. Refer to the SPI Controller IP User Guide (FPGA-IPUG-02069, v2.3) for the applicable documentation.

Corrections to Previous Release Notes

All previous IP versions are supported by the Lattice Propel software.

SPI Controller IP v2.4.0

Software	Software Version	Summary of Changes
Lattice Radiant	2025.1	• Added support for LFMXO5-35, LFMXO5-35T, LFMXO5-65, and LFMXO5-65T devices. • Added support for LFD2NX-15, LFD2NX-25, LFD2NX-35, and LFD2NX-65 devices.

SPI Controller IP v2.3.0

Software	Software Version	Summary of Changes
Lattice Radiant	2024.2	• Added support for Certus™-N2 device (LN2-CT-20). • Added support for Certus-NX devices (LFD2NX-9 and LFD2NX-28). • Fixed timing from ssn_o assertion to first sclk_o edge when *Clock Prescaler* is equal to 4 to ensure that receive data is correctly sampled.

SPI Controller IP Earlier Versions

IP Version	Summary of Changes
2.1.0	• Increased FIFO depth. • Added Avant™ G/X support.
2.0.0	Changed terminology to Controller.
1.4.2	Added driver version number, inline comments, and non-blocking transfer mode.
1.4.1	Updated to remove glitch in SS line when using SPI ENABLE register and Slave Select Pulse Mode = Non Pulse.
1.4.0	Added Avant support.
1.3.1	Added *SPI Enable Register* attribute (unchecked by default).
1.3.0	• Added IP driver and Propel™ 2.2 support. • Added SPI Enable Register. • Changed Clock Prescaler lower limit from 1 to 2.
1.2.0	Added LFMXO5 support.
1.1.0	Added LFCPNX support.
1.0.2	• Desired SCLK Frequency maximum value is now *System Clock Frequency*/2. • Reduced APB/AHB-Lite read latency from 2 to 1.

IP Version	Summary of Changes
1.0.1	Added LFD2NX support.
1.0.0	Preliminary release.

References

- SPI Controller IP User Guide (FPGA-IPUG-02069)
- Avant-E web page
- Avant-G web page
- Avant-X web page
- Certus-N2 web page
- Certus-NX web page
- CertusPro-NX web page
- CrossLink-NX web page
- MachXO5-NX web page
- SPI Controller IP Core web page
- Lattice Radiant Software web page
- Lattice Propel Design Environment web page
- Lattice Solutions IP Cores web page
- Lattice Solutions Reference Designs web page
- Lattice Insights for Lattice Semiconductor training courses and learning plans

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