PCIe x1 IP

IP Version: v3.0.0

Release Notes

FPGA-RN-02060-1.4

December 2025

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Contents

1. Introduction

This document contains the Release Notes for the PCIe x1 IP. For specific details about the IP, refer to the following:

- PCIe x1 IP Core User Guide (FPGA-IPUG-02091)
- Lattice Avant and Nexus PCIe Host DMA Driver Software User Guide (FPGA-TN-02386)
- Lattice Avant and Nexus PCIe Basic Memory-Mapped Host Driver (Non-DMA) User Guide (FPGA-TN-02387)
- PCI Express for Nexus FPGAs web page

PCIE x1 IP v3.0.0

Software	Software Version	Summary of Changes

Lattice Radiant™	2025.2	• IP Update
		  • Made enhancements to the IP user interface.
		• Feature Updates
		  • Enabled DMA.
		  • Enabled MSI-X feature in AXI Bridge mode.
		• Example Design Update
		  • Added DMA Example Design simulation and hardware support.
		  • Enabled QuestaSim Lattice-Edition simulation.
		• Driver updates
		  • Added driver support for DMA.

PCIE x1 IP v2.1.0

Software	Software Version	Summary of Changes
Lattice Radiant	2025.1.1	• Driver updates • Added driver support for non-DMA TLP mode.

PCIE x1 IP v2.0.1

Software	Software Version	Summary of Changes
Lattice Radiant	2025.1	• Updated the PCIe IP License string. • Enabled the clock user out signal.

PCIE x1 IP v2.0.0

Software	Software Version	Summary of Changes
Lattice Radiant	2025.1	• Added new device support for Certus™-NX (LFD2NX-35 and LFD2NX-65). • Added new device support for MachXO5™-NX (LFMXO5-35T and LFMXO5-65T). • The Hardware and Simulation capable Example Design is enabled for both AXI-S and TLP data interfaces. • Feature Updates: • AXI Bridge Mode enablement. • Removed AHB-L related features. This feature is still available in older IP versions (v1.2.5 or older) • The IP's user interface configuration is revamped and port names are aligned to be similar to the PCIe IPs used in other Lattice FPGA device families.

PCIE x1 IP v1.2.5

Software	Software Version	Summary of Changes
Lattice Radiant	2024.2	• Added new device support for Certus-NX (LFD2NX-28). • Fixed CrossLink-NX constraint file.

PCIE x1 IP Earlier Versions

IP Version	Summary of Changes
1.2.4	Reduced simtime for Modelsim OEM simulator.
1.2.2	Added ED Testbench.
1.2.1	Added Address Space mapping for Propel.
1.2.0	Added Propel support.
1.1.3	Updated for Linux support.
1.1.2	• Updated IP user interface. • Fixed several issues on DMA. • Added DMA data checking on TB.
1.1.1	Fixed issue on path with space character in component generator script.
1.1.0	Added LFD2NX-40.
1.0.2	Corrected aux_clk_i connection on default interface.
1.0.1	Initial release.
1.0.0	Preliminary release.

References

- PCIe x1 IP Core User Guide (FPGA-IPUG-02091)
- Lattice Avant and Nexus PCIe Host DMA Driver Software User Guide (FPGA-TN-02386)
- Lattice Avant and Nexus PCIe Basic Memory-Mapped Host Driver (Non-DMA) User Guide (FPGA-TN-02387)
- Certus-NX web page
- CrossLink-NX web page
- MachXO5-NX web page
- PCI Express for Nexus FPGAs web page
- Lattice Propel Builder software
- Lattice Radiant FPGA design software
- Lattice Insights for Lattice Semiconductor training courses and learning plans

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For frequently asked questions, please refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase

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